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SXRT investigations on electrically stressed 4H-SiC PiN diodes for 6.5 kV

Birgit Kallinger[1, a], Patrick Berwian[1,b], Jochen Friedrich[1,c], Christian Hecht[2,3,d], Dethard Peters[2,3,e], Peter Friedrichs[2,3,f] and Bernd Thomas[2,4g]

[1]Fraunhofer IISB, Dept. Crystal Growth, Schottkystr. 10, 91058 Erlangen, Germany

[2]SiCED Electronics Development, Günther-Scharowsky-Str. 1, 91058 Erlangen, Germany

[3]now with: Infineon Technologies AG, Schottkystr. 10, 91058 Erlangen, Germany

[4]now with: Dow Corning Semiconductor Solutions, 5300 Eleven Mile Road, Auburn, MI 48611, USA

[a]birgit.kallinger@iisb.fraunhofer.de, [b]patrick.berwian@iisb.fraunhofer.de, [c]jochen.friedrich@iisb.fraunhofer.de, [d]christian.hecht@infineon.com, [e]dethard.peters@infineon.com, [f]peter.friedrichs@infineon.com, [g]bernd.thomas@dowcorning.com

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Abstract. 4H-SiC PiN diodes for 6.5 kV were manufactured on both 4° and 8° off-cut substrates and subjected to an electrical stress test on wafer level and subsequent analysis of structural defects present in the active area of the diodes. For 8° off-cut diodes, the electrical characteristics with respect to leakage current and forward voltage drift are worse than the electrical characteristics of 4° off-cut diodes. Furthermore, a large number of stacking faults was found in 8° off-cut diodes, but little evidence for bipolar degradation was found in 4° off-cut diodes. Therefore, bipolar degradation was significantly reduced by avoiding BPDs in the active area of PiN diodes, i.e. by the use of 4° off-cut substrates. Furthermore, a strong correlation was found between the electrical screening test on wafer level and critical defects.

Introduction

The so-called bipolar degradation of 4H-Silicon Carbide (4H-SiC) power electronic devices has been an obstacle for the commercialization of high-voltage, bipolar diodes for the last ten years. This certain type of device degradation is characterized by drift of the forward characteristics of PiN diodes after electrical stressing, which is accompanied by the formation and expansion of stacking faults within the active area of the device. According to the mechanism of recombination enhanced dislocation glide (REDG) [1], such stacking faults originate from Basal Plane Dislocations (BPDs), which are replicated from the 4H-SiC substrate to the epilayer. Therefore, it is expected that the bipolar degradation of power electronic devices can be suppressed by using BPD-free epilayers for the production of bipolar devices.

The first step for suppressing the bipolar degradation of PiN diodes was the optimization of the epitaxial process for growth of thick, BPD-free epilayers. This optimization study revealed that a small off-cut angle of the substrate is beneficial for the growth of BPD-free epilayers [2-6]. Now, it has to be verified by fabrication of PiN diodes that the bipolar degradation is successfully suppressed on BPD-free epitaxial layers and that bipolar degradation occurs for PiN diodes fabricated on BPD-containing epilayers. Therefore, we will present our recent results on electrical characteristics and structural defects of PiN diodes after electrical stressing, which were fabricated on 4° and 8° off-cut substrates.

Experiment

For manufacturing of 6.5 kV PiN diodes homoepitaxial layers were grown by Chemical Vapor Deposition (CVD) in a horizontal hot-wall reactor (VP508GFR) as described in [2-5]. The epilayers were grown on the (0001)Si-face of 4° and 8° towards <11-20> off-cut substrates. All epilayers met the specifications for the diode fabrication process with respect to doping, thickness and the respective homogeneities. PiN diodes with a p-emitter area of 7.5 mm² (chip size 12.4 mm²) were fabricated at SiCED [7]. The electrical characterization as well as the electrical stressing of the PiN diodes were done at SiCED. Based on the electrical forward characteristics of the bipolar diodes before and after electrical stressing, the diodes were classified as "pass" and "fail".

Finally, diodes from both classes were selected for the investigation of structural defects present in the devices' active areas by Synchrotron X-ray Topography (SXRT). These investigations were performed in back-reflection geometry at the TOPO-TOMO beam line of the Synchrotron Light Source ANKA in Karlsruhe, Germany, as described in [3,5].

Results and Discussion

Electrical characterization of PiN diodes. All 6.5 kV PiN diodes were subjected to an electrical screening test on wafer level. First, the reverse characteristics of all diodes were determined. The resulting leakage currents of all diodes at blocking voltages of V_r = 100 V and V_r = 6000 V are shown in terms of cumulative frequency plots in Fig. 1a and 1b, respectively. As shown in Fig. 1a, the diodes manufactured on 8° off-cut substrates showed a broad distribution of leakage current, whereas the 4° off-cut diodes exhibited a steep increase at very low leakage currents. The red line displays the expectation value for the leakage current of $I_r < 5 \times 10^{-9}$ A at V_r = 100 V. Up to 50 % of the 4° off-cut diodes met the expectation value, but less than 20 % of the 8° off-cut diodes met it. A similar result is found regarding the leakage current of all diodes at a blocking voltage of V_r = 6000 V, i.e. about 50 % of 4° off-cut diodes fulfilled the expectation value of $I_r < 1 \times 10^{-6}$ A, but very few 8° off-cut diodes met the criterion.

Furthermore, the forward characteristics of all diodes were tested based on the following electrical screening test on wafer level: measurement of DC forward characteristics, followed by forward stressing with pulsing at 10 A and finally a repetition of the forward characteristics measurement. Based on these measurement results, ΔV_f was determined as V_{f2}-V_{f1} and used as the classification criterion, i.e. diodes with -0.02 V < ΔV_f < 0.01 V are classified as "pass" diodes. The results for all diodes are shown in Fig. 1c. According to this classification criterion, 96 % of 4° off-cut diodes and 60 % of 8° off-cut diodes were classified as "pass". When applying a more demanding stability criterion of $\Delta V_f \pm 0.003$ V, 60 % of 4° off-cut diodes still met this criterion while only < 15 % of 8° off-cut diodes met it.

Structural defects in PiN diodes. A total of about 30 diodes of classes "pass" and "fail" were investigated with regard to extended structural defects by means of synchrotron x-ray topography. As shown in Fig. 2a, "pass" diodes fabricated on 4° off-cut substrates contained threading screw dislocations (TSDs) and threading edge dislocations (TEDs). In some of these "pass" diodes, very few Basal Plane Dislocations (BPDs) and up to 3 stacking faults (SF) were found. Therefore, 4° off-cut diodes classified "pass" were almost free of BPDs and SFs.

In "fail" diodes fabricated on 4° off-cut substrates, macroscopic defects such as downfalls or technological defects were found as shown in Fig. 2b. These macroscopic defects are often surrounded by many structural defects, especially by BPDs. No stacking faults were found in these 4° off-cut, "fail" diodes, indicating that no bipolar degradation occurred during the electrical stress test.

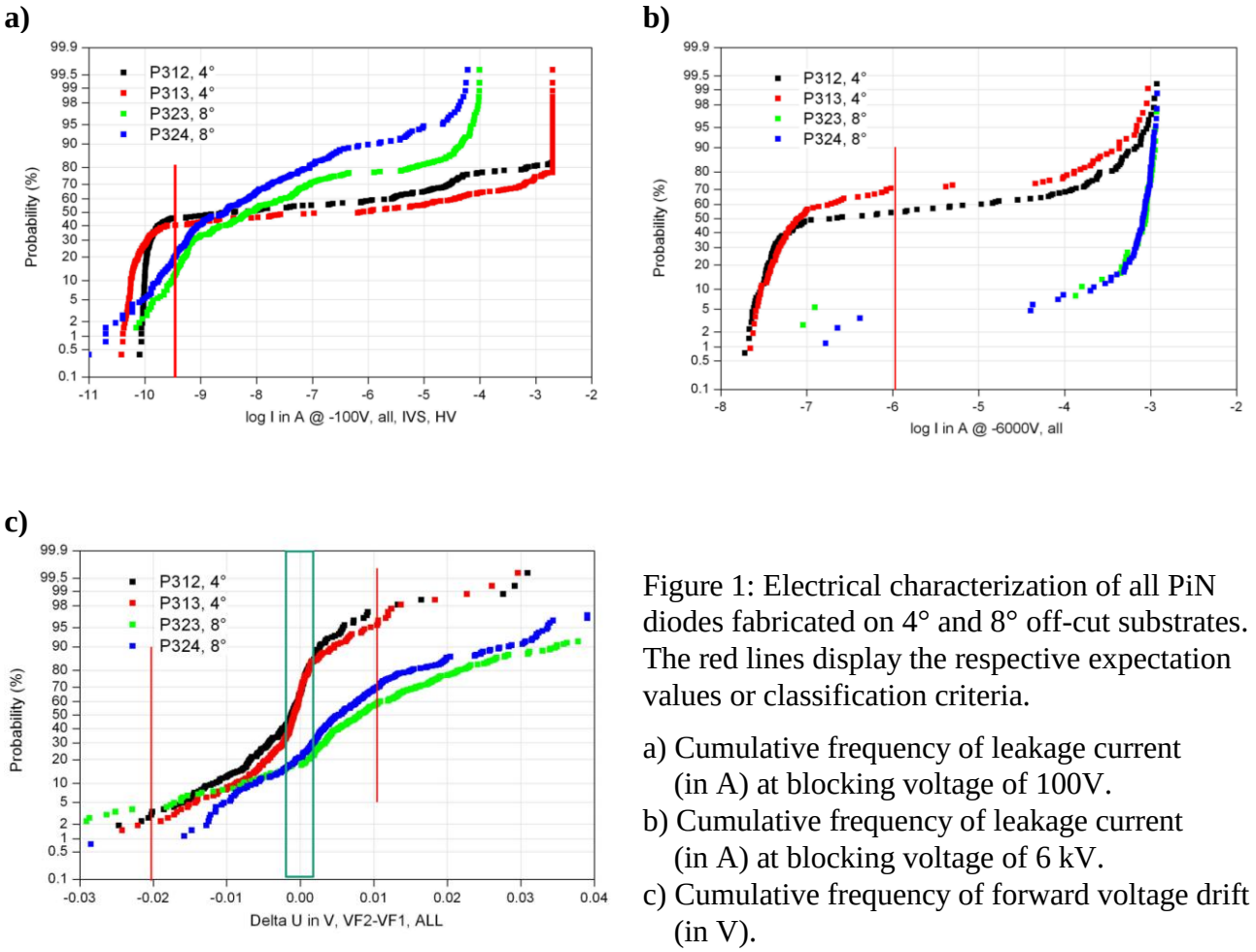

Figure 1: Electrical characterization of all PiN diodes fabricated on 4° and 8° off-cut substrates. The red lines display the respective expectation values or classification criteria.

a) Cumulative frequency of leakage current (in A) at blocking voltage of 100V.
b) Cumulative frequency of leakage current (in A) at blocking voltage of 6 kV.
c) Cumulative frequency of forward voltage drift (in V).

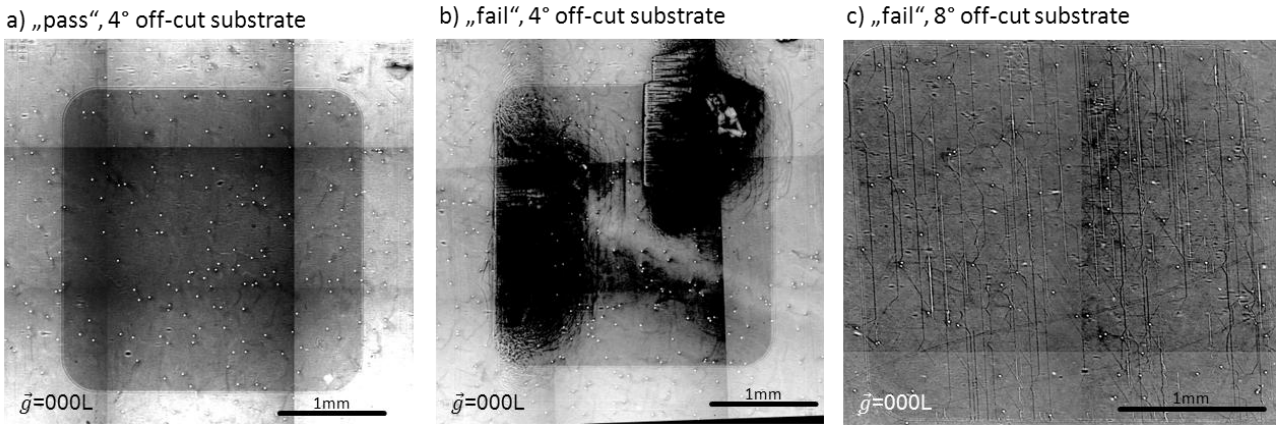

Figure 2: SXRT topographs taken from PiN diodes under diffraction condition g=000L. The active area of the diodes appears darker than the surrounding area. Threading screw dislocations (TSDs) are visible as bright point-shaped contrasts in all topographs. In Fig. 2b, a macroscopic defect is located at the top right corner of the diode, which is surrounded by numerous Basal Plane Dislocations (BPDs, dark line contrasts). Stacking faults are represented by straight contrasts in Fig. 2c.

In “fail” diodes manufactured on 8° off-cut substrates, a large number of stacking faults was found as shown in Fig. 2c. The densities of TEDs and TSDs were comparable with those of 4° off-cut diodes. The large number of stacking faults in 8° off-cut, “fail” diodes indicates clearly that bipolar degradation took place during the electrical stress test.

Therefore, bipolar degradation of PiN diodes can be significantly reduced by using epilayers, which are initially free of BPDs.

Summary

4H-SiC PiN diodes for 6.5 kV were manufactured on both 4° and 8° off-cut substrates and subjected to an electrical stress test on wafer level and subsequent analysis of structural defects present in the active area of the diodes. For 8° off-cut diodes, the drift of forward voltage characteristics is more pronounced with respect to the absolute value of ΔV_f. Furthermore, only 60 % of 8° off-cut diodes were classified “pass”. In “fail” diodes fabricated on 8° off-cut substrates, a large number of stacking faults was found by SXRT, indicating that bipolar degradation is a severe problem for 8° off-cut diodes. Contrary to that, few stacking faults or basal plane dislocations were found in 4° off-cut diodes. “Fail” diodes fabricated on 4° off-cut substrates suffer from macroscopic defects such as downfalls or technological defects. No evidence for bipolar degradation was found in 4° off-cut diodes. Regarding the electrical characteristics of 4° off-cut diodes, they exhibit a higher percentage of “pass” diodes and steeper profiles in the cumulative frequency plots than 8° off-cut diodes. Therefore, bipolar degradation was significantly reduced by avoiding BPDs in the active area of PiN diodes. Furthermore, a strong correlation was found between the electrical screening test on wafer level and critical defects.

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