Challenges and solution approaches for simulation-based reliability assessment – degradation modeling

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***Abstract*— To verify the reliability of electronic circuits and systems in automotive applications, qualification according to the industry-standards, such as AEC-Q100, is state of the art. But will it be sufficient for future applications? Simulation-based reliability assessments in IC and system development are intended to complement qualification and allow efficient investigations of product reliability. Aging simulations for analog circuits have been available for years, but are hardly used. This article discusses degradation models as one bottleneck, outlines different requirements and approaches, and points to standards that could be a future solution.**

Keywords—aging simulation, degradation models, transistor reliability, qualification

I. Introduction

Today, integrated circuits (IC) and electronic systems offer enormous possibilities of functionality. Therefore, they are broadly used in multiple products over our private and business lives. In addition to functionality, different fields of applications demand for robust and reliable electronic systems. This is especially true for automotive and industrial applications, where ICs and electronic systems have to operate for 10+ years under harsh environmental conditions. For automotive electronics, some systems are expected to be operating for 24 hours every day in the mid-term future [1], which poses additional reliability challenges.

The Automotive Electronics Council (AEC) standard AEC-Q100 provides procedures that have to be followed to confirm automotive readiness for an IC [2]. However, it is argued that the corresponding qualification test will not be sufficient in the future [1]. Simulation-based approaches are promising to supplement product qualification.

Especially for analog IC design, the aging simulation has been available for years, but it has not evolved into a standard verification step. In this article, we outline the bottlenecks that hinder a widespread use of aging simulations. In detail, we focus on degradation models of integrated transistors as one issue that needs further developments in the future.

II. Qualification according to AEC-Q100

The standard AEC-Q100 is a bundle of tests that have to be performed for automotive products [2]. They are organized in different test groups that can be split into testing the product and testing the underlying base technologies, such as wafer processing and packaging. Two example tests are temperature cycling (TC) and high-temperature operating life (HTOL). TC has to be performed on 3 lots with 77 devices each. For example for automotive grade 1, 1,000 cycles between -55 °C and 150 °C or equivalent have to be applied to the unbiased product. The functionality has to be tested at room and hot temperatures before and after stressing. HTOL uses the same number of test devices. The devices are biased and operated at an elevated temperature of 125 °C (grade 1) for 1,000 hours. Functionality is tested at room, cold, and hot temperature before and after stressing. For both tests, 0 fails are allowed. While the procedures are industry-proven and trusted due to good experiences, the tests suppress important information. In particular, we cannot judge on how the fails are distributed when 0 fails are observed. Will the first fail occur after 1001 cycles or hours or will all test devices remain functional for further 10,000 cycles or hours? Furthermore, it is not completely clear how the stress test conditions correlate to use scenarios in real life.

To judge on the underlying base technologies, AEC-Q100 test group D contains multiple tests that have to be performed on wafer level. Stress migration and electro migration tests analyze the back end of line and time-dependent dielectric breakdown tests examine the quality of dielectrics. Integrated transistors, the so-called front end of line, are mainly affected by the physical degradation mechanisms hot carrier injection (HCI) and bias temperature instability (BTI). Corresponding tests investigate their impact on the transistor performance.

III. Circuit-level aging simulation

Circuit level aging simulations are intended to virtually investigate the impact of HCI and BTI on IC performance. They are available in different design environments and, according to Fig. 1, extend the standard verification in analog design, where evaluation testbenches are simulated to analyze the nominal circuit performance. From additional simulations of typical use scenarios, the mission profiles, transient stress signals are individually extracted for each transistor. Degradation models transform the stress into changed transistor behaviors. Writing back the changed behavior to the netlist results in a virtual representation of the aged circuit, e.g. after n years of operation. This aged netlist can be investigated based on simulations that apply the same evaluation

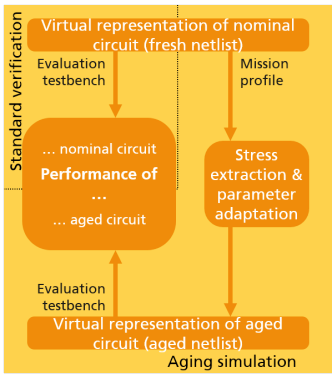

Fig. 1: Principle flow of aging simulations

testbenches as before. Thus, the performance of the aged circuit can be investigated and compared to the specification.

The aging simulation flow has two sensitive inputs. First, mission profiles have to well represent typical use scenarios and should be consistently applied across different levels of hierarchy in IC and system design. A generalization of mission profile descriptions for different use cases and a format standardization proposal is subject to current research activities [3]. Second, degradation models have to be available to transform stress signals into changed transistor behavior. Section IV discusses challenges and approaches in detail.

It has to be noted that aging simulations cause a significant additional verification effort. While verification times have already shown to be the major bottleneck in design projects, designers tend to dismiss aging simulations.

IV. Degradation Modeling

Degradation models mimic the impacts of degradation mechanisms like HCI and BTI on transistor behavior. There are multiple aspects that need to be considered, and they are introduced in the following.

First, degradation models affect foundries, designers and EDA tool providers. Our perspective on their different requirements is summarized in TABLE I. Foundries seem to prefer general modeling approaches that are easy to use, maintain, and parametrize as well as easy to transfer to further devices and technology nodes. When degradation models are delivered as parts of process design kits (PDK), they should equally support different EDA environments to address a broad range of foundry customers. Designers are interested in using degradation models in their design environment. The models should capture all relevant effects, impact factors, and other requirements for the particular design project. For EDA tool providers, well established proprietary degradation models can support canvassing for and retention of customers. Simulation tools provide application programming interfaces (APIs) to support integrating custom degradation models. Today, the APIs are tool-specific but models can be implemented to equally support different environments [4]. A working group of the Compact Model Coalition (CMC) of the Silicon Integration Initiative (Si2) works on the standardized interface OMI [5] to allow a more efficient model implementation into different EDA environments.

Second, degradation models can be defined in three ways, while combinations are possible. (a) Subcircuits, usually controlled sources, can be placed around the unchanged transistor to mimic degradation independent of the underlying nominal compact model. An example with a controlled voltage source in series to the gate contact and a controlled current source parallel to the drain-source branch is shown in Fig. 2(a). The subcircuit approach causes losses in simulation performance due to additional nodes and branches [6].

TABLE I: Different Requirements on Degradation Models

Foundry	EDA tool provider	IC designer
➢ Consistent support of **multiple EDA environments** (acc. to customer requirements) preferred	➢ Well-established built-in (proprietary) models can support canvassing for and retention of customers ➢ Custom models should work with EDA provider's tools	➢ Degradation model should be available in the **particular EDA environment**
➢ **General** approaches that well describe technology properties ➢ Easy to use & **maintain** as well as easy to **transfer** to further devices and technology nodes		➢ Model should well capture the **particular requirements in** current design **project**

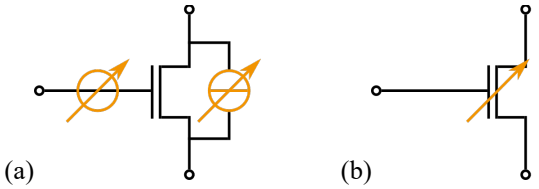

Fig. 2: (a) Example for subcircuit model; (b) Principle of extending compact models or adapting selected compact model parameters

(b) Compact models can be extended to cover the physics of degradation effects by additional equations and model parameters. Research teams have achieved good progress, e.g. in [7]. (c) Selected parameters of the underlying compact model can be adapted to mimic transistor degradation. To the best of our knowledge, the industry prefers this approach of adapting model cards as a good tradeoff between complexity, accuracy, and simulation performance.

Third, degradation models can be based on physical and empirical approaches. Physical models aim at describing the microscopic contributions to transistor degradation. They are parametrized based on measurement data. Empirical models are a mathematical approach to describe the data observed in particular reliability experiments. Physical models can be much more accurate, and empirical models usually cause much less characterization and parametrization effort.

We demonstrate the approach of an empirical model with adapting model cards based on artificial HCI data and 22nm Low Power Predictive Technology Models (PTM) [8]. We map the relative shifts in linear and saturation currents

$$\text{d\_IDLIN} = \left|-0.71 \cdot \exp\left(-\frac{5}{V_{\text{dstress}}}\right) \cdot t^{0.25}\right| \quad (1)$$

$$\text{d\_IDSAT} = \left|-1.56 \cdot \exp\left(-\frac{7}{V_{\text{dstress}}}\right) \cdot t^{0.25}\right| \quad (2)$$

as in Fig. 3 to relative shifts in the parameters u0 and vsat of the underlying BSIM4 models, i.e. to d_u0 and d_vsat. Aging simulations use parameter settings of

$$\text{u0} = (1 + \text{d\_u0}) \cdot \text{u0\_nominal} \quad \text{and} \quad (3)$$

$$\text{vsat} = (1 + \text{d\_vsat}) \cdot \text{vsat\_nominal}\,. \quad (4)$$

From the evolutions of the parameter shifts over time t and stress drain voltage V_{dstress} in Fig. 4, we conclude that a predefined, i.e. unique and fixed, equation for both parameters is not applicable without a loss of accuracy due to the different time dependencies. As an example, we express the shifts of the BSIM4 parameters as models of the form of (1) and (2):

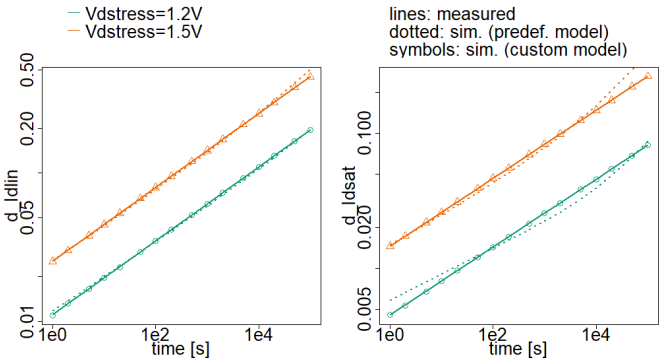

Fig. 3: Artificial measured HCI data, simulation results with predefined model acc. to (5) and (6), and simulation results with custom models

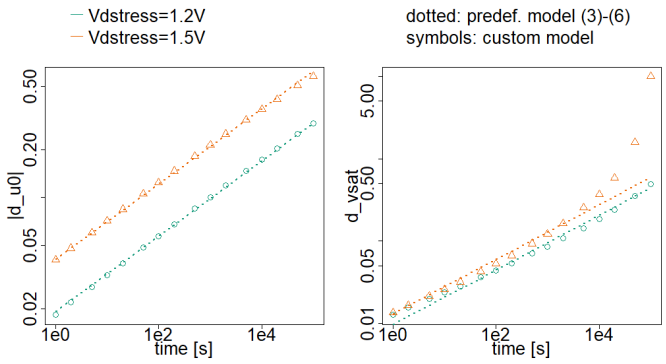

Fig. 4: Relative shifts of BSIM4 parameters $u0$ and $vsat$ to model $IDLIN$ and $IDSAT$ degradation

$$\mathrm{d\_u0} = -0.834 \cdot \exp\left(-\frac{4.53}{V_{\mathrm{dstress}}}\right) \cdot t^{0.237} \qquad (5)$$

$$\mathrm{d\_vsat} = 0.0426 \cdot \exp\left(-\frac{1.78}{V_{\mathrm{dstress}}}\right) \cdot t^{0.332}. \qquad (6)$$

The simulation results with this predefined model are added to Fig. 3 (dotted lines). In our particular scenario, the predefined model introduces inaccuracies to the predicted IDSAT degradation, especially for short periods of moderate stress and for long periods of large stress. Modeling engineers would have to judge on whether theses inaccuracies are acceptable for the particular technology or application case.

Separate custom model equations are an alternative to improve the model accuracy. While (3) can be used to well describe the shift in the BSIM4 parameter u0, another approach has to be found for the parameter vsat. Special attention has to be paid to the time dependency in the model equation, since both non-constant stress waveforms and time extrapolation have to be supported. Fortunately, a broad class of modeling approaches is available for this purpose, e.g. from [9]. Since separate model equations have to be implemented individually into the simulator APIs, custom models cause an increased effort. Nevertheless, the drastically improved model accuracy, which can be observed in the simulation results with the custom models in Fig. 3, usually outweighs the increased implementation effort and model complexity.

The complexity of an empirical degradation model strongly depends on the number of impact factors, such as time t, stress drain & gate voltage V_{dstress} & V_{gstress}, temperature T, or device length L and width W. A common modeling approach is to add one factor per variable to the model equation. For example, the temperature dependency could be added to (3) by an additional Arrhenius factor,

$$\exp\left(\frac{E_{\mathrm{a}}}{k_{\mathrm{B}} \cdot T}\right) \quad \text{or} \quad \exp\left(\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}} \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)\right) \qquad (7)$$

with the activation energy E_{a}, the Boltzmann constant k_{B}, and the reference temperature T_0. Note that in the case of separate custom model equations for different parameters, multiple approaches might have to be used.

From our experience, the model complexity further rises when additional observables have to be considered. Besides linear and saturation currents, threshold voltage, maximum transconductance, off-current, or subthreshold slope (all potentially for different values of drain-source voltages V_{ds}) are further observables that could be of interest depending on the application case and accuracy requirements. To achieve a reasonable accuracy, additional parameters of the underlying compact model have to be adapted by using degradation model equations. As an example, 6 compact model parameters were shifted to fit the degradation of 5+ observables in [10].

Standardized degradation models would be helpful to develop common flows from reliability measurements to degradation models and further to a wide-spread use of aging simulations to support the design of reliable ICs and electronic systems. However, different issues will have to be overcome first. (1) The different player's requirements appear hard to be addressed simultaneously. (2) The complicated physics behind degradation effects, such as HCI and BTI, are difficult to describe with reasonably simple mathematical approaches. (3) Reliability measurements and degradation modeling cause significant effort and costs. Nevertheless, multiple research teams work. Who will have to pay the price, foundries, EDA providers, IC designers, system integrators, or end customers?

Different teams in research and development work on solutions to these issues. An example is a dedicated working group at the CMC [5].

V. Summary & Outlook

This article presents a status report of reliability considerations in design projects for ICs and electronic systems. Especially for automotive electronics, the industry relies on standardized qualification procedures, such as AEC-Q100, but they will not be sufficient for future products. Simulation-based reliability assessments are promising supplements but have not evolved into standard verification steps. At the example of circuit level aging simulations, we highlight obstacles to progress in reliability investigations based on simulations. One issue is degradation modeling, for which challenges and approaches are discussed in detail.

Research and industry have noticed the bottlenecks. We are confident that current and future activities will overcome today's problems and establish simulation-based reliability investigations as standard steps in the design of ICs and electronic systems for safety-critical and long-lived applications.

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