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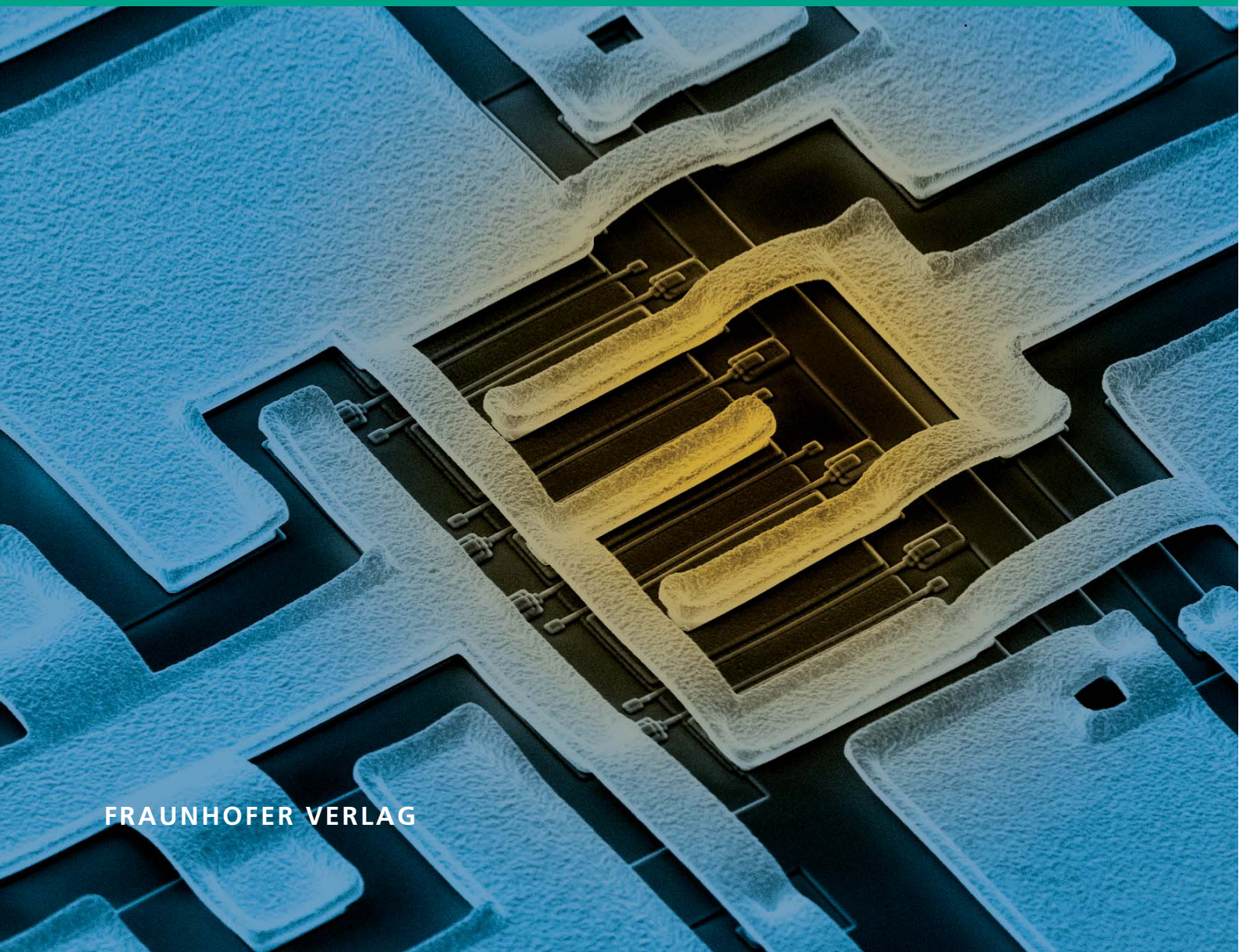
SCIENCE FOR SYSTEMS No. 3

Christian Haupt

AlGaN/GaN-BASED MILLIMETER-WAVE HIGH ELECTRON MOBILITY TRANSISTORS



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Bibliografische Information der Deutschen Nationalbibliothek
Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliografie; detaillierte bibliografische Daten sind im Internet über http://dnb.d-nb.de abrufbar.
ISBN: 978-3-8396-0303-1

D 25

Zugl.: Freiburg, Univ., Diss., 2011

Umschlaggestaltung: Fraunhofer IAF
Druck: Mediendienstleistungen des
Fraunhofer-Informationszentrum Raum und Bau IRB, Stuttgart

Für den Druck des Buches wurde chlor- und säurefreies Papier verwendet.

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AlGaN/GaN-based millimeter-wave high electron mobility transistors

Dissertation

zur Erlangung des Doktorgrades
an der Technischen Fakultät

der Albert-Ludwigs Universität Freiburg im Breisgau

vorgelegt von

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April 2011

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Datum der Prüfung: 20.7.2011

The popular stereotype of the researcher is that of a skeptic and a pessimist. Nothing could be further from the truth! Scientists must be optimists at heart, in order to block out the incessant chorus of those who say "It cannot be done.".

Academician Prokhor Zakharov, University Commencement

Dedicated

To my family and friends.

Abstract

Gallium Nitride (GaN) offers unique material characteristics to enable the fabrication of field effect transistors with high output powers at millimeter wave frequencies. At the start of this work GaN-amplifiers operating at K-band frequencies were available. However, an increasing demand exists for power amplifiers beyond 50 GHz such as radar applications or RF-broadcasting systems.
In this work a scaling approach is studied to develop a transistor technology which achieves a high gain as well as a high output power at W-band frequencies and can be applied in the existing fabrication process for monolithic microwave integrated circuits (MMIC). Following the theoretical scaling rules for field effect transistors lateral and vertical critical dimensions of 100 nm and 10 nm must be achieved, respectively. Therefore various new fabrication processes were developed in this work to enable the new critical dimensions with a sufficient production yield for MMIC fabrication.
Transistors fabricated with these methods were evaluated regarding the influence of the scaled geometries on the device characteristics using S-parameter as well as DC-measurements. As a result a transistor technology could be established which achieves a transconductance above 600 mS/mm this is one of the highest reported values for GaN-based HEMTs so far. Furthermore, a very low parasitic capacitance of 0.3 pF/mm was achieved. As a consequence, these transistors feature a current-gain cut-off frequency of more than 110 GHz.
Besides the high frequency characteristics short channel effects and their influence on the device characteristics were also evaluated. From these studies the following results were obtained: The scaled transistors are dominated by a drain induced barrier lowering (DIBL) which is mainly a function of the aspect ratio of gate length to barrier thickness. It was also found that a critical aspect ratio of approximately 14 is necessary to suppress the DIBL-effect.
Finally, first generations of MMICs based on the developed transistor technology were characterized using S-parameter and large-signal measurements. These amplifiers exhibit a high output power at 60 GHz and 94 GHz of 21.8 dBm

and 22.8 dBm, which correspond to a power density of 0.84 W/mm and 0.53 W/mm, respectively. These measurements demonstrate the first successful MMIC amplifier operation of GaN-based HEMTs at W-band frequencies in Europe. Furthermore, a high production yield regarding the MMIC fabrication process of more than 85% could be demonstrated across a 3-inch wafer.

Zusammenfassung

Galliumnitrid (GaN) besitzt einzigartige Materialeigenschaften, welche die Herstellung von Feldeffekttransistoren mit hohen Ausgangleistungen bei Millimeterwellenfrequenzen ermöglichen. Zu Beginn dieser Arbeit erreichten GaN-basierte Verstärker sehr gute Ausgangleistungen bis hin zu K-Band Frequenzen, aber die Nachfrage nach Leistungsverstärkern, die oberhalb von 50 GHz operieren können, vergrößerte sich in den letzten Jahren enorm.

In dieser Arbeit wurde eine Verbesserung der Hochfrequenzeigenschaften dieser Leistungsverstärker mittels Skalierung der gesamten Transistorgeometrien untersucht. Der entwickelte Herstellungsprozess musste dabei mit dem vorhandenen MMIC-Prozess (millimeter wave monolithic integrated circuit) kompatibel sein, um eine direkte Entwicklung von Verstärkerschaltungen für W-Band Frequenzen zu ermöglichen. Legt man die theoretischen Skalierungsregeln für Feldeffekttransistoren zugrunde, muss die neue Generation der Transistortechnologie minimale Abmessungen von 100 nm in lateraler und 10 nm in vertikaler Ausrichtung erreichen. Deswegen war es im Verlauf dieser Arbeit notwendig neue Prozesse zu entwickeln, die kleinere kritische Dimensionen bei gleichzeitig hoher Ausbeute ermöglichen.

Die so hergestellten Transistoren wurden anschließend durch Messungen der S-Parameter und Kennlinienfelder hinsichtlich des Einflusses jeder variierten Transistorgeometrie auf die Bauelementeigenschaften detailliert evaluiert. Das Ergebnis dieser Studien war die Etablierung eines Fertigungsprozesses für Transistoren, welche Steilheiten von über 600 mS/mm erreichen. Diese gehören zu den höchsten jemals veröffentlichten Steilheiten für GaN-Transistoren. Weiterhin konnten die parasitären Kapazitäten auf den extrem geringen Wert von 0,3 pF/mm reduziert werden. Beide Eigenschaften zusammen ermöglichen, dass diese Transistoren Grenzfrequenzen für die Stromverstärkung oberhalb von 110 GHz erreichen.

Neben den Hochfrequenzeigenschaften wurden in dieser Arbeit auch Kurzkanaleffekte und ihr Einfluss auf die Transistoreigenschaften ausführlich evaluiert. Auf Grundlage dieser Studien können folgende Aussagen getroffen werden: Der dominante Kurzkanaleffekt für die skalierten Transistoren ist der DIBL-Effekt (drain induced barrier lowering). Dieser wird vor allem vom Aspektverhältnis von Gatelänge zu Barrierendicke beeinflusst. Für GaN-Transistoren ist ein kritisches Aspektverhältnis von ungefähr 14 ausreichend, um den DIBL-Effekt zu unterdrücken.

Abschließend wurde eine erste Generation von MMICs basierend auf der entwickelten Transistortechnologie mittels S-Parameter- und Großsignalmessungen charakterisiert. Die untersuchten Verstärker weisen dabei eine Ausgangsleistung von 21.8 dBm bei 60 GHz und 22.8 dBm bei 94 GHz aus. Europaweit ist dies die erste erfolgreiche Demonstration von aus GaN-Transistoren bestehenden MMIC-Verstärkern für den Einsatz im W-Band. Weiterhin konnte gezeigt werden, dass die Produktionsausbeute der untersuchten Schaltungen mehr als 85% beträgt für 3-Zoll Wafer.

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List of Symbols

$C_{contact}$	Contact capacitance
C_{foot}	Gate foot capacitance
C_{fringe}	Fringe capacitance
C_{gate}	Capacitance of the whole gate module
C_{gd}	Drain-sided gate capacitance
C_{gs}	Source sided gate capacitance
C_{head}	Gate head capacitance
C_{para}	Parasitic capacitance
C_{side}	Capacitance of the gate foot sidewalls
D	Density of states
d_{bar}	Barrier thickness
d_{AlGaN}	Thickness of the Aluminum Gallium Nitride layer
d_{head}	Distance of the gate head from the semiconductor surface
d_{SiN}	Thickness of the passivation layer
E_c	Conduction band energy
E_{crit}	Critical energy field strength
E_F	Fermi energy
E_g	Band gap energy
E_n	Discrete energy level with regard to the Fermi level
E_v	Valance band energy
F	Potential energy
f_{max}	Maximum frequency of oscillation
f_T	Current-gain cut-off frequency
G	Large-signal gain
g_{ds}	Output conductance
g_{m_ext}	Extrinsic transconductance
g_{m_int}	Intrinsic transconductance
$I_{d,min}$	Minimum drain current
I_{sat}	Saturated drain current

L_g	Gate length
L_{gd}	Gate drain spacing
L_{gs}	Gate source spacing
L_{head}	Gate head overhang
m^*	Effective mass of electrons
n_e	Electron concentration
n_h	Hole concentration
n_s	Sheet carrier concentration
P_{dc}	Dissipated DC-power
P_{in}	Input power
P_{out}	Output power
P_{pi}	Piezo electric polarization
P_{sp}	Spontaneous polarization
q	Elementary electron charge
$R_{contact}$	Contact resistance
R_d	Drain resistance
R_g	Gate resistance
R_{gd}	Sheet resistance between drain and gate
R_{gs}	Sheet resistance between source and gate
R_i	Intrinsic load resistance
R_{on}	On-resistance
R_s	Source resistance
$\underline{S}_{11}$	input reflection coefficient
$\underline{S}_{12}$	reverse transmission coefficient
$\underline{S}_{21}$	forward transmission coefficient
$\underline{S}_{22}$	output reflection coefficient
t_{gb}	Aspect ratio of gate length to barrier thickness
U_{br}	Breakdown voltage
U_k	Knee voltage
v_{sat}	Saturated electron velocity

x_{Al}	Aluminum concentration
α	Scaling factor
μ_0	Low-field electron mobility
ε	Relative dielectric material constant
ε_0	Dielectric constant
σ	Polarization sheet charge
$\hbar$	Planck constant
Φ_b	Schottky barrier height
N_D^+	Number of ionized donors
N_A^-	Number of ionized acceptors

List of Abbreviations

2DEG	Two dimensional electron gas
Al	Aluminum
AlGaAs	Aluminum Gallium Arsenide
AlGaN	Aluminum Gallium Nitride
AlInGaN	Aluminum Indium Gallium Nitride
AlN	Aluminum Nitride
CMOS	Complementary metal oxide semiconductor
FIB	Focused Ion Beam
FP	Field plate
GaN	Gallium Nitride
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
InP	Indium Phosphide
IP	Internet protocol
LDMOS	Laterally diffused metal oxide semiconductor
MBE	Molecular beam epitaxy
MMIC	Monolithic microwave integrated circuits
mmW	Millimeter-wave
MOCVD	Metal-organic chemical vapor deposition
MOSFET	Metal oxide semiconductor field effect transistor
PAE	Power added efficiency
Si	Silicon
WLAN	Wireless local area networks

1. Introduction and State-of-the-Art

1.1 Demand of millimeter wave transistors with high output power and high efficiency

The development of semiconductor technology is driven by the desire of realizing more functionality in smaller chip areas, or of openining new markets for semiconductor devices. Silicon based transistors exhibit outstanding performances at very low costs for data processing applications. Compound semiconductors such as Gallium Nitride excel in applications where high power output powers are needed. In the last years intensive research and development have been conducted to increase the operating frequency of transistors based on compound semiconductors to meet the demand regarding high power and high frequency applications. One big market for such power amplifiers is the broadcasting of telecommunication signals [Mar10]. Today nearly 70% of the world population uses cell phones and 30% has access to the internet (see Figure 1-1). According to studies from the International Telecommunication Union the rapid growth of the worldwide telecommunication sector (shown in Figure 1-1) will continue in the next years [ITU10].

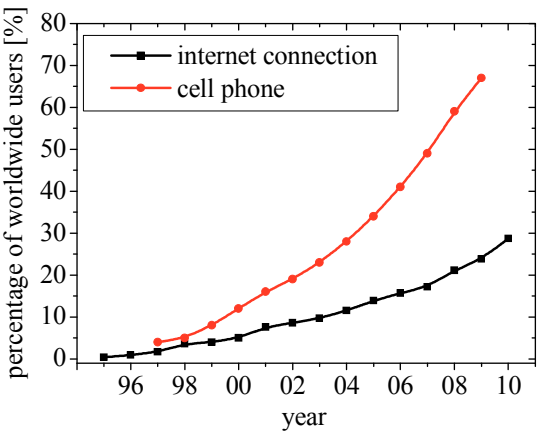

Figure 1-1: Growth of the wireless communication and access to internet services in the last decades. Data was taken from [ITU10] and [IWS10].

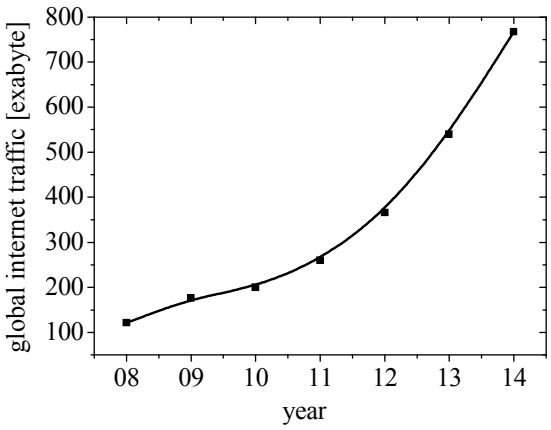

Figure 1-2: Development of the global internet traffic per year in Exabyte (from 2011-2014 estimation). Values are taken from [VNI10].

Due to the development of wireless local area networks (WLAN) and improvement of the mobile phone technologies, the previously distinct applications of personal computers, telephones and televisions are merging together. Today high-traffic internet-services such as video on demand and voice over IP are available to an increasing number of mobile users. The internet traffic volume per year, depicted in Figure 1-2, is expected to increase exponentially in the next years, and a global data volume of nearly 800 Exabyte will be reached in 2014 [VNI10]. With the increased data rates and consumer numbers the power consumption of the transmission systems will also grow exponentially if the systems are still based on Si-transistors in the future. To provide the architecture for the increasing demands of bandwidth, transistors which can operate at frequency bands well in the millimeter wave range are necessary. But the available broadcasting systems feature very low efficiencies per transmitted bit at these frequencies because many transistors have to be combined to achieve the necessary output power, and an active cooling system is required to dissipate the thermal losses from the transistors. These developments in the telecommunication market create an increasing demand for efficient power amplifiers with operating frequencies above 50 GHz to enable the high data rates and support the large user numbers.

Besides the telecommunication market, high power amplifiers with operating frequencies above 50 GHz can be utilized in a wide field of applications. The license-free frequency band between 57 and 64 GHz is of high interest [Smu02] for short range point-to-point wireless Gbit/s data transmissions. The extremely high atmospheric attenuation of V-band signals (50-75 GHz), due to a resonance of the oxygen or hydrogen molecule, is actually used as an advantage. The high dampening of the signal allows the addressing of many users in small areas without causing signal interferences which is ideal for next generation WLAN technologies or cable free high definition home cinema systems. Another application for V-band amplifiers is inter-satellite communication. The spectrum congestion at C-band from the operating satellites, demands the devel-

opment of new technologies to enable data transmissions between new communication satellites [Sui09] or positioning systems such as the Galileo Project. Besides the need in wireless communication, high power transistors are also being developed for automotive radar applications which operate at the frequency band between 74 and 77 GHz [Yos09]. These radar systems are an essential part of adaptive cruise control and safety systems of future automobiles.

In contrast to the above mentioned short range applications the atmospheric radio window at 94 GHz allows the development of many long range systems. With amplifiers, which can operate at this frequency, sensor systems can be developed to monitor the atmosphere and greatly improve long term weather forecast [Kyu09]. Similar amplifiers can also be utilized in radar systems for landing guidance under adverse weather conditions [Cea07] and therefore minimize the risk by landing without a clear line of sight to the ground. Also concealed weapon detectors can be fabricated using amplifiers at 94 GHz [Jun09]. But such radar systems are not limited to security applicationws but can also be utilized for industrial process controls of otherwise non-observable fabrication steps, which greatly enhances the production yield [Skl06]. Furthermore sensors systems are currently developed for real time high resolution optical observation of intercellular activities of cell cultures [Pic10]. Also non-lethal weapons can be constructed using high frequency high power amplifiers. These active denial systems transmit a narrow millimeter wave at 95 GHz which immobilize but do not harm the opponent. Such non-lethal weapons are especially needed to protect humanitarian or peacekeeping missions.

Compound semiconductors based on Gallium Nitride (GaN) possess unique material characteristics which theoretically allow the mass fabrication of transistors with high output power and high power-added efficiencies at frequencies well above 50 GHz. They are therefore a promising solution for the above mentioned applications. But due to the novel material a definite technology to achieve operating frequencies above 50 GHz was not available at the begin-

ning of this study. Therefore, a major field of the actual research regarding GaN-based HEMTs and one topic of this work is the improvement of the high frequency characteristics of GaN-transistors. The transistors are systematically characterized to determine the scaling behavior of our transistors regarding the developed technology and the novel material system. Finally, amplifier circuits operating in the frequency range between 50 to 94 GHz are presented to demonstrate the functionality of the developed transistor technology at chip level.

1.2 Chapter Outline

To place the research done in this work in context with the worldwide development of semiconductor technology a brief overview of the state of the art is given in the next sections of this chapter. For this purpose different material systems are compared in regard to their output power capabilities at high frequencies. Additionally, the historical development of GaN-based transistor technology is summarized and current research topics regarding this novel material system are presented to show the wide field of applications for GaN-electronics.

In the second chapter the common figures of merit for frequency and output power of field effect transistors are derived as a function of the device geometries and material properties. Furthermore, the theoretical scaling rules for our field effect transistor design are derived to provide the foundation of the studies and characterizations done in this work.

In chapter 3 the theory of AlGaN/GaN hetero epitaxy is described with special emphasis on adjusting the sheet carrier concentration by a variation of the barrier parameters. From these theoretical considerations wafers with specific barrier properties for mmW-transistors were developed and later used for the fabrication and analysis of high frequency transistors.

The technology used for the fabrication of AlGaN/GaN transistors is summarized in chapter 4 with the special emphasis on the scaling limits caused by the available technology and where the development of new technologies enabled a further device scaling.

In chapter 5 and 6 the transistors are characterized to determine the effective scaling laws of the fabricated devices. First the increase of the maximum transconductance is evaluated in chapter 5. Thereby, two different technologies to achieve thin barriers are discussed and their effect on other device parameter especially leakage currents. In the first part of chapter 6 the scaling behavior of all major geometries of the gate module is evaluated in regard to a reduction

of the gate capacitance. In the second part of the chapter, the influence of the passivation material on the parasitic gate capacitances is studied. Furthermore devices with source terminated field plates are analyzed in regard to a reduction of the drain-sided gate capacitance.
In chapter 7 short-channel effects are discussed, and design rules are derived to prevent these effects. Special emphasis is thereby taken to evaluate the critical aspect ratio of gate length to barrier thickness at which short-channel effects are successfully suppressed.
In chapter 8 large signal measurements of a first generation of power amplifiers with operating frequencies up to 94 GHz based on the millimeter wave transistors are presented as a proof-of-concept for the successful application of the developed technology at MMIC level.
In the final chapter all results are summarized and a short outlook is given how the high frequency and output power can be improved by further developments of the process technology or epitaxial growth.

1.3 Overview of state-of-the art transistors in regard to output power at high frequencies

To be competitive on the power electronics market, the output power and efficiency of novel transistors must exceed the values achieved by well established technologies based on Silicon, Gallium Arsenide or Indium Phosphide (see Figure 1-3). Transistors bases on these materials reach operating frequencies well above 100 GHz [Rad10]. However, these amplifiers can only operate at low voltages and therefore low power. To compensate these limitations, many amplifiers have to be combined to achieve the desired output power which leads to highly complex device architectures and a reduced efficiency of the whole system [Bas09]. High electron mobility transistors (HEMT) based on Gallium Nitride (GaN) and Aluminum Gallium Nitride (AlGaN) offer unique properties to achieve both high frequency and high power operation (see Figure 1-3).

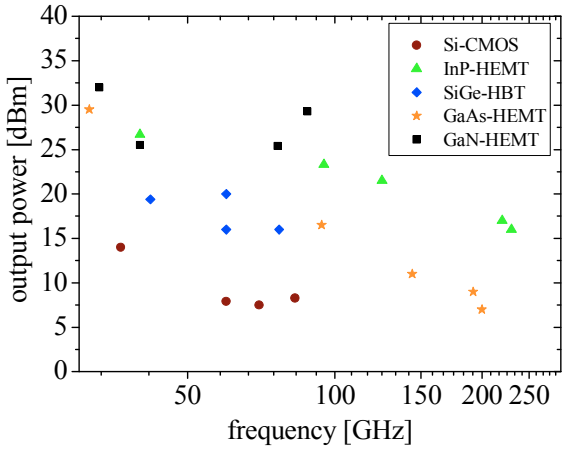

Figure 1-3: Overview of state of the art power amplifier of common semiconductor materials compared in regard to frequency and output power. Only the maximum reported values are shown in the diagram. The technologies and layout of the amplifiers can differ between material systems.

As can be seen in Table 1-1 the low field mobility and saturated velocity of GaN is equal or lower compared to other semiconductor materials. The outstanding material characteristic is the high critical breakdown field, which is mainly caused by the wide band gap of GaN. Combined with typical current densities in excess of 1.5 A/mm, GaN-based devices allow the highest output power densities at the same frequency (see Figure 1-3) among all available transistor technologies. Between 2-30 GHz GaN-transistors achieve output powers which are unmatched by any other material systems.But only few developments have been made in regard to highly scaled HEMTs with operating frequencies above 50 GHz. Recent publications by Micovic et al. [Mic10] showed an output power of 28.2 dBm at 88 GHz, which demonstrates the high power capability of GaN even at higher frequencies. The reason for the lack of high frequency and high power GaN amplifiers are due to the technological challenges to fabricate highly scaled devices based on the relatively new material system. Therefore, a brief overview of the process developments up to the present for GaN-based HEMTs will be given in the next section.

Table 1-1: Material parameter for commercially used semiconductors. The data are taken from technology reviews by Mishra et al. [Mis02], [Che04], [Mis08].

Parameter	Unit	Silicon	Gallium Arsenide (AlGaAs/ InGaAs)	Indium Phos-phide (InAlAs/ InGaAs)	Gallium Nitride (AlGaN/ GaN)
Band gap	eV	1.1	1.42	1.34	3.49
Electron mobility at room temperature (300 K)	cm^2/Vs	1500	8500	10000	1600
Saturation electron velocity	10^7 cm/s	1.0	1.3	1.0	1.3
Peak electron velocity	10^7 cm/s	1.0	2.1	2.3	2.1
Critical breakdown field	MV/cm	**0.3**	**0.4**	**0.5**	**3.0**

1.4 Overview of the development of GaN-based HEMT technology

Over the last two decades, great progress has been made regarding the technology of GaN-HEMTs. First proofs-of-concepts showed saturation currents of 20 mA/mm with transconductance of 28 mS/mm [Kha93]. The need for high power amplifiers led to an intensive research of GaN HEMTs in the following years and major breakthroughs in device processing as well as AlGaN/GaN hetero epitaxy were achieved. The major breakthroughs were:

- The application of Silicon Nitride (SiN) passivation to reduce the high frequency dispersion [Gre00].
- The development of Ti/Al/Ti/Ni based ohmic contacts with low contact resistance [Liu98].
- The use of an additional field plate structure and slanted gates to reduce electric field peaks and improve the breakdown voltage [And03], [Hos09].

- Commercially available Silicon Carbide (SiC) wafers of up to 4-inch diameters with low defect densities as substrates for the hetero epitaxy [Mul02], [Smi08]
- Improvement of the breakdown voltage and the leakage currents by using Fe-doped GaN-buffers [Bra05].
- Adoption of a GaN cap layer to improve reliability and Schottky barrier height [Kha02], [Aru05].

Due to these developments, amplifiers with output powers of 12-200 W at frequencies of 3-18 GHz are commercially available today [Cre10], [Sed10], [Tri10].

1.4.1 State-of-the-Art of GaN millimeter wave technology

The recent research regarding millimeter-wave technologies concentrates mostly on the restrictions and challenges which are caused by the material system and the very small critical dimensions necessary for the fabrication of mmW-transistors. In Figure 1-4 a schematic cross section with all major design geometries of a HEMT is shown.

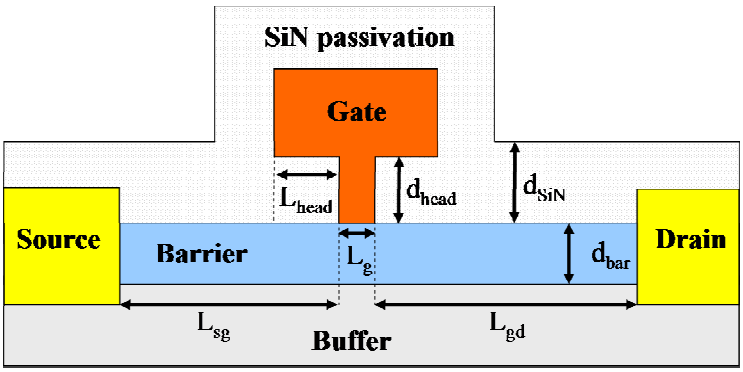

Figure 1-4: Schematic cross section of a HEMT with all major design dimensions: L_{sg} is the source to gate spacing, L_{gd} the gate to drain spacing, L_{head} the length of the gate head overhang, L_g the gate length, d_{head} the distance from the semiconductor surface to the gate head, d_{bar} the thickness of the barrier and d_{SiN} the thickness of the SiN-passivation layer.

The most common development is the scaling of all device geometries, in particular the barrier thickness (d_{bar}) and gate length (L_g) [Chu10], [Hig08]. As d_{bar} becomes smaller L_g has to be reduced as well to keep the aspect ratio of the gate length to barrier thickness (t_{br}) constant. If t_{br} becomes too small, field effect transistors exhibit severe short-channel effects which greatly limit the performance of the device [Jes07]. Also the fact that the barrier thickness has to be scaled down to a few nanometers causes many severe parasitic effects. Due to the short distance of the channel to the gate, more electrons can tunnel through the barrier which increases the gate leakage currents [Pol08]. Thin barriers have also a significant effect on the high frequency dispersion. The primary causes of this effect are charged surface states located next to the gate foot [Gre00]. If d_{bar} is reduced, the influence of these surface traps increases and thereby the high frequency dispersion. To prevent the charging of the surface states, GaN-based HEMTs are passivated with a thick layer of Silicon Nitride (SiN) [Gre00]. These passivation layers are also needed to achieve a good reliability of the device [Kim03] and can therefore not be omitted, especially if the transistor technology should be used to fabricate amplifier circuits. But if the gate is fully covered in SiN (see Figure 1-4) the parasitic capacitance of the gate module increases which drastically deteriorates the high frequency characteristics. Therefore, novel passivation technologies are being studied to optimize the gate capacitance and reduce the DC-RF current slump [Hig08].

Besides the improvements in process technology, modified layer stacks of the barrier and buffer are also being studied [Sun10]. The incorporation of a 1-2 nm thin Aluminum Nitride (AlN) spacer increases the sheet carrier concentration in the channel and improves the low field mobility due to a better confinement of the electrons. But reported values for the access resistances of ohmic contacts which are fabricated on wafers with an AlN spacer are currently four times higher than the contact resistances achieved on AlGaN/GaN heterostructures [Dee10]. However for mmW-transistors extremely low contact resistances are needed to minimize the high frequency performance loss caused

by source resistance. Another research topic regarding the barrier design is the development of double heterostructures. Due to the incorporation of an AlGaN or InGaN layer inside the buffer, the conduction band offset causes a back barrier for the electrons. As a result the modulation efficiency of the gate enhances and short-channel effects are reduced [Sun10].

A major concern of GaN-electronics is the relatively high production cost compared to established technologies. One cause for this disadvantage is the high price of SiC substrates. To minimize the production costs, great efforts are made to enable a heteroepitaxy on much cheaper Silicon substrates. First proves-of-concept for millimeter wave GaN-HEMTs on Silicon substrates have been shown by Sun et al. [Sun09] but the output powers are halved compared to similar devices on SiC substrates [Sun10]. In Table 1-2 current technologies for mmW-HEMTs based on GaN are summarized and compared with regard to their high frequency characteristics. As figures of merit the current-gain cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) are used. A detailed description of the correlation between f_{max} and f_T and the device geometries and technologies will be given in chapter 2.

Table 1-2: Recent research and developments of high frequency GaN-based HEMTs. The transistors are compared with regard to passivation thickness (d_{SiN}), gate length (L_g), barrier thickness (d_{bar}), current-gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}).

Technology	d_{SiN} [nm]	L_g [nm]	d_{bar} [nm]	f_T [GHz]	f_{max} [GHz]	Source
gate recess	0	60	< 10	**70**	**300**	Chu10
in situ passivation + AlN spacer	2	60	6	**190**	**241**	Hig08
AlInGaN back barrier + AlN spacer	100	100	11	**144**	**137**	Sun10
AlInGaN barrier + Silicon substrate	100	100	10	**102**	**89**	Sun09
Silicon substrate	100	75	20	**107**	**150**	Tir10

1.4.2 Further research topics regarding GaN-HEMT technology

Beside the development of mmW-transistor technology, various other research projects are currently being conducted regarding GaN-based electronics. To complete the overview of the ongoing research in HEMT technology, a short summary of these other topics will be given in the following section.

A major field of research is the further improvement of gain, output power densities and power added efficiency of GaN-HEMTs for C to K band amplifiers. The wide field of research involves, but is not limited to:

- The fabrication and design of novel shield-plate technologies [Küh10a], [Küh10b].
- The study of advanced amplifier concepts which are available due to the high power, high frequency characteristics of GaN-based HEMTs [Hei10].
- The evaluation of novel device packaging technologies [Ree10], [Riu10].

The enhancement of the reliability is also of great importance for the development of market ready power amplifiers [Wen10]. Long time stress tests indicate that GaN-based transistors possess unique degradation mechanisms which are still not completely understood. Therefore one direction of the current research is the development of new technologies to improve the reliability and counteract the unique degradation mechanisms [Bae10], [Dam09]. Beside the research regarding power amplifiers, GaN-based HEMTs are also developed for high power switching applications. The main goal in this field of research is the improvement of the breakdown voltage well above 500 V. Therefore, metal insulator semiconductor HEMTs (MIS-HEMT) or multilayer field plate designs are currently studied and promising proofs-of-concept have already been reported [Bah10], [Kam10].

2. Figures of merit and scaling properties of high electron mobility transistors

For the successful scaling of transistor devices, it is necessary to understand how the electrical properties of the devices are related to the transistor geometries which were introduced in Figure 1-4. Therefore the most common characteristics to compare mmW-transistors will be derived as a function of design parameters and material constants in this chapter.

With the scaling of the transistor geometries, restricting conflicts between different parameters can occur or the same transistor geometry can have an opposite effect on either the high frequency or power characteristics. Further short-channel effects can significantly reduce the power performance of highly scaled transistors. All these limitations will be discussed and scaling strategies will be defined to optimize the high frequency- and high power operation at the same time.

2.1 Small-signal figures of merit

Small-signal measurements are of vital importance for the characterization of millimeter-wave transistors. In the following sections the concepts of small-signal measurements and the equivalent circuit model used in this work are presented. From these considerations, the figures of merits regarding the current-gain and power gain are derived for an ideal transistor. In this work mainly the constant field scaling of HEMTs will be discussed due to the fact that a constant voltage scaling would lead to extremely high electrical field strength at the gate edge, which would cause an avalanche breakthrough under normal device operation.

2.1.1 Small-signal modeling

A transistor can be fully described as a two port network. The device-under-test is considered as a black box and connected at the input to a high frequency signal generator as well as to a load impedance at the output (see Figure 2-1). The input and output voltages are u_1 und u_2 whereas the corresponding currents are i_1 and i_2. The device can than be described using a set of correlation parameters between the different voltages and currents. Depending on the measurements conditions many network parameters can be derived. A common variant are the Y-parameters which are defined as follows:

$$\begin{pmatrix} \underline{i}_1 \\ \underline{i}_2 \end{pmatrix} = \begin{pmatrix} \underline{y}_{11} & \underline{y}_{12} \\ \underline{y}_{21} & \underline{y}_{22} \end{pmatrix} \begin{pmatrix} \underline{u}_1 \\ \underline{u}_2 \end{pmatrix}. \tag{2.1}$$

To measure each Y-parameter, perfectly open and short-circuits at the input and output of the device must be realized. At millimeter-wave frequencies, these necessary conditions can no longer be achieved. Therefore S-parameter measurements are commonly used at high frequencies. They are defined as power ratios of traveling waves at the input and output of the test device. However, Y-parameters are more directly related to physical components of the transistor as S-parameters and are therefore still used to discuss the properties

of mmW-transistors. Because both network parameters describe the same device they can be converted using simple formulas [Fri95].

Each set of parameters is only valid at the measured frequency. In order to completely characterize the transistor, the small-signal parameters are commonly measured over a wide frequency range. The complete data set is than fitted to a defined model which can be used to interpret the device characteristics regarding the technology or to design integrated circuits based on the measured transistor. In this work a small signal equivalent circuit consisting of discrete electronic elements is utilized to interpret the S-Parameter measurements. In the next sections the specific model used in this work is briefly described. Furthermore the various device properties and figures of merit of HEMTs are derived.

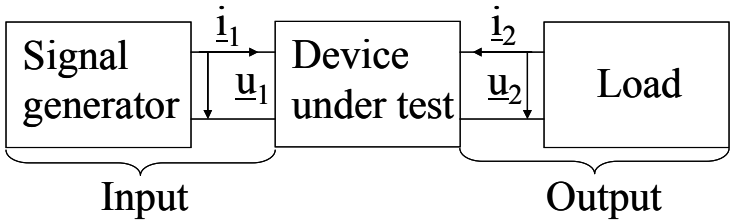

Figure 2-1: Schematic diagram of the two port concept used to characterize transistors.

2.1.2 Small-signal equivalent circuit

A transistor can be described using an equivalent circuit out of discrete elements. In Figure 2-2 the small-signal equivalent circuit used in this work is displayed. If the network parameters are known all the elements of the equivalent circuit can be derived [Shi95], [Qua02].

The small-signal equivalent circuit is commonly divided into an intrinsic and extrinsic shell (see Figure 2-2). The intrinsic components are necessary to describe the transistor function whereas the extrinsic shell defines the parasitic components of the transistor.

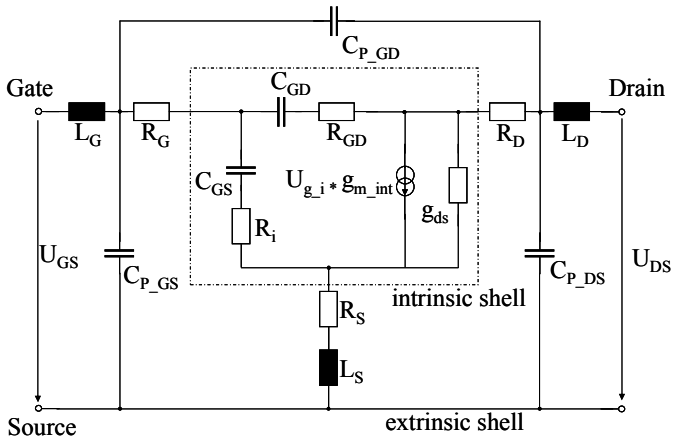

Figure 2-2: Small-signal equivalent circuit for HEMTs with the following elements: L_G, L_D and L_S are the gate, drain and source inductance; R_G, R_S and R_D are the gate, source and drain resistances; C_{P_GS}, C_{P_GD} and C_{P_DS} are extrinsic capacitances between the cor-responding pads; R_i is the intrinsic gate load resistance; C_{GS} and C_{GD} are the source and drain-sided gate capacitances; g_{m_int} and g_{ds} are the intrinsic transconductance and output conductance; U_{g_int} is the intrinsic gate voltage.

In Figure 2-3 scanning electron microscopy (SEM) pictures of a typical HEMT transistor used in this work is depicted as well as a focused ion beam (FIB) cross section of the active area of the transistor. As can be seen, the intrinsic transistor is just a very small part of the whole device. Most of the device area is occupied by large contact pads, necessary to connect the HEMT with probes for

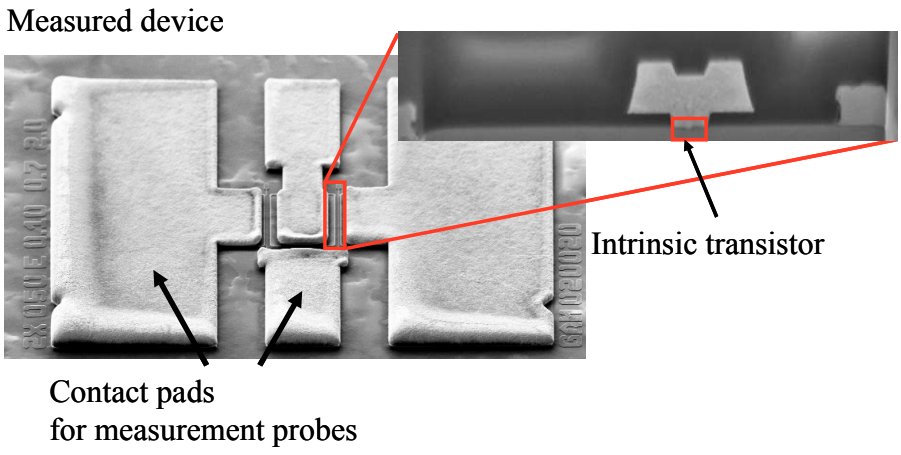

Figure 2-3: HEMT device fabricated in the course of this work with large contact pads for measurements and cross section of the active area with the intrinsic transistor.

the measurements to characterize the transistor. Under measurement conditions the contact pads generate a capacitive coupling (C_{pad}) between each other which distort the results of the measurements.

Because the transistors are later used in integrated circuits and directly imbedded in the layout (see Figure 2-4) it is extremely important to evaluate the capacitive influence of the contact pads. Determination of the elements of the small-signal equivalent circuit is only the first step in developing new transistor technologies. In theory the gate source capacitance (C_{gs}) and gate drain capacitance (C_{gd}) are only defined by the gate foot (see Figure 2-3). For practical HEMTs these capacitances are additionally a function of the parasitic capacitances generated by the gate head which will be discussed in more detail in section 2.4.

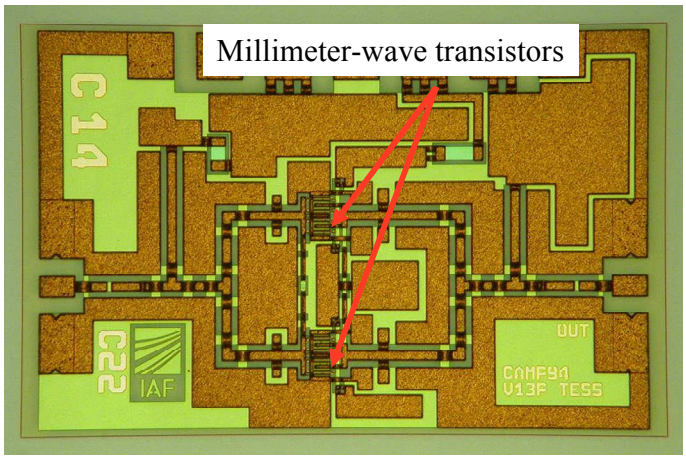

Figure 2-4: Power amplifier with two integrated millimeter wave transistors.

2.1.3 The small-signal current-gain and current-gain cut-off frequency

The most common characteristic used to compare high frequency transistors is the small-signal current-gain cut-off frequency (f_T) [Sch01], which is derived from the small-signal current-gain (h_{21}) given by:

$$h_{21} = \frac{-\left|\underline{S}_{11}\right|}{\left(1-\left|\underline{S}_{11}\right|\right)\cdot\left(1+\left|\underline{S}_{22}\right|\right)+\left|\underline{S}_{12}\right|\cdot\left|\underline{S}_{21}\right|}, \tag{2.2}$$

where $\underline{S}_{11}$ is the input reflection coefficient, $\underline{S}_{21}$ the forward transmission coefficient, $\underline{S}_{12}$ the reverse transmission coefficient and $\underline{S}_{22}$ the output reflection coefficient for a 50 Ω terminated network at the input and output. Normally h_{21} is not given as a dimensionless ratio but in decibels in the form of:

$$h_{21}[dB] = 20\log_{10}(h_{21}). \tag{2.3}$$

In Figure 2-5 the small-signal current-gain (h_{21}) is depicted for HEMTs fabricated in this work. As can be seen in the diagram the slope of h_{21} corresponds very well to the theoretical decrease of -20 dB per decade. The cut-off frequency (f_T) is reached when h_{21} is equal to 0 dB (see Figure 2-5). Due to the parasitic elements from the contact pads the values for h_{21} at high frequencies or near 0 dB diverge from the linear behavior. Therefore, a well established method to extract the cut-off frequency is to fit the measurement data at lower frequencies to the -20 dB slope [Sch01]. If the cut-off frequency is known, the small-signal current-gain (h_{21}) for all frequencies can be calculated. Due to this fact f_T is a common figure of merit to compare different technologies in regard to their small-signal current-gain.

As can be seen in the Figure 2-5, h_{21} depends strongly on the device technology, especially the scaling of the device geometries which is indicated by the reduced gate length. But many more design parameters have to be considered. In order to identify the major geometries for a successful device scaling the influence of the physical device parameters on the cut-off frequency will be discussed in the next sections.

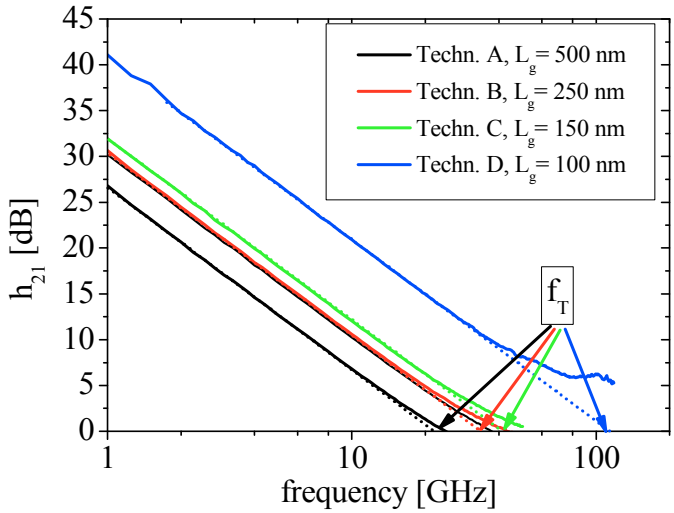

Figure 2-5: Small-signal current-gain and extrapolated cut-off frequency for AlGaN/GaN HEMTs with different technologies and device scaling.

2.1.4 Constant field scaling of an ideal transistor regarding the small-signal current-gain

Neglecting the influence of parasitic elements the current-gain cut-off frequency can be given as [Sch03]:

$$f_T = \frac{g_{m\_\mathrm{int}}}{2\pi C_{foot}}. \tag{2.4}$$

Where $g_{m\_int.}$ is the intrinsic transconductance of the transistor and C_{foot} is the capacitance of the gate foot.

One method to enhance the cut-off frequencies of field effect transistors is to increase the transconductance while keeping the electric field of the gate foot constant (constant field scaling). For an ideal transistor without parasitic capacitances, C_{foot} can be calculated from the small-signal equivalent circuit as the sum of the source-sided gate capacitance (C_{gs}) and the drain-sided capacitance (C_{gd}). For HEMTs g_{m_int} can be given as a function of the device geometries as well as material constants of the barrier and electron channel as follows [Die01]:

$$g_{m\_\mathrm{int}} = \frac{\varepsilon\varepsilon_0 v_{sat}}{d_{bar}}\left(1 - \frac{1}{\sqrt{1 + 2q\dfrac{\mu_0 n_s d_{bar}}{\varepsilon\varepsilon_0 v_{sat} L_g}}}\right), \tag{2.5}$$

with L_g the gate length, d_{bar} the barrier thickness, v_{sat} saturation velocity, μ_0 the low-field mobility, n_s the sheet carrier concentration of the electron channel and ε the dielectric constant of the barrier.
If the gate length is very short equation (2.5) becomes:

$$g_{m\_\mathrm{int}} = \frac{\varepsilon\varepsilon_0 v_{sat}}{d_{bar}}. \tag{2.6}$$

As can be seen in (2.6) the intrinsic transconductance is dominated in this case by the saturation velocity of the electrons inside the channel and by the barrier thickness. The most accessibly parameter is d_{bar} which must be scaled down to increase f_T. But to keep the lateral electric field of the gate and therefore C_{foot} constant the gate length must be reduced by the same factor as d_{bar}

2.1.5 The small-signal power-gain and maximum frequency of oscillation

Up to now only the current-gain figure of merit was discussed, but for the design of power amplifiers the power-gain is the more important parameter. In general the power gain is the ratio of the output power to the input power of the transistor. But in actual measurements the power gain is influenced by the matching conditions between transistor, load and signal generator. Furthermore, a possible self oscillation of the transistor must be suppressed if the transistor is used for power amplification. Therefore several small-signal power-gain definitions are commonly used which will be described briefly in this section.

A transistor is unconditionally stable at a certain frequency if the stability factor (k) is greater than unity whereas k is defined by [Rol62]:

$$k = \frac{1 + \left|\underline{S}_{11} \cdot \underline{S}_{22} - \underline{S}_{12} \cdot \underline{S}_{21}\right|^2 - \left|\underline{S}_{11}\right|^2 - \left|\underline{S}_{22}\right|^2}{\left|\underline{S}_{12}\right|^2 \cdot \left|\underline{S}_{21}\right|^2}, \tag{2.7}$$

Given this definition, the following small-signal power gains can be derived:

If the stability factor is greater unity, a self-oscillation of the transistor cannot occur regardless of the input and output impedances. Given a perfect matching of the transistor to the load and the signal generator the transistor delivers the maximum available gain (MAG). The MAG can be calculated by:

$$MAG = \frac{\left|\underline{S}_{21}\right|}{\left|\underline{S}_{12}\right|}(k - \sqrt{k^2 - 1}), \text{ for } \underline{y}_{12} \neq 0 \text{ and } k \geq 1 \tag{2.8}$$

For k-factors smaller than unity the transistor can become unstable depending on the gain, as well as the existing input and output matching. In this case the maximum stable gain (MSG) is often given to describe the gain of the transistor up to which no self-oscillation can occur regardless of the operating conditions

$$MSG = \frac{\left|S_{21}\right|}{\left|S_{12}\right|}, \text{ for } \underline{y}_{12} \neq 0 \text{ and } k < 1. \tag{2.9}$$

The unilateral gain (U) is defined as the maximum gain if the output-to-input feedback is compensated for each frequency. Due to the fact that an output-to-input feedback greater than zero is necessary for an unintentional oscillation, the unilateral gain is independent of the k-factor.

$$U = \frac{\left|\underline{S}_{21}\right|^2}{\left(1 - \left|\underline{S}_{11}\right|^2\right) \cdot \left(1 - \left|\underline{S}_{22}\right|^2\right)}, \tag{2.10}$$

Similar to the current-gain, the power gains are commonly given in dB whereas MAG and U decrease with a slope of -20 dB per decade, and MSG with -10 dB per decade.

2.1.6 Constant field scaling of an ideal transistor regarding the small-signal power-gains

Similar to the current-gain cut-off frequency, the figure of merit for the small-signal power gain is the maximum frequency of oscillation (f_{max}). This value is reached when the power gain equals unity. Depending on the power gain definition f_{max} can be derived from MAG or U. In this work, mainly MSG and MAG are used to compare different transistors and technologies and therefore f_{max} is based on the MAG values ($f_{max,MAG}$). A rough estimation of $f_{max,MAG}$ for an ideal HEMT can be given as [Sch01]:

$$f_{\max,MAG} \sim \sqrt{\frac{\pi}{8}\frac{f_T}{R_g C_{gd}}}\,. \tag{2.11}$$

As can be seen in (2.11), the maximum frequency of oscillation is a function of the cut-off frequency (f_T), gate line resistance (R_g) and the drain-sided gate capacitance (C_{gd}). If R_g is kept constant and f_T can be scaled by the factor α, f_{max} will increase with $\alpha^{1/2}$. In Figure 2-7 the MSG/MAG values, $f_{max,MAG}$ and the point where k equals unity is shown for different scaled technologies. In the diagram only the gate length is shown as an indicator for the scaling process. Actually many more device geometries were scaled down from technology A to D, such as barrier thickness, passivation thickness, the gate head overhang and source drain distance. As can be seen the scaled HEMTs fabricated with our mmW-technology follow the general trend given by (2.11). It is therefore not necessary to discuss the scaling of f_{max} individually and most of the time only f_T will be evaluated in detail, in this work. According to formula (2.11) the gate drain capacitance must be reduced by the scaling factor to achieve the same increase as the cut-off frequency. As will be discussed in chapter 2.3 this reduction can only be accomplished by a scaling of the parasitic gate capacitances.

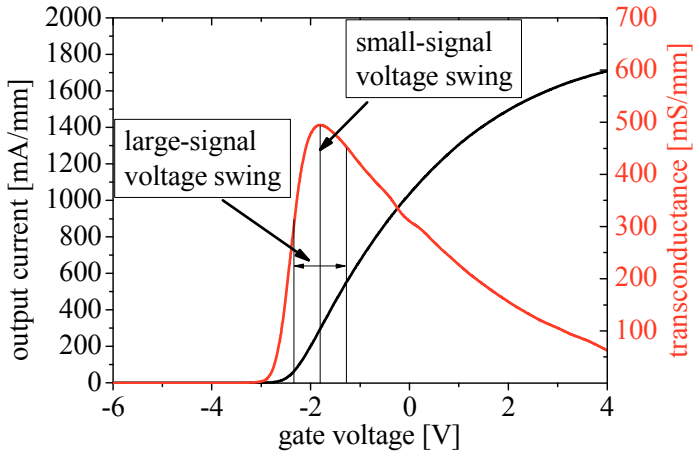

Figure 2-6: Transfer characteristic of an AlGaN/GaN HEMT. The small and large-signal voltage swings are only a schematic depiction and do not represent actual measurement conditions used in this work.

The small-signal power-gains are measured at the maximum transconductance and at very low input powers. In Figure 2-6 the transfer characteristic of a typical HEMT fabricated in this work is depicted.

As can be seen the transconductance exhibits a very narrow peak. If the transistor is measured at large input powers, the transistor is not always operating at the peak transconductance due to the greater voltage swing of the input signal. As a consequence, the large-signal gain is always lower than the small-signal gain. Additionally a perfect output and input matching of the transistor cannot be achieved with our available measurement equipments. Therefore, the large-signal power-gain measured in this work is typically reduced by 3 dB compared to the MSG/MAG values under the condition that the transistor is operating in the linear gain region (see chapter 8). Given these conditions, the small-signal power-gains are viable figures of merit for the development of power transistors under large signal operations. To completely describe the small-signal power gain over all frequencies, it is not sufficient to know f_{max} alone. Due to the different slopes of MSG and MAG the frequency at which MSG equals MAG is of vital importance. Because the k-factor equals unity at this frequency the value is often called k-point. The k-point depends highly on

the parasitic elements of the transistor and will therefore be discussed in more detail in chapter 2.3.

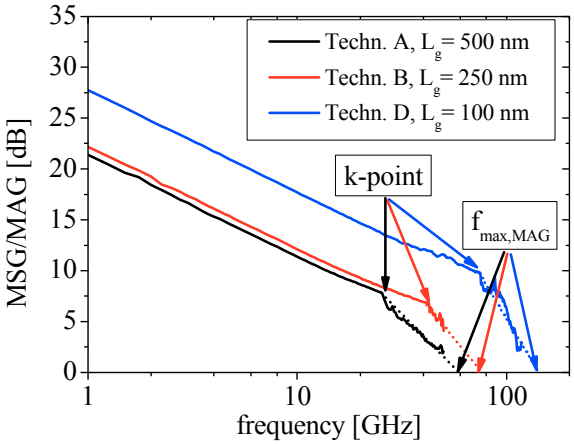

Figure 2-7: Maximum stable gain (MSG), maximum available gain (MAG), k-point and extrapolated maximum frequency of oscillation ($f_{max,MAG}$) for AlGaN/GaN HEMTs with a gate width of 100 µm but different technologies and device scaling. All devices were measured at maximum transconductance and 7 V drain bias.

2.2 Figures of merit regarding the output power

In order to compare the power performance, the most common figures of merit are the saturated output power (P_{out}) and the power added efficiency (PAE). In this chapter these parameters will be discussed using a transistor in class-A operation. The design rules derived from this discussion can also be used for other operation modes.

2.2.1 Maximum output power

Assuming sinusoidal input signals, the output power in class-A operation can be calculated by:

$$P_{out} = \frac{1}{8}\left(I_{sat} - I_{d,\min}\right)\left(U_{\max} - U_k\right). \tag{2.12}$$

The saturation current (I_{sat}) is defined by the sheet carrier concentration and saturated velocity of the electrons in the channel:

$$I_{sat} = q\, n_s v_s\,. \tag{2.13}$$

A reduction of n_s due to device scaling or parasitic effects has therefore a significant negative impact on I_{sat} and subsequently on the output power.

The output power is also decreased by a poor pinch-off characteristic at high drain voltages. Due to a low modulation efficiency or buffer isolation, a significant drain current ($I_{d,min}$) can flow at high drain voltages which will severely reduce the output power. The limit of the maximum drain voltage (U_{max}) is the breakdown voltage (U_{br}) of the device. Most GaN-HEMTs exhibit an avalanche breakdown. If the space charge region at the drain side reaches the ohmic contact and the drain voltage is further increased, the electric field along the drain side rises until the critical field strength is reached and impact ionization occurs. A common approach to enhance U_{br} is to increase the gate drain spacing. But such a design will have a negative effect on the knee voltage (U_k) which is a function of the on-resistance (R_{on}) (see Figure 2-8). If the transistor operates in the unsaturated region the drain current is limited by the on-resistance which is equal to the sheet resistance of the whole transistor area and the contact resistances of source and drain. If the source-drain spacing is increased the transistor will exhibt a higher R_{on} and will therefore saturate at a higher knee voltage.

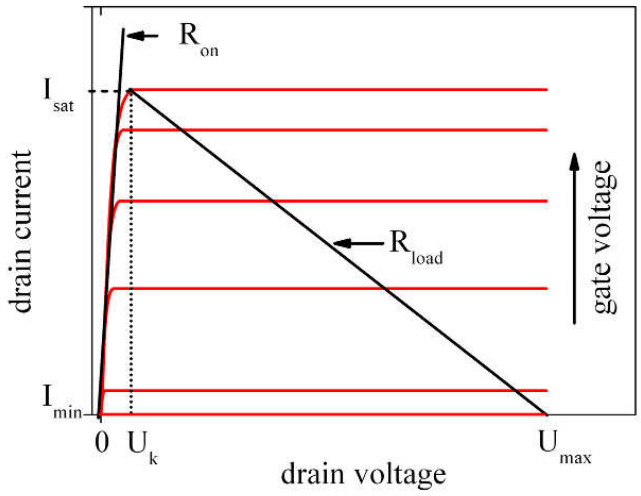

Figure 2-8: Schematic diagram of the output characteristics of a transistor in class-A operation.

But this conditions will decrease the possible maximum output power of a transistor in class-A operation (see (2.12)). Therefore, L_{gd} must be designed for high-frequency power amplifiers in such a way that both voltages are optimized at the same time.

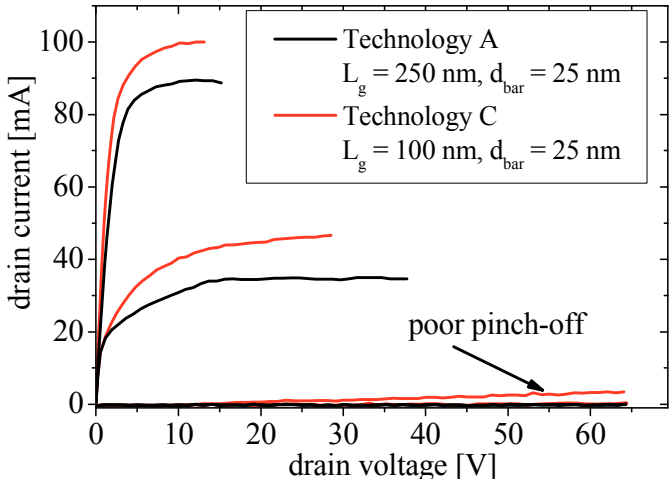

Figure 2-9: Output characteristic of AlGaN/GaN HEMTs fabricated with two different technologies. Technology C exhibits a poor pinch-off at high drain voltages compared to technology A.

2.2.2 Power added efficiency

The power added efficiency is the second important figure of merit for the power characteristics and is defined by:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out}}{P_{dc}}\left(1 - \frac{1}{G}\right), \tag{2.14}$$

with P_{dc} the DC power delivered to the transistor, P_{out} the RF output power, P_{in} the RF input power and G the large signal gain.

As discussed before, the output power is reduced due to parasitic resistances, leakage currents and the high frequency dispersion. These effects are the main reason for a poor PAE regarding the technology of power amplifiers. Another device parameter which directly influences the PAE is the large signal gain of the transistor as can be seen in (2.14). A high gain is therefore not only necessary to enable a high output power but also to achieve an optimum efficiency.

2.3 Non-idealities and parasitic effects regarding the device scaling and process technology

The transistor design used in this work (see Figure 1-4 and Figure 2-3) possesses many parasitic elements. Beside these parasitics some design parameters have an opposite effect on the high frequency characteristics or output power and must be chosen in such a way that both device characteristics are maximized.

For a successful scaling of our transistor technology all parasitic effects and limitations must be identified in order to develop a technology for mmW-transistors. In the next section these effects will be discussed, and a brief outlook will be given regarding the solutions evaluated in this work.

2.3.1 Parasitic effects of thin AlGaN barriers

In general, AlGaN/GaN-HEMTs with thin barriers can exhibit two major parasitic effects which are an increased gate leakage current and an enhanced RF dispersion.

With reduced barrier size the probability of an electron tunnelling through the barrier increases exponentially [Tak98]. For ideal group III-N barriers with a perfect crystal lattice, the critical dimension for which a significant tunnel current can flow is only a few nanometers [Pol08]. But in actual epitaxial layers stacking faults and impurities can generate traps which enhance the tunneling current. The lower limit of d_{bar} can therefore be much larger.

AlGaN/GaN HEMTs exhibit a current slump at high frequencies. This dispersion effect is caused by charged surface states located next to the gate [Vet01]. Due to the high electric field at the drain side of the gate, electrons can tunnel through the barrier and occupy these surface states. At high frequencies the trapped electrons cannot follow the electric field from the gate and as a result, the region at the drain-side of the gate becomes charged. The electric field from the charged traps depletes the electron channel and causes a reduction of

the drain current. If the barrier thickness is scaled down, the influence of the surface traps increases which severely reduces the output power of the transistor [Til01].

The technologies used, to achieve thin barriers can cause further challenges for the development of mmW-HEMTs. The scaling of the barrier thickness of GaN-based HEMTs can be achieved by two methods, either by the growth of thin barrier layers or by an etching of the barrier in the gate region, therefore often called gate recess [And10]. Each one imposes different challenges to the scaling of the transistor.
The sheet carrier concentration of AlGaN/GaN HEMTs depends inversely on the barrier thickness [Amb99]. But this effect can be compensated by an increase of the Al-concentration of the barrier [Amb00]. Therefore, the growth of AlGaN/GaN heterostructures and the influence of the barrier properties on the sheet carrier concentration is of great importance for the development of AlGaN/GaN mmW-HEMTs and will be discussed in more detail in chapter 3.
If an additional gate recess is used to enable thin barriers, the sheet carrier concentration in the source and drain regions is not affected and the same barrier structure can be used for different transistor technologies. But GaN and its ternary compounds are highly chemically stable. Therefore, wet etching methods are not available for the processing of GaN-HEMTs [Zhu05] and plasma etching processes must be utilized for the gate recess. But such dry etching processes can damage the crystal structure of the remaining barrier or cause an unintentional doping of the heterostructures with ions from the etching plasma. These impurities and crystal damages act as traps and enhance the gate leakage currents [Pan09]. At the beginning of this work a definite process to scale the barrier of AlGaN/GaN HEMTs was not available. In this work two different technologies to achieve thin barriers were developed: the growth of a thin barrier layer, and the dry etching of the AlGaN-layer in the gate region. Both technologies will be evaluated in chapter 5 with respect to an improvement of the intrinsic transconductance. Further the influence of the different

technologies on the leakage currents and high frequency dispersion will be studied.

2.3.2 Influence of the source resistance on the transconductance

In practical field effect transistors the extrinsic transconductance is significantly lower than the intrinsic transconductance. The applied gate voltage is reduced by the voltage drop across the source resistance which causes a reduction of the extrinsic transconductance and cannot be neglected in an analysis for AlGaN/GaN HEMTs [Rus07]. Both transconductances are correlated by:

$$g_{m\_ext} = \frac{g_{m\_\mathrm{int}}}{1 + R_S g_{m\_\mathrm{int}}}. \tag{2.15}$$

In order to achieve high extrinsic transconductances the loss caused by the source resistance (R_S) has to be minimized. The source resistance, like all other elements of the small-signal equivalent circuit, is frequency dependent. Because of the small electrical field and the absence of a space charge region at the source side of the transistor, R_S correlates very well with the values obtained by DC-measurements. In this case, the source resistance can be described as the sum of the ohmic contact resistance (R_{con}) and the sheet resistance between source and gate (R_{gs}):

$$R_S = R_{gs} + R_{con} \text{ with } R_{gs} = \frac{L_{gs}}{\mu_0 n_s q}, \tag{2.16}$$

In order to scale R_S both the sheet resistance between source and gate and the contact resistance must be minimized.

The sheet resistance (R_{gs}) is a function of the low field mobility and sheet carrier concentration, and can be optimized if n_s and μ_o are increased. Both parameters are influenced by the quality of the hetero epitaxy and the barrier properties especially barrier thickness and Aluminum content. A detailed description of the correlations between the different parameters will be given in chapter 3.

The spacing between source and gate (L_{gs}) is the only design parameter which can reduce the source resistance. But with shorter L_{gs} the contact resistance can limit the scaling of R_s. Therefore, one part of this work will be to evaluate the scaling behavior of the source resistance regarding the source gate spacing and the influence on the transconductance (see chapter 5).

2.3.3 Parasitic capacitances of the gate module

In Figure 2-2 the small-signal equivalent circuit was introduced. According to this model the intrinsic gate capacitance is expressed by the drain and source-sided gate capacitance (C_{gs} and C_{gd}). As can be seen in Figure 2-10, the gate capacitance for the common HEMT layout is far more complex. Both capacitances are a superposition of many parasitic elements and the gate foot capacitance (see Figure 2-10). For our HEMTs processed C_{gd} is nearly independent of the gate foot length (see Figure 2-11). This trend is a common behavior among FETs and C_{gd} is therefore often associated with the parasitic capacitances but this correlation is only a rough approximation and cannot be used for a detailed analysis. If the gate length is scaled down without a scaling of the gate head, the gate capacitance will be dominated by the parasitic elements.

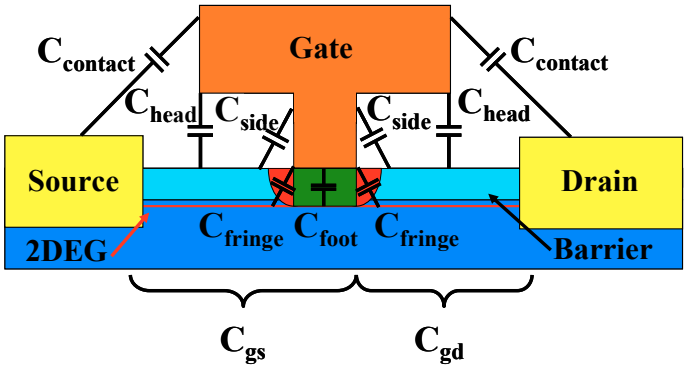

Figure 2-10: Schematic cross section of a HEMT with all capacitances of the gate module.

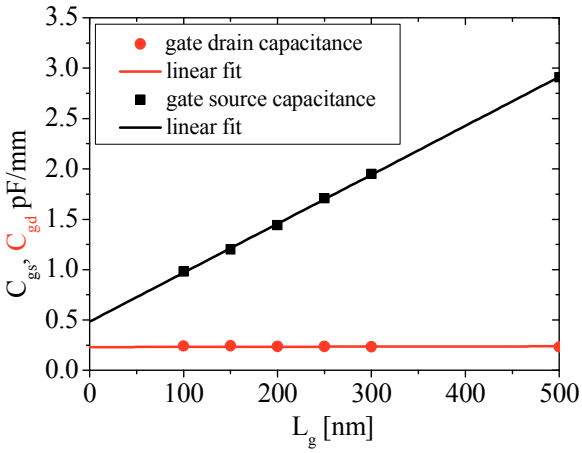

Figure 2-11: Extrapolated gate drain and gate source capacitance from S-parameter measurement for AlGaN/GaN HEMTs with gate length from 100 to 500 nm but otherwise same device layout and process technology.

As can be seen in Figure 2-11, the extrapolation of the measured gate capacitances results in a total parasitic offset of 0.75 pF/mm for this particular technology whereas the capacitance of a 100 nm gate foot is only 0.5 pF/mm which can be derived from the slope of C_{gs} over L_g or by substraction the off set capacitcances from the sum of C_{gs} and C_{gd} at L_g = 100 nm. To improve the ratio of the parasitic to the gate foot capacitances the parasitic elements must also be scaled down. It is therefore necessary to evaluate the capacitive influence of each part of the gate module for the development of highly scaled HEMTs. The exact correlation between the geometries of the gate module and the corresponding capacitances depends thereby strongly on the process technology and layout of the transistor. Therefore all capacitances of the gate module regarding our technology must be extracted from geometry variations, which will be done in detail in chapter 6. In this section only the general trends and correlations between layout geometries and the respective capacitance will be discussed in order to provide a basic overview.

For two conductive areas which are electrically isolated from each other and have different potentials the capacitance is defined as:

$$C = \varepsilon_o \varepsilon_r \frac{\oint_A \vec{E} d\vec{A}}{\int_s \vec{E} d\vec{s}}, \tag{2.17}$$

with ε the dielectric constant between both elements, E the electric field, A an arbitrary area surrounding one of the elements and s the distance between both. For the gate head most parasitic capacitances can be roughly approximated as a plate capacitor. In this case (2.17) becomes:

$$C = \varepsilon_o \varepsilon_r \frac{A_{plate}}{d}, \tag{2.18}$$

where A_{plate} is the area of the plates facing each other and d is the distance between both plates.

With (2.18) the following methods to minimize the gate capacitance can be derived:

1.) Use of a low-ε dielectric as passivation layer,

2.) Large distances between the charged areas,

3.) Small area of the gate module.

A common method to achieve a low parasitic capacitance is by non-passivation of the device. But due to the need of a passivation to prevent the RF dispersion and to be compatible with our MMIC process a SiN passivation is needed. To study the effect of a low-ε passivation such a material is simulated by a thin SiN- passivation layer which covers the whole device but leaves an air gap between the gate head and surface. With this method, the influence of a quasi low-ε dielectric passivation on the parasitic capacitances can be studied while still passivating the device (see chapter 4).

Besides the passivation layer the parasitic elements can be reduced by an optimization of the device geometries. Going from the ohmic contacts to the gate foot (see Figure 2-10), the first parasitic capacitance is the coupling of the gate head with the source or drain contacts ($C_{contact}$). A major parameter to minimize $C_{contact}$ is the gate source and gate drain spacing. As was discussed in

chapter 2.2 a source drain distance as short as possible is desired for a low on resistance. But according to (2.18) $C_{contact}$ might increase rapidly for short spacings. Therefore, $C_{contact}$ must be evaluated as a function of the gate source spacing for the developing of mmW-HEMTs.

Beside the interaction with the contact pads, the overhang of the T-shaped gate (see Figure 2-10) creates a parasitic capacitance to the electron channel (C_{head}). Following (2.18), C_{head} can be scaled by a reduction of the overhang size as well as an increase of the gate head to surface distance. But both parameters were limited by the available process technology at the start of this work. Therefore, an advanced fabrication technology for the new mmW gate module was developed in the course of this work to further minimize the parasitic influence of the gate head (see chapter 4).

Not only the gate head generates parasitic capacitances but also the gate foot. The sidewalls of the gate foot causes a capacitive coupling to the electron channel (see Figure 2-10). From a design perspective this capacitance can only be reduced by a short distance of the gate head to the surface which is obviously directly opposed to the scaling of C_{head}. The approach in this work is to maximize the gate head distance. Due to the fact that if the distance is reduced the overall parasitic capacitance would increase because the gate head area is far greater than the area of the sidewalls.

Another parasitic capacitance of the gate foot is the fringe capacitance. Due to stray fields of the gate foot capacitance, the areas next to the gate foot are also modulated which increases the gate foot capacitance.

2.3.4 Influence of the gate head scaling on the gate line resistance

As was discussed in section 2.1.5, a low gate line resistance is essential to achieve high f_{max} values (see formula (2.11) and subsequently a high power gain. This constrain imposes certain limitations to the design of the gate module. The gate line resistance is defined by the gate width, the area of the gate cross section (see Figure 1-4) and the gate material. If the gate head is scaled

down in order to decrease the parasitic capacitances, R_g will be negatively affected. The height of the gate head and the gate metal cannot be changed due to process restrictions (see chapter 4). Therefore, the increase of R_g can only be compensated by a shorter gate width, but in doing so the maximum output power of the transistor is drastically reduced. Considering a typical gate width of 50 µm, it can be shown that the gate head must be at least 400 nm in diameter to achieve sufficient low R_g values. With this design rule, a f_{max} of more than 1.5 times f_T can be achieved (see Figure 2-5 and Figure 2-7). This circumstance allows the design of power amplifiers which can operate above the current-gain cut-off frequency (see chapter 8).

2.3.5 Short-channel effects

Whether or not short-channel effects have to be taken into account depends on the gate length (L_g) and the aspect ratio of gate length to barrier thickness (t_{gb}) [Num91].

As the gate length becomes shorter and t_{gb} is below a material specific threshold, the superposition of the vertical electrical field and the lateral electric field from the drain can no longer be ignored. The gate voltage causes a potential barrier for the electrons in the channel but the electric field from the drain reduces this barrier at the drain side. If the width of the potential barrier is very short, most of the potential well is decreased, and electrons start to flow over or tunnel through the remaining barrier. If the drain voltage is further increased the barrier is completely overwhelmed by the vertical field and the drain current is no longer controlled by the gate voltage [Ure06a], [Bah09]. This drain induced barrier lowering (DIBL) causes several negative effects regarding small-signal characteristics as well as output power and PAE. Due to the reduction of the barrier a higher gate voltage is needed to achieve the off-state. This effect can be directly measured as a shift of the threshold voltage. Furthermore, the subthreshold current can increase due to a tunneling current caused by the short potential barrier. In forward operation the DIBL

effect causes an increase of the output conductance (g_{ds}). But with higher g_{ds} a greater percentage of the drain current no longer charges the different capacitances of the transistor, but flows directly from source to drain (see Figure 2-2). As a consequence all gains of the transistor are reduced and subsequently all small-signal figures of merit. Therefore, a low g_{ds} is of vital importance for the development of mmW-HEMTs.

In large signal operation the poor pinch-off (see Figure 2-9), reduced breakdown voltage (see Figure 2-12) and high frequency dispersion are the major limiting effects. The poor pinch-off and dispersion reduces the current swing and the low breakdown voltage limits the possible voltage swing, resulting in a drastically decrease of the output power. Due to the reduced gain and higher leakage current also the PAE of the transistor decreases significantly. Therefore, both the breakdown voltage as well as g_{ds} are important figures of merit for the short-channel effects regarding mmW-HEMTs.

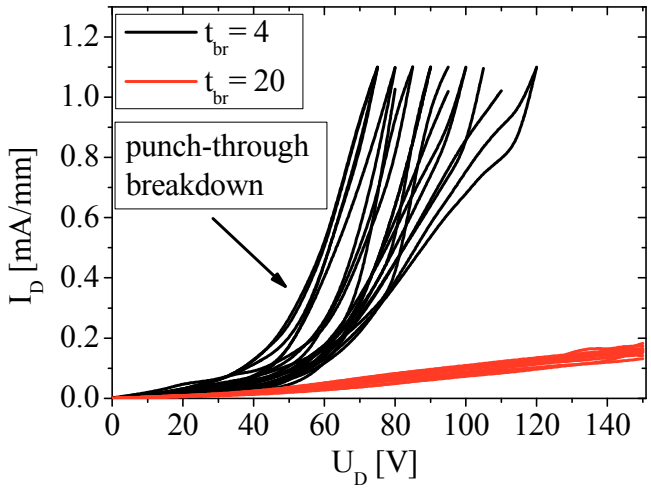

Figure 2-12: Breakdown measurements for AlGaN/GaN HEMTs with different aspect ratios of gate foot to barrier (t_{gb}). The transistors with $t_{gb} = 4$ exhibits a punch-through breakdown caused by a short-channel effect.

For AlGaN/GaN HEMTs very few studies regarding these short-channel effects have been reported so far [Jes07]. Most of the principles used to describe the effects in highly scaled HEMTs are taken from publications on AlGaAs/GaAs HEMTs. Although the scaling rules apply to all field effect transistors, the critical aspect ratio and gate length depend strongly on the material properties. It is therefore necessary to study the influence of thin barriers on the short-channel effects and to determine the optimum aspect ratios for AlGaN transistors.

2.4 Conclusion

In this chapter the general scaling rules for an ideal field effect transistor were derived with the help of common small and large signal figures of merit. But as was discussed in the last section, many parasitic elements of our transistor technology and conflicting characteristics result in a far more complex process development for mmW-HEMTs. Due to the relatively new material system, the scaling behavior of AlGaN/GaN HEMTs is an ongoing research topic. In this section the previous scaling discussion is summarized, and an overview is given which device geometries and parameters are studied in this work is given.

Considering the discussion of section 2.3, more comprehensive expressions are necessary for the common small-signal figures of merit. With the consideration of parasitic elements the equation for the cut-off frequency, maximum frequency of oscillation and the frequency where MSG equals MAG (k=1) can be given as follows [Lie76]:

$$f_T \approx \frac{g_{m\_\mathrm{int}}}{2\pi\left(C_{gs}+C_{gd}\right)\left(1+g_{ds}R_S\right)+2\pi C_{gd}g_{m\_\mathrm{int}}R_S}, \tag{2.19}$$

$$f_{\max,MAG} \approx \frac{f_T}{4\left[g_{ds}\left(R_i+R_s+R_g\right)+\frac{\left(R_i+R_s+2R_g\right)C_{gd}}{2\pi}f_T\right]^{1/2}}, \tag{2.20}$$

$$f(k=1) \approx \frac{1}{2\pi\left[\frac{1}{f_T} + \frac{(R_i + R_s + 2R_g)\,C_{gd}}{\frac{C_{gd}}{C_{gs}} + g_{ds}R_s} + \frac{(R_i + R_s + R_g)\,g_{ds}}{\frac{g_{m\_\mathrm{int}}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}} + g_{ds}R_s\right)}\right]}. \quad (2.21)$$

As can be seen in equation (2.19-21), the small-signal figures of merit for a common HEMT design depend strongly on the parasitic elements of the transistor. Combined with the discussion in section 2.2 and 2.3 the following scaling rules can be formulated:

1.) Increase of g_{m_int} by a reduction of the barrier thickness (d_{bar}).

2.) At the same time the gate length (L_g) must be reduced by the same factor to keep the gate foot capacitance constant.

3.) The parasitic capacitances of the gate module must be minimized, especially C_{gd} must be decreased to achieve high power-gains.

4.) To minimize the loss of transconductance for the extrinsic transistor the source resistance (R_s) must also be reduced by the scaling factor.

5.) The gate line resistance (R_g) must not increase to prevent a drastic decrease of the power-gain for a constant single-finger gate width.

To optimize the large signal characteristics such as output power and PAE the on-resistance must also be reduced by the scaling factor.

In Table 2-1 the theoretical scaling rules for the studied HEMT layout are summarized. For GaN-based transistors the actual scaling behavior is not yet known due to the relatively new material system and device technology. Therefore, a major part of this work is to experimentally evaluate the scaling properties in regard to our mmW-HEMT technology. Due to the scaling of nearly all device geometries many new limiting or parasitic effects can occur such as high gate leakage currents or short-channel effects. The analysis and discussion of these

effects is another major part of this work.In order to conduct the necessary experiments and measurements, new fabrication technologies had to be developed, which allow the fabrication of highly scaled HEMTs with lateral critical dimensions down to 100 nm and barrier thicknesses down to 6 nm. In the next two chapters the technologies used to fabricate our mmW-HEMTs are discussed in more detail with a special emphasis on the scaling restrictions imposed by our process technology or epitaxy of the AlGaN/GaN heterostructures.

Table 2-1: Scaled device parameters and geometries studied in this work.

Device characteristic	**Desired scaling factor of the device characteristic**	**Scaled geometry**	**Desired scaling factor for the device geometry/property**
Intrinsic transconductance	α	**Barrier thickness**	1/α
Source resistance	1/α	**Source gate spacing**	1/α
Parasitics capacitances	1/α	**Gate head overhang** **Passivation material** **Barrier thickness**	combined 1/α
Gate foot capacitance	1	**Gate length**	1/α
Gate line resistance	1	**Gate head overhang**	1/α
On resistance	1/α	**Source drain spacing**	1/α

3. Fundamentals of AlGaN/GaN growth and properties of the two dimensional electron gas

As discussed in the previous chapter, the barrier properties have a significant impact on the transistor characteristics. To achieve high transconductance the barrier must be as thin as possible. But in doing so the saturation current should not be negatively affected. Therefore, it is necessary to understand how the different barrier and channel properties can be modified by the design parameters.

At the beginning of this chapter the growth and properties of AlGaN/GaN epitaxial layers will be briefly introduced. Following this, a brief explanation is given why a quasi two-dimensional electron gas (2DEG) forms at the hetero interface between the AlGaN barrier and GaN buffer. The next sections concentrate on the models used for simulations and analytical calculations used to predict the influence of the barrier properties such as Al-content and barrier thickness on the mobility and sheet carrier concentration of the 2DEG. These calculations are used to design layer structures with the desired properties to fabricate mmW-HEMTs. In the last part of this chapter the simulated results are compared with Hall measurements of the fabricated heterostructures.

3.1 Growth of AlGaN/GaN heterostructures by metal organic chemical vapor deposition

All heterostructures used in this work are grown in a metal organic chemical vapor deposition (MOCVD) reactor. The principle of these reactors is that vaporized metal organic precursors flows over a headed wafer [Jen91]. Due to the high temperature of the wafer surface the precursors crack into gaseous radicals (*R*) and the desired basic components of the epitaxial layers. A more detailed summary of all surface reactions can be seen in Figure 3-1. In case of AlGaN/GaN-growth TEG (triethylgallium), TMA (trimethylaluminium) and ammonia are the gaseous precursors of Gallium, Aluminum and Nitrogen, respectively.

In a simplistic manner the reaction can be described as:

$$R_3Met + NH_3 \rightarrow MetN + 3RH_3 \tag{3.1}$$

A more detailed description of the chemical reactions in a MOCVD system for GaN epitaxy is given in [Mih98].

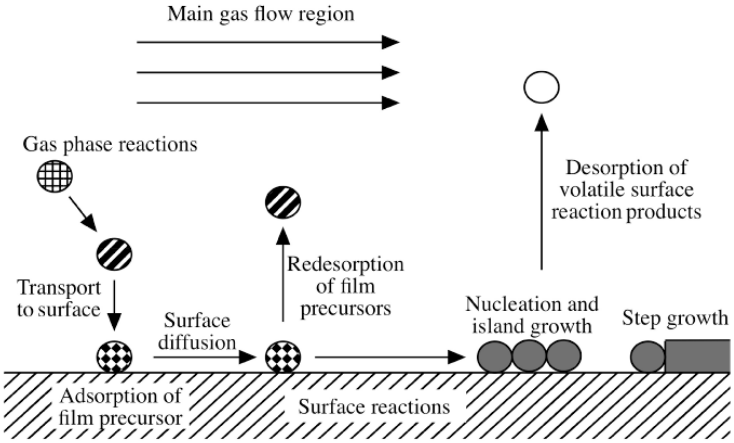

Figure 3-1: Schematic diagram of all surface reaction via a MOCVD epitaxy [Jen91].

For the growth of AlGaN/GaN structures temperatures in the range of 1000 – 1200°C and a chamber pressure of 50 – 900 mbar are used.The quality and properties of the epitaxy depends strongly on these parameters and an optimal composition must be found for different barrier designs [Kel99]. The substrate is an important factor for the transistor performance. Any lattice mismatch between the substrate and the epitaxial layer leads to the formation of threading dislocations along the c-axis caused by the strain relaxation in the epitaxial layer [Dav03]. If such dislocations reach the AlGaN barrier they can become charged and act as centers of Coulomb scattering [Jos03]. As a result the device characteristics, especially leakage currents, mobility of the electrons in the channel and long term stability, degrade [Mar10]. In case of lattice mismatch, GaN-wafer could provide perfect substrates, but the size of such wafers currently does not exceed two inches. Also the thermal conductivity (λ) is nearly four times lower compared to SiC substrates (see Table 3-1). Head dissipation however, is a major issue for high power devices [Con08]. Many applications in aerospace, telecommunication or automotive electronics require transistors which can operate at high temperatures without complex external cooling.

Table 3-1: Crystal properties of group III Nitrides in comparison to substrate materials. The data was taken from [Str92], [Wei98], and [Vur03].

	a-axis lattice constant (a_o) [Á]	**c-axis lattice constant (c_o) [Á]**	**mismatch of GaN [%]**	**thermal conductivity (λ) [W/Km]**
GaN	3,189	5,158	0	130
AlN	3,112	4,982	2,47	200
Sapphire	4,758	12,991	-13,8	42
6H-SiC	3,08	15,12	3,54	490

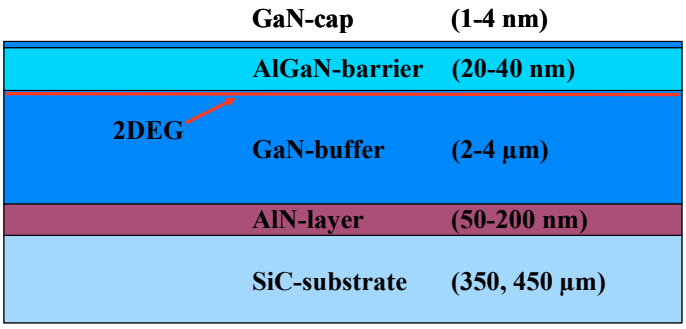

Figure 3-2: Schematic diagram of an AlGaN/GaN heterostructure grown on SiC substrate with typical values for the layer thicknesses.

Therefore, a substrate with a high thermal conductivity is needed. SiC provides the best compromise between lattice mismatch and thermal conductivity for group III-N-based HEMTs [Mio06] and is mainly used in fabrication of such devices [Mis08], [Mic10]. A schematic diagram of the epitaxial structure is depicted in Figure 3-2. After cleaning and heading of the wafers an AlN layer is grown on SiC to enable a Ga-face epitaxy of the next layers [Dim00]. The following 2 – 4 µm thick isolating GaN-buffer layer reduces dislocations and stacking faults in the crystal induced by the lattice mismatch. On top of the buffer an AlGaN barrier is grown with Al-contents of 10 to 35% and typical thicknesses between 20 and 40 nm. All wafers are capped with a few nanometer thin GaN layer to increase the long term chemical stability of the surface and the ohmic contacts of HEMT devices [Koh10].

For HEMT devices the electric properties of the channel are a major performance issue and a detailed understanding of the accessible barrier parameters Al-content and barrier thickness on the electrical properties of the 2DEG-channel is necessary for device development. In the next sections the fundamental theory which describes the 2DEG at the AlGaN/GaN heterointerface is summarized. Afterwards, basic concepts are discussed to simulate heterostructures with regard to accessible parameters of the epitaxy process.

3.2 Two-dimensional electron gases induced by gradients in spontaneous and piezoelectric polarization at AlGaN/GaN interfaces

AlGaN/GaN heterostructures used in this work were grown in Ga-face polarity and c-plane [0001] orientation without an intentional doping of the barrier [Walt09], [Koh09]. The Ga-face orientation causes the confinement of the 2DEG at the AlGaN/GaN interface opposed to a confinement at the GaN/AlGaN interface for N-face oriented heterostructures [Dim00]. The following discussion is therefore restricted to Ga-face type only.

The different electro-negativity of the metal and nitrogen atoms as well as the asymmetry of the wurtzite crystal structure causes a spontaneous polarization (P_{sp}) [Ber97]. Due to the different lattice constants of AlGaN and GaN (see Table 3-1) the barrier layer grows biaxially strained if the layer thicknesses do not exceed a critical value, so that strain relaxation due to cracking of the AlGaN layer can occur [Hea00]. The biaxial strain in the AlGaN layer deforms the crystal and causes a piezoelectric polarization in the barrier. The sum of the piezoelectric and spontaneous polarization of the AlGaN barrier minus the spontaneous polarization of the GaN buffer results in a positive polarization sheet charge (σ) (see Figure 3-3) at the AlGaN/GaN interface [Amb99].

Additionally, the two semiconductors AlGaN and GaN possess different band gap energies (E_g). This causes a band discontinuity at the interface of the two materials. The conduction band offset (ΔE_c) is more than 75% of ΔE_g. For a 22 nm thin AlGaN barrier with 22% Al content ΔE_c is 0.46 eV and ΔE_v is 0.1 eV (see Figure 3-4).

Both the conduction band offset and the positive polarization charge at the hetero interface causes an accumulation of electrons, provided by surface donors or unintentional doping. The electric field of the accumulation layer decreases within a few nanometers into the GaN buffer (see Figure 3-4) thus forming a triangular shaped potential well for electrons along the z-axis.

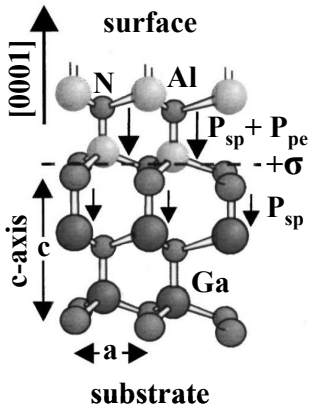

Figure 3-3: Schematic structure of an AlGaN/GaN interface with spontaneous and piezoelectric polarization and resulting polarization sheet charge [Amb99].

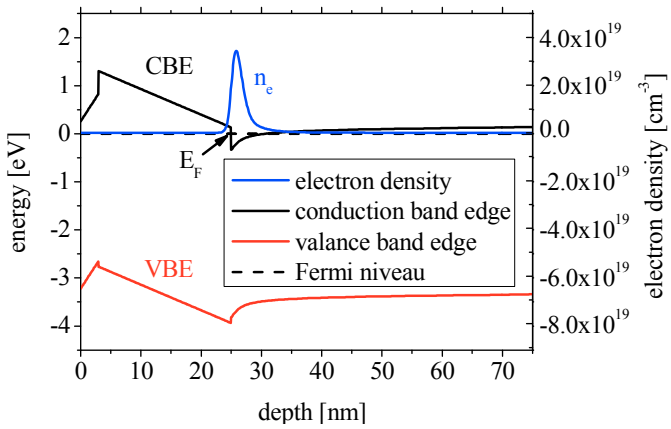

Figure 3-4: Simulated depth profile (along the z-axis) of the conduction, valence band edge and electron concentration of a 22 nm thick $Al_{0.22}Ga_{0.78}N$ barrier with a 3 nm thick GaN cap layer.

Therefore, electrons can move freely along the xy-plane, but they can only occupy defined states inside the momentum or position space in the z-direction. This reduces the interactions of electrons with their environment to two dimensions, and the accumulation of electrons can be described as a two-dimensional electron gas. The major advantages of this quasi-2DEG are the reduced phonon scattering as well as the strongly decreased recombination rate of the electrons with donors. As a consequence this electron channel features an improved mobility compared to bulk GaN and very high sheet carrier concentrations. At room temperature, a mobility up to 2000 $cm^2/(V\,s)$ has been reported [Ski05] whereas bulk GaN has a mobility of 440 $cm^2/(V\,s)$ [Shu96]. For the sheet carrier concentration, values up to $1.5x10^{13}$ cm^{-2} can be achieved with AlGaN/GaN heterostructures [Mok02]. To describe the correlation between material properties of the heterostructures and electrical characteristics of the electron channel, different models and theories can be used.

In the next two sections an analytical approach and basic theories to simulate the 2DEG at the AlGaN/GaN heterointerface will be given. Both approaches are later used to determine optimized layer structures which provide the desired characteristics for the fabrication of mmW-HEMTs.

3.3 Analytical model of the sheet carrier concentration

For AlGaN/GaN heterostructures the sheet carrier concentration can be calculated using the following equation [Amb00]:

$$n_s = \left[\frac{\sigma(x)}{q} - \left(\frac{\varepsilon(x)\varepsilon_o}{q^2 d_{AlGaN}} \right) \left(q\phi_B + E_F(x) - \Delta E_c(x) - \frac{q^2 N_D {d_{AlGaN}}^2}{2\varepsilon(x)\varepsilon_0} \right) \right], \tag{3.2}$$

with σ the polarization induced sheet charge, q the elementary charge, ε, ε_o dielectric constants, d_{AlGaN} the thickness of the AlGaN barrier, E_F the Fermi level, ΔE_c the conduction band offset and N_D the charged donor concentration in the barrier. In undoped AlGaN barriers N_D is less then 10^{16} cm^{-2} and the influence on the sheet carrier concentration can be neglected:

$$n_s = \left[\frac{\sigma(x)}{q} - \left(\frac{\varepsilon(x)\varepsilon_o}{q^2 d_{AlGaN}} \right) \left(q\phi_B + E_F(x) - \Delta E_c(x) \right) \right]. \tag{3.3}$$

The dominant factors of the remaining formula (3.3) are the polarization induced sheet charge and the thickness of the AlGaN barrier. As discussed in the previous chapter, the barrier has to be scaled down in order to improve the high frequency characteristics of HEMTs. But as can be seen in equation (3.3) this would drastically reduce the sheet carrier concentration and as a consequence the saturation current and output power. To compensate the effect of a thin barrier the polarization induced sheet charge must be increased. As discussed before, the sheet charge is caused by a gradient of the piezoelectric polarization (P_{pe}) and spontaneous polarization (P_{sp}):

$$\frac{\sigma}{e} = \Delta P = P_{pe} + \Delta P_{sp}. \tag{3.4}$$

The spontaneous polarizations of AlGaN and GaN are material constants. It has been found experimentally that for many compound semiconductors with three elements the material constants can be calculated by a linear interpola-

tion of the binary base compounds [Zor01]. For AlGaN the material constants are therefore derived from a linear superposition of AlN and GaN constants in the form of:

$$k_{Al_xGa_{(1-x)}N} = x_{Al} \cdot k_{AlN} + (1-x)k_{GaN}\,. \tag{3.5}$$

where x_{Al} is the Al-content and k the material constant.

Following that, the spontaneous polarization of AlGaN can be given as:

$$P^{sp}_{AlGaN} = x \cdot P^{sp}_{AlN} + (1-x)P^{sp}_{GaN}\,. \tag{3.6}$$

And the total spontaneous polarization at the hetero interface is:

$$\Delta P_{sp} = P^{sp}_{AlGaN} - P^{sp}_{GaN}\,. \tag{3.7}$$

Due to the pseudomorphic growth of AlGaN on top of the unstrained GaN buffer the AlGaN barrier adopts the crystal lattice parameter of GaN. As a consequence, the crystal structure of the AlGaN layer is biaxially deformed which causes a piezoelectric polarization inside the barrier. Due to the fact that the thick GaN buffer is unstrained the piezoelectric polarization is zero in the buffer and only the piezoelectric polarization in the AlGaN layer must be considered, which can be calculated by using the following formula:

$$P_{PE} = e_{33}s_z + e_{31}(s_x + s_y)\,. \tag{3.8}$$

Where s_z is the strain along the c-axis and s_x, s_y are strains in the xy-plane which are assumed to be isotropic and e_{33} and e_{31} are piezoelectric constants of the AlGaN-barrier. The strain is given by the lattice mismatch between strained and unstrained AlGaN:

$$s_z = \frac{c - c_o}{c_0},\;\; s_y = s_x = \frac{a - a_0}{a_0}\,. \tag{3.9}$$

Where c_0 and a_0 are the lattice constants of the unstrained crystal and c and a are the constants for the strained layer. Because the crystal can be described as an elastic structure the strain of the c-axis is coupled with the strain of the a-axis via elastic constants C_{13} and C_{33}.

$$\frac{c - c_0}{c_0} = -2\frac{a - a_0}{a_0}\frac{C_{13}}{C_{33}}. \tag{3.10}$$

Combining formulas (3.8), (3.9) and (3.10) the piezoelectric polarization becomes:

$$P_{pe} = -2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right). \tag{3.11}$$

All the material constants in formula (3.11) are a function of the Al-content of the AlGaN barrier and can be calculated using the approach described in (3.5). The material constants used for the calculations in this work are shown in Table 3-2.

Table 3-2: Crystal properties of group III Nitrides.

constant	GaN	AlN	source
a_0 (Å)	3,189	3,112	[Vur03]
e_{31}	-0.60	-0.49	[Ber97]
e_{33}	1.46	0.73	[Ber97]
C_{31} (Gpa)	106	108	[Vur03]
C_{33} (Gpa)	398	373	[Vur03]
P_{sp} (C/m²)	-0.034	-0.090	[Vur03]
E_g (eV)	3.510	6.250	[Vur03]

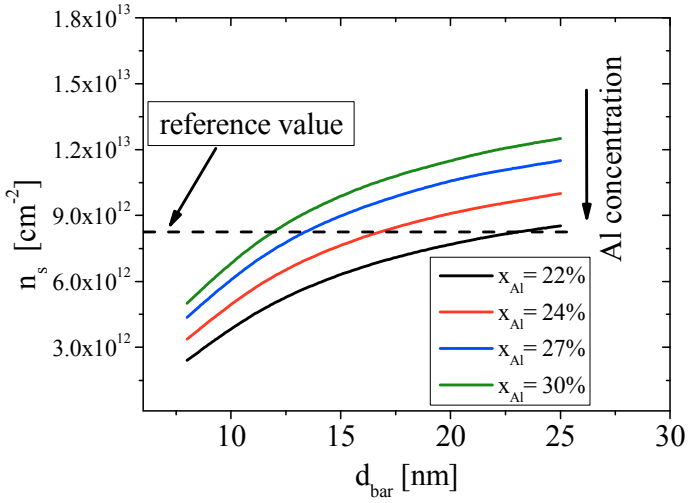

Figure 3-5: Calculation of the sheet electron concentration of the 2DEG for various Al-contents and barrier thicknesses.

In Figure 3-5 the sheet carrier concentration over the barrier thickness is depicted for different Al-concentrations varying from 22% to 30%. As can be seen in the diagram, at d_{bar} = 10 nm and x_{Al} of 22% the sheet carrier concentration is more than halved. Because the 2DEG is later used as the channel of the transistor, n_s is directly proportional to the current density and subsequently the output power density of HEMTs. Therefore, a reduction of n_s must be prevented for the development of high power mmW-HEMTs. To compensate this negative effect of a thinner barrier, the Aluminum concentration of the AlGaN barrier must be increased. But a higher Al-content can have many severe side-effects such as a reduced critical thickness before the strain of the heterostructure causes the cracking of the barrier, or an increased probability of unintentional doping of the AlGaN layer with oxygen atoms, which can act as traps and limit the performance of HEMTs. To minimize these side-effects the Al-content has to be as low as possible. Given these circumstances the heterostructures were optimized to achieve the same sheet carrier density as the initial heterostructures with d_{bar} = 25 nm and x_{Al} = 22% but without an increase of the Al-content above 30%. HEMTs fabricated with the initial heterostructure feature excellent output power densities up to 10 GHz, and complete charac-

terizations were available at the start of this work. Therefore, this barrier is used as a reference to compare the results of the mmW- HEMTs developed in this work. As can be seen in Figure 3-5 for d_{bar} = 12 nm and x_{Al} = 30% the same n_s values as for the reference barrier are reached, which is sufficient for the development of a mmW-HEMT technology.

The analytical formulas used in this section can only be used to estimate the barrier characteristics. A more sophisticated method is the numerical solution of the Schrödinger-Poisson equation for the heterostructure. In the next section of this chapter the basic principles and equations will be given for the simulation of the 2DEG.

3.4 Simulation of the sheet carrier concentration

The simulation program BandEng used for this work is a 1D Schrödinger-Poisson solver [Gru10]. In order to calculate n_s the discrete energy levels (E_n) of the electron wave function inside the triangular potential, the Fermi energy (E_F) and the potential energy (F) of the triangular well must be calculated iteratively.

The sheet carrier concentration n_s is given by integrating the product of the two dimensional density of states D_{2D} with the occupation probability f(E_F, E_n):

$$n_s = \int_0^\infty D_{2D}(E) \cdot f(E_F, E_n)\, dE_n \,, \tag{3.12}$$

where E_n is a discrete energy level with regard to the Fermi level E_F. For a 2D-system with a triangular shaped potential the density of states is:

$$D_{2D} = \frac{m^*}{\pi \hbar}, \tag{3.13}$$

with m^* the effective mass of electrons in the 2DEG and $\hbar$ the Planck constant. The occupation probability is given by:

$$f(E_F,E_n)=\frac{1}{1+\exp\left(\frac{E_n-E_F}{kT}\right)}. \tag{3.14}$$

Following that, n_s is:

$$n_s=\frac{m^*}{\pi\hbar}kT\cdot\ln\sum_{n=0}^{\infty}\left[1+\exp\left(\frac{E_n-E_F}{kT}\right)\right]. \tag{3.15}$$

The discrete energy level E_n can be determined by solving the Schrödinger equation:

$$\left(\frac{\hbar^2}{2m^*}\Delta+eFx-E_n\right)\psi(x)=0 \tag{3.16}$$

where F the potential energy of the triangular well.

The energy field can be calculated using the Poisson equation:

$$\nabla\varepsilon(-\vec{F})=q=-e(n_e-n_h-N_D^++N_A^-) \tag{3.17}$$

With n_h the hole concentration, n_e the electron concentration, N_D^+ ionized donors and N_A^- ionized acceptors. For undoped AlGaN donors and acceptors and because only electrons accumulate at the interface the hole density can also be neglected. For one dimension the energy field becomes:

$$F=\frac{e\,n_e}{\varepsilon\varepsilon_0} \tag{3.18}$$

The Fermi level is also a function of the electron density and can be described by [Cha06]:

$$E_F=k_1(T)+k_2(T)\sqrt{n_s}+k_3(T)n_s \tag{3.19}$$

k_1, k_2, k_3 are determined by a numerical method proposed by Kola [Kol8].

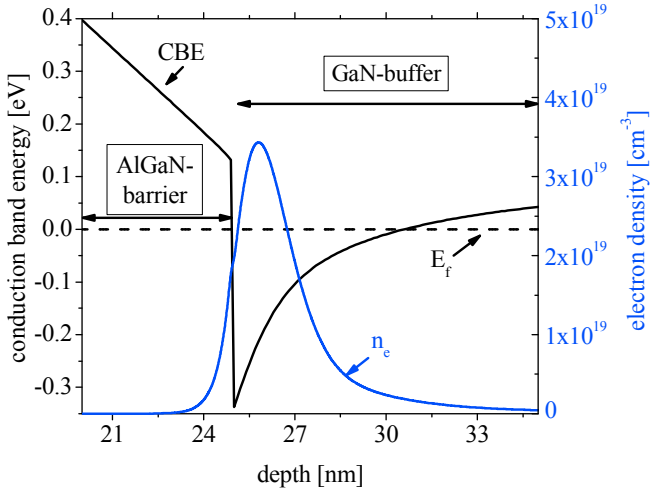

Figure 3-6: Solution of the Schrödinger equation regarding the conduction band egde and electron density for an AlGaN/GaN heterostructure with d_{bar} = 25 nm and x_{al} = 22%.

To calculate the sheet carrier concentration, the equations (3.15), (3.16), (3.18) and (3.19) are solved iteratively in band diagram simulators. A result for a simulation of an AlGaN/GaN structure is depicted in Figure 3-6. As can be seen in the diagram the conduction band edge exhibits a triangular shaped potential well at the interface and most of the electrons are confined inside the well. Due to the fact that the potential well has a finite height the electron distribution is not zero inside the AlGaN-barrier or GaN-buffer. These electrons are mostly responsible for leakage currents of HEMTs which will be discussed further in chapter 7. In Figure 3-7 the results of the simulation using BandEng are shown. The general trend of the sheet carrier concentration is the same as calculated with the analytical model (see Figure 3-5).

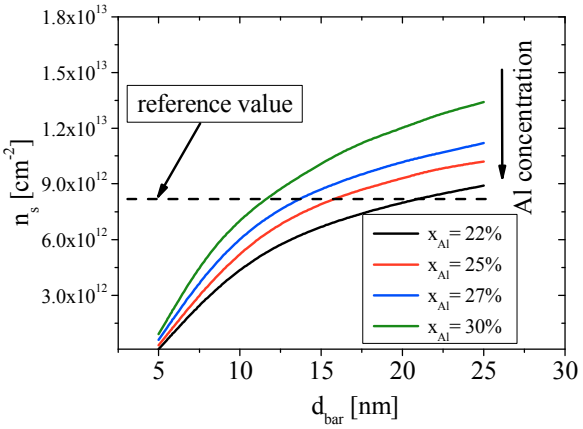

Figure 3-7: Simulated sheet carrier concentrations for different barrier thicknesses and Al contents from 22% up to 30% as well as the reference value for n_s measuered for the reference barrier.

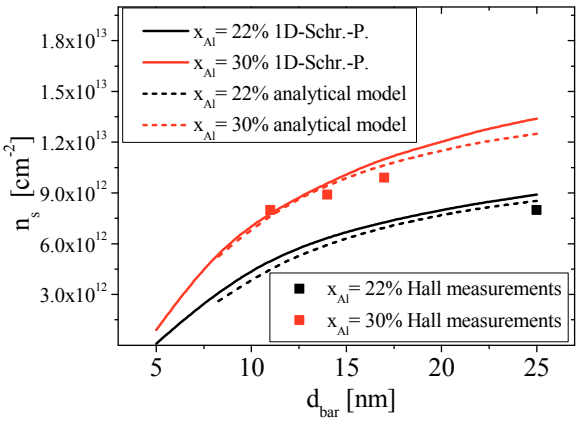

Figure 3-8: Comparison between simulated data and measured sheet carrier concentration using Hall measurements.

In Figure 3-8 the calculated trends using the analytical model and the simulation software as well as the measured n_s values obtained by Hall measurements are depicted. The sheet carrier concentrations of the actual heterostructures correspond well with the predicted trends. For d_{bar} greater 11 nm and x_{Al} of 30 % the simulation overestimates n_s. Due to the fact that the difference in n_s increases with the barrier thickness, a partial relaxation of grown AlGaN layers can be the cause of this discrepancy. But due to the lack of further samples also a simulation or measurement error can be the reason for the discrepancy between measured and simulated values.

To study the effects of thinner barriers on transconductance, gate capacitance and short-channel effects, barriers thicknesses of 11, 14, 17 and 20 nm were grown. To be able to compare the results of those wafers to a well established technology [Wal09], also standard heterostructures with d_{bar} of 25 nm and 22% Al-content were fabricated. Table 3-3 summarizes all heterostructures used in this work in regard to the barrier parameters and common figures of merit of the 2DEG. As can be seen, not only the sheet carrier concentration (n_s) but also the low field mobility (μ_0) of the wafers with thin barriers and higher Al-concentration is in the same range as the reference barrier. For the wafer with

d_{bar} greater 17 nm the low field mobility decreases due to the higher interaction of the 2DEG with the AlGaN interface. This reduction is compensated by the enhanced sheet carrier concentration, resulting in an overall slight decrease of the sheet resistance (R_{sheet}). As a consequence the sheet resistance between all wafers is nearly the same. This fact is important to achieve comparable extrinsic resistances for the test devices on each wafer. The technologies used for the processing of the various HEMTs fabricated in the course of this study will be described in the next chapter.

Table 3-3: 2DEG characteristics for all wafer used in this section.

	Al content [%]	**d_{bar} [nm]**	**R_{sheet} [Ω/□]**	**n_s [cm^{-2}]**	**μ_0 [cm^2/Vs]**
reference barrier	22	25	509	$8.0x10^{12}$	1520
thin barriers with increased x_{Al}	29	20	438	$9.7x10^{12}$	1407
	30	17	457	$9.9x10^{12}$	1380
	30	14	440	$8.9x10^{12}$	1550
	30	11	459	$8.1x10^{12}$	1540

4. Process technology of millimeter-wave HEMTs

For the lateral device scaling the process technology is of great importance. As the feature geometries become smaller, novel process technologies are necessary to enable the challenging critical dimensions of the new process. Especially gate modules with gate lengths below 500 nm require sophisticated lithography systems.
In this chapter, not all process steps to fabricate an AlGaN/GaN-HEMT will be discussed but the essential stages which define key components of the basic transistor cell. Also the limits of the scaling caused by the available process technology will be discussed in this chapter.

In the course of this work two process technologies were used to fabricate mmW-HEMT. At first a complete process technology was developed at the Center for Micro- and Nanotechnologies, TU-Ilmenau (ZMN) to evaluate a first generation of transistors. Later the more established process technology of the Fraunhofer Institute for Applied Solid State Physics (IAF) was modified to enable the processing of mmW-HEMT with gate length of 100 nm. The general process flow of both technologies is the same and only the differences between both technologies will be discussed.

4.1 Ohmic contacts

The first step of our HEMT processing is the fabrication of the source and drain contacts. The area of the contact pads is defined by an optical lithography system which has a minimal feature size below 0.5 µm for ideal wafers. Due to the strain in the heterostructure, the wafers used for the fabrication of AlGaN/GaN transistors are always bowed. Furthermore, thick resist layers are necessary for the lift-off process. Both facts increase the smallest feature size and subsequently the shortest distance between source and drain (L_{sd}). Given a symmetric source-gate and drain-gate spacing and neglecting the gate length, the minimum distance from a contact pad to the gate foot is 0.5 µm for the available lithography process. Following the lithography step, a Ti/Al/Ti/Au based metal stack is evaporated on top of the wafer. After the removal of the remaining resist (lift-off) only the contact pads remain. To enable an ohmic contact the wafer is annealed at high temperatures (between 750 and 850°C) and part of the metal diffuses into the barrier and contacts the 2DEG-channel [Dor06]. But the annealing process causes also a lateral diffusion of the metal. As a consequence the edge roughness increases to 0.1-0.2 µm (see Figure 4-3). If the source-gate spacing is only 0.5 µm this effect leads to a drastic reduction of the transistor yield. To compensate the increased edge roughness the minimum spacing must be increased to 0.7 µm. For the study regarding the influence of the source-gate spacing on the source resistance, transistors with L_{sg} down to 0.5 µm were fabricated, but later only minimum spacings of 0.7 µm were used to increase

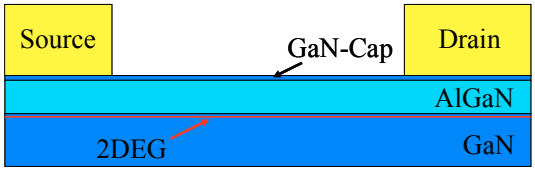

Figure 4-1: Schematic cross section of a HEMT after the removal of the resist mask.

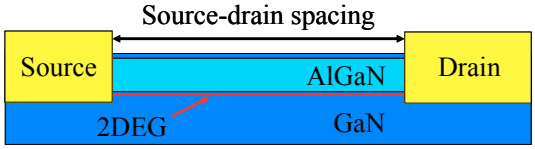

Figure 4-2: Schematic cross section of the HEMT after the anneal process.

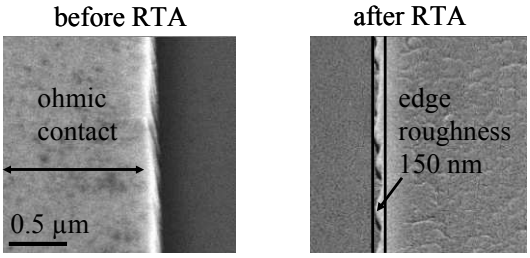

Figure 4-3: Edge roughness of the ohmic contacts before and after the rapid thermal annealing (RTA).

the process yield and prevent parasitic effects from the lateral diffusion of the ohmic contacts. The electrical contact resistance ($R_{contact}$) is highly dependant on the process parameters and the available equipment [Jac02], [Rom09], [Qui09]. For the available contact technology $R_{contact}$ does not change even if the Al-content or thickness of the AlGaN layer varies between wafers, (see Figure 4-4). The processes for the fabrication of ohmic contacts, which are used in this work, yield contact resistances of 0.15 Ωmm for IAF technology and 0.3 Ωmm for ZMN-technology (Figure 4-4). These values are state of the art for annealed ohmic contacts, compared to publications of other groups [Jac02], [Rom09], [Qui09]. An improvement of the contact resistance was therefore not a subject of this work and the contact resistance is considered a fixed value for GaN-HEMTs in the further analyses.

After the passivation of the wafer surface with SiN and the isolation of the discrete transistors the gate module is fabricated. Because the dimension of the gate foot is well below 500 nm an electron beam lithography system is used to define the resist mask for the gate module. To study the effect of geometry scaling and different passivation thicknesses two processes were developed for the gate module. The characteristics and advantages of both technologies will be discussed in the next two sections.

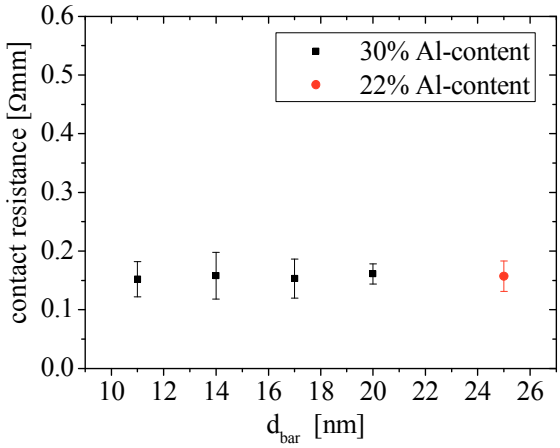

Figure 4-4: Contact resistance for barriers with 22% and 30 %Al-content and different barrier thicknesses (d_{bar}).

4.2 The SiN-gate module

In the SiN assisted gate process the gate foot is dry etched into the SiN passivation layer using an electron beam defined resist mask. Later the gate head is fabricated by optical lithography and electron beam evaporation of a Ni/Pt/Au metal stack. To keep the gate foot capacitance constant for all barrier thicknesses various gate lengths from 500 nm down to 100 nm were fabricated. For our EBL-process, the minimum feature size of the gate foot trench is limited by the thickness of the resist layer. But a thick resist is necessary to etch the gate foot trench in the SiN layer due to the fact that the selectivity of the available plasma etching process between the resist and SiN is only 3:1. Therefore, the thickness of the passivation layer (d_{SiN}) limits the minimum feature size of the gate foot trench. The general rule of our SiN-gate technology is that the smallest gate length is equal to the thickness of the passivation layer. An independent increase of d_{SiN} to reduce the parasistics of the gate head is therefore not possible. To allow gate lengths down to 100 nm all wafer with the SiN gate module are passivated by a 100 nm thick SiN layer.

The size of the gate head and subsequently the geometries of the gate head overhangs are defined by optical lithography. The minimum feature size of the gate head was 0.7 µm at the beginning of this work.

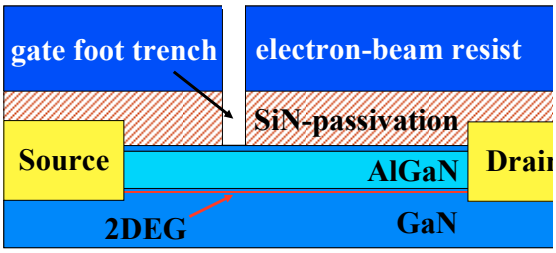

Figure 4-5: Schematic cross section of an HEMT after the dry etching process of the gate foot trench.

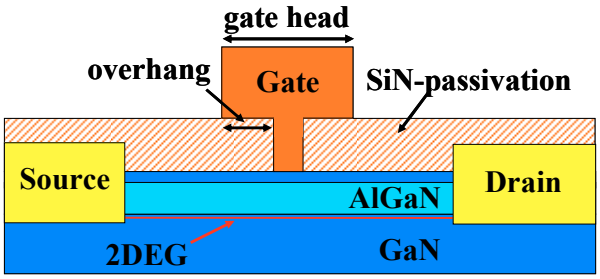

Figure 4-6: Schematic cross section of the HEMT after gate metallization.

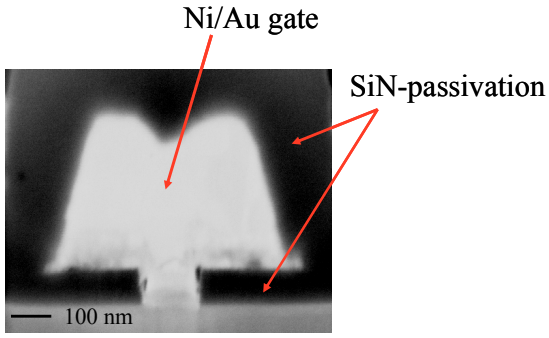

Figure 4-7: FIB-cross section of the gate module after metallization and deposition of the 2nd SiN-passivation layer.

Due to optimizations of the optical lithography process the minimum feature sizes have been reduced to 0.5 µm. Given these minimum dimensions the smallest SiN-gate module has a gate foot length of 100 nm with 200 nm gate head overhangs and a gate foot height of 100 nm. Because of the modular processing of the SiN-gate module a wide range of gate geometries can be fabricated on the same wafer. To study the effects of the gate length scaling, transistors with L_g from 500 down to 100 nm were fabricated. For the evaluation of the parasitic gate head capacitances gate modules with overhangs ranging from 200 to 500 were designed.

After the processing of the gate module all devices are again passivated with a second SiN-passivation layer. As a result the gate module is completely covered in SiN (see Figure 4-6).

4.3 The T-gate module

To study the influence of the SiN passivation on the parasitic capacitances a free standing T-gate module was developed. The different sensitivities of three distinct EBL-resists are used to create a T-shaped gate module in one lithography step (see Figure 4-8). Similar technologies are used for the processing of mmW-transistors and a detailed description can be found in [Lal01] [Mat81]. With this process the gate geometries are independent of the SiN thickness. The limiting factors are now the thicknesses of the three resist layers which can be optimized for the desired gate geometries. Besides the new degree of freedom regarding the passivation material and thickness, the T-gate module features several improvements which further decrease the parasitic components of the gate module. The gate head size could be reduced to 400 nm whereas the distance of the gate head from the surface could be increased from 100 to 125 nm.

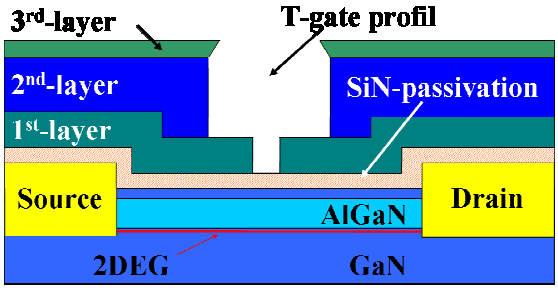

Figure 4-8: Three layer resist for the fabrication of T-shaped gates.

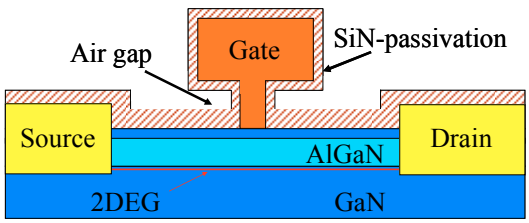

Figure 4-9: Schematic cross section of the HEMT with the T-gate module.

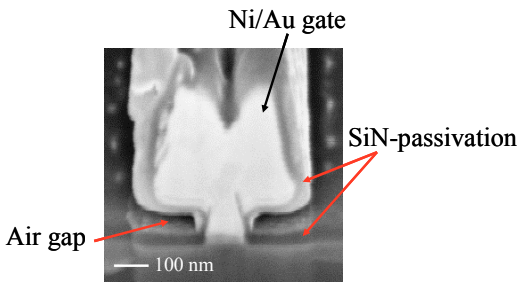

Figure 4-10: FIB-cross section of a HEMT fabricated using the T-gate module.

As can be seen in Figure 4-9 and Figure 4-10, the T-gate modul can be passivated in such a way that an air gap below the gate head remains. Such devices are used in this work to simulate the effect of a low-ε material on the parasitic capacitances

4.4 Self aligned gate recess

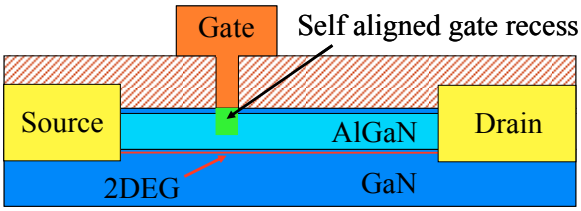

Figure 4-11: Schematic diagram of the self aligned gate recess process.

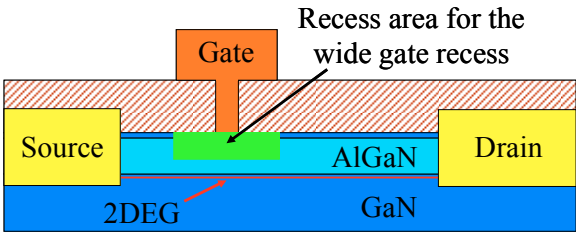

Figure 4-12: Schematic cross section of a HEMT with the wide gate recess.

The growth of thin heterostructures is only one method to achieve barriers with the desired thickness. Another approach is the etching of the AlGaN layer, in the gate foot area, during the device processing. The most important advantage of this method is that the majority of the source and drain regions are unaffected by the etching process and the source and drain resistances remain the same compared to non etched devices. Therefore, an adjustment of the barrier properties is not needed.

For the recess technology two general device layouts for the recess process are possible:

1.) A self aligned recess technology using the gate foot trench as etching mask (see Figure 4-11). This technology has the advantage that it is easily added to existing process flows, because an additional etching mask is not needed. Commonly, atomic force microscopy (AFM) is used to control such etching processes with regard to surface roughness, etch depth and process residues. Due to physical limitations of our measurement probes, AFM measurements cannot be performed at 100 nm wide trenches. The only possibility is to draw conclusions from test patterns with larger di-

mension. But for short trenches the behavior of the etching process can change [Per96]. Therefore, this approach is always susceptible to misinterpretations.

2.) Another method is to use an additional mask for the gate recess step. The lateral dimension of this layer must be greater than the gate foot (see Figure 4-12) to compensate a typical alignment error of the available lithography equipment of 50-200 nm between two lithography steps. An advantage of this approach is that an AFM-measurement of the recess trench is possible. But due to the greater etched area, regions besides the gate are also thinned, which will increase the channel resistance due to the depletion of the 2DEG or reduce the low field mobility due to an etching damage.

In this work only the self-aligned gate recess process is used, due to the facts that, the technology is easily added to the device process flow and the influence on the extrinsic device parameters is expected to be less, compared to a wide recess.

GaN and its ternary compounds are highly chemically stable. This characteristic is used by many sensor applications [Sch10, Abi09] but in semiconductor processing the high stability causes several process challenges. Commonly wet etching methods are used for recess processes to prevent a lattice damage caused by a plasma process. Despite world wide intensive research, no process compatible wet etching method is currently available for GaN [Zhu04]. Therefore, plasma etching processes based on Cl_2 or chlorine compounds are utilized to reduce the barrier thickness [She06], [And10]. Another challenge for the recess process is the absence of an etch stop layer. It is possible to add a thin AlN layer into the barrier, which has a far lower etch rate as AlGaN. But based on the position inside the barrier, each AlN layer modifies the band structure in a different way. A study of the barrier thickness under the gate and the influence on g_{m_ext} would therefore be influenced by an unknown effect of the AlN

layer. For a first study, the recess was therefore carried out without such modifications to the barrier structure. But without an etch stop the recess depth can only be controlled by the etching rate and process time. This causes an uncertainty regarding the recess depth. To minimize the fluctuation, a process with a very low etching rate is necessary. Additionally, the physical component of the plasma process must be reduced to minimize the damage of the remaining barrier.
For the ZMN technology a BCl_3 based gate recess was developed as well as a Cl_2 based plasma etching process for the IAF technology. Both recess variants have very low chamber pressures to reduce the etching rate and strongly reduced bias potentials to minimize the physical component.

With these different technologies and the new heterostructures described in chapter 3, HEMTs with different design layouts were fabricated. The goal of these series of experiments was to determine the influence of each major design parameter on the high frequency characteristics. In the next two chapters the results of the characterization and the de-embedding of the major electrical parameters of the HEMT basis cell will be discussed in detail.

5. Scaling properties of HEMTs regarding the maximum transconductance

The transconductance (g_m) is the most important device parameter of field effect transistors in order to achieve high frequencies. To improve g_m the influence of device geometries, epitaxy and technologies must be evaluated. In chapter 2 the theoretical dependencies of device and barrier parameters on g_{m_ext} were discussed. From these considerations two methods to enhance the transconductance have been derived:

1.) Reduction of the loss from intrinsic to extrinsic transconductance.

2.) Improvement of the intrinsic transconductance by device and barrier scaling.

The source resistance is the primary cause of the reduced extrinsic transconductance. In section 6.1 various methods are studied to minimize this loss. The influence of gate length on g_{m_int} is studied in section 6.2 and discussed whether a short gate length approximation can be used. In the following section the scaling behavior of the intrinsic transconductance regarding the barrier thickness is evaluated. Two technologies were developed to achieve thin barriers. They are compared with regard to g_{m_int} and possible device degradation such as high leakage currents. GaN exhibits an overshoot of the saturation velocity at electric field strengths of 50-100 kV/cm but common values for HEMTs under operation exceed 400 kV/cm at the drain side of the gate. According to Palacios [Pal06] a source terminated field plate can significantly reduce the electric field peaks which improves the saturation velocity and the transconductance. In section 6.5 this behavior will be evaluated by measuring devices with our field plate technology, and simulating an equivalent HEMT structure with the ATLAS software. In the final section all results are summarized, and an outlook for optimized mmW-HEMT scaling is given.

In the next chapters only the scaled geometries of the measured transistors will be given. A full description of the device layout can be found in Appendix A using the individual device code. If not otherwise specified all HEMTs are measured on wafers with 25 nm barrier thickness and 22% Al-content.

5.1 Influence of the source resistance on the extrinsic transconductance

The source-gate voltage controls the electric field under the gate and therefore the current along the channel. The gate voltage is reduced by the voltage drop along the source resistance (R_S) of the HEMT, which causes a reduction of the measured extrinsic transconductance. The intrinsic (g_{m_int}) and extrinsic values (g_{m_ext}) can be correlated by equation (2.15). As discussed in chapter 2, R_s is defined by the material system and technology (see equation (2.16)). According to equation (2.15) the extrinsic transconductance exhibits a non linear trend for high g_{m_int} or very low R_S. If the source resistance increases or g_{m_int} is very low the behavior changes to a nearly linear slope. To determine the behavior for GaN-based devices, HEMTs with different R_S are examined. In Figure 5-1 the extrinsic and intrinsic transconductance for transistors with source resistances from 0.4 up to 1.4 Ωmm are depicted. As can be seen, the extrinsic transconductance depends strongly on R_S, and the decrease of g_{m_ext} over the source resistance follows a nearly direct proportional trend regarding R_S.

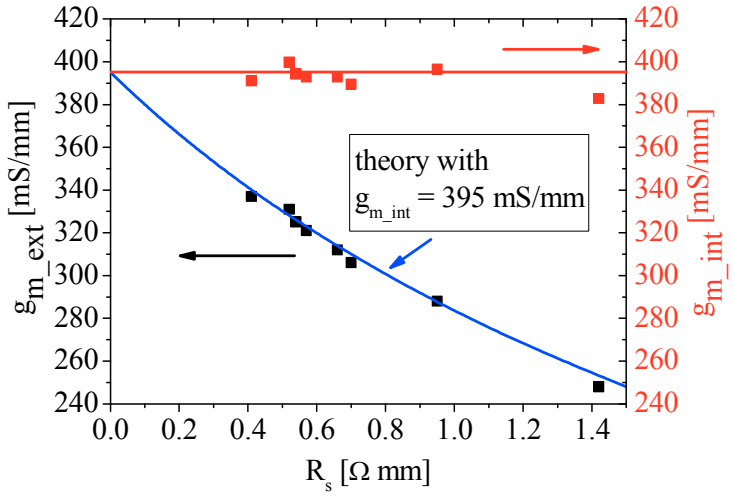

Figure 5-1: Extrinsic and intrinsic maximum transconductances, measured at 7 V drain bias over source resistance. Additionally the theoretical slope of g_{m_ext} is shown using equation (2.15) and an intrinsic transconductance of 395 mS/mm.

To exclude an influence of the gate-drain resistance on g_{m_ext}, HEMTs with drain resistances (R_D) from 0.51 to 1.1 Ωmm (E203-E205) were measured. The maximum extrinsic transconductances are depicted in Figure 5-2. As can be seen the drain resistance has nearly no effect on g_{m_ext}. Therefore, only the influence of the source resistance will be studied in the next sections.

The source resistance derived by S-parameter measurements and calculations using the small-signal equivalent circuit (see Figure 2-2) depends strongly on the frequency. Further a statistical error occurs due to the fact that the extrinsic source resistance (R_s) and the intrinsic load resistance of the gate foot (R_i) cannot be separated without an exact model of the extrinsic shell, which is only available if a specific layout or technology is established. For the development of new HEMT technologies another method has to be used. In this work, the source resistances are derived from a three terminal DC measurement between source and gate.

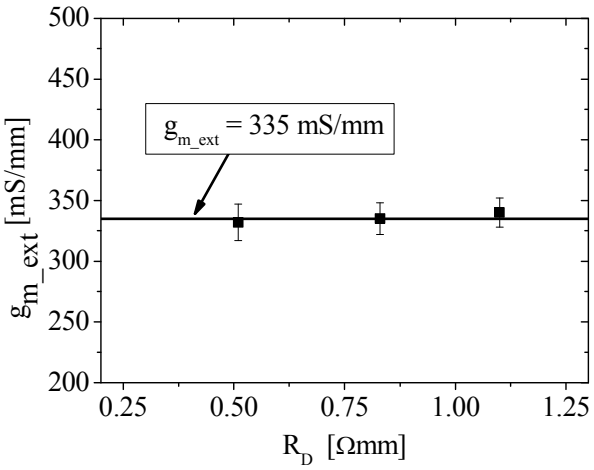

Figure 5-2: Extrinsic maximum transconductances measured at 7 V drain bias over drain resistance.

5.1.1 Reduction of the source resistance by a scaling of the source gate spacing

As was discussed in chapter 2, the source resistance must be reduced by the same scaling factor as all other device parameters. For our specific HEMT technology a source resistance of less than 0.25 Ωmm is required to successfully scale the transistor. In the next two sections different technologies are discussed to achieve this goal.

Because R_s is a sum of the contact resistance (R_{con}) and the channel resistance ($R_{channel}$) between source and gate, a common approach for field effect transistors is to minimize $R_{channel}$ by a scaling of the source-gate distance. In Table 5-1 all resistances for transistors with 0.5, 0.7 and 1.0 µm source-gate spacings are shown (MW81, MW41, A204).
As can be seen in Table 5-1 the channel resistance ($R_{channel}$) scales directly with the source gate spacing. But due to the fact that R_{con} is constant and in the same range as $R_{channel}$ the overall scaling of R_S is much weaker.

Table 5-1: Summary of the contact resistance (R_{con}), channel resistance ($R_{channel}$) and source resistance (R_S) of HEMTs with scaled source gate spacings.

L_{sg} [µm]	R_{con} [Ωmm]	$R_{channel}$ [Ωmm]	R_S [Ωmm]	percentage of R_{con} on R_S [%]
0.5	0.15	0.26	0.41	37
0.7	0.15	0.37	0.52	29
1.0	0.15	0.52	0.67	23

5.1.2 Reduction of the source resistance due to a decreased sheet resistance

Another approach to minimize the source resistance is to decrease the sheet resistance (R_{sheet}) of the 2DEG channel. Various methods are discussed in the literature to achieve low R_{sheet}:

1.) Highly Si-doped GaN-cap or barrier layer [Pei07].

2.) Si-implantation of the GaN buffer near the contact pads [Nom07].

3.) Thin AlN layer at the interface [Xue10].

4.) Barriers with high Al content [Koh09] [Din10].

5.) Heterostructures with thicker barrier layers [Amb00].

A variation of barrier parameters can be easily realized with our existing heteroepitaxy process. With an optimization of the Al-content and barrier thickness, the sheet resistance of the wafers can be minimized (see chapter 3). In Figure 5-3 the sheet resistances of wafers with different barrier parameters are shown. With increasing sheet carrier concentration the low-field mobility decreases (see chapter 3) which causes the minimum at d_{bar} = 14 nm and x_{Al} = 30%.

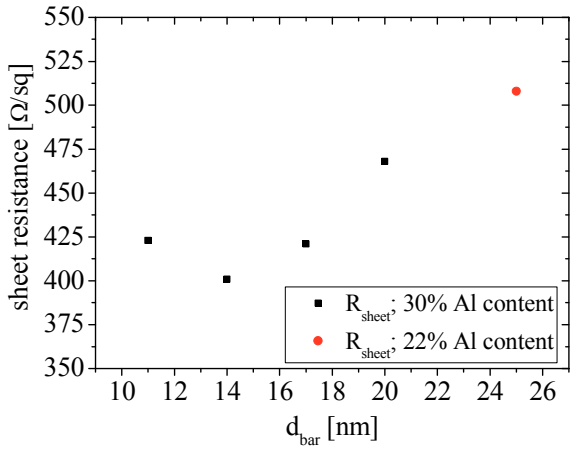

Figure 5-3: Sheet resistance for wafers with different barrier thicknesses and Al-content.

In Table 5-2 the sheet resistances for the wafers used in this work are summarized. Furthermore, all components of the source resistances for transistors with 0.5 µm source-gate spacings are shown (MW81). Similar to the scaling of the source spacing a reduction of the sheet resistance has only a diminished effect on R_S. Under these circumstances wafers with sheet resistances below 200 Ω/sq are necessary to achieve the scaling goal. But such wafer did not exist in the course of this work. The lowest values for R_{sheet} on wafers with AlGaN/GaN barriers are above 250 Ω/sq. To reduce R_{sheet} advanced barrier designs have to be used such as AlN-spacer layer [Wan07], or AlN-GaN super lattices [Zha10]. Furthermore quaternary materials such as AlInGaN are intensively studied to achieve sheet resistances below 200 Ω/sq [Zim10].

Table 5-2: Scaling of the source resistance (R_S) and channel resistance ($R_{channel}$) with reduction of the sheet resistance (R_{sheet}).

R_{sheet} [Ω/□]	R_{con} [Ωmm]	$R_{channel}$ [Ωmm]	R_S [Ωmm]	comment
200	0.15	0.14	0.29	theoretical value
400	0.15	0.28	0.41	measured
455	0.15	0.32	0.47	measured
512	0.15	0.36	0.51	measured

5.1.3 Summary of the source resistance scaling

With our mmW-HEMT-technology with a 14 nm thick barrier containing 30 % Al and 0.5 µm source-gate spacings a source resistance of 0.41 Ωmm is possible. But this value is still considerably higher than the desired value of 0.25 Ωmm. The main limitation is our process to fabricate the ohmic contacts. Due to the high edge roughness of the annealed contacts the source gate spacings can only by scaled down to 0.5 µm. This would be sufficient for an ohmic contact with a negligible contact resistance but the values obtained with our process are in the range of the channel resistance of the highly scaled HEMTs. Due to the fact that our technology achieves state of the art values for annealed contacts an improvement can only be expected by using novel contact technologies which are currently not available. In Figure 5-4 the reduction of f_T is extrapolated for a HEMT with R_s = 0.41 Ωmm instead of 0.25 Ωmm but otherwise constant parameters using equations (2.15) and (2.19). As can be seen in the diagram the loss increases for higher frequencies and at 100 GHz a difference of 10 GHz is caused by the high source resistance compared to an ideally scaled device. Therefore, the remaining HEMT parameters must be further scaled down to achieve the desired gain at high frequencies.

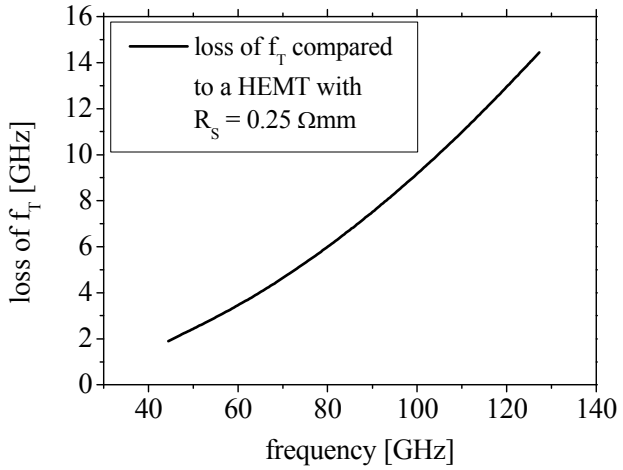

Figure 5-4: Reduction of f_T over frequency for a HEMT with R_S= 0.41 Ωmm instead of 0.25 Ωmm.

5.2 Influence of the gate length on the transconductance

According to FET theory (see chapter 2), for very small gate length (short-channel) the transconductance of HEMTs is independent of the gate length and only limited by the saturation velocity and barrier thickness. Devices with very large gate length (long-channel) are limited by the low field mobility and the transconductance becomes a function of the gate length (see Figure 5-5). Using these equations and the material constants given in Table 1-1 and Table 3-2, the gate length of an AlGaN/GaN-HEMT must be shorter than 50 nm to

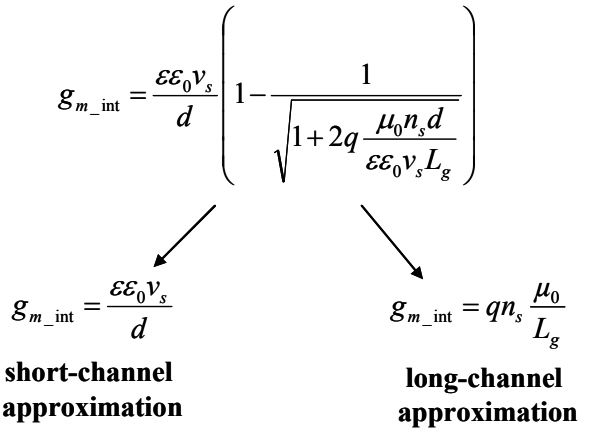

Figure 5-5: Intrinsic transconductance as a function of device and barrier parameters as well as short- and long-channel approximations.

allow a short-channel approximation or larger than 5 µm to fulfill the long channel approximation in good agreement. The gate length used in this work is in the range of 100 nm to 500 nm, rendering both approximations invalid for the examined HEMTs. Many simplifications had to be used to derive the equations in Figure 5-5. For a general understanding and approximation these equations are sufficient, but for an evaluation of actual device behavior devices with scaled gate length have to be characterized with regard to their short-channel behavior. To study the effect of the gate length on g_{m_int}, devices with gate length from 500 nm down to 100 nm (A101, MW43, E104, MW51, MW52 and MW53) are measured on wafers with d_{bar} = 25 and d_{bar} = 14 nm. The peak intrinsic transconductance is derived using (2.15) as well as the measured extrinsic transconductance and source resistance. These values are then compared

to the theoretical trend of g_{m_int} over L_g given by equation (2.5). As can be seen in Figure 5-6 and Figure 5-7 the intrinsic transconductance increases for shorter gate length and follows the general trend given by equation (2.5). The slightly different slope of g_{m_int} on the wafer with d_{bar} = 25 nm (see Figure 5-6) are most likely caused by fringing effects due to the fact that wafers with thinner barriers (see Figure 5-7) correlate better with the theoretical trend.

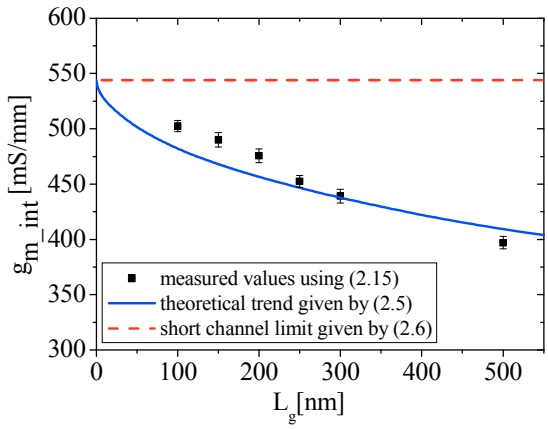

Figure 5-6: Maximum intrinsic transconductance over gate length on a wafer with 25 nm barrier thickness. Additionally the theoretical trend given by (2.5) and the short gate length limit given by (2.6) are depicted.

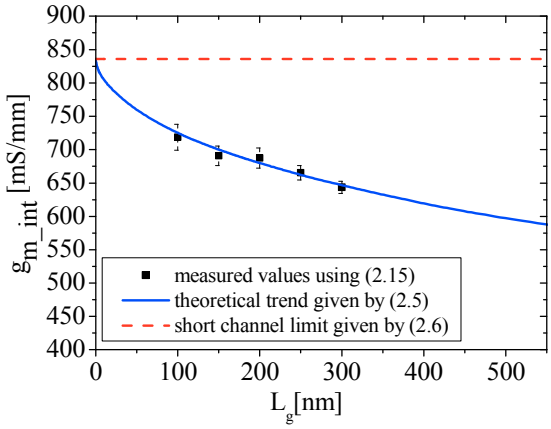

Figure 5-7: Maximum intrinsic transconductance over gate length on a wafer with 14 nm barrier thickness. Additionally the theoretical trend given by (2.5) and the short gate length limit given by (2.6) are depicted.

This effect will be discussed in more detail in chapter 6. But also a general error due to small fluctuations of the gate length or an extraction error can also explain this behavior and cannot be ruled out by the available sample size.

Transistors with L_g of 100 nm approach the short-channel limit for g_{m_int}. For such HEMTs the transconductance is strongly dominated by the electron velocity and barrier thickness whereas the gate length has only a marginal influence on g_{m_int}. Therefore, the short-channel approximation is used in the following chapters to describe the theoretical limits of g_{m_int}. In the next sections different methods and technologies are studied to optimize the intrinsic transconductance with special emphasis on barrier scaling and an improvement of the electron velocity.

5.3 Influence of the barrier thickness on the transconductance

In this section only gate length scaled devices with L_g = 100 nm will be studied. As evaluated in the previous section the intrinsic transconductance can be given for such dimensions by the short-channel approximation given by equation (2.6). In this chapter process variants are studied to decrease the barrier thickness and therefore enhance the transconductance.
The reduction of d_{bar} can be achieved basically by two methods (see chapter 2 and 3):

1.) The growth of a thin barrier which will be evaluated in section 5.3.1

2.) A recess etching of the barrier under the gate which will be discussed in section 5.3.2

5.3.1 Reduction of the barrier thickness by thin grown barriers

The growth of a thin AlGaN layer is an effective method to decrease the barrier thickness because no additional process steps are needed. The details of AlGaN heteroepitaxy via MOCVD and the influence of barriers properties on the 2DEG characteristics were discussed in detail in chapter 3. Therefore, only a short summary will be given here. With the reduction of the barrier thickness charged donor states at the surface end up below the Fermi level for thin barriers and can therefore no longer provide the electrons for the 2DEG. This causes a strong reduction of n_s and an increase of the sheet resistance. The negative effect of the barrier reduction can only be compensated by an increase of the Al-content. To study the effect of the barrier thickness on g_{m_int}, wafers with d_{bar} of 11 nm, 14 nm and 17 nm were grown by MOCVD. To achieve the same sheet carrier concentrations as wafers with 25 nm barrier the Al-content was increased to 30%. To be able to compare the results to the reference barrier, wafers with d_{bar} = 25 nm and x_{Al} = 22% were processed together with wafers with thin barriers. On all wafers the transfer characteristic and transconductance are measured for HEMTs with L_g = 100 nm (MW41). The re-

sults are depicted in Figure 5-8 and Figure 5-9. As expected, the extrinsic transconductance increases with thinner barriers from 395 to 610 mS/mm. But the increase of g_{m_ext} is far to low to achieve the desired value of 850 mS/mm, according to the scaling rules (see chapter 2). One cause of the reduced gain of g_{m_ext} is the high source resistance of our technology discussed in section 5.1. But this effect can only explain a loss of g_{m_int} to g_{m_ext} in the range of 10-20%.

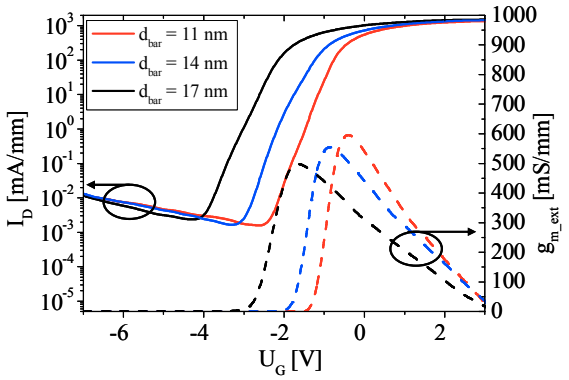

Figure 5-8: Transfer characteristics and extrinsic transconductance for HEMTs with barrier thicknesses of 17 nm (red), 14 nm (blue) and 11 nm (black). All barriers have 30% Al-content. All transistors are measured at 7 V drain voltage.

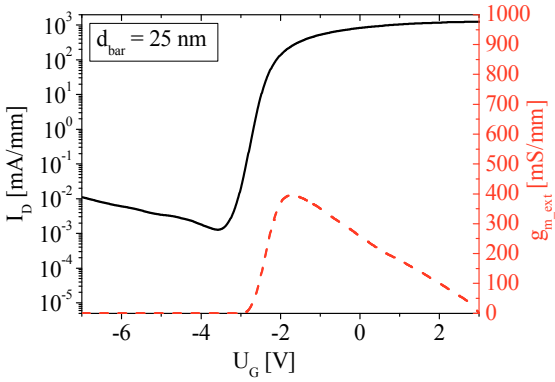

Figure 5-9: Transfer characteristics and extrinsic transconductance of reference HEMTs with d_{bar} = 25 nm and 22% Al-content, measured at 7 V drain voltage.

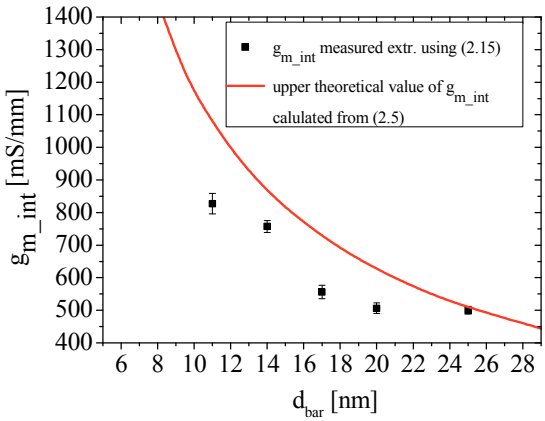

Figure 5-10: Intrinsic transconductance over barrier thickness compared to calculated values using equation (2.5) for HEMTs with 100 nm gate length.

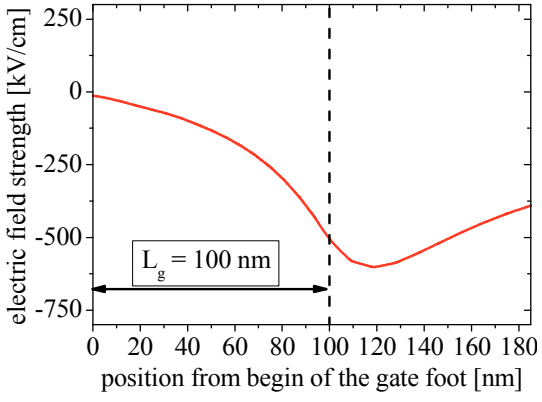

Figure 5-11: Simulation of the electric field strength along the gate foot for a device with L_g = 100 nm.

In Figure 5-10 the intrinsic transconductance is depicted, excluding the influence of R_s by using equation (2.15). As can be seen the trend of g_{m_int} is far below the expected increase given by (2.5). Measurement errors or process fluctuations cannot explain the difference, as the mean variance between 21 transistors on one wafer is far less than the discrepancy. Also a drastic change of the crystal quality between the wafers can be ruled out, due to the fact that all wafers exhibit comparable sheet carrier concentrations and low field mobilities (see Table 3-3). A further proof of the barrier quality is that the reverse leakage current at U_D = -7 V does not change between the wafers (see Figure 5-8 and Figure 5-9). In Figure 5-11 the simulation of the electric field strength for the gate region of a HEMT with L_g = 100 nm is shown.

To minimize possible errors due to the design layout, exactly the same device geometries as the measured HEMTs (MW41) were used in the simulation. As can be seen in the diagram, the electrons are exposed to a strong gradient of the electric field. At these dimension the drift-diffusion model used to derive equation (2.5) is no longer adequate. For transistors with longer gate length this effect should be less compared to the devices with L_g = 100 nm.
Therefore, HEMTs with L_g = 250 nm were measured and g_{m_int} was extrapolated as described before. The intrinsic transconductance of these devices as well as the theoretical trend given by (2.5) is depicted in Figure 5-12. For barrier thicknesses greater than 17 nm, g_{m_int} is in good agreement to the theoretical values. If the gate length is kept constant, the electric field rises for thinner barriers, and at d_{bar} < 17 nm the extrapolated transconductances diverge from the theoretical trend. These results verify, that for scaled HEMTs the drift-diffusion model is no longer adequate to predict the transconductances of GaN-HEMTs.

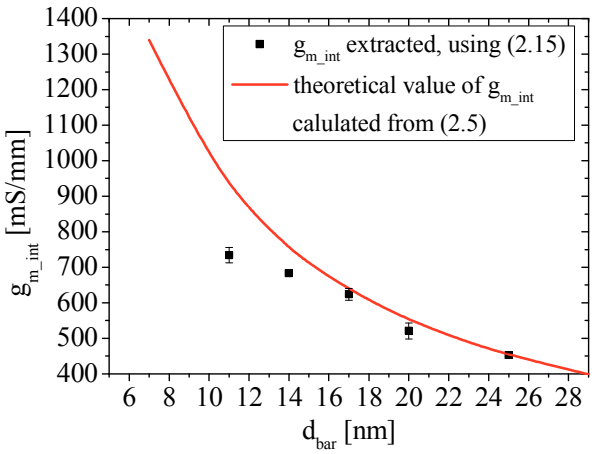

Figure 5-12: Intrinsic transconductance over barrier thickness compared to calculated values using equation (2.5) for HEMTs with 250 nm gate length.

5.3.2 Reduction of the barrier thickness using a gate recess

Another approach to reduce the barrier thickness is to etch the AlGaN layer in the gate foot area during device processing. The most important advantage of this method is that only the barrier near the gate foot is thinned. Most of the source and drain regions are unaffected by the etching process, and the source and drain resistances remain the same for all HEMTs regardless of the barrier thickness under the gate foot. Therefore, an adjustment of the barrier properties is not needed, and easy comparisons between HEMTs with etched and non etched devices are possible. As described in chapter 3 only the self aligned recess is studied in this work because of the relative easy incorporation of the process in the available process flow and the reduced influence on the source resistance.

Extraction of the barrier thickness from the threshold voltage

For the study of the recess process, it is of utmost importance to determine the remaining barrier thickness as exactly as possible. Due to the fact that the recess process utilized in this work is only controlled by the etching time, the barrier thickness is not exactly defined by the process (see chapter 4). Also AFM-measurements cannot be applied to monitor the etching depth because the

available equipment is limited to minimum trench geometries of 500 nm. But such large trenches cannot be used as a reference structure, because the etching rate can change towards higher aspect ratios of L_g to height of the etching mask [Lee91].

From the literature a recess of GaN HEMTs is mostly used to shift the threshold voltage towards positive values and achieve enhancement mode HEMTs [Sai06]. This behavior will be used in this work to monitor the remaining barrier thickness. Following the discussion in chapter 3.1 the threshold voltage of a transistor with an undoped heterostructure derives as:

$$U_{th} = \Phi_b + E_F - \Delta E_c - \frac{\sigma}{\varepsilon\varepsilon_r} d_{bar}, \tag{5.1}$$

with Φ_b the Schottky barrier height for the gate metal. According to theory the threshold voltage should be a linear function of the barrier thickness if the Al-content and Schottky-metal is the same. To verify (5.1), the threshold voltage is measured on wafers with different Al-content and barrier thicknesses. In Figure 5-13 the measured values are compared to the calculated trend. The values are in very good agreement to the simulated trend. An uncertainty of 1 nm remains but this is much smaller than the error from etch rate calculations.

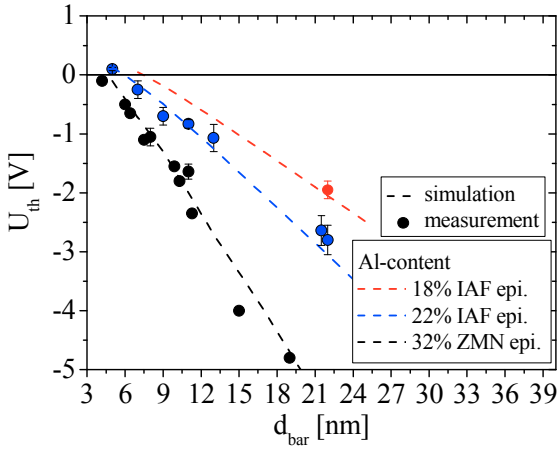

Figure 5-13: Comparison of simulated values of the threshold voltage and measured devices on wafer with 18, 22 and 32% Al content over the barrier thickness.

Therefore, all barrier thicknesses are derived from (5.1) in the following studies. The diagram (Figure 5-13) also demonstrates that normally-off or also called enhancement mode HEMTs are possible by using a gate recess process.

Self aligned gate recess

For all gate recess experiments wafers with d_{bar} = 25 nm and x_{Al} = 22% were used and recess depths from 2 to 19 nm were realized on these wafers. The extrinsic transconductance (see Figure 5-14) increases from 400 mS/mm to 510 mS/mm with decreasing barrier size. The devices on this wafer (H1) have greater source gate distances and therefore a higher source resistance compared to devices measured in the previous chapter. The higher R_S explains the diminished increase of g_{m_ext} compared to the wafers with thin d_{bar}. In Figure 5-15 the intrinsic transconductance is depicted, excluding the effect of R_s. As can be seen in the diagram, the slope of g_{m_int} is also limited by the short-channel effect discussed previously. But due to the fact that thinner barriers can be realized with the gate recess process, intrinsic transconductances of more than 900 mS/mm can be achieved (see Figure 5-15). In Figure 5-16 the slope of g_{m_int} is depicted for both technologies.

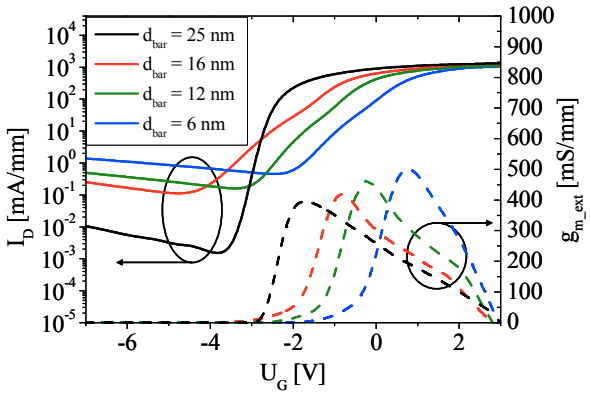

Figure 5-14: Transfer characteristics and extrinsic transconductance for transistors with different barrier thicknesses and L_g = 150 nm after gate recess. All HEMTs have barriers with 22% Al-content and are measured at 7 V drain voltage.

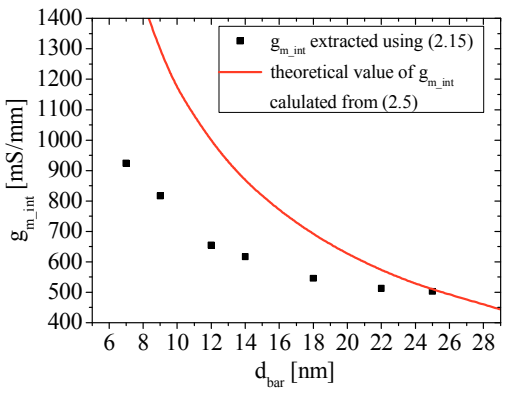

Figure 5-15: Intrinsic transconductance over barrier thickness compared to calculated values using equation (2.5) for HEMTs with 150 nm gate length.

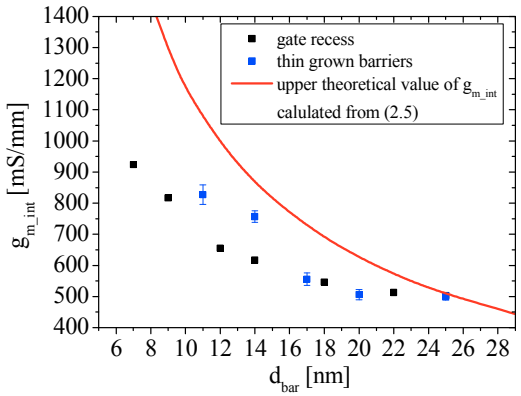

Figure 5-16: Comparison of g_{m_int} over d_{bar} extrapolated from HEMTs with either thin grown barriers or a gate recess process. Additionally the theoretical trend is depicted, using equation (2.5) and a gate length of 100 nm.

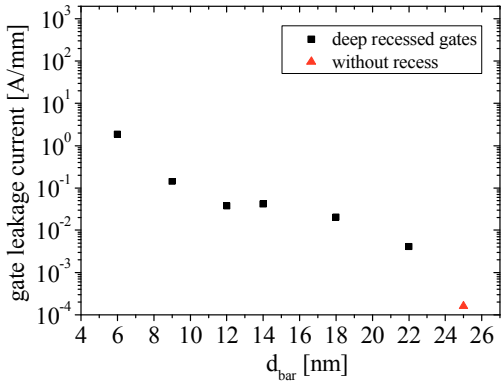

Figure 5-17: Gate leakage current for HEMTs with different recess depth compared to a device without a dry etch process.

The general trend of g_{m_int} is the same but HEMTs with thin grown barriers show better results between d_{bar} values of 11 and 14 nm. This effect can be explained by a damaging of the remaining barrier which is caused by the gate recess process. In Figure 5-15 the gate leakage current of recessed transistors versus d_{bar} is shown. As soon as an etching process is applied the gate leakage current increases significantly. Given the fact that thin grown barriers do not exhibit such a behavior, a damaging of the barrier due to the etching process is most likely the cause of the increased leakage current. One possible origin is the implantation of chlorine ions into the space between the lattice atoms which than become traps inside the barrier and enhances the tunneling of electrons from the 2DEG to the surface (see chapter 2). The implantation of fluor into the barrier and a modification of the surface due to fluorine plasma etching processes are well documented [Yua08], [Wan09], [Hun10c]. Another possibility is the increased etching rates at lattice dislocations. Such effects are utilized in dislocation studies to monitor the quality of the heteroepitaxy [Vis02], [Nak06]. The deep etched dislocations occurring due to the gate recess can become leakage paths and enhance the gate leakage current. Both effects will generate traps inside the barrier which must be charged by the gate voltage before the electric field of the gate can modulate the channel. As a conse-

quence the transconductance is severely decreased, compared to devices without a recess process.

A common technique for recessed devices to suppress these gate leakage currents is the fabrication of MIS-FETs (metal isolator semiconductor field effect transistor) [Liu09], [Ger09]. In a MIS-HEMT structure a 5-20 nm thin isolator layer is deposited after the recess step which greatly reduces the leakage current. But for a transistor process aimed at maximizing the high frequency performance, such an isolator layer must posses many outstanding characteristics. The thickness of the isolator layer must be below 5 nm and must consist of a low-ε material in order to not increase g_{m_int} (see equation (2.15)). Furthermore, the very thin isolation layer must be grown without defects to prevent a gate leakage current. Beside these challenging task for the epitaxy, the defects inside the remaining AlGaN barrier remain and therefore the reduction of $g_{m\_int.}$

In summary, the same trend of the g_{m_int} could be observed for gate recessed devices and thin grown barriers. With the recess technology smaller d_{bar} and subsequently higher g_{m_int} are possible. For thin barriers and at a gate length of 100 nm both techniques exhibit a drop in g_{m_int} compared to the expected trend due to the non-saturation of the electron velocity caused by the short distance in which the electron are accelerated by the high electric field.

The high leakage current of recessed devices limits the use of such HEMTs in integrated circuits. HEMTs with thin grown barriers show no degradation in their leakage behavior and are therefore used in all further studies in this work.

5.4 Influence of source terminated field-plate structures on the transconductance

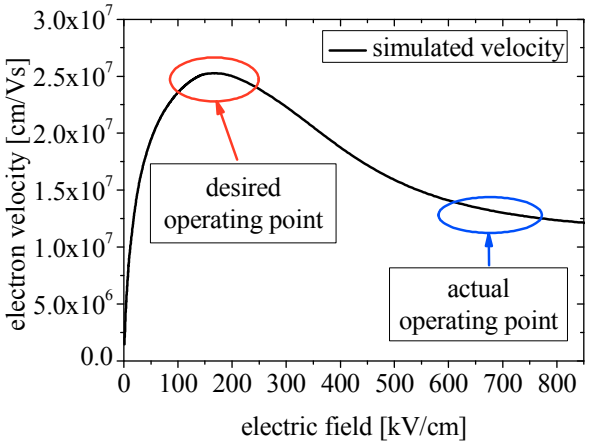

Figure 5-18: Simulation of the electron velocity in bulk GaN versus the electric field using the model derived by Schwiertz and Polyakov [Sch05].

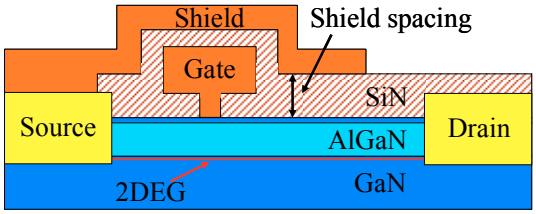

Figure 5-19: Schematic cross section of a HEMT with additional source terminated field plate (shield).

For AlGaN/GaN-HEMTs operating at mmW-frequencies Palacios et al. [Pal08] suggested an additional field plate structure to reduce the electric field strength at the drain side of the gate. As discussed in the last section the high gradient of the electric field at the drain side of the gate causes a short-channel effect which limits the electron velocity. It was further suggested by Palacios et al. [Pal08] that the electric field strength can be reduced to dimensions at which a velocity overshoot effect (see Figure 5-18) according to the gradual channel approximation and drift diffusion model can be observed. In this case the transconductance will be strongly increased and subsequently all dependent parameters such as cut-off frequency and power-gain of the transistor. However, according to the results of the last section the gradual channel approximation as well as the drift diffusion model are no longer valid for highly scaled GaN-based HEMTs. Therefore a detailed analysis regarding the influence of an additional field plate on the transconductance of mmW-HEMTs is conducted in

A schematic cross section of a HEMT with a source terminated field plate is shown in Figure 5-19. To distinguish the field plate of the gate head overhang

from the source terminated field plate the following naming conventions are used in this work: the field plate of the gate head is called the overhang whereas the additional field plate structure is named the shield. HEMTs with 300, 400 and 500 nm drain-sided overhangs (MW31, MW33, MW35) are compared to similar devices with a 1 µm long shield at the drain side of the transistor (MW32, MW34,MW36) to study the effect of different field plate designs on the transconductance. As can be seen in Figure 5-20, neither an increased overhang size nor an additional shield structure has a significant effect on g_{m_int}.

To better interpret these results transistors with and without shield are simulated using the Silvaco ATLAS program. The simulator calculates the electric field strength in two dimensions. For the following discussions only the field component along the channel is depicted (x-axis). It must be noted, that the results of the simulation cannot exactly reproduce the behavior of actual devices but only the general trend. The uncertainties are mostly caused by the used models for the simulation software and the abstraction of the actual HEMT cross section. To minimize the error, a HEMT with the same dimensions as MW32 or MW33 is used as the layout basis for the simulation. Besides the measured HEMT layout the effect of a reduced shield-to-surface spacing on the electric field distribution will also be studied. Transistors with shield spacings of 400, 225 and 130 nm were simulated whereas 400 nm corresponds to the actual device geometry. The results for a HEMT at off-state bias points with drain voltages of 20 and 50 V are depicted in Figure 5-21 and in Figure 5-22, respectively.

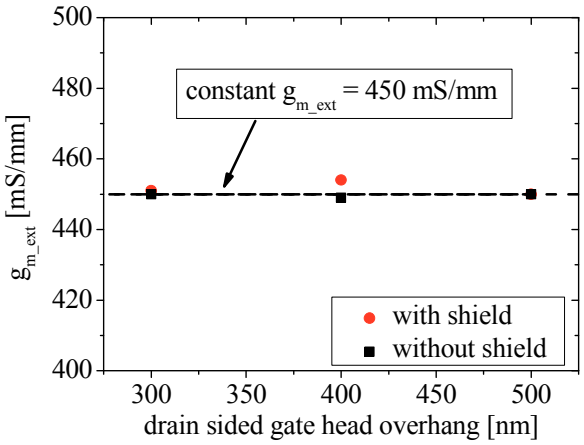

Figure 5-20: Comparison of HEMTs with and without shield over drain-sided gate head overhang with regard to the extrinsic transconductance. The gate length of all devices is 100 nm.

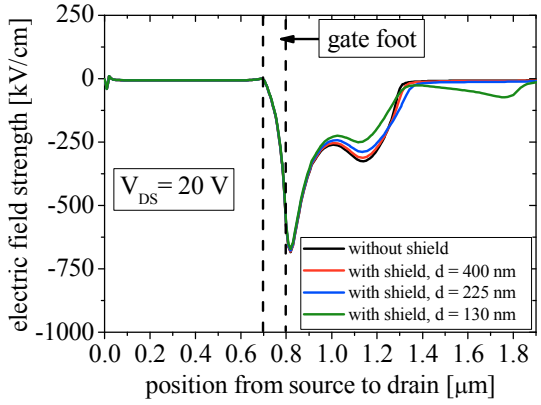

Figure 5-21: Simulations of the electric field distribution of transistors without a field plate (black line) and with different shield-plate distances (colored lines) at off-state with a drain bias of 20 V.

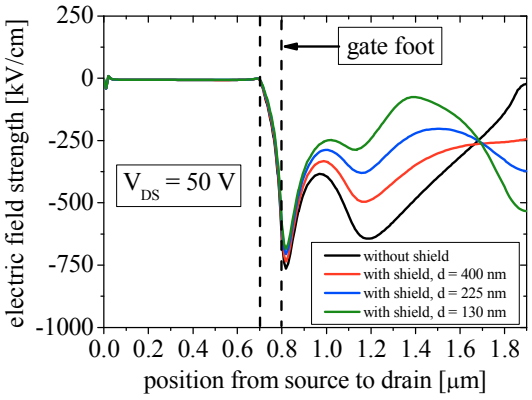

Figure 5-22: Simulations of the electric field distribution of transistors without a field plate (black line) and with different shield-plate distances (colored lines) at off-state with a drain bias of 50 V.

The comparison of both bias points and all shield configuration shows that the peak of the electric field can be reduced by 100 kV/cm but this reduction is not high enough to reach the necessary field strength of 150 kV/cm for the velocity overshot (see Figure 5-18). Given the assumtion that a velocity overshoot still exist for HEMTs with L_g = 100 nm. According to the simulations, the electric field of our mmW-technology is dominated by the barrier properties and gate length of the device. But it is of note that in the drain region and at a high drain bias the shield-plate has a noticeable effect on the electric field distribution. The shield reduces the field peak at the drain overhang and generates a

more uniform field distribution in the drain region (see Figure 5-22). The homogeneous distribution of the electric field decreases C_{gd} and improves the breakdown characteristic which will be studied in more detail in chapter 6. With smaller shield-to-surface spacings the effect of the additional field plate increases. But for a spacing smaller than 200 nm the edge of the shield-plate causes a field enhancement. Following the simulations the optimized distance of the shield metal to achieve a nearly constant field distribution along the drain region is in the range of 200 nm for a drain bias of 50 V (see Figure 5-22).

5.5 Conclusion

In this chapter the improvement of the extrinsic transconductance regarding a scaling of R_s, L_g, and d_{bar} is evaluated. Compared to the technology available at the beginning of this work the extrinsic transconductance could be improved from 330 mS/mm to 610 mS/mm (see Figure 5-23). But the scaled HEMTs feature a diminished increase of g_{m_ext} compared to the scaling laws (see Table 2-1). This behavior is caused by the poor scaling of R_S and that electrons do not reach the saturation velocity for short gate lengths.

For the development of a mmW-HEMT technology a recess of the gate foot cannot be utilized, despite the possibility to achieve thinner barriers and therefore higher g_{m_int}. The high leakage current prevents the use of this technology in a MMIC process until an improved plasma etching process is developed. HEMTs with thin grown barrier show no increase of the leakage current compared to the reference epitaxy. Also the R_S on these wafers is always better than the values on the reference wafer. Therefore, only non-recess devices are studied further in this work.

With the improvement of g_{m_ext} (scaling of R_s, L_g, and d_{bar}) cut-off frequencies of 64 GHz can be achieved (see Figure 5-24). The cut-off frequency follows the increase of $g_{m\_ext,}$ but if the barrier thickness and gate length is scaled down the increase of f_T becomes limited. This effect is caused by the high parasitic capacitance of the gate module which must be scaled down to achieve cut-off fre-

quencies of more than 60 GHz. In the next chapter the parasitic elements of the gate module are identified and it is shown how they can be minimized due to scaling or process optimization.

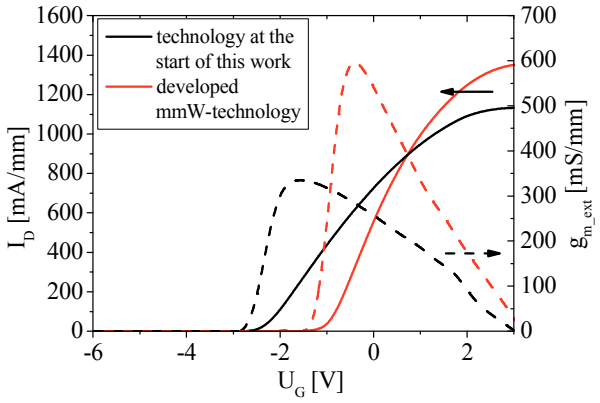

Figure 5-23: Transfer characteristic of a transistor with the reference technology available at the start of this work and the developed mmW-HEMT technology.

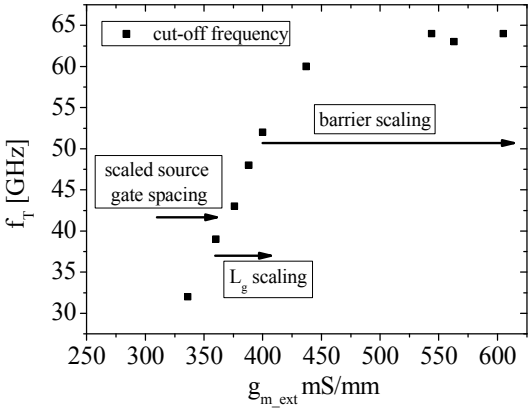

Figure 5-24: Current-gain cut-off frequency over transconductance for HEMT fabricated with the SiN-gate technology.

6. Scaling properties of mmW-HEMTs regarding the capacitance

In order to successfully scale the transistor, the gate length must be reduced by the same factor as the barrier thickness to keep the gate foot capacitance constant (see chapter 2). However, much more important is the reduction of the parasitic capacitance of the gate module in order to improve the gain at high frequencies. Therefore, the scaling factors of the whole gate module and the influence of the technology regarding the gate capacitances must be evaluated for the development of a mmW-HEMT technology. The most common method to determine the intrinsic HEMT parameters is by S-parameter measurements and a subsequent transformation to Y-parameters, which are then used to calculate discrete components utilizing the small-signal equivalent circuit which was discussed in chapter 2.

For the design and simulation of MMIC amplifiers, the values of the extrinsic and intrinsic shell of the transistor and gate capacitances are sufficient. But for a successful scaling of the transistor, a more in-depth analysis of the various capacitances related to the gate is necessary. In Figure 1-4 a schematic cross section of a HEMT with its physical capacitive components was shown. In the next sections each of the distinct capacitances is evaluated individually starting from the extrinsic shell, and then subsequently extrapolating all physical components of the gate capacitance, which are:

1. The capacitance of the gate head to the drain and source contact pads ($C_{contact}$);
2. The capacitance of the gate head overhangs (C_{head});
3. The capacitance of the gate foot, sidewalls and fringe capacitances (C_{foot}, C_{side}, C_{fringe}).

In high power amplifiers additional source terminated field-plates are commonly used to improve the breakdown characteristic and to reduce the feed-

back capacitance of the gate module [Küh10]. Therefore, the influence of such a field-plate on the capacitances of a mmW-gate module will be evaluated.
The dielectric constant of the passivation layer has a tremendous impact on the capacitance of the gate module. The effect of a low-ε passivation layer is studied in this chapter by passivating the gate with SiN in such a way that an air-gap remains below the gate head.

6.1 Definition of the measurement conditions

Because the capacitances are bias dependent (see Figure 6-1 and Figure 6-2) two important bias points are used in this work:

1. The off-state point is measured at pinch-off (at least 2 V below the threshold voltage) with a source drain voltage of 0 V. At this bias point the gate capacitance is independent of the gate foot and the drain electric field. Therefore the gate capacitance becomes only a function of the parasitic elements at these bias conditions.
2. The on-state point is defined by a gate voltage which causes a saturation of the drain current and a source drain voltage of more than 7 V. At this bias point, capacitances caused by the gate foot electric field can be evaluated.

If not otherwise specified, all measurements are taken on wafer with a 25 nm barrier with 22% Al-content, which were processed with the SiN-gate technology (see chapter 4). Only the examined geometries and the device code for the measured HEMT devices are given in the next chapters. A full description of each device can be found in appendix A using the individual device code.
To be able to compare HEMTs with different number of gate fingers or gate widths, most device parameters are normalized to the gate width. For a discussion of the scaling properties of the gate module that specification must be modified to account for the scaled geometries and the following definition is used in this work.

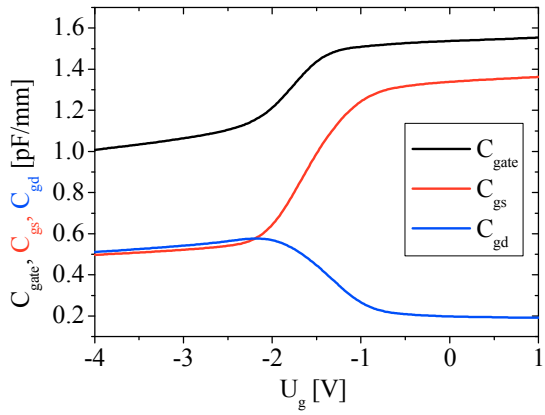

Figure 6-1: Capacitance of the gate module and its components at different gate source voltages and a constant drain voltage of 0V. C_{gd} and C_{gs} are extracted values using the small-signal equivalent circuit and C_{gate} is the sum of C_{gd} and C_{gs}.

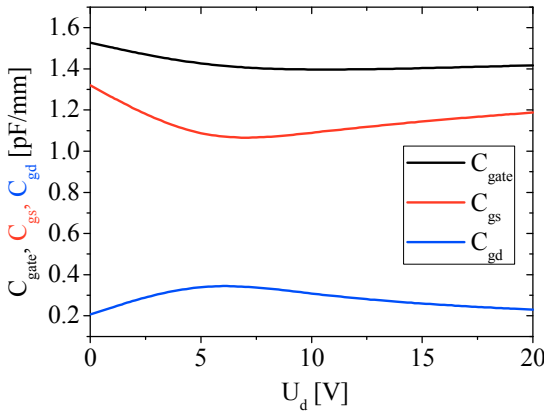

Figure 6-2: Capacitance of the gate module and its components at different drain voltages and constant gate voltage of -0.5 V. C_{gd} and C_{gs} are extracted values using the small-signal equivalent circuit and C_{gate} is the sum of C_{gd} and C_{gs}.

All scaling parameters are given in unit per area (A), where one side is given by the gate width in mm and the other by the scaled geometry in units of 100 nm. For example the capacitance per area of the gate foot is 0.48 pF/A, which results in a gate foot capacitance of 0.96 pF/mm for a 200 nm gate. With this convention, the extracted scaling properties can be easily compared to usual units.

6.2 Capacitive coupling of the extrinsic shell

In this work, single test HEMTs are used to measure the capacitances of the gate module. To contact such transistors with the probes of a network analyzer, the device must be designed with relatively large contact pads compared to the size of the actual transistor (see Figure 2-3). These pads have capacitive coupling between each other which must be eliminated in order to extract the intrinsic capacitances of the transistor. Commonly only the extrinsic portions are described as parasitic capacitances. For this work this definition is not adequate and a more comprehensive definition is used. All capacitances which are independent of the gate foot length are called parasitic capacitances (C_{para}).
For a given pad design, the extrinsic capacitance is constant.

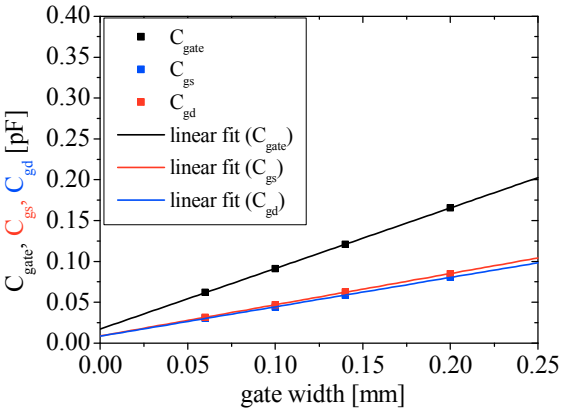

Figure 6-3: Off-state capacitance of HEMTs with different gate widths and extrapolation of the extrinsic pad capacitance.

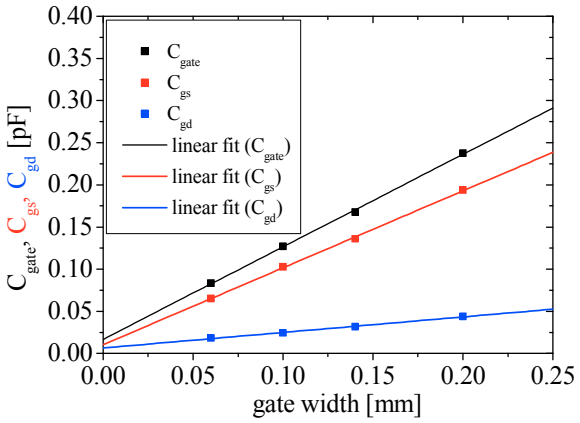

Figure 6-4: On-state capacitance of HEMTs with different gate widths and extrapolation of the extrinsic pad capacitance.

Therefore, a common method to determine these capacitances is to measure transistors with different gate widths but otherwise same design and extrapolate the capacitance for a gate width of 0 µm. The remaining offset value at 0 µm is the capacitance caused by pad-to-pad coupling. Because the extrinsic part is independent of the bias conditions the extrapolated pad capacitance for on-state and off-state measurements should result in the same value. For this study transistors with gate widths of 60, 100, 140 and 200 µm (MW54, MW41, MW55, and MW56) were measured. The results for HEMTs at off- and on-state bias conditions are shown in Figure 6-3 and Figure 6-4 respectively. The linear extrapolation results in both cases in an extrinsic pad-to-pad capacitance of 0.17 pF which will be subtracted from the measured capacitances in all further studies regarding C_{gate} in this study.

6.3 Scaling behavior of the gate capacitance regarding the pad-to-gate spacings

As was discussed in chapter 2 and evaluated in chapter 5, the source gate spacing must be reduced for a successful scaling of the transconductance. Furthermore, the drain gate spacing must be minimized for mmW-HEMTs to reduce the on-resistance of the transistor (see chapter 2). But in doing so the capacitive coupling of the source or drain contact to the gate module ($C_{contact}$ in Fig-

ure 2-10) may rise significantly. It is therefore necessary to determine the influence of the contact-to-gate spacing on the gate capacitance. For this study transistors with gate drain spacings of 0.7, 1.0 and 2.0 µm but otherwise same layout (E104, E105 and E106 respectively) were used. To exclude an influence of the space charge region at the drain side in on-state operation, all transistors are measured in off-state. As can be seen in Figure 6-5 the gate capacitance is constant for all gate-drain spacings. This result can be explained by the still large distance of 0.7 µm from the gate module to the contact pads.
In the next section the influence of the gate head overhang will be discussed, which will verify this hypothesis.

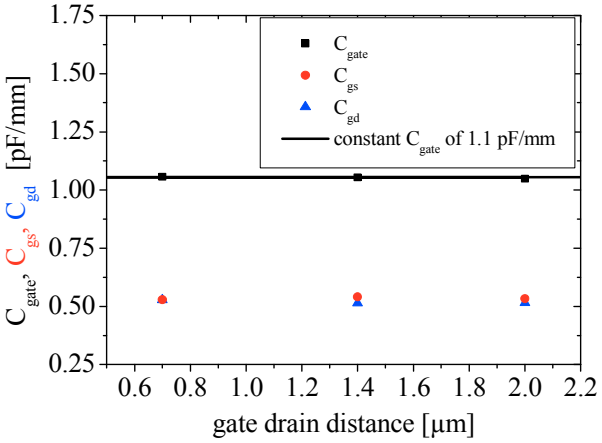

Figure 6-5: Off-state capacitance of HEMTs with different gate drain spacing.

6.4 Scaling behavior of the gate capacitance regarding the gate head overhang

To evaluate the influence of the gate head overhang on the gate capacitance (C_{head} in Figure 2-10), transistors with a drain-sided gate head overhang of 200, 300, 400 and 500 nm (MW41, MW31, MW33, MW35) were measured at an off-state bias point to prevent a distortion by the drain field and achieve a symmetric distribution of the gate head capacitances. The gate capacitance at this bias point is defined only by parasitic capacitances (C_{para}) and can be used to determine the influences of design scaling on the parasitic capacitances. The extrinsic pad capacitances which are evaluated in chapter 6.1 are subtracted

from all extracted values. The parasitic capacitance displayed in Figure 6-6, exhibits a clear linear dependency on the gate head overhang. This trend is expected, because the gate head to channel capacitance can be described as a plate capacitor and a reduction of the area is proportional to a change in capacitance (see equation (2.18)). The linear fit of the capacitances results in a capacitance per scaled area of 0.07 pF/A for a one sided gate head overhang. A two sided scaling of the gate head should therefore result in 0.14 pF/A. To confirm this hypothesis, two transistors with 200 and 300 nm symmetric overhangs are compared (E101 and E106) to the theoretical values (see Figure 6-7). As can be seen in the diagram the theoretical prediction agrees well with actual measurements.

With this result the very low influence of the pad capacitance can be explained (see chapter 6.3). A metal or equipotential layer 125 nm away from the 2DEG causes a capacitance per area of 0.07 pF/A. For a device with 0.7 µm pad gate spacing and an overhang of 0.2 µm, the pad-to-gate head distance is 0.5 µm whereas the gate head to 2DEG distance (L_{head} in Figure 1-4) is only 0.1 µm. The capacitive coupling is further reduced due to the fact, that the gate head height is 400 nm whereas the metal of the contact pads is only 200 nm thick.

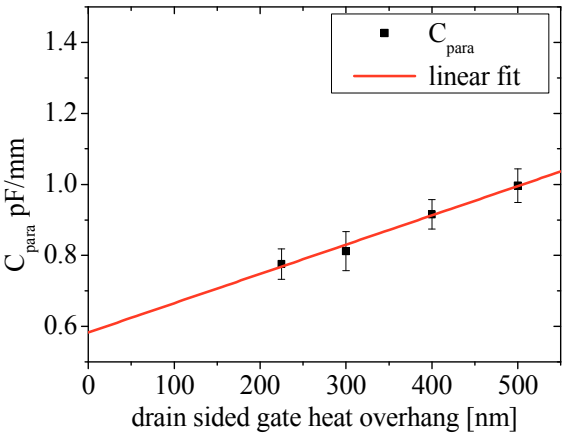

Figure 6-6: Parasitic capacitances over drain-sided gate head overhang (dots) with linear fit of the measured values (line).

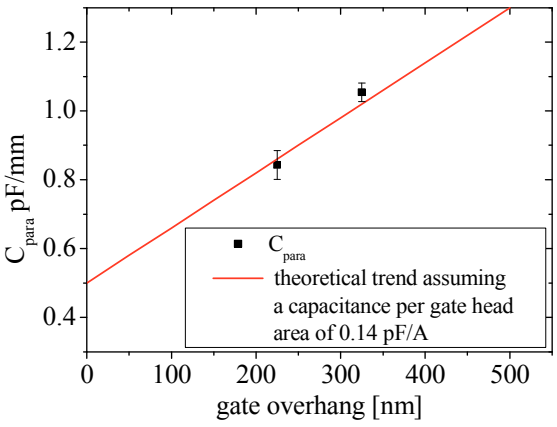

Figure 6-7: Parasitic capacitances of transistors with symmetric two sided gate heads of 225 nm and 325 nm and theoretical prediction (line).

As a consequence, the capacitance of a contact pads to the gate module ($C_{contact}$) is much lower than the measurement deviation and extrapolation error, and cannot be extracted from the available data.

6.5 Capacitances of the gate foot

After all previous parasitic capacitances (C_{ext}, C_{head}) have been subtracted the gate foot capacitance (C_{foot}) and the parasitic capacitance of the gate line (C_{fringe}, C_{side}) will be examined in this section. First, the influence of the gate foot length will be evaluated. In the second part the fringe and the sidewall capacitances will be discussed.

6.5.1 Scaling behavior of the gate capacitance regarding the gate foot

Due to the sequential progress to extract each capacitance, the extrapolation error accumulates. To increase the accuracy of the extrapolated gate foot capacitance, two methods are utilized in this section:

1.) Transistors with different gate length are measured and the capacitance per gate foot area is extrapolated similar to the gate head variation in section 6.4.

2.) The same transistors are measured from off-state to on-state but without drain bias. The difference between these two states is caused by the gate foot capacitance.

For the extrapolation of the gate foot capacitance the transistors A101, MW43, E104, MW51, MW52 and MW53 with gate length from 100 to 500 nm were measured. In Figure 6-8 the gate capacitance is depicted after the gate head and extrinsic capacitance has been subtracted. The gate capacitance shows a clear linear dependency regarding the gate length. In a first approximation, the gate foot can be described as a plate-capacitor and a reduction of the plate area is proportional to a change in capacitance (see equation (2.18)). The linear fit of the gate capacitance results in a gate foot capacitance per gate area of 0.40 pF/A for a HEMT with d_{bar} = 25 nm.

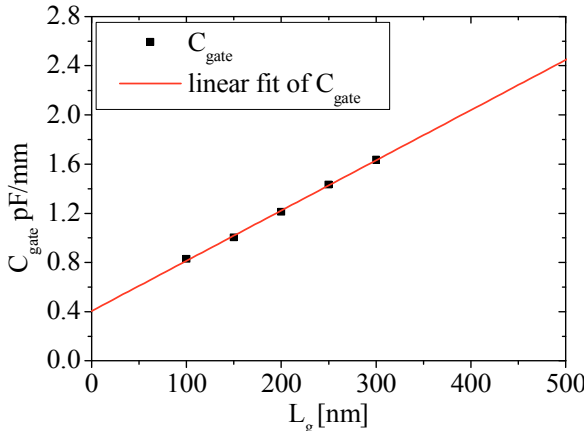

Figure 6-8: Capacitance of the gate module over gate length of 100 nm to 300 nm (dots) with a linear fit of the measured values (line) measured at on-state but only 0 V drain bias to prevent an influence of the drain electric field on the gate electric field.

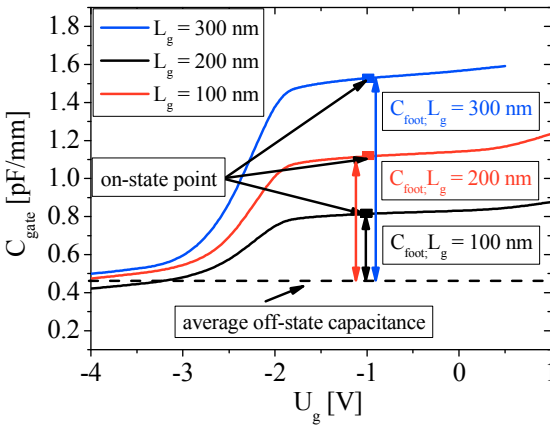

Figure 6-9: Gate capacitance from off to on-state for HEMTs with 100, 200, 300 nm gate length and drain bias of 0 V.

For the second extrapolation method three transistors with gate length of 100, 200 and 300 nm (MW43, MW51, and MW 53) are measured from U_g -4V to 1V without drain bias (see Figure 6-9). The off-state was defined at a gate bias of -4 V and the on-state at -1 V. The differences between those states are caused by the respective gate foot capacitance. For this approach the determined mean value of C_{foot} is 0.36 pF/A, which is in good agreement to the extracted values using a fit over L_g (see Figure 6-7).

6.5.2 Scaling behavior of the gate capacitance regarding the barrier thickness

As was discussed in chapter 2, the gate foot capacitance increases if the barrier thickness is scaled down in order to improve the transconductance. In theory the gate foot capacitance should scale with the same factor as g_{m_int}, but highly scaled gate foot structures may feature parasitic capacitances from non idealities of the gate electric field and capacitive coupling of the gate foot sidewalls to the 2DEG. Both effects will therefore be evaluated in this section.

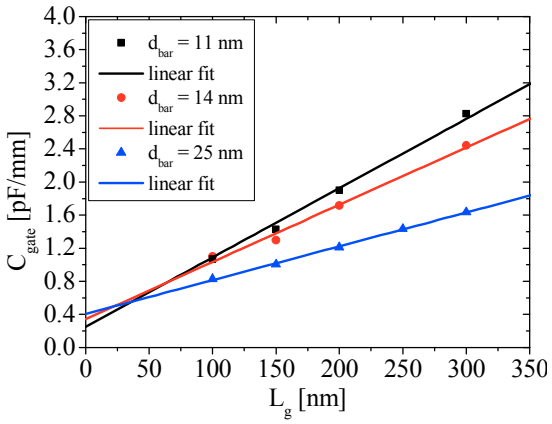

Figure 6-10: Capacitance of the gate module over gate length with a linear fit of the measured values for barrier thicknesses of 11 nm, 14 nm and 25 nm.

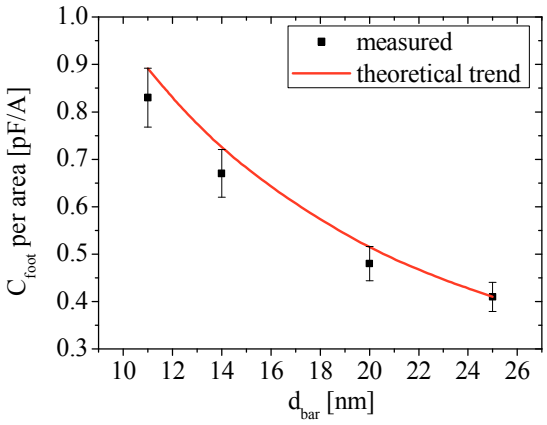

Figure 6-11: Measured and theoretical trend of C_{foot} over d_{bar}. The error bars represent the overall error of the extraction process.

For the studies HEMTs with L_g of 100 nm on wafers with 11, 14, 20 and 25 nm barrier thickness are fabricated and characterized in regard to their gate capacitance. For the extraction of the gate foot capacitance all previous parasitic capacitances were subtracted from the measured data. The resulting capacitances are depicted in Figure 6-10 and Figure 6-11. As can be seen in both diagrams, the gate foot capacitance increases for smaller d_{bar} and follows the theoretical trend given by equation (2.18) but the slope of the measured C_{foot} is smaller compared to the theoretical prediction. Additionally, an offset at L_g = 0 nm remains (see Figure 6-10). The discrepancy cannot be satisfyingly explained by an extraction error alone (see Figure 6-11). The combined mean device fluctuation and extraction error is in the range of 10%, which results in a maximum error below 0.15 pF/mm (see Figure 6-11). There are two remaining possible causes for the parasitic gate foot capacitance:

1.) Fringe capacitances (C_{fringe}) of the gate foot,

2.) Capacitive coupling of the gate foot sidewall with the 2DEG (C_{side}).

The electric field of a short gate is no longer homogeneous. At the edges of the gate foot, stray fields modulate the 2DEG and cause so called fringe capacitances (C_{fringe}). This effect can be described by an extension of the effective gate length.

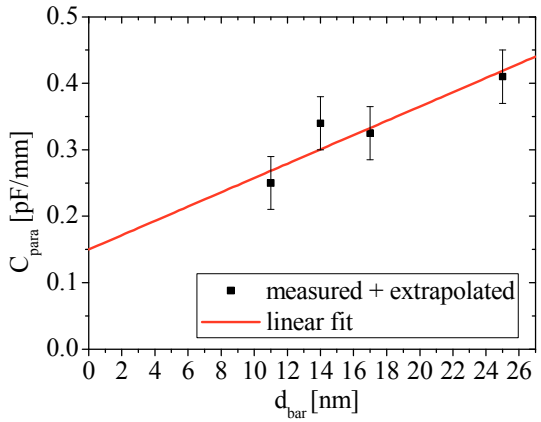

Figure 6-12: Measured C_{foot} without C_{fringe} and theoretical trend over d_{bar}. The error bars represent the overall error of the extraction process.

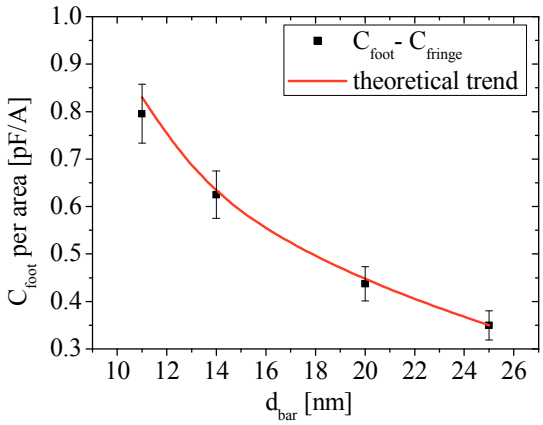

Figure 6-13: Measured C_{foot} without C_{fringe} and theoretical trend over d_{bar}. The error bars represent the overall error of the extraction process.

According to Oxly et al. the gate length increases by twice the barrier thickness [Oxl05]. If the aspect ratio t_{br} can be increased the electric field becomes more and more homogeneous and the fringe capacitances are reduced. HEMTs with smaller barrier thicknesses should therefore exhibit smaller fringe capacitances. As can be seen in Figure 6-10 and Figure 6-12, the measured data verifies the assumption. The offset value of the capacitance decreases for thinner barriers from 0.4 pF/mm to 0.25 pF/mm (see Figure 6-12). As can be seen in the diagram the extraction and measurement error is very high compared to the remaining capacitance. Therefore, precise values for the fringe capacitance can not be given but only a rough estimation.In Table 6-1 the extrapolated C_{fringe} for each measured barrier thickness is summarized. The reduced fringe capacitance for thinner barriers explains the difference between the theoretical trend and the measured gate foot capacitance in Figure 6-11. If C_{fringe} is subtracted from each gate foot capacitance, the scaling of C_{foot} follows the theoretical scaling rules in very good agreement (see Figure 6-13). For the development of mmW-HEMTs this effect is of great importance because the transistors with thin AlGaN barriers exhibit a better scaling behavior regarding a reduction of the gate foot length due to the smaller offset capacitance caused by C_{fringe}. As a consequence, smaller gate capacitances are possible for the same scaling factor which results in higher gains at mmW-frequencies.

After the elimination of the fringe capacitance and taking into account the extraction error, a parasitic off-state value of 0.1-0.2 pF/A remains (see Figure 6-12). That parasitic capacitancecan only be explained by a parasitic coupling of the gate sidewalls (C_{side} in Figure 2-10) with the 2DEG. The sidewalls can be considered as equipotential areas of a capacitor and the 2DEG as the other equipotential layer with the SiN as dielectric. This configuration is similar to the gate head overhang of the T-shaped gate except that both areas are not parallel orientated to each other but orthogonal. The capacitances per area should be approximately in the same range as the gate head capacitance.

This is a rough estimation because the actual field distribution is far more complex, but should be sufficient for a comparison. The capacitance per gate head area and sidewall parasitics are 0.14 pF/A and 0.1-0.2 pF/A, respectively, verifying that both are in the same range. Therefore, the remaining offset in Figure 6-10 is attributed to sidewall capacitances of the gate foot in this work. It cannot by determined if C_{side} is a function of d_{bar} by the available data, because the extraction error of C_{side} becomes more than 50% which is caused by the high number of de-embedded layers of capacitances, the available sample size and the low values of C_{side}.

One method to decrease C_{side} and also C_{head} is to change the dielectric material surrounding the gate module. Therefore, two different passivation technologies are compared in regard to a reduction of the parasitic capacitances in the next section.

Table 6-1: Extrapolated fringe capacitance for the measured barrier thicknesses.

d_{bar}	**11 nm**	**14 nm**	**17 nm**	**25 nm**
C_{fringe}	0.1 pF/mm	0.15 pF/mm	0.2 pF/mm	0.3 pF/mm

6.6 Influence of the passivation on parasitic capacitances

For the study of millimeter wave HEMT characteristics, non passivated devices are a common technique to reach high cut-off frequencies [Hig08]. For such transistors the relative dielectric constant becomes 1 instead 6-8 for SiN. The low dielectric constant reduces the parasitic capacitances of the gate head and the sidewalls at the same factor and subsequently improves the high frequency gain. But to guarantee the reliability of devices and circuits based on GaN-HEMTs the chip and subsequently the transistor must be passivated.

One method to reduce the parasitic capacitances and still passivate the device is to use a low-ε material as isolation layer. For the development of an optimized millimeter wave process, the low-ε material was simulated by depositing a thin SiN layer in such a way that an air gap remains between the gate head and the surface (see Figure 4-9 and Figure 4-10). By using this method the influence of a low-ε material on the parasitic capacitances can be studied without a fundamental change to the passivation process. All devices (H1, MW41, and A234) are measured on wafers with 25 nm barrier thickness and 22% Al-content.

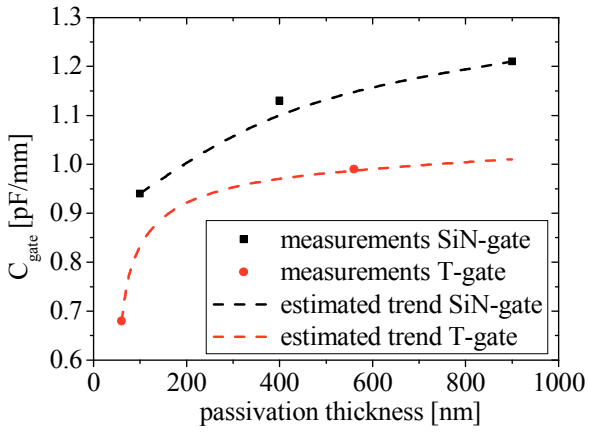

Figure 6-14: Gate capacitance over passivation thickness for a HEMT with 25 nm d_{bar}, measured at an on-state point with 10 V drain bias.

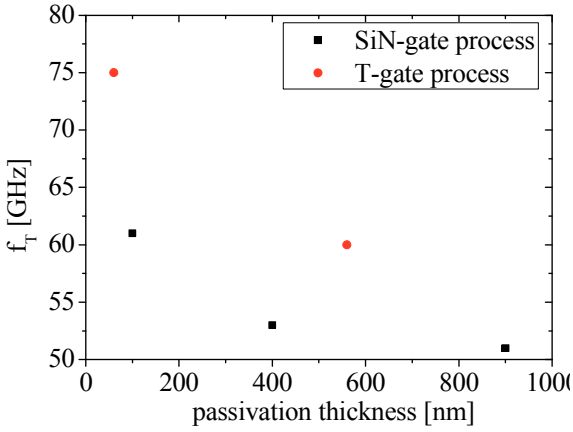

Figure 6-15: Current-gain cut-off frequency over passivation thickness, measured at $g_{m,max}$ and 7 V drain bias.

In Figure 6-14 the gate capacitances of transistors with passivation thicknesses from 60 nm to 900 nm are depicted. Like in the previous sections, the extrinsic capacitances are subtracted from C_{gate}. The gate head overhang of the T-gate module is scaled down further compared to the SiN-gate modules (see Table 6-2). This difference causes an additional decrease in the parasitic capacitances compared to the SiN gate technology but for a study of the overall trend the data is sufficient. As can be seen in Figure 6-14, at a passivation thickness of 60 nm C_{gate} is severely decreased. In this case the air-gap between the gate head and wafer surface decreases the dielectric constant around the gate head in the same way as a low-ε material. Once the gap between gate head and the wafer surface is filled (greater 100 nm passivation thickness) the capacitance rises to a nearly constant value. A further increase of the passivation layer has a much weaker influence on the parasitic capacitance. The effect on the current-gain cut-off frequency can be seen in Figure 6-15. As expected, the frequency drops significantly for full passivated devices. This decrease is even more pronounced for wafers with higher transconductances, because the relative change is greater. Following the extrapolated results, a technology with a low-ε dielectric between gate head and surface of the semiconductor is necessary to achieve high operation frequencies.

Table 6-2: Comparison of relevant SiN-Gate and T-Gate geometries regarding parasitic capacitances.

	Gate head overhang (symmetric)	**Gate head to surface distance**
SiN-gate	250 nm	100 nm
T-gate	160 nm	125 nm

6.7 Influence of an additional field-plate on the capacitance

Additional field plates, also called shields, are utilized in HEMTs to reduce peaks of the electric field at the drain side of the gate. The additional field-plate is a metal layer connected to the source contact of the transistor and extends a defined length across the gate module towards the drain. A schematic cross-section of such a transistor is shown in Figure 5-19. The active part of the shield is the additional field plate in the drain region, which is mostly defined by the length of the field plate and the distance from the semiconductor surface. In this work the length of the field plate and shield-to-surface spacing for all measured HEMTs is 1 µm and 400 nm, respectively.

In Figure 6-16 simulations of the electric field distribution along a HEMT for a device with and without shield are shown. The dimensions of the simulated transistors are based on measured HEMTs (MW33 and MW11) to maximize the accuracy of the results. The reduced field peaks at the drain side and more homogeneous field distribution with a field-plate improves the breakdown characteristics, power added efficiency (PAE) and reduces the drain-sided gate capacitance (C_{gd}) [Kue09], [Kue10].

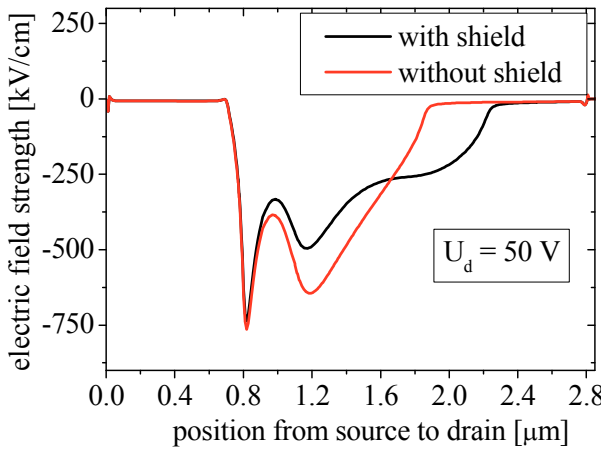

Figure 6-16: Simulations of the electric field distributions from source to drain for a HEMT with and without shield at an on-state bias point of U_g = -1 V and U_d = 50 V.

In this chapter the influence of such a shield structure on the capacitance of scaled gate modules will be evaluated. Transistors with drain-sided gate head overhangs of 300, 400 and 500 nm were fabricated with an 1 µm field-plate, and compared to devices without shield (MW33, MW35, MW11, MW13, MW15). All transistors were measured on wafers with 25 nm barrier thickness and 22% Al-content.As can be seen in Figure 6-17 the additional field plate has a negative effect on the overall gate capacitance. The difference between C_{gate} increases with larger gate head size indicating that the capacitive coupling of the gate head with the shield metal is the primary cause of this behavior. To further localize the origin of the parasitic shield capacitance and determine the effect on the parasitic capacitances of the transistor, the gate-source and gate-drain capacitances are depicted in Figure 6-18 and Figure 6-19 respectively. With an additional field plate C_{gs} increases whereas C_{gd} decreases. This behavior can only be explained by a capacitive coupling of the gate head metal and the shield structure. As expected from chapter 6.2 the drain gate capacitance rises with larger drain-sided gate head overhangs (see Figure 6-19). But due to the reduction of the electric field peak in the drain region, the gate-drain capacitance decreases with an additional shield structure by a constant value of 0.1 pF/mm for all gate head

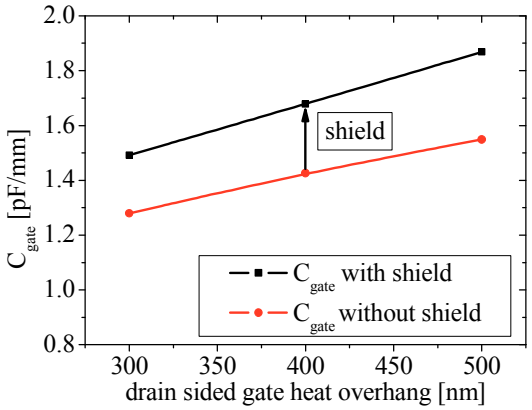

Figure 6-17: Comparison of HEMTs with source terminated shield-plate to transistors without field plates for devices with increasing gate head diameters. All HEMTs are measured at on-state and 10 V drain bias.

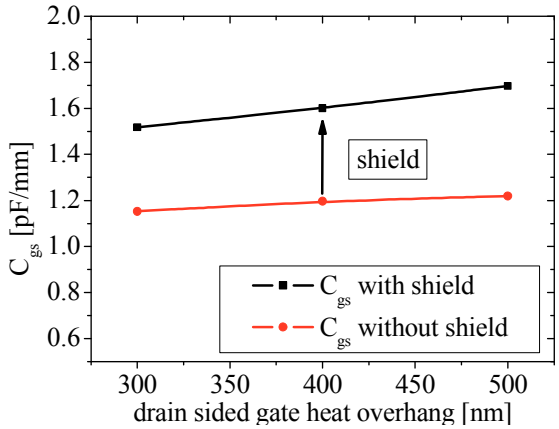

Figure 6-18: Comparison of source-gate capacitances of transistors with shield (black dots) and transistors without shield (red stars), measured at on-state and 10 V drain bias.

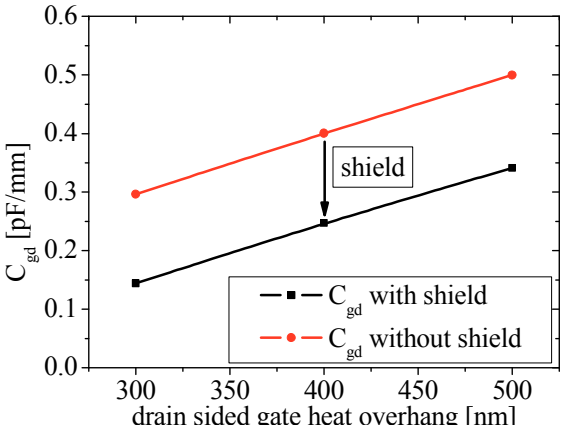

Figure 6-19: Comparison of drain-gate capacitances of transistors with shield (black dots) and transistors without shield (red stars), measured at on-state and 10 V drain bias.

overhangs. This effect can be used to minimize the feedback capacitance of amplifiers based on such HEMTs but the overall high frequency characteristic will decrease because of the higher total capacitance. To minimize this effect an overlap of the shield metal with the gate head must be avoided in the design process of such HEMTs. One method is to decrease the gate head overhang but following Figure 6-18, the gate head has to be scaled down to dimensions at which the gate line resistance would be disproportionately high. Another solution is to change the design of the shield. If the active part of the shield structure can be connected to the source-pad outside the source and gate head region the capacitive coupling can be decreased. But due to the fact that there will be always a small overlap at the drain region to suppress peaks of the electrical field at the gate head, the increase of C_{gs} cannot be completely avoided. Therefore, a HEMT design with an additional shield structure will always be a trade-off between high $f_{T,}$ f_{max} and low $C_{gd.}$

6.8 Conclusion

The goal of this chapter was to evaluate all physical capacitances of an AlGaN/GaN based HEMT and to determine the scaling behavior for each component. In Table 6-3 the gate foot and parasitic capacitance of the developed technologies are summarized and compared to the technology available at the start of this work. With the scaling of d_{bar} in order to improve g_{m_int}, the gate length must be reduced to 100 nm to keep C_{foot} constant for the scaled HEMT technology. As can be seen in Table 6-3 the actual C_{foot} for the mmW-technologies is even smaller than 1.0 pF/mm of the reference technology. The difference is mainly caused by the over scaling of L_g compared to d_{bar}. While the gate length was reduced by a factor of 2.5 the barrier thickness could only be scaled by a factor of 2.27 in this study.

According to the scaling rules also the parasitic capacitances must be decreased below 0.35 pF/mm for a successful scaling of the HEMT. The reduction of C_{para} from 0.8 to 0.5 pF/mm was achieved by a scaling of the gate head and by the reduced C_{fringe} for smaller barrier thicknesses. However a reduction according to the scaling rules could not be achieved for SiN passivated gate modules due to the fact that the gate head overhangs cannot be reduced further without a severe increase of the gate line resistance and subsequently a dramatically decrease of the maximum available power-gain. But with the use of a quasi low-ε material for the passivation layer, it is possible to achieve a C_{para} below the necessary value of 0.35 pF/mm.

Table 6-3: Comparison of the active and parasitic capacitances of the available technology at the start of this work and the developed mmW-technology.

	available technology at the start of this work : SiN-gate (L_g = 250 nm and d_{bar} = 25 nm)	**mmW-technology with SiN passivation: T-gate (L_g = 100 nm and d_{bar} = 11 nm)**	**mmW-technology with quasi low-ε passivation: T-gate (L_g = 100 nm and d_{bar} = 11 nm)**
active capacitance (C_{foot})	1.0 pF/mm	0.9 pF/mm	0.9 pF/mm
parasitic capacitance (C_{para})	0.8 pF/mm	0.5 pF/mm	0.3 pF/mm
parasitic capacitance (C_{para}) with 1,0 µm shield	1.05 pF/mm	0.75 pF/mm	-

With the combined over-scaling of C_{foot} and C_{para} the diminished scaling of g_{m_ext} evaluated in chapter 5 can be compensated. HEMTs fabricated with this technology achieve a cut-off frequency of 2.5 times f_T compared to transistors available at the start of this work (see Figure 6-20). For the development of power amplifiers the power gain is the more important characteristic. In Figure 6-21 the small signal power gain for the same transistors as in Figure 6-18 is depicted. As can be seen the power gains for the quasi low-ε technology increases by 4.5 dB. However the gain for the SiN passivated device is much smaller. This indicates that the parasitic capacitances of our HEMT layout have a significant influence on the power gain.

Also the maximum frequency of oscillation scales not by the desired factor (see Figure 6-21). The smaller gain can be explained by a high gate line resistance of our transistors but further studies are necessary to prove this hypothesis. Another factor is the challenging task to extrapolate f_{max}. If f_{max} is extrapolated using the theoretical slope of -20dB per decade starting from the k-point (see chapter 2), the measured HEMTs would feature f_{max} values as high as 230 GHz which would fulfill exactly the scaling rule. But this extrapolation method would clearly contradict the measured slope shown in Figure 6-21.

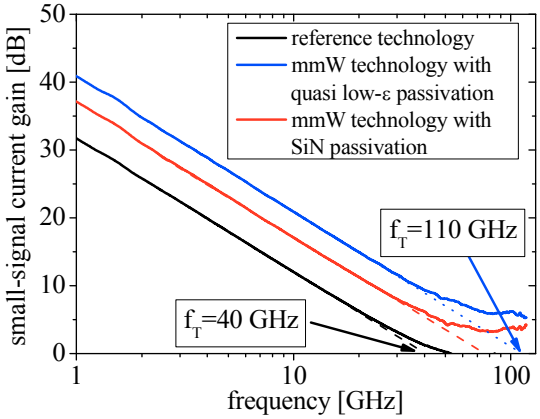

Figure 6-20: Small-signal current-gain over frequency of HEMTs fabricated with the reference technology and the developed mmW-technologies.

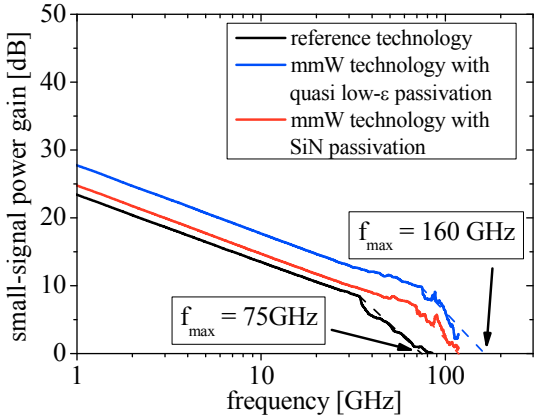

Figure 6-21: Small-signal power-gain over frequency of HEMTs fabricated with the reference technology and the developed mmW-technologies.

But the available network analyzer can measure only up to 120 GHz. At this frequency range the very small but unavoidable calibration errors have a significant influence on the measured data and the diminished slope can therefore also be caused by a measurement error.

Besides the scaling of the transistor geometries also the influence of an additional field plate on the capacitances was evaluated in this chapter. The implementation of a source terminated field plate causes a reduction of the gate-drain capacitance of 0.15 pF/mm at a drain voltage of 10 V. But this decrease is counteracted by the increase of the source-gate capacitance of 0.4 pF/mm. As a result C_{para} increases by a constant offset of 0.25 pF/mm if a shield is used. To prevent this effect the design of the shield has to be changed to a layout with a strongly decreased overlap between the gate module and the shield metal.

As discussed in chapter 5 HEMTs with a short gate length exhibit a non-saturation of the electron velocity due to a short channel effect. In the next chapter the scaled HEMTs are studied in more detail to determine further short channel effects and their influence on the device performance.

7. Short-channel effects of scaled AlGaN/GaN HEMTs

The occurrence of short channel effects can have severe negative impact on the transistor characteristics [Bre01]. The non-saturation of the electron velocity for HEMTs with L_g below 250 nm and the effect on g_{m_ext} was discussed in chapter 5. In chapter 6 the fringe capacitances caused by stray fields of the gate and their influence on C_{para} of highly scaled HEMTs were evaluated. Beside these effects the drain induced barrier lowering (DIBL) caused by the superposition of the vertical electric field from the gate and the lateral electric field (see chapter 2) can no longer be ignored for small gate lengths. From theoretical considerations the DIBL-effect can have the following consequences on the transistor characteristics:

1.) A threshold voltage shift toward more negative values;

2.) An increase of the drain leakage current and severely decreased breakdown voltage in off-state operation;

3.) A higher output conductance in on-state operation.

All of these effects are greatly influenced by the material system and to some extend also by epitaxy and process technology. A detailed analysis is therefore necessary to verify short-channel effects on AlGaN/GaN HEMTs. Because the DIBL-effect is mainly a function of the aspect ratio of the gate length to barrier thickness (t_{br}), HEMTs with various combinations of L_g and d_{bar} were studied.
Besides the DIBL-effect HEMTs with short gates can exhibit additional short channel effects such as tunneling currents in off-state because the potential barrier of the gate becomes to short [Num91]. Therefore HEMTs are also studied in this chapter in order to evaluate the existence of such short channel effects.

7.1 Influence of the DIBL-effect on the threshold voltage and sub-threshold region

In the gradual channel approximation the potential well of the gate region is considered uniform at the drain side of the gate foot and independent of the drain electric field. For very small gate lengths these approximations are no longer valid. The gate potential for such HEMTs is reduced due to a superposition with the drain electric field. A direct observable effect is that a more negative gate voltage is needed to reach off-state operation which can be measured as a negative voltage shift of the threshold voltage. As can be seen in Figure 7-1, for smaller L_g, U_{th} shifts considerably towards more negative values. This trend is mainly caused by the smaller aspect ratio for shorter gate length provided that d_{bar} is constant. To study the influence of t_{br} on the voltage shift, HEMTs with d_{bar} of 17, 14 und 11 nm and L_g of 300, 250, 200, 150 and 100 nm were measured. The results are depicted in Figure 7-2. As can be seen in the diagram the threshold voltage shift increases for t_{br} lower than 14 and that the same trend can be observed for each d_{bar}. This behavior indicates that the DIBL effect for our AlGaN/GaN HEMT technology is mainly a function of t_{br} and not only the gate length.

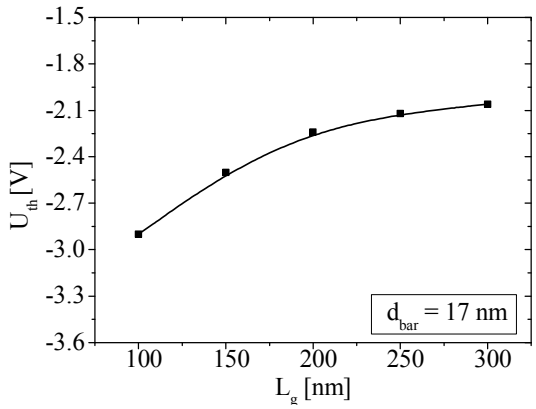

Figure 7-1: Threshold voltage versus gate length for HEMTs with d_{bar} = 17 nm.

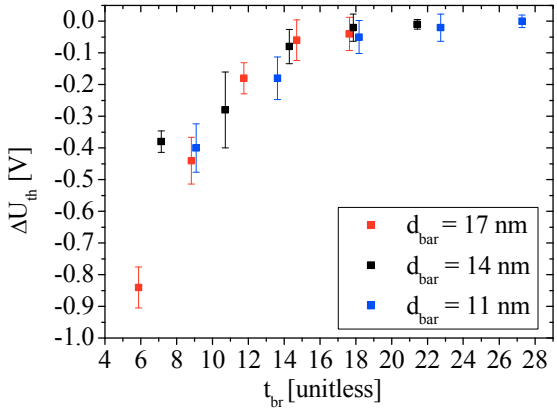

Figure 7-2: Threshold voltage shift over aspect ratio of gate length to barrier thickness for HEMTs with d_{bar} of 17, 14 and 11 nm. As the reference point for the calculations the U_{th} value at t_{br} = 28 was used.

Following the available data a critical aspect ratio of approximately 14 is necessary to surpress the DIBL effect. This result has a severe impact on the design of mmW-transistors. Up to now the hypothesis was used that the aspect ratio of 10 based on the available technology at the start of this work is also sufficient for scaled AlGaN/GaN HEMTs. This assumption is clearly not correct considering the data given in Figure 7-2. But if a t_{br} of 14 must be achieved for mmW-HEMTs, much thinner barrier thicknesses for a given gate length are needed. For a HEMT with L_g = 100 nm the barrier thickness has to be reduced from 10 to 7 nm to achieve the critical aspect ratio.

Even with perfect device scaling, the lateral size of the gate barrier becomes smaller for shorter gate length and electrons can tunnel through the short potential barrier. Therefore, either a higher gate voltage is needed to reach the minimum drain current (I_{dmin}) or if L_g becomes to short the electric field of the gate can no longer generate a sufficient potential barrier. As a consequence the HEMT will always exhibit a high I_{dmin} due to a tunneling current. To evaluate such an effect I_{dmin} and the corresponding gate voltage is measured for HEMT with L_g of 100, 150, 200, 250 and 300 nm on wafers with d_{bar} of 25, 17, 14 and 11 nm. The minimum drain current for all devices is shown in Figure 7-3.

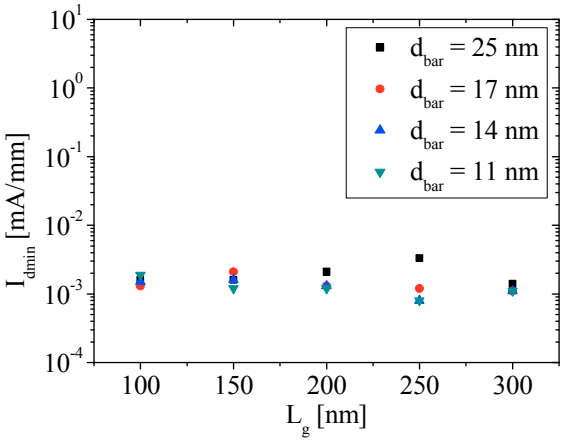

Figure 7-3: Minimal drain current versus gate length measured on wafer with different barrier thicknesses and at U_d = 7 V.

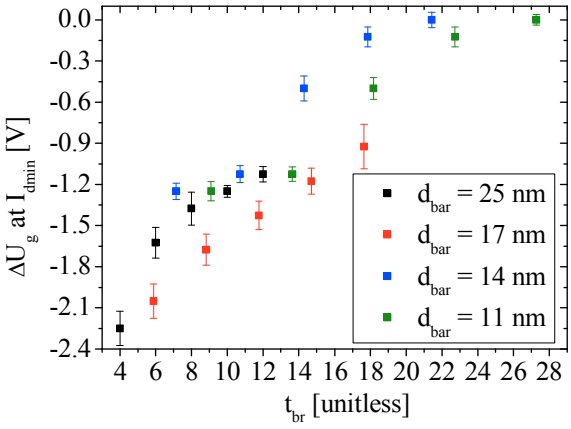

Figure 7-4: Difference of the required gate source voltage to reach minimal drain current of 1.6 µA/mm versus the aspect ratio of gate length to barrier thickness. As reference point for the calculation the value for t_{br} = 28 was used. All HEMTs are measured at U_d = 7 V.

All HEMTs exhibits nearly the same values and an increase of I_{dmin} towards smaller gate lengths cannot be observed. This verifies that the potential barrier for L_g of 100 nm can still be large enough to completely pinch-off the electron channel. But an increased gate voltage is needed to reach this operating point depending on t_{br} (see Figure 7-4). As a consequence devices with a small aspect ratio exhibit a higher subthreshold leakage current which will decrease the efficiency of the transistor. Similar to Figure 7-2 the critical aspect ration is in the range of 14 to 16 for the measured HEMTs.

7.2 Influence of the DIBL-effect on the on-state characteristics of AlGaN/GaN HEMTs

In on-state operation the influence of the drain electric field on the field of the gate can cause many severe parasitic effects such as an increase of the output transconductance of the transistor (see chapter 2). Therefore the influence of the DIBL-effects on the on-state characteristic of the mmW-HEMTs will be studied in this section with regard to the gate length and aspect ratio. As can be seen in Figure 7-5 HEMTs with 100 nm gate length and a barrier thickness of 25 nm (t_{br} = 4) show a severe degradation of the output characteristic. For high drain voltages the transistor exhibits a poor pinch-off characteristics which can be explained by the increased influence of the drain field on the gate potential and the short effective potential barrier due to the poor aspect ratio. Because of the decreased modulation efficiency of the gate electric field on the channel, HEMTs also feature a high output conductance.

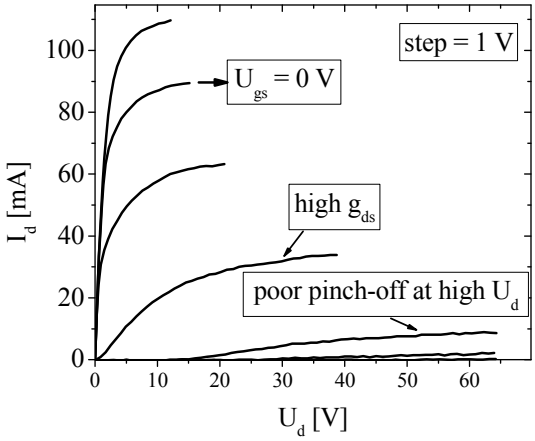

Figure 7-5: Output characteristic of a HEMT with L_g = 100 nm and d_{bar} = 25 nm. U_g is increased in steps of 1 V from -5 to 1 V.

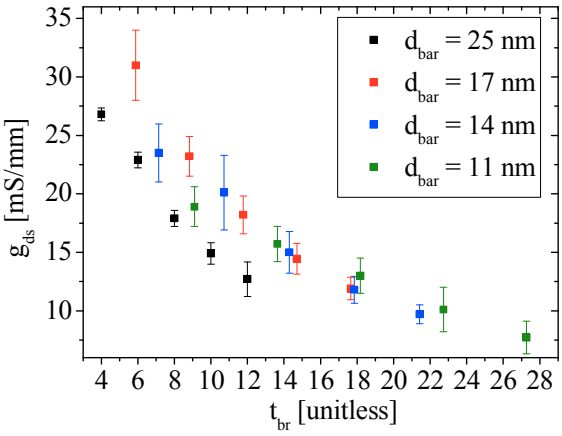

Figure 7-6: Output conductance over t_{br} for wafers with 25, 17, 14 and 11 nm barrier thicknesses.

As discussed in chapter 2 both effects can strongly limit the gain and output power of the transistor. For a successful development of a mmW-technology it is therefore important to prevent these effects. Following the studies in the previous section, determining the critical aspect ratio at which AlGaN/GaN-HEMTs no longer exhibit such short channel effects is of great importance for the design of a highly scaled HEMT technology. As a figure of merit for the on-state short channel effects the output transconductance was studied in more detail. HEMTs with different t_{br} are measured with regard to their output conductance (g_{ds}). The output conductance is extrapolated using the small-signal equivalent circuit and S-parameter measurements at $g_{m,max}$ and 7 V drain bias.

The results of these measurements are shown in Figure 7-6. The trend of g_{ds} over t_{br} is nearly the same as observed in the previous section. Transistors with an aspect ratio below an t_{br} of 14 to 16 exhibit a severe degradation of the output conductance which further verifies the importance of the aspect ratio for AlGaN/GaN HEMTs.

7.3 Influence of the DIBL-effect on the breakdown characteristic of AlGaN/GaN HEMTs

To study the influence of device geometries especially t_{br} on the breakdown behavior, HEMTs with gate length of 100, 150 and 250 nm (A101, E101, MW45 respectively) were characterized on wafers with 25, 17, 14 and 11 nm barrier thickness. The most common breakdown mechanism for AlGaN/GaN HEMTs is the avalanche breakdown described in chapter 2. If the electric field along the channel exceeds a critical threshold, additional free electrons are generated due to impact ionization, and the drain current increases exponentially. As a consequence the thermal losses of the transistor rise rapidly and the transistor is destroyed in most cases. In Figure 7-7 the avalanche breakdown characteristic for a HEMT with L_g = 250 nm and d_{bar} = 25 nm is depicted. The device has a breakdown voltage (U_{br}) of 120 V and the sudden increase of the drain current for U_d greater 120 V is clearly visible. But for the scaled mmW-HEMTs another breakdown characteristic becomes more dominant. The drain current versus drain voltage for a short channel HEMT is shown in Figure 7-8. As can be seen in the diagram, for the short channel HEMT with L_g = 100 nm but otherwise the same geometries as the device measured in Figure 7-7 a strong increase of the drain current occurs at much lower drain voltages as for the transistor with an avalanche breakdown characteristic. Furthermore, the increase of I_d is much slower and is completely reversible. As described in the section before, the DIBL-effect causes a poor pinch-off behavior. The breakdown characteristic of the scaled HEMTs is a direct progression of this characteristic. For high U_d the electric field from the drain reduces the potential barrier further and the drain current is no longer controlled by the gate voltage. Because there is no definitive value for U_{br} for this punch through effect the breakdown voltage is defined in this work as the drain voltage where I_d = 0.3 mA/mm for a gate bias of –7 V. According to the previous studies the short channel effects of the studied HEMTs are mostly dominated by the aspect ratio t_{br}.

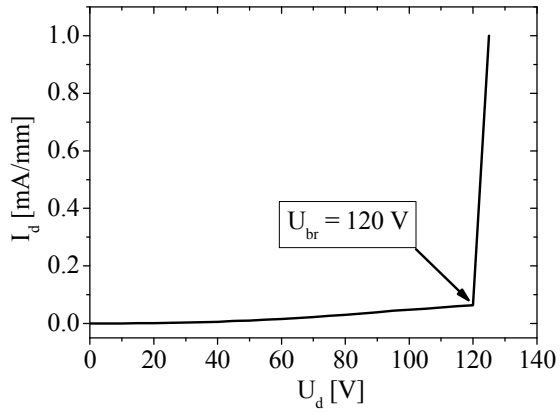

Figure 7-7: Avalanche breakdown of a HEMT with L_g = 250 nm.

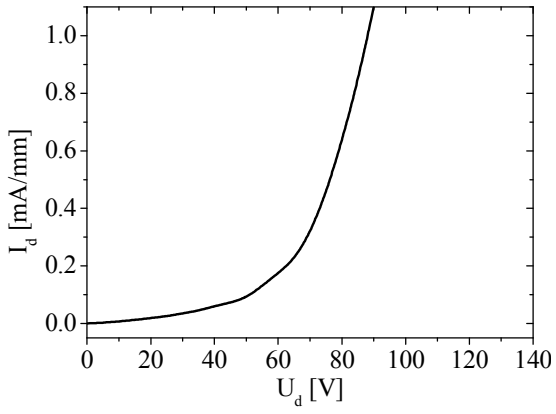

Figure 7-8: Breakdown characteristic of a HEMT dominated by the DIBL-effect.

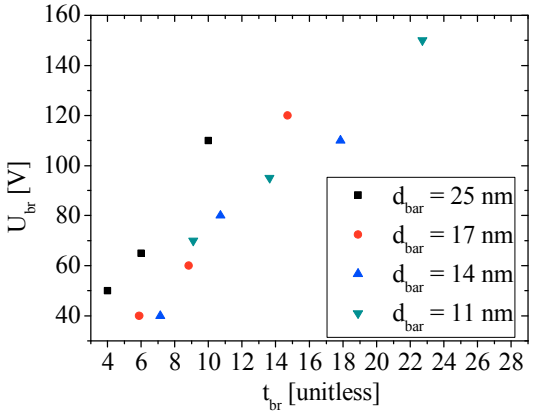

Figure 7-9: Breakdown voltage over aspect ration of gate length to barrier thickness for wafers with d_{bar} of 11 14, 17 and 25 nm. All HEMTs were measured at -7 V U_g and a substrate temperature of 150°C.

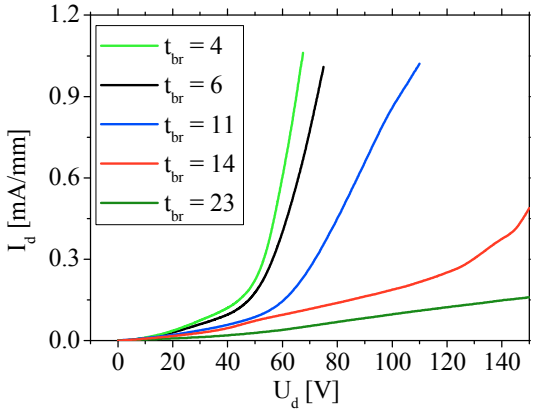

Figure 7-10: Breakdown characteristic for HEMTs with t_{br} from 4 to 23. All HEMTs were measured at -7 V U_g and a substrate temperature of 150°C.

Therefore the breakdown voltage of HEMTs with gate length from 100 to 250 nm and barrier thicknesses from 11 to 25 nm was measured. All HEMTs were measured at 150°C substrate temperature to simulate operation conditions for power amplifier circuits. As can be seen in Figure 7-9 U_{br} over t_{br} follows a linear slope. Given the critical t_{br} of 14 determined previously, the developed HEMTs achieve breakdown voltages of 90 V. This result proves that even highly scaled AlGaN-HEMTs can feature very high U_{br} values. In Figure 7-10 the drain current over drain voltage for different t_{br} is shown. With higher t_{br} the breakdown characteristic changes from a DIBL breakdown to an avalanche breakdown behavior whereas the transistor with an aspect ratio of 14 marks the

transition between both regions. For the design of HEMTs the dominant breakdown behavior is of great importance.

In Table 7-1 an overview of HEMTs with both breakdown characteristics and drain-gate spacing of 0.7 and 2.0 µm are given. In case of an avalanche breakdown characteristic, U_{br} is mostly defined by the drain-gate spacing. As was show in the field simulations in chapter 5 (see Figure 5-21 and Figure 5-22) the electric field at the gate edge does not increase for higher U_d but the electric field extents towards the drain contact. As soon as the space charge region reaches the drain contact only small changes of the drain voltage causes a high increase of the electric field at the gate and the critical field strength for an avalanche breakdown will be exceeded. Therefore the gate-drain spacing is of great importance for the design of HEMTs which are dominated by an avalanche breakdown characteristic. But with larger spacings also the on resistance of the transistor increases. The drain-gate spacing must therefore be designed in such a way that both parameters are optimized at the same time. But if the transistor exhibits a severe DIBL-effect the breakdown voltage is decreased from at least 100 V to 40 V, and the drain-gate spacing has almost no effect on U_{br} (see Table 7-1). In this case the spacing of the HEMT can be reduced to minimum values to achieve a low $R_{on.}$ However the reduction of R_{on} has a far less impact on the large signal output power than the severe decrease of U_{br} (see chapter 2). The reduction of R_{on} is further mitigated by the fact that the scaling of the source-drain spacing has only a diminishing influence on R_{on} due to the relatively high contact resistances compared to the sheet resistance (see chapter 5). Therefore, it is necessary to prevent the DIBL breakdown as far as possible. In the next section the studies regarding the critical aspect ratio to prevent short channel effects caused by the drain induced barrier lowering is summarized, and an outlook is given how further developments of the barrier and buffer layer can prevent these short channel effects.

Table 7-1: Comparison of HEMTs with DIBL dominated breakdown behavior and avalanche dominated breakdown characteristics regarding an influence of the gate drain spacing on the breakdown voltage.

Breakdown characteristic and device description	t_{br} [unitless]	Spacing [µm]	U_{br} at I_d = 0.3 µA/mm [V]
Avalanche breakdown (L_g = 250 nm, d_{bar} = 11 nm, A101)	23	0.7	50
		2.0	> 150
Transition between avalanche and DIBL breakdown (L_g = 150 nm, d_{bar} = 11 nm, A101)	14	0.7	40
		2.0	100
DIBL breakdown (L_g = 100 nm, d_{bar} = 14 nm, MW45)	7	0.7	30
		2.0	40

7.4 Conclusion

It was proven in this chapter, that for HEMTs with gate length down to 100 nm the short channel effects are solely caused by the drain induced barrier lowering which is mainly a function of the aspect ratio of gate length to barrier thickness. It was further shown, that if AlGaN/GaN HEMTs are dominated by the DIBL-effect nearly all device characteristics of the transistors degenerate. The critical aspect ratio to prevent the DIBL-effect is therefore of great importance for the design of mmW-HEMTs. At the start of this work only few studies regarding the critical aspect ratio for AlGaN/GaN HEMTs were available. Therefore, a detailed evaluation of the critical aspect ratio was conducted in this chapter. Thereby, figures of merit for the on-state, off-state and subthreshold region were determined and subsequently studied in regard to a deterioration of the device characteristics as a function of t_{br}. In all studies a critical aspect ratio in the range of 14-16 was determined which is further verified by the studies of Jessen et. al. who evaluated a minimum t_{br} of 15 [Jes07]. This value is very high compared to other compound semiconductor materials. For AlGaAs based HEMTs aspect ratios from 2.5 up to 6 are reported to be suffi-

cient to suppress short-channel effects [Das85], [Kuz90], [Num91]. To achieve the evaluated minimum aspect ratios of 14 for AlGaN/GaN HEMTs with L_g = 100 nm a barrier thickness of 7 nm is necessary. As discussed in chapter 3 and 4 the epitaxy or recess etching of the barrier to achieve such a small thickness is very challenging. Given the fact that all wafers must be capped with a 3 nm thick GaN layer to passivate the surface, only a 4 nm AlGaN barrier remains. According to the theory described in chapter 3, the Al-content of such a thin layer must exceed 50 % to compensate the small barrier thickness. Such barriers would be highly susceptible to process fluctuations due to the small d_{bar}, high Al-content and subsequently increased incorporation of oxygen impurities. Also a recess process to etch the barrier under the gate foot is not possible without severely damaging the remaining barrier which strongly increases the leakage current of the transistor (see chapter 5). Furthermore no processes are available for AlGaN/GaN-HEMTs which can recover the damaged areas due to annealing because the necessary temperature would destroy all previous process steps. Also the damaged areas can not be removed by a wet etching technique because no such process exist due to the high chemical stability of GaN.
Several novel barrier designs to minimize short-channel effects, especially the reduction of U_{br}, are possible. A rather easy method to achieve thin barriers and high sheet carrier concentrations is the use of AlN as barrier layer [Hig08]. But due to the higher band gap compared to AlGaN the fabrication of ohmic contacts is very challenging, and only contact resistances which are severely higher than the values for AlGaN/GaN HEMTs were reported. The same is true for quaternary compound semi-conductors based on AlGaN and Indium which would otherwise be a very good material system for mmW-HEMTs. First studies of AlInGaN barriers showed very promising results [Lim10] but further improvements of the fabrication process are necessary. Besides a change of the barrier material also the buffer can be modified to suppress short channel effects. Uren et al showed that a doping of the buffer layer with iron can counteract short channel effects [Ure06a]. Furthermore double heterostructures are

studied regarding a reduction of the DIBL-effect and a higher modulation efficiency of the gate [Bah09]. An AlGaN layer inside the buffer functions as a back barrier for the electrons and the gate potential. As a consequence the modulation efficiency of the gate is increased and the influence of the drain electric field on the gate electric field is strongly reduced.

Further studies have to be conducted to evaluate a reduction of the DIBL-effect on our mmW-technology due to additional changes of the barrier or buffer design. With the available epitaxy technology and general barrier design in the course of this work only a t_{br} of 9 can be achieved for HEMTs with L_g = 100 nm. As a consequence the U_{br} auf these devices is far less compared to a transistor with greater gate length. Therefore a design of mmW-HEMTs with this technology demands a trade-off between either high frequency operation or high output power. For a first generation of high frequency power amplifiers the HEMTs were designed towards a maximum gain at frequencies above 50 GHz, and the goal of further development iterations will be to maximize the output power. In the next chapter large signal measurements of the first generation circuits are presented to demonstrate the functionality of the developed mmW-technology on chip level.

8. 60 GHz and 94 GHz amplifiers based on the developed mmW-HEMT technology

The goal of this work was to study concepts for a successful scaling of the available transistor technology to achieve amplifier operations above 50 GHz. From the studies done in this work, HEMTs with thin grown barriers and the T-gate module demonstrated the best high frequency characteristics and lowest deterioration of other device parameters at the same time. With this mmW-technology it is possible to increase f_T to 110 GHz as well as f_{max} to 160 GHz (see Figure 6-20 and Figure 6-21). Parallel to the development of the basic transistor cell new design concepts for mmW-amplifiers were also evaluated. The detailed study of these circuits was not a subject of this work and was mainly done by D. Schwantuscke and A. Tessmann. Therefore, the overall design of these amplifiers will only be briefly discussed in the next sections. A more detailed description of the design process can be found in [Sch10]. The main focus of this chapter is the demonstration of high power amplifier operation at 60 GHz and 94 GHz and the production yield of the mmW-process.

Due to design restriction of the available fabrication process for integrated circuits the chips and subsequently all transistors are always completely passivated with SiN. As a consequence the current and power-gain of these HEMTs are reduced in comparison to the optimum mmW-technology evaluated in this work (see Figure 6-20 and Figure 6-21). Therefore, integrated cascode amplifier were designed to compensate this loss and to evaluate advanced design concepts for mmW-amplifiers (see Figure 8-1 and Figure 8-2).

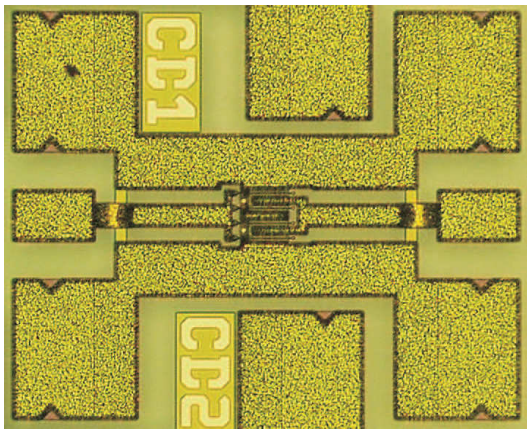

Figure 8-1: HEMT test device based on the developed mmW-technology as common source circuit (common source HEMT).

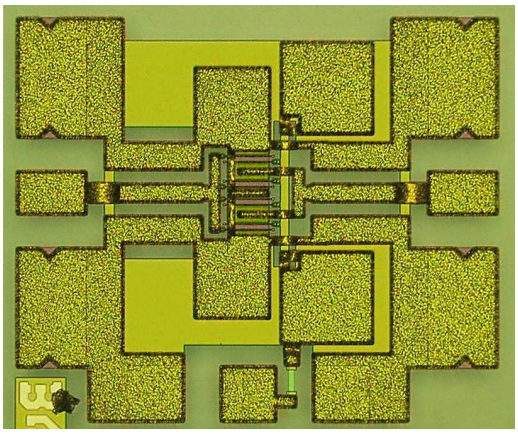

Figure 8-2: Cascode amplifier based on the developed mmW-HEMT technology.

For the cascode HEMT design concept two transistor stages are combined into one basic transistor cell which is depicted in Figure 8-2. Thereby one stage is composed as a common-source circuit and one as common-gate circuit. Because this basic cell resembles a transistor with two gates, it is commonly referred to as a dual-gate HEMT. The main advantages of these cascode HEMTs are the improved broadband characteristics and higher gain compared to the single HEMT of the same size. A more detailed description of the device physics and characteristics of the dual-gate HEMTs can be found in [Sch10].

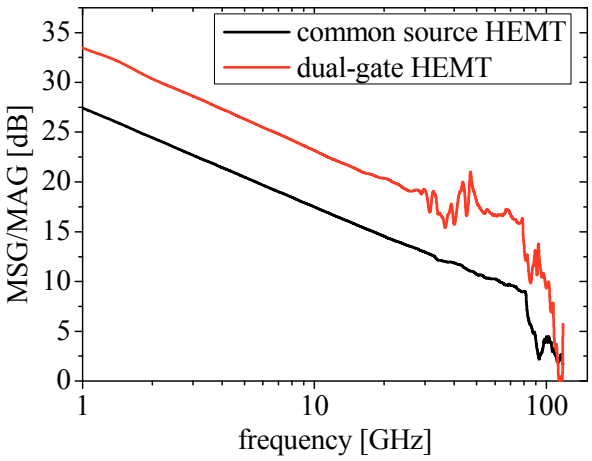

Figure 8-3: Measurement of the small-signal power-gain over frequency for a common source and dual-gate HEMT with the same gate-width.

In Figure 8-3 the small-signal power gain characteristics (MSG/MAG) up to 120 GHz for a single and dual gate HEMT fabricated with the developed mmW-technology are depicted. The non-steady behavior of the dual-gate HEMT above 30 GHz is caused by the very small $|\underline{S}_{12}|$ values which are in the range of the measurement limit of the available network analyzer (Agilent 8150-XF). As can be seen in the diagram the power-gain of the dual-gate HEMT is at least 5 dBm higher than the common source HEMT which verifies the improved high frequency characteristics of the dual-gate concept.

In the next section amplifiers are shown which are based on the common source or dual-gate basic transistor cells.

8.1 Small and large-signal measurements of 60 GHz amplifiers

In this section a single-stage common source amplifier operating at 60 GHz is discussed in more detail. In Figure 8-4 the chip image of the measured amplifier is depicted. Due to a variation of the gate width and number of fingers the optimal configuration of 4x45 µm was evaluated [Sch10]. Therefore all studied amplifiers are based on this geometry and gate width. Furthermore a matching network was developed to achieve a good input and output matching at 60 GHz [Sch10]. The measured small-signal gain ($|\underline{S}_{21}|$) for the common source amplifier is 7.4 dB (see Figure 8-5) which is 2.5 dB lower than the measured small-signal gain of the single HEMT (see Figure 8-2).

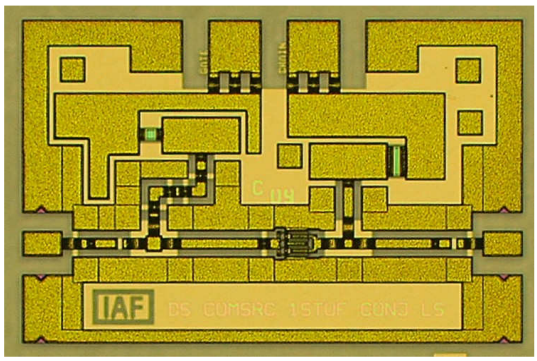

Figure 8-4: Chip picture of a single-stage common source amplifier designed for an operating frequency of 60 GHz. The depicted chip area is 1.5x1 mm².

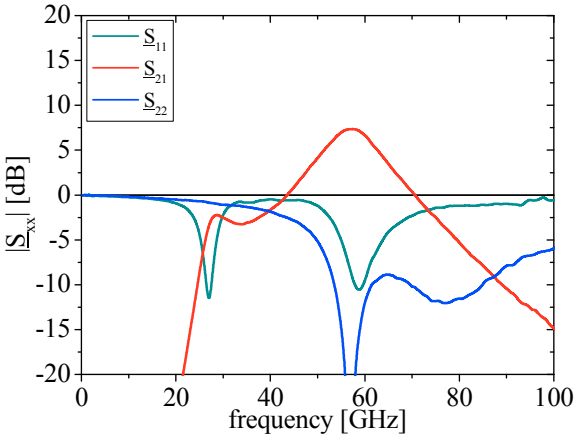

Figure 8-5: Small-signal S-parameter measurements of the 60 GHz amplifier depicted in Figure 8-4.

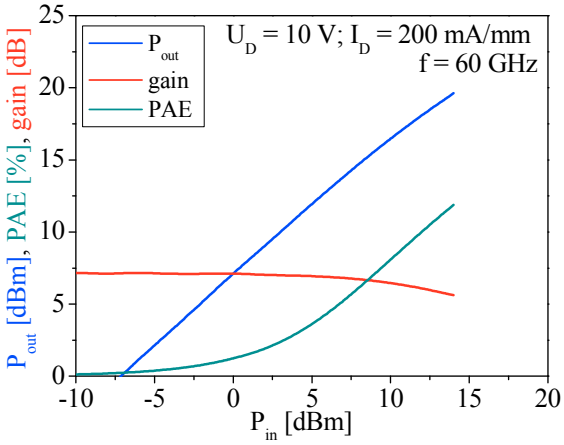

Figure 8-6: Large-signal measurements of the 60 GHz amplifier depicted in Figure 8-4.

This difference is cause by additional losses of the intput and output matching network of 1.25 dB and 0.75 dB, respectively, due to the fact that the MMICs were designed for broadband operation. As can be seen in Figure 8-5 the output and input matching network achieves very good results at 60 GHz, and the input and output return loss ($|\underline{S}_{11}|$ and $|\underline{S}_{22}|$ respectively) are smaller than -10 dB. As figures of merit of the large-signal operation the output power (P_{out}), power added efficiency (PAE) and large-signal gain were measured. Due to a restriction of the maximum input power of the available measurement equipment, the amplifiers could only be measured up to a maximum input power (P_{in}) of 14 dBm. As can be seen in Figure 8-6 such an P_{in} is not enough to reach the saturation of the output power, and subsequently, the PAE. At an P_{in} of

14 dBm the output power and PAE are 21.8 dBm and 12%, respectively. The saturated output power density for this single MMIC corresponds to 0.84 W/mm.

8.2 Demonstration of 60 GHz dual-gate amplifier operation

Similar to the common source amplifier layout depicted in Figure 8-4 a dual-gate amplifier was designed. A chip picture of the amplifier circuit with an input and output matching network for an operating frequency of 60 GHz and drain bias of 10 V is shown in Figure 8-7. Due to the very similar circuit design and geometries the common source und dual gate amplifier can be easily compared with respect to their small and large-signal characteristics.

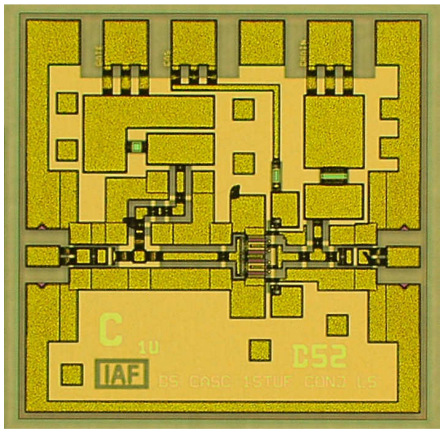

Figure 8-7: Chip picture of a single-stage dual-gate amplifier designed for an operating frequency of 60 GHz. The depicted chip area is 1x1 mm².

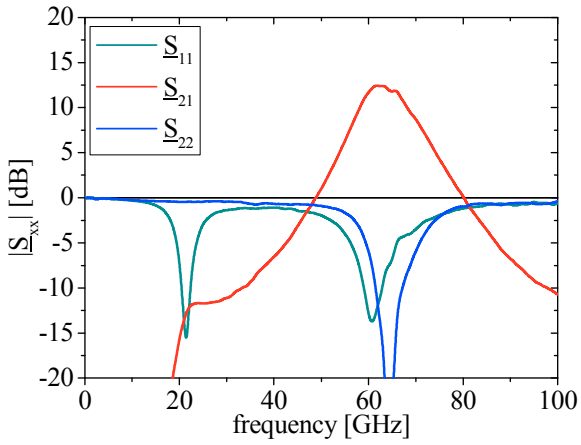

Figure 8-8: Small-signal S-parameter measurements over frequency for the dual-gate amplifier depicted in Figure 8-7.

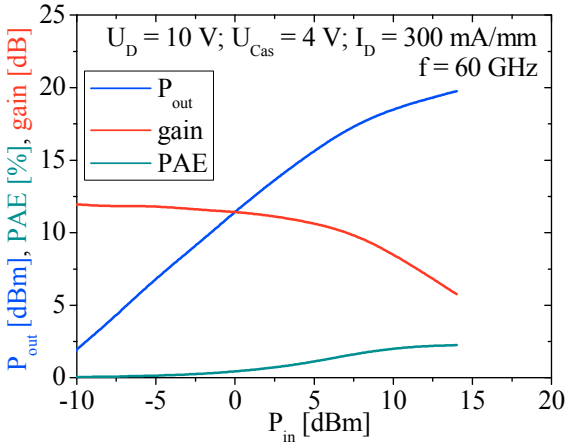

Figure 8-9: Large-signal S-parameter measurements of the 60 GHz dual-gate amplifier depicted in Figure 8-7.

As expected from the small-signal measurements of a single transistor (see Figure 8-3) the gain increases by 5 dB for the dual-gate amplifier, and a small-signal as well as large-signal gain of 12.4 dB were measured. The input and output matching of the dual gate achieves the same good values as the common source amplifier, and a return loss smaller 10 dB can be achieved at 60 GHz. However the -1 dB compression point is reduced to a much smaller output power compared to the common source amplifier (see Figure 8-6). Also the output power at P_{in} = 14 dBm is only 20 dB which is equal to a power density of 0.28 W/mm for this chip. The earlier compression and reduced output power is mainly caused by the lower drain bias of each cascode stage. The dual-gate amplifier was designed for an operation voltage of 10 V and as a consequence the drain bias for each transistor stage is only 5 V. The low operation voltage of the first generation of amplifiers results mainly from the challenging task to stabilize the dual gate amplifier at high drain voltages due to the fact that the gain increases for higher drain biases, and the amplifier becomes unstable.

One method to achieve a better compression behavior is to design amplifier circuits with two dual gate HEMTs in parallel [Sch10]. The results of these amplifiers will be discussed in the next section. Furthermore the production yield of the fabricated circuits is evaluated in more detail.

8.3 Production yield of the 60 GHz dual-gate amplifier

In Figure 8-10 a chip photograph of the 60 GHz circuit with two double-gate HEMTs in parallel is shown. The large signal measurements of 19 chips across a 3-inch wafer of this MMIC are depicted in Figure 8-11. As can be seen in the diagram the compression behavior and output power were comparable to the results of the common source amplifier shown in Figure 8-6. However to achieve a better compression behavior and subsequently a better PAE the gain of the transistor is reduced to 10 dB. This example demonstrates the great design flexibility of our mmW-technology and that the actual amplifier parameter can be matched to a wide spectrum of applications by the design of the MMIC. However in most cases a trade-off between conflicting parameters is necessary.

For the fabrication of MMICs with advanced circuit design a high production yield of the HEMT process and especially the gate module is required. The circuit in Figure 8-10 has a total number of 16 separate gate fingers whereas each finger has a gate width of 45 µm. The basic requirement for device operation is that each separate gate module must be fabricated without failure or discontinuity. If just a small area of the gate line is missing the whole amplifier will not be operational. However, even small fluctuations or misplacements can have severe consequences on the device characteristics of highly scaled HEMTs. A deviation of the mean gate length of 20 nm will directly result in a change of the gate capacitance of 20% (see chapter 6).

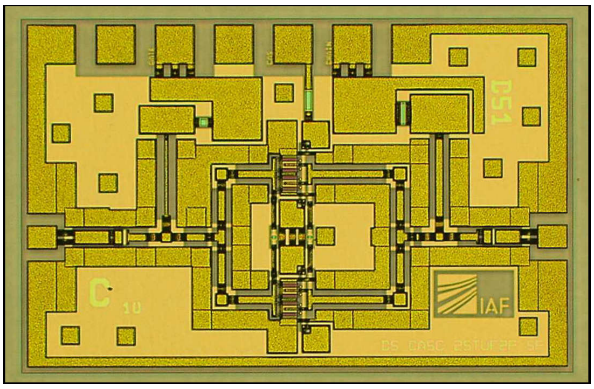

Figure 8-10: 60 GHz dual-gate amplifier with two dual gate HEMTs in parallel. The depicted chip area is 1.5x1 mm².

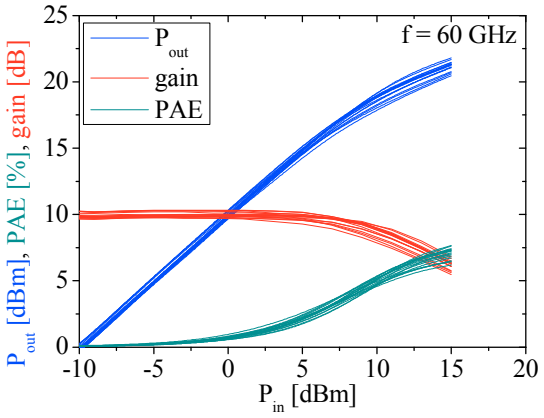

Figure 8-11: Large-signal measurements at 60 GHz for 18 single dies of the amplifier depicted in Figure 8-10.

Therefore the technology to fabricate the gate module must be capable of reproducing gate fingers with gate length deviations below 10 nm for total gate width of 0.72 mm for this MMIC and more than 13 mm for the 19 amplifiers measured in Figure 8-11. From the total 21 chips across the 3-inch wafer only three had severe fabrication failures which can be attributed to particles, misplacement due to a calibration error and edge effects at the boundry of the wafer. The remaining 18 chips show a remarkable uniformity of the large signal measurments. These results prove that the developed mmW-Technology is capable of reproducing the same gate geometries over more than 13 mm total gate width and across a 3-inch wafer. Besides the gate geometries also all other critical device properties such as barrier thickness, source-gate as well as drain-gate spacing, contact resistances of the ohmic contacts and the Schottky contact of the gate must be highly stable. The measurements verify that at least on wafer level these parameters can be precisely controlled by the mmW-process.

8.4 Demonstration of 94 GHz dual-gate amplifier operation

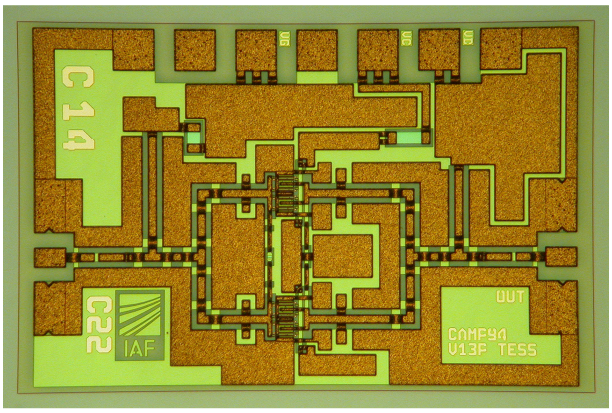

Figure 8-12: 94 GHz amplifier with two dual-gate HEMTs in parallel. The depicted chip area is 1.5x1 mm².

In this section the properties of a dual-gate MMIC designed for amplifier operation at 94 GHz are presented to complete the overview of mmW-circuits based on the developed transistor technology. The design of this amplifier was done by A. Tessmann and a more detailed description of the design layout and analysis can be found in [Qua11].

The basic amplifier design is similar to the 60 GHz dual-gate amplifier (see Figure 8-10) and a chip image of the MMIC is depicted in Figure 8-12. As can be seen in Figure 8-13 the output return loss of the dual-gate 94 GHz amplifier is only 4 dB. The reduced matching can be explained by a higher gain of the actual mmW-process than was expected from previous experiments and modeling. In further development iterations the small and large signal models will be adjusted and comparable matching losses as the 60 GHz amplifiers should be possible.

In continuous wave operation (CW) the amplifier achieves a linear gain of 12 dB as well as a maximum output power (at P_{in} = 20 dB) of 22.8 dBm which results in a power density of 0.53 W/mm for this chip. Furthermore a good PAE of 7% was measured for the dual-gate 94 GHz amplifier. The good gain and output power are only possible due to the reduced relative bandwidth compared

to the 60 GHz amplifiers. These results demonstrate the first 94 GHz operation of a GaN-MMIC in Europe, and world wide only few other research groups have reported similar results [Mas09], [Mic10]. Compared to amplifiers based on GaAs HEMTs with a similar basic layout [Tes99] the GaN amplifier features an increase of the output power by more than 4 dB. This increase can be mainly attributed to the higher possible drain bias of the GaN-amplifier and due to further developments in the fabrication process even higher output powers are expected.

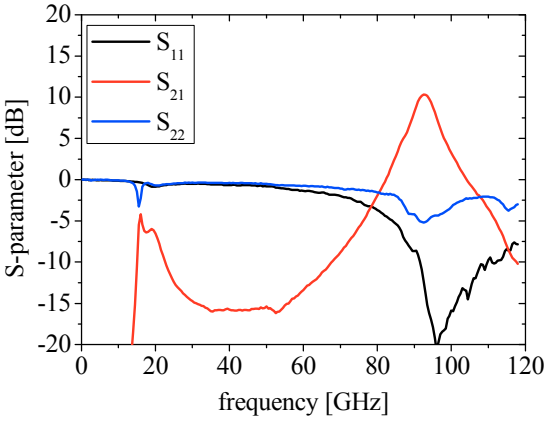

Figure 8-13: Small-signal S-parameter measurements over frequency for the dual-gate amplifier depicted in Figure 8-12.

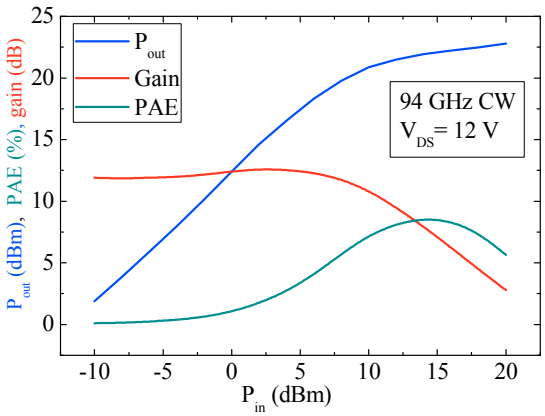

Figure 8-14: Large-signal characterization over input power of the dual gate amplifier depicted in Figure 8-12.

8.5 Conclusion

The design of a mmW-process to fabricate integrated circuits is a very challenging task. The necessary changes of the HEMT layout, barrier design and passivation must be chosen in such a way that a high production yield is possible and that it can be incorporated into an MMIC process. In such a fabrication line the HEMT and especially the gate module is exposed to far more production steps as would be necessary for the functionality of the basic transistor cell. This requires a high mechanical stability of the gate module as well as a precise control and adjustment of each process step for the MMIC fabrication. Furthermore the deviation limits of the critical dimensions of the HEMT demand extreme precise control of the lithography process. The mean deviation of the

gate length must be smaller than 10 nm over a gate width of nearly 1 mm for just one integrated circuit. Besides the gate length nearly every design parameter was scaled down and subsequently the maximal deviation of each device geometry. Therefore each new process step must be evaluated regarding an influence on other process steps or deterioration of secondary device parameters. For example the gate recess processes developed in the course of this work can not be used in our process line because an etching damage can not be prevented or recovered with the available technology. The damaging of the remaining barrier causes a severe increase of the gate leakage current (see chapter 5).

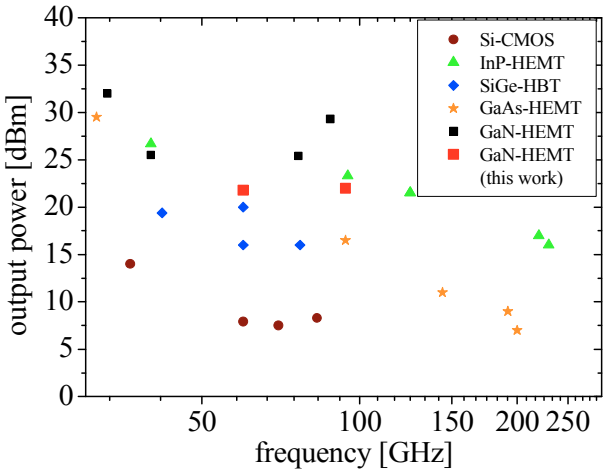

Figure 8-15: Comparision of the output power over frequency of the presented MMICs and reported values for amplifiers based on common semiconductor materials.

Obviously such HEMTs can not be utilized in MMICs and another solution to achieve thin barrier was required. To demonstrate the feasibility of the developed mmW-process various amplifiers at 60 GHz as well as 94 GHz were characterized in this chapter. The first generation of mmW amplifiers achieved very good gains and output powers at their respective frequency. In Figure 8-15 the results given in this work are compared with the best reported output powers for GaN and other common semiconductor materials, so far. As can be seen in the diagram the output powers of our devices exceed the values for GaAs, SiGe

and Si-CMOS transistors. It is of note that the overview in Figure 8-15 gives only a rough comparison of the power capabilities of the material system because it does not account for the used chip space, power density, device layout and the different types of amplifier circuits but it should be adequate to compare the general trend between the different materials. The smaller output power of our devices compared to results of other research groups regarding GaN-HEMTs results from a non optimal design of the first generation of mmW-amplifiers regarding the output power. In future development steps the design and fabrication process of the MMIC as well as the basic HEMT will be improved and a strong increase of the output power is expected.

In the final chapter of this work all results are summarized, and an outlook is given how further process developments or design changes can improve the high frequency and power characteristics of the mmW-HEMTs.

9. Conclusion and outlook

For many high frequency applications, especially for transmitting radio or radar signals, the power amplifier is a limiting factor. Amplifier systems based on common semiconductor materials such as Silicon achieve very small output powers at frequencies above 50 GHz. Therefore, many transistors have to be combined to achieve the necessary output power. As a consequence the efficiency of the whole amplifier decreases due to internal loss caused by the additional combiner circuits.

Gallium Nitride offers unique material characteristics, especially a high critical breakdown field strength, for the fabrication of high-power amplifier systems. Based on this material, AlGaN/GaN heterostructures are used to fabricate field effect transistors with outstanding device characteristics compared to most other semiconductor materials. Over the last few decades great improvements have been made in the development of GaN-HEMT technologies. At the beginning of this work the available fabrication process for GaN-transistors achieved gate lengths of 250 nm with typical cut-off frequencies of 40 GHz. In order to achieve frequencies above 50 GHz this technology had to be scaled down. The goal of this work was to develop and to evaluate a complete process flow for scaled HEMTs to achieve a high gain at mmW-frequencies and which must be compatible with a MMIC process.

The first step in the development of the new mmW-HEMT technology was to specify the general scaling method. Due to the fact that AlGaN/GaN HEMTs feature a very high internal field strength, any approach besides a constant field scaling would result in a drastically reduced breakdown voltage and subsequently a low output power density of the device. According to the theory of constant field scaling of field effect transistors, all device geometries must be reduced by the same factor. To determine the new device geometries, the theoretical scaling rules were applied to the available technology. From these con-

siderations the new technology node must achieve minimum lateral geometries of 100 nm (gate length) and vertical critical dimensions of 10 nm (barrier thickness) to achieve a high gain up to 100 GHz. The very small geometries require a precise control of the process steps, and new techniques had to be incorporated into the process flow to allow the fabrication of the scaled device. At first a complete HEMT process was developed at the Technical University Ilmenau to conduct basic research and developments towards a mmW-technology. Later the results were transferred to the Fraunhofer Institute for Applied Solid State Physics in Freiburg and a mmW-technology to fabricate MMICs with operating frequencies up to 94 GHz was realized. The major developments for the new process line were:

1.) The development of two gate-module processes which are capable of fabricating gate length down to 100 nm.
    a. For the first studies the SiN-gate module was used which uses a SiN mask for the definition of the gate foot and optical lithography to define the gate head.
    b. Later, a T-gate module was developed which uses a 3-layer resist stack to define the whole gate module in one step. The T-gate module allows a further scaling of the gate head overhangs as well as a greater degree of freedom of the passivation material.
2.) In conjunction with the new gate module process, several related techniques had to be developed such as:
    a. A new cleaning process for the highly scaled gate foot including wet chemical processes as well as plasma processes.
    b. Characterization methods to monitor the gate length including AFM-measurements as well as SEM-images of focused ion beam cross-sections.

   c. A drastic increase of the calibration and placement accuracy of the electron beam lithography obtained by an advanced calibration routine as well as improved quality of the calibration marks.

3.) Improvement of the minimal geometry size of the optical lithography to enable smaller gate head sizes as well as source-gate and drain-gate spacings.

4.) Development of two gate recess processes:
   a. First a BCl_3 based plasma etching process for the first tests and evaluations at the TU-Ilmenau
   b. Afterwards a Cl_2 based plasma etching process at the IAF in Freiburg.
   c. Additionally, a technique based on the threshold voltage shift of recessed AlGaN barriers had to be developed to monitor the very small etching depths of only a few nanometers. This method was required due to the fact that common measurement methods can no longer be applied at these dimensions and in combination with the fabrication circumstances.

5.) Modification of the overall process flow to account for the scaled geometries of the mmW-HEMTs such as:
   a. Change of the lift-off processes to reduce the mechanical stress on the gate module.
   b. New cleaning steps and a modified annealing process of the ohmic contacts to improve the topography of the source and drain contacts.
   c. Adjustment of the geometries and process flow to fabricate the contact metal stack for MMICs to account for the scaled geometries of the mmW-HEMT process.

6.) Given the existing process restriction of the available MMIC process a change of the passivation material (SiN) was not possible. Therefore, a quasi low-ε passivation technique was developed to simulate the influence of a low-ε material on the device performance.

7.) Simulation and design of AlGaN/GaN heterostructures with reduced barrier thicknesses and characterization with regard to the electron mobility and sheet carrier concentration of the 2DEG using Hall measurements.

It is to note that all of these changes in process flow, epitaxy and design were only possible by an intensive teamwork and input of the respective specialists and are explicitly not the work of the author alone.

Because of the novel material system the actual scaling characteristic of AlGaN/GaN HEMTs were not known at the start of this work. Therefore, an extensive series of experiments were planed to evaluate the influence of all scaled device geometries on the transistor characteristics. Furthermore, parasitic side effects had to be monitored such as leakage currents or short channel effects which can cause a severe degradation of the device performance. To extrapolate the required data, transistors with defined geometry variations were designed and fabricated.

Later all these test devices were characterized using elaborate characterization methods. The available process flow for 3-inch wafers allows the fabrication of 21 dices with a defined area of 12x12 mm². Each of these dices features a complete series of test HEMTs. To minimize the measurement errors due to fluctuations of the device properties, the transistors of each of the 21 dices were characterized. At first S-parameter were measured at defined operation points such as on-state, off-state and maximum transconductance. In the second step, the small-signal equivalent circuit elements were calculated using the results from the S-parameter measurements. Afterwards the device properties were plotted

versus the geometry variation and the desired scaling behavior was extrapolated. Furthermore, DC-measurements as well as breakdown measurements were conducted to complete the characterizations of the scaled HEMTs. From these evaluations the following major results can be given:

1.) An increase of the extrinsic transconductance from 330 to over 600 mS/mm was achieved by a scaling of the barrier thickness to 11 nm without a reduction of the sheet carrier concentration and electron mobility of the 2DEG.

2.) However, the extrinsic transconductance does not scale by the desired factor which can be attributed to:
   a. A diminished influence of the source-gate scaling on the source resistance due to the relatively high contact resistances. As a result the voltage drop across the source region does not scale with the increased g_{m_int} which causes a severe loss from intrinsic to extrinsic transconductance.
   b. A poor scaling of the intrinsic transconductance as a function of the barrier thickness which is caused by the high gradient of the gate electric field for highly scaled HEMTs.

3.) The scaling rule to keep the gate foot capacitance constant by reducing the gate length by the same factor as d_{bar} could be obeyed. Actually, a small over-scaling was achieved due to the fact that L_g could be slightly more decreased than the reduction of the barrier thickness.

4.) The parasitic capacitances for fully SiN-passivated HEMTs could be reduced from 0.8 pF/mm to 0.5 pF/mm due to the scaling of the gate head overhangs and lower fringing capacitances for thinner barriers.

5.) However the desired values for C_{para} of 0.35 pF/mm could only be achieved by using a low-ε material as passivation layer.

In Table 9-1 the desired HEMT geometries as well as major device characteristics according to the scaling rules are compared to the value achieved in this work. These HEMTs achieve cut-off frequencies of 80 GHz if fully SiN-passivated or 110 GHz for a passivation with a quasi low-ε material.

Table 9-1: Comparison of the developed mmW-technology with the values derived from the scaling rules.

HEMT geometry	desired	achieved	HEMT characteristic	desired	achieved
Barrier thickness	10 nm	11 nm	**Extrinsic transconductance**	850 mS/mm	610 mS/mm
Source-gate spacing	0.4 µm	0.5 µm	**Gate foot capacitance**	1.0 pF/mm	0.9 pF/mm
Gate length	100 nm	100 nm	**Parasitic gate capacitances (SiN-passivation)**	0.35 pF/mm	0.5 pF/mm
Gate head overhang	100 nm	150 nm	**Parasitic gate capacitances (quasi low-ε passivation)**	0.35pF/mm	0.3 pF/mm

To verify the feasibility of the developed mmW-technology at chip level, a first generation of mmW-amplifiers operating at 60 and 94 GHz were presented. These amplifiers achieved very good output powers of 21.8 dBm and 22.8 dBm, which correspond to a power density of 0.84 W/mm and 0.53 W/mm, respectively. This is the first demonstration of an GaN-based MMIC amplifier operation at 94 GHz in Europe and shows the great potential of AlGaN/GaN HEMTs for high power and high frequency applications.

As the gate length is scaled down short-channel effects can limit the device performance. Due to a characterization of scaled HEMTs in off-state, on-state and in the subthreshold region it could be verified that the short-channel effects of AlGaN/GaN HEMTs with L_g down to 100 nm are caused

by the drain-induced barrier lowering. Furthermore a critical aspect ratio, to suppress the DIBL effect, in the range of 14-16 was determined.

The mmW-HEMT technology presented in this work is only the first iteration of an ongoing development process. As discussed in this work, the mmW-HEMTs are still limited by some process restrictions. Furthermore many studies could not be conducted in this work due to the available sample size and time frame. In the following part a short outlook will be given how the mmW-process can be further improved and which additional studies have to be conducted regarding highly scaled AlGaN/GaN HEMTs:

- The contact resistances of the ohmic contacts must be reduced for mmW-HEMTs from 0.15 Ω/mm to 0.01 Ω/mm to minimize the increasing loss from intrinsic to extrinsic transconductance. Additionally, a fabrication process for the source and drain contacts should be used which does not require a high temperature annealing step. This will greatly enhance the edge roughness of the contacts. As a consequence the source-drain spacing can be further reduced without a decrease of the production yield. Both measures together will greatly increase the transconductance of the mmW-transistors. However such a process step would require an intensive development effort because new process steps such as a Si-implantation or a recess of the ohmic contacts have to be incorporated into the existing MMIC fabrication process.
- Besides the reduction of $R_{contact}$, a change of the passivation process towards a low-ε material such as benzocyclobutene (BCB) will greatly increase the gain of mmW-HEMTs.
- Given the fact that HEMTs with L_g = 100 nm are used, the barrier thickness must be reduced to 7 nm to successfully suppress the DIBL-effect and subsequently enhance the breakdown

voltage. But such thin barriers can only be achieved by a change of the barrier material. AlN or AlInGaN barriers have been reported with similar or better characteristics of the 2DEG compared to AlGaN/GaN heterostructures. However the fabrication of ohmic contacts, especially the very low values required for mmW-HEMT, are very challenging for these materials.

- Another method to increase U_{br} is the design of double heterostructures whereby the second AlGaN layer inside the GaN buffer acts as a back barrier which increases the modulation efficiency of the gate and subsequently U_{br}.
- However, an increase of U_{br} can be futile for the development of power amplifier if the thermal losses at much small drain voltages are the limiting factor for a stable device operation. It is therefore necessary to determine in further studies the dominant restricting factor for the drain voltage.
- If the breakdown voltage is a negligible parameter for the output power of mmW-amplifiers, the gate length can be scaled down further without a change of the barrier thickness. This will reduce the gate foot capacitance and as a consequence the gain of the transistor will be drastically improved. But short channel effects such as an increased output conductance will reduce the efficiency of these transistors.
- Furthermore, less is known about the long-term stability of AlGaN/GaN-HEMTs. Studies on C-band amplifiers demonstrated that HEMTs based on AlGaN/GaN heterostructures feature unique degradation mechanisms which are attributed to the high strain of the AlGaN barrier or a piezo-mechanical stress. However, initial experiments show that these degradation

mechanisms are strongly reduced for scaled barriers but further studies are necessary to verify this hypothesis.

In summary the first generation of a MMIC process with operating frequencies up to 94 GHz with an output power of 22.8 dB was successfully developed which demonstrates the great potential of GaN-based HEMTs at millimeter wave frequencies.

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Appendix A

Transistor layouts measured in this work

Device code	Number of fingers x gate width	Gate length	Gate head over-hangs (Source side/drain side)	Source gate spac-ing / drain gate spacing	Shield
MW01	4x50 µm	0.15 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW11	4x50 µm	0.1 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW31	4x50 µm	0.1 µm	0.1 / 0.3 µm	0.7 / 2.0 µm	no
MW32	4x50 µm	0.1 µm	0.1 / 0.3 µm	0.7 / 2.0 µm	1.0
MW33	4x50 µm	0.1 µm	0.1 / 0.4 µm	0.7 / 2.0 µm	no
MW34	4x50 µm	0.1 µm	0.1 / 0.4 µm	0.7 / 2.0 µm	1.0
MW35	4x50 µm	0.1 µm	0.1 / 0;5 µm	0.7 / 2.0 µm	no
MW36	4x50 µm	0.1 µm	0.1 / 0;5 µm	0.7 / 2.0 µm	1.0
MW41	2x50 µm	0.1 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW42	2x50 µm	0.1 µm	0.1 / 0.3 µm	0.7 / 2.0 µm	no
MW51	2x50 µm	0.2 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW52	2x50 µm	0.25 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW53	2x50 µm	0.3 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW54	2x30 µm	0.1 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW55	2x70 µm	0.1 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW56	2x100 µm	0.1 µm	0.2 / 0.2 µm	0.7 / 2.0 µm	no
MW81	2x50 µm	0.1 µm	0.2 / 0.2 µm	0.5 / 1.0 µm	no
E104	2x50 µm	0.15 µm	0.3 / 0.3 µm	0.7 / 2.0 µm	no
E203	2x50 µm	0.25 µm	0.3 / 0.3 µm	0.7 / 2.0 µm	no

E204	2x50 µm	0.25 µm	0.3 / 0.3 µm	0.7 / 1.4 µm	no
Device code	**Number of fingers x gate width**	**Gate length**	**Gate head overhangs (Source side/drain side)**	**Source gate spacing / drain gate spacing**	**Shield**
E205	2x50 µm	0.25 µm	0.3 / 0.3 µm	0.7 / 0.7 µm	no
E501	2x50 µm	0.5 µm	0.3 / 0.3 µm	0.7 / 2.0 µm	no
A102	2x50 µm	0.5 µm	0.3 / 0.3 µm	1.5 / 4.0 µm	no
A204	2x50 µm	0.25 µm	0.3 / 0.3 µm	1.0 / 3.5 µm	no

Appendix B

X-Ray defraction profiles of a reference wafer with a intented barrier properties of d_{bar} = 25 nm and x_{Al} of 22%.

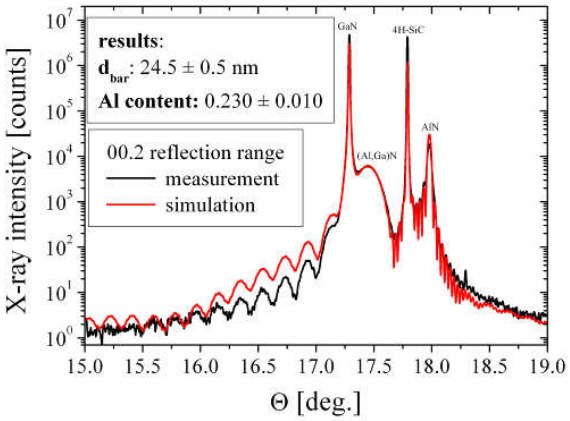

Figure 9-1: Measured and simulated X-ray defraction profile of a wafer with d_{bar} = 25 nm and x_{Al} of 25% (centre of the wafer).

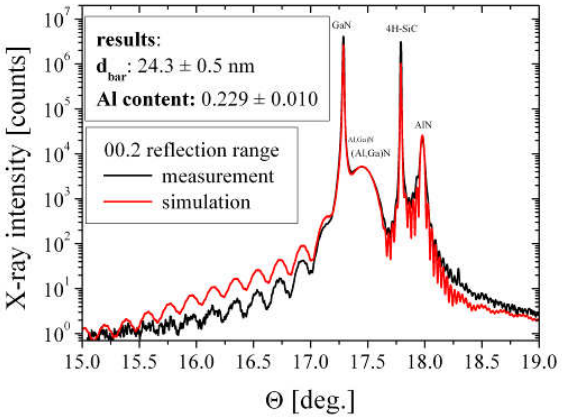

Figure 9-2: Figure 9-3: Measured and simulated X-ray diffraction profile of a wafer with d_{bar} = 25 nm and x_{Al} of 25% (between centre and edge of the wafer).

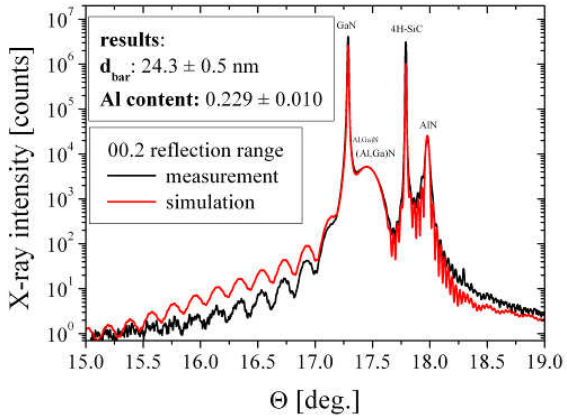

Figure 9-4: Figure 9-5: Measured and simulated X-ray defraction profile of a wafer with d_{bar} = 25 nm and x_{Al} of 25%.

As can be seen by comparing all three measurements the deviation from the intended parameters is below 1 nm and 1 % for the barrier thickness and Al-

content, respectively. The uniformity across the wafer is also very good with deviations below 0.2 nm and 0.1% for d_{bar} and x_{al}, respectively.

X-Ray defraction profiles of a wafer with a scaled barrier design with properties of d_{bar} = 17 nm and x_{Al} of 30%.

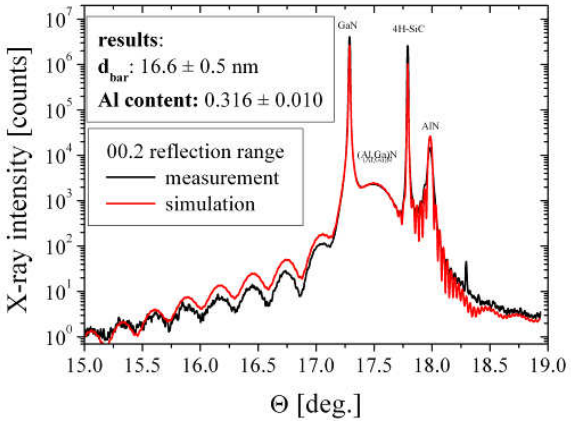

Figure 9-6: Measured and simulated X-ray defraction profile of a wafer with d_{bar} = 17 nm and x_{Al} of 30% (centre of the wafer).

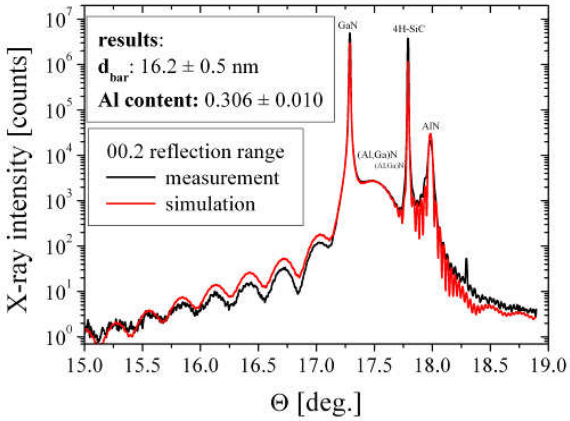

Figure 9-7: Measured and simulated X-ray defraction profile of a wafer with d_{bar} = 17 nm and x_{Al} of 30% (between centre and edge of the wafer).

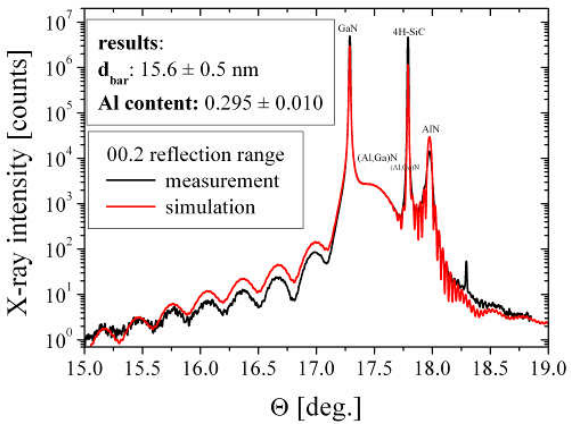

Figure 9-8: Measured and simulated X-ray defraction profile of a wafer with d_{bar} = 17 nm and x_{Al} of 30% (edge of the wafer).

As can be seen by comparing the depicted diagrams with the measurements of the reference wafer, comparable deviations from the intended parameters as

well as the deviation across a wafer could be achieve for the scaled barrier design.

Acknowledgements

At first I would like to thank my doctoral adviser Professor Oliver Ambacher for the opportunity to fulfill one of my childhood dreams. Finally I understand how this little gray computer chip can calculate all the data down to the single transistor. Furthermore I want to express my gratitude for the great support during this work.

Also many thanks to my reviewer Dr. Frank Schwierz for the valuable discussions regarding the scaling of field effect transistors and general advice for this work.

Special thanks to Dr. Stephan Maroldt for all the late night measurements to satisfy my curiosity, the long discussions about GaN-HEMTs, amplifier design as well as S-parameters, and in addition for being a good friend and companion along the "bumpy road" towards the green apples.

Furthermore, I want to thank my supervisors Dr. Arnulf Leuther, Dr. Rüdiger Quay and Dr. Michael Mikulla for being never ending sources of knowledge, motivation and support, and also for the great help to see the bigger picture when I was lost in details.

But all this work would not have been possible without the great teams of the technology departments of the ZMN in Ilmenau and the IAF in Freiburg. Therefore I want to express my deepest gratitude for their patience, unlimited support and assistance in all the technology developments and fabrications. I want to thank especially Dr. Thomas Stauden, Dr. Wilfried Pletschen, Dr. Wolfgang Bronner, Dr. Patrick Waltereit and Dr. Rudolf Kiefer for their excellent help in developing new process steps and sharing their vast knowledge regarding HEMT fabrications. Furthermore, my gratitude to Brian Raynor and Karlheinz Glorer for sharing their expert knowledge and assistance in mastering the art of electron beam lithography. Also great thanks to the expert teams of laboratory assistants from the ZMN and IAF especially Birgitt Hartmann, Dr. Gudrun Kaufel and Nicola Rollbühler for their efforts far beyond the expected.

I would also like to thank Dr. Klaus Köhler and Stephan Müller for their assistance and contributions regarding the developments and characterizations of scaled heterostructures.
Also I want to thank all the collegues from the high frequency department of the IAF for their great efforts regarding the multitude of measurements to characterize the vast amounts of transistors especially Roger Lozar and Thomas Maier. Furthermore, I want to thank Dr. Friedbert van Raay and Markus Mußer for the detailed and helpful discussions regarding HEMT characteristics and device behavior.
Last but not least, I acknowledge the financial support by the "Bundesministerium für Bildung und Forschung" (BMBF) within the mobileGaN and GaN on/off program.

Curriculum Vitae

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10/2007	Begin of the doctorate at the Centre for Micro und Nanotechnology, Technical University Ilmenau, Germany.
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2006	Second mandatory internship at the paragon AG for automotive and electronic solutions, Suhl, Germany. Assignment: Design of a CAN-bus measurement board for the in-house quality control.
9/2005 – 10/2007	Main study period with the emphasis on: nanotechnology, high frequency electronics und vacuum technology, Technical University Ilmenau, Germany.

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Gallium Nitride (GaN) offers unique material characteristics to enable the fabrication of field effect transistors with high output powers at millimeter wave frequencies. At the start of this work GaN-amplifiers operating at K-band frequencies were available. However, an increasing demand exists for power amplifiers beyond 50 GHz such as radar applications or RF-broadcasting systems.

In this work a scaling approach is studied to develop a transistor technology which achieves a high gain as well as a high output power at W-band frequencies and can be applied in the existing fabrication process for monolithic microwave integrated circuits (MMIC). Following the theoretical scaling rules for field effect transistors lateral and vertical critical dimensions of 100 nm and 10 nm must be achieved, respectively. Therefore various new fabrication pro-cesses were developed in this work to enable the new critical dimensions with a sufficient production yield for MMIC fabrication.

Transistors fabricated with these methods were evaluated regarding the influence of the scaled geometries on the device characteristics using S-parameter as well as DC-measurements. As a result a transistor technology could be established which achieves a transconductance above 600 mS/mm this is one of the highest reported values for GaN-based HEMTs so far. Furthermore, a very low parasitic capacitance of 0.3 pF/mm was achieved. As a consequence, these transistors feature a current-gain cut-off frequency of more than 110 GHz.

Besides the high frequency characteristics short channel effects and their influence on the device characteristics were also evaluated. From these studies the following results were obtained: The scaled transistors are dominated by a drain induced barrier lowering (DIBL) which is mainly a function of the aspect ratio of gate length to barrier thickness. It was also found that a critical aspect ratio of approximately 14 is necessary to suppress the DIBL-effect.

Finally, first generations of MMICs based on the developed transistor technology were and 94 GHz of 21.8 dBm and 22.8 dBm, which correspond to a power density of 0.84 W/mm and 0.53 W/mm, respectively. These measurements demonstrate the first successful MMIC amplifier operation of GaN-based HEMTs at W-band frequencies in Europe. Furthermore, a high production yield regarding the MMIC fabrication process of more than 85% could be demonstrated across a 3-inch wafer.

ISBN 978-3-8396-0303-1