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Development and Characterization of Bifacial p-Type Silicon Shingle Solar Cells with Edge Passivation

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To my family

Kurzfassung

Die vorliegende Dissertation beschäftigt sich mit der Entwicklung und Charakterisierung von bifazialen „*p*-Type Shingled Passivated Edge, Emitter, and Rear“ (*p*SPEER) Solarzellen. Die neuartige Zellstruktur verbindet die Konzepte der Bifazialität, des Schindelns und der „Passivated Emitter and Rear Cell“ (PERC) Solarzellentechnologie. Um die *p*SPEER-Solarzellen herzustellen, werden vollformatige Solarzellen mit angepassten Metallisierungslayouts nach der Kontaktausbildung in Schindelsolarzellen aufgetrennt. Die Rekombination an den neu gebildeten Zellkanten führt zu einer Verringerung des Pseudo-Füllfaktors *pFF* und damit zu Zelleffizienzverlusten. Das thermische Laserstrahl-Separieren (TLS) ermöglicht glatte Zellkanten mit geringer Oberflächendefektdichte. In Kombination mit der im Rahmen dieser Arbeit entwickelten „Passivated Edge Technology“ (PET), bildet die TLS-Technologie die Grundlage für die Reduktion der Oberflächenrekombinationsgeschwindigkeit an den Zellkanten. Die PET-Prozesssequenz selbst umfasst eine Aluminiumoxid (Al_2O_3) Schichtausbildung bei niedrigen Abscheidetemperaturen von maximal 130°C mittels thermischer Atomlagenabscheidung und einen thermischen Aktivierungsschritt („Post-Deposition Anneal“, PDA) bei 200°C oder darunter. Diese Niedertemperatur-Prozessierung verhindert die Schädigung bereits vorhandener Metallkontakte und Passivierungsschichten. Die Anwendung von TLS und PET auf *p*SPEER-Solarzellen führt zu einer neuen Zellarchitektur: „*p*SPEER$^{\text{PET}}$“.

Der TLS-Prozess wurde während der gesamten Arbeit so optimiert, dass der Einfluss des Trennprozesses auf die elektrische Leistung der Schindelsolarzellen minimiert wird. Es zeigt sich, dass die *pFF*-Verluste nach TLS hauptsächlich auf die Bildung der neuen Kanten und nicht auf den Laserprozess selbst zurückzuführen sind. Die aufgebrachten Al_2O_3-Schichten zeigen nach PDA eine ausgezeichnete Oberflächenpassivierungsqualität. Dies zeigt sich unter anderem durch symmetrisch passivierte Floatzone-Silicium Lebensdauerproben, für die sehr geringe effektive Oberflächenrekombinationsgeschwindigkeiten $S_{\text{eff}} = 4{,}4\ \text{cm/s}$ auf *p*-dotiertem und $S_{\text{eff}} = 5{,}7\ \text{cm/s}$ auf *n*-dotiertem Silicium demonstriert werden.

Auf Zellebene erreicht eine *p*SPEER$^{\text{PET}}$-Solarzelle eine Spitzenleistungsdichte $p_{\text{out}} = 23{,}7\ \text{mW/cm}^2$ unter Berücksichtigung einer zusätzlichen rückseitigen Bestrahlungsstärke von $10\ \text{mW/cm}^2$. Eine Wiedererlangung von bis zu etwa $80\%_{\text{rel}}$ des trennungsbedingten *pFF*-Verlusts durch die PET wird demonstriert. Der Fortschritt bei der Zelltrennung, der Niedertemperatur Al_2O_3-Oberflächenpassivierung und der Kantenpassivierung sind auch für andere Solarzelltypen, wie Silicium-Heterojunction Solarzellen und Solarzellen mit Tunneloxid-passivierten Kontakten (TOPCon), von sehr hohem Interesse.

Abstract

This dissertation deals with the development and characterization of bifacial p-type shingled passivated edge, emitter, and rear (pSPEER) solar cells. The new cell structure connects the concepts of bifaciality, shingling, and the p-type silicon passivated emitter and rear cell (PERC). To obtain the pSPEER solar cells, full wafer-sized host cells with corresponding metallization layouts are separated into shingle solar cells after contact formation. Recombination at the newly formed cell edges leads to a reduction in pseudo fill factor pFF and thus to losses in energy conversion efficiency. Thermal laser separation (TLS) offers the possibility to obtain smooth cell edges with low surface defect density. In combination with the post-separation passivated edge technology (PET), developed within this work, the TLS technology forms the basis for reducing the surface recombination velocity at the cell edges. The PET process sequence itself encompasses an aluminum oxide (Al_2O_3) layer formation at low deposition temperatures with a maximum of 130°C by means of thermal atomic layer deposition and a post-deposition annealing (PDA) step that takes place at set temperatures equal or below 200°C. This low temperature processing prevents the damage of already existing metal contacts and passivation layers. Applying TLS and PET on pSPEER solar cells leads to a new cell architecture, called "pSPEER$^{\mathrm{PET}}$".

The TLS process has been optimized throughout the work, such that the impact of the separation process on the electrical performance of the shingle solar cells is minimized. It is found that the pFF losses after TLS are mainly attributed to the formation of the new edges and not to the laser process itself. The applied Al_2O_3 layers show excellent surface passivation quality after PDA. This is shown, among others, by symmetrically passivated floatzone silicon lifetime samples for which very low effective surface recombination velocities $S_{\mathrm{eff}} = 4.4$ cm/s on p-type silicon and $S_{\mathrm{eff}} = 5.7$ cm/s on n-type silicon are demonstrated.

On the cell level, a peak output power density $p_{\mathrm{out}} = 23.7$ mW/cm^2 is achieved for a pSPEER$^{\mathrm{PET}}$ solar cell considering 10 mW/cm^2 rear side irradiance. A recovery of up to about $80\%_{\mathrm{rel}}$ of the separation-related pFF loss by the PET is demonstrated. The progress in the cell separation, the low temperature Al_2O_3 layer surface passivation, and the edge passivation are also of very high interest for other solar cell types such as silicon heterojunction solar cells and tunnel oxide passivated contacts (TOPCon) solar cells.

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1 Introduction

1.1 Motivation and objectives

In today's world, the growth of global energy consumption has lead to a rise in harmful greenhouse gas emissions, mainly due to fossil fuel-based combustion [1]. As the global energy demand increases, the need for alternative ecologically-friendly technologies is inevitable to decouple consumption from emissions [2]. In hand with the necessity of reducing energy consumption, energy efficient and climate-friendly renewable energy conversion technologies are indispensable [3]. Photovoltaic (PV) technology converts light into electricity. Since solar energy is the most abundant renewable energy source [4], harvesting sunlight by means of PV is an approach to make use of its availibility. Due to advancements in PV research and production technology, historic price reduction data from 1976 until end of 2019 portray a drop in average PV module sales price per watt peak (Wp) with a learning rate of around 23.5% for each doubling of cumulative shipments (in Wp) [5]. The drastic fall of prices has paved the way towards a total global installed module power of around 628 GWp until the end of 2019 [5]. In other words, the vital role of PV in the energy transition towards climate-friendly systems has already become unquestionable by presenting itself as an economically viable technology.

The focus in the PV community is still set towards further improving the energy conversion efficiency η of cells and modules to continue decreasing the prices per Wp of manufactured devices. Moreover, the sustainable use of resources in the production leads to an additional decrease in the environmental footprint and the energy payback time of the technology. Around 95% of the PV modules in total production are based on crystalline silicon semiconductor materials [6]. For the fabrication of these crystalline silicon solar cells, p-type monocrystalline Czochralski-grown silicon (Cz-Si) [7] wafers are expected to hold a significant market share in the upcoming ten years [5]. On the solar cell level, full-area aluminum

back surface field (Al-BSF) solar cells started to dissapear from mass production and are replaced by cell structures with additional dielectric silicon surface passivation layers and local electrical contacts [5]. The passivated emitter and rear cell (PERC), first published in 1989 as a lab-scale solar cell [8], currently leads the cell/module market share. The transition from Al-BSF to PERC is derived as a result of the cell efficiency benefit achieved by considering practical adaptations to already existing production steps and processes. For instance, the introduction of dielectric passivation layers on the rear side coupled with its local electrical contacting increases the cell performance. The rear side passivation for p-type silicon cells thereby consists of a dielectric layer stack, e.g., comprised of aluminum oxide (Al_2O_3) and silicon nitride (SiN_X), resulting in reduced surface recombination and thus increased η of the solar cells. The formation of a local back BSF also facilitates the fabrication of PERC-based bifacial cells [9]. These bifacial solar cells can also absorb irradiance impinging on their rear side. This feature allows for potentially higher device output power densities p_{out} in application conditions with additional albedo light [10].

As an approach to improve module output power, full wafer-sized solar cells (e.g., with an edge length of 156.75 mm) are separated into smaller-sized cells (e.g., half cells) prior to module integration [11, 12]. Smaller-sized cells generate lower current in the string leading to decreased electrical resistance losses on the interconnection level. As a consequence of the relatively straightforward addition of the separation process in the latest stage of cell manufacturing, the concept is already exploited in mass production [13]. Additionally, conventional ribbon interconnection is challenged by alternative techniques such as the shingling (i.e overlapping) interconnection, revived from an idea first proposed in 1956 [14]. The concept of shingling is realized when a cell's rear side metal contact (of a certain polarity n-type or p-type) overlaps the neighboring cell's front side metal contact (of the opposite polarity). The cell-to-cell mechanical and electrical contact omits cell spacing leading to a visually busbarless string, thus reducing optical losses on the module level.

Nevertheless, for silicon solar cells such as PERC, the cell separation process after the formation of electrical contacts leads to the creation of "new" edges lacking intentional dielectric passivation. Thus, the cell efficiency can drop, mainly due to an increase in the surface recombination velocity at the edge surface (also known as edge recombination). Edge

passivation becomes more relevant for cells with even smaller sizes and thus higher perimeter-to-area ratios [15], e.g., such as shingle solar cells. Also, high quality edge passivation is even more critical with the increase of η levels. Some edge passivation approaches are discussed in the literature [16–22] to mitigate edge recombination. However, the implementation of these methods in production remains challenging since they feature either numerous costly pre-metallization processes (i.e., prior to contact formation of the cell electrodes) and/or technically complex post-metallization processes. To keep the appeal of the separation after the fabrication of full wafer-sized cells, technical solutions to minimize edge recombination are needed.

This dissertation introduces the concept of a solar cell that combines the three following characteristics: (i) the bifacial PERC technology, (ii) separated shingle cells, and (iii) edge passivation. The new solar cell concept is called the *p*-type silicon shingled passivated edge, emitter, and rear (*p*SPEER) solar cell. An essential objective of the work is to optimize laser-based separation processes, primarily thermal laser separation (TLS) [23], as an attempt to reduce separation-related surface recombination losses of separated silicon solar cells. The work demonstrates experimental methods to enhance the understanding of the effects of separation processes on the electrical performance of advanced silicon solar cells (including cell structures with passivated contacts). The work also introduces the innovative passivated edge technology (PET) as a post-metallization edge passivation technique that includes low temperature passivation layer deposition and post-deposition annealing processes. The dissertation also demonstrates an in-depth experimental study of surface passivation effects on *n*-type and *p*-type silicon by Al_2O_3 attained at low temperatures by atomic layer deposition (ALD). The investigation of the deposition and annealing reaction kinetics allows the development of tailor-made surface passivation processes for post-metallization processes such as PET and other applications where low temperature processes with short duration are required. The work also displays cell batch results of PET-processed shingle solar cells.

1.2 Dissertation outline

Chapter 2 explains the fundamental theoretical background needed to understand the work done in the dissertation. The chapter discusses the

mechanical and optical properties of crystalline silicon. It also explains the basic functioning principle of silicon solar cells. In addition, a depiction of the one- and two-diode models is given to describe crucial solar cell output parameters. The current-voltage (IV) characterization setup and the SunsV_{OC} measurement method are also presented. Additionally, the loss mechanisms in silicon solar cells and their impact on cell output parameters are portrayed. Charge carrier recombination is also described in addition to the fundamentals of silicon surface passivation.

In *Chapter 3,* state-of-the-art silicon solar cell concepts and technologies existing before the start of the dissertation work in 2017 are discussed. Basic PERC solar cell process routes are depicted and specific details relevant for the fabrication of bifacial PERC solar cells are discussed. This chapter also features work completed before 2017 in the field of separated silicon solar cells with emphasis on shingle solar cells. Furthermore, it discloses a review of edge recombination models and characterization techniques published prior to the start of this dissertation.

Chapter 4 introduces the concept and the basic fabrication process sequence of *p*SPEER solar cells. In the light of the process route, the formed structures of the *p*SPEER solar cell device are defined to set the terminology used throughout the following chapters. The concept and elementary process sequence of the passivated edge technology (PET) are introduced. Taking the specific case of *p*SPEER solar cells, the application of PET leads to the newly derived cell architecture, the *p*SPEER^{PET} solar cell. Adaptations of the current-voltage measurement setup for the measurement of shingle solar cells is shown. The SunsV_{OC} contacting approach used in this work is presented.

Chapter 5 deals mainly with the separation processes of silicon solar cells. It starts with a general overview of existing methods for the separation of crystalline semiconductors with a review on previous work done in the field of post-metallization separation of silicon solar cells. The chapter then focuses on the thermal laser separation (TLS) by introducing the equipment used and the relevant process parameters for the experiments performed in this dissertation. To further understand the impact of the TLS on local electrical properties and optimize the process, a photoluminescence-based imaging method is introduced. The experiments separate the influence of surface recombination from that of the complete separation on metallized cells.

Chapter 6 motivates the necessity of low temperature surface passivation and their application. The chapter also investigates the impact of low temperature atomic layer deposition (ALD) for Al_2O_3 coatings of *p*- and *n*-type floatzone silicon (Fz-Si) lifetime samples. The reaction kinetics between the deposition and post-deposition annealing temperatures are studied with the consideration of deposition thicknesses and thin film layer properties. Besides, the stability of attained effective lifetime and effective surface recombination velocity results are investigated.

Chapter 7 first provides a review of edge passivation methods from the literature. As a main topic, post-metallization PET processes are examined to obtain edge-passivated *p*SPEER$^{\text{PET}}$ solar cells with enhanced cell efficiencies. The overview of cell efficiencies attained during the time span of the dissertation is also revealed.

In *Chapter 8* a summary of the work is provided. Additionally, an outlook proposes future fields of investigation and optimization derived from the presented work.

The *Appendix* presents versatile additional material for further clarification. It includes information about the IV measurement setup used to obtain certified cell measurements for shingle solar cells in the *Fraunhofer ISE CalLab PV Cells*. Additional details about the ellipsometry setup used for the measurement of Al_2O_3 layer properties are provided. The metallization layout generations of *p*SPEER solar cells developed in this dissertation are also listed.

2 Silicon Solar Cell Fundamentals

2.1 Introduction

This chapter provides the theoretical framework required as a crucial background to understand the work accomplished in this dissertation. The working principle of the basic crystalline silicon solar cell is explained. Moreover, the key output parameters that describe electrical properties are clarified by relying on the one- and two-diode models of solar cell devices. As essential characterization methods unfolding the device's electrical performance, the current-voltage measurement and the SunsV_{OC} technique are also described. Additionally, loss mechanisms in solar cells are presented by focusing on the optical losses, charge carrier recombination, and resistive losses. The characterization methods of charge carrier recombination used in the work namely the photoconductance decay measurement and the photoluminescence imaging technique, are described. Thereafter, a comprehensive depiction of the chemical and field effect surface passivation concludes this chapter.

2.2 Physical properties of crystalline silicon

In solid-state physics, solids are categorized into amorphous and crystalline materials [24]. Unlike amorphous materials, the atoms of crystals are placed in a periodic, ordered manner forming a crystal lattice from which a unit (primitive) cell can be derived [25]. The repetitive distance between the atoms is known as the lattice constant a [26]. This lattice structure defines mechanical, optical, and thermal properties.

Crystal structure and mechanical properties

In the case of silicon, each atom forms four covalent bonds creating a tetrahedron to obtain what is called a diamond cubic lattice structure [27].

The alignment of atoms is relevant for properties that are of interest in semiconductor applications. For that the Miller indices (h, k, l) are crystallographic notations that describe the orientation of atomic planes and directions in a three-dimensional coordinate system [28, 29]. They are derived by considering the reciprocal of the atomic planes' intercept with the crystallographic axes. A classification is made to define a vector direction by the nomenclature [h, k, l], single plane by (h k l), set of planes by {h k l}, while a set of directions is denoted by $< h\ k\ l >$. Based on the arrangement of atoms in crystalline silicon, the prominent crystal orientation planes (100), (110), and (111) are defined; see Fig. 2.1. Due to the symmetry of the lattice, the planes can also be written as {100}, {110}, and {111}.

When there is a continuity of the crystal lattice periodicity within the material, it is named as a single-crystal or as a monocrystalline material [30]. In the case of having numerous crystals with different orientations within the solid, the material is considered as multicrystalline where grain boundaries separate the different crystal orientations within [30]. For the fabrication of crystalline silicon solar cells, both multicrystalline and monocrystalline wafers are commonly used [6]. In this work, only monocrystalline wafers, specifically Czochralski-grown silicon (Cz-Si) [7] wafers are considered for the fabrication of solar cell devices. In addition, floatzone silicon (Fz-Si) [31] wafers that have very low concentrations of impurities compared to Cz-Si are used for the preparation of test samples for surface passivation experiments [31]. The crystal orientation for wafers from both techniques is defined during the ingot pulling process (for details of Cz-Si and Fz-Si ingot pulling processes please refer to Ref. [25]). Like many anisotropic brittle solids, in crystalline silicon the orientation-dependent interatomic forces determine the orientation-dependent

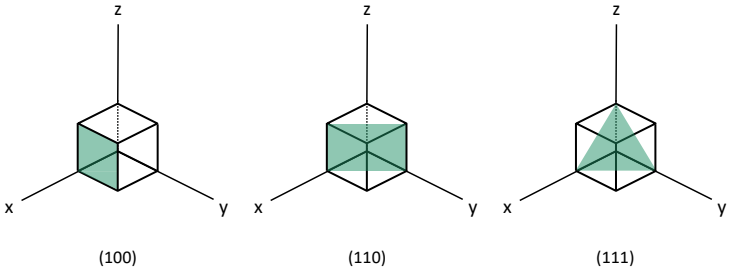


Fig. 2.1. Orientation of crystal planes in crystalline silicon lattice. The figure is redrawn from Ref. [26].

mechanical properties of the sample [30]. *Hooke*'s law governs the linear elastic behavior of materials under stress σ_{mech} (force per unit area) and strain $\varepsilon_{\text{mech}}$ (relative deformation) having the Young's modulus E_{mech} as an orientation-dependent proportionality constant; see equation (2.1).

$$\sigma_{\text{mech}} = E_{\text{mech}}\, \varepsilon_{\text{mech}} \tag{2.1}$$

Brittle materials break (fracture) when the fracture point on the stress-strain curve is attained. Higher E_{mech} values imply higher σ_{mech} at a constant deformation. The silicon wafers tend to cleave in the favored directions <111>, <110> having room temperature E_{mech} values of 185 GPa and 170 GPa respectively [30]. Whereas the direction <100> features a E_{mech} value of 130 GPa [30]. The Cz-Si wafer formats in the PV industry are defined by their edge length as well as their diameter [32]. In this work, mostly pseudo square "M2" format wafers having an edge length of 156.75 mm and a diameter of 210 mm are used; see Fig. 2.2(a). These wafers cleave in the favored direction of 45° angle with respect to the edge length. The Cz-Si wafer thicknesses W used in this work, range from 160 µm $\leq W \leq$ 180 µm. In the case of Fz-Si wafers used in this work, they feature a (100) surface orientation and a wafer diameter of around 100 mm; see Fig. 2.2(b). The samples cleave in favored 90° angles in relation to the "flat". The wafers used are either 200 µm or 250 µm thick, to be stated in the experimental sections of the work.

Optical properties

The optical properties of silicon are of vital importance for the light coupling required for efficient solar cell devices. Since this work also involves laser processing of crystalline silicon, optical properties of such substrates are discussed. To start with, light with photon energy E_{ph} is

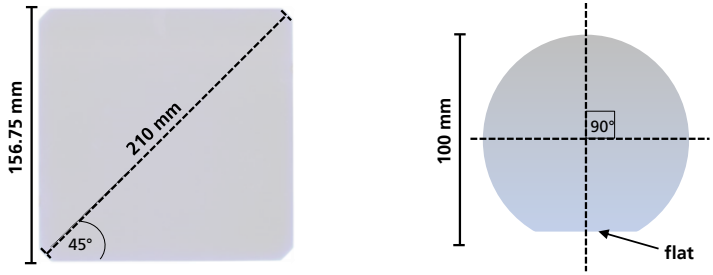


Fig. 2.2. Top view of wafer formats used (a) for the fabrication of solar cells and (b) for the lifetime samples.

absorbed in the semiconductor material by exciting electrons from an initial energy level called the valence band (E_V) to the higher energy level called the conduction band (E_C). E_{ph} is quantized such as it is inversely proportional to the wavelength of the incident light λ by the expression hc/λ, where h is Planck's constant and c is the speed of light in vacuum. Band-to-band absorption takes place only if $E_{ph} \geq E_C - E_V$, as no allowed energy states exist in between E_C and E_V with the so-called bandgap $E_G = E_C - E_V$. E_G of crystalline silicon is determined to be around 1.12 eV at 300K [26]. The excitation of an electron from E_V to E_C leaves behind a hole (positively charged elementary particle), creating an electron and a hole. If the energy of the photon is less than E_G, it is transmitted through the material without creating charge carriers (i.e., electrons and holes). For indirect bandgap materials such as crystalline silicon, in the case $E_{ph} > E_G$ the excess energy is converted to vibrational energy in the phenomenon known as thermalization. In other words, absorption of light in semiconductor materials is dependent on the wavelength of the light hitting its surface.

The *Beer-Lambert* law uses the absorption coefficient α which is a material property that describes the decrease of the incident light intensity I_0 per unit of material length z [27] by

$$I_L(z) = I_0(1 - R_L)\, exp\,(-\alpha z)\,, \tag{2.2}$$

where R_L is the dimensionless reflection coefficient which describes the fraction of reflected light intensity to that of the incident light.

The value is dependent on λ of the incident light. Moreover, the penetration depth δ_p is in turn the inverse of α and describes the position in the material at which the intensity of the incident light I_L reaches $1/e$ of its initial incident intensity I_0. The α and δ_p as a function λ for silicon at a constant temperature $T = 300$ K are plotted in Fig. 2.3. High-energy photons (e.g., blue light) from the incident light are absorbed near the surface. Photons with less energy (e.g., red light) get absorbed in deeper positions of the silicon substrate. Non-absorbed photons get transmitted out of the sample in case the sample is not accordingly thick enough.

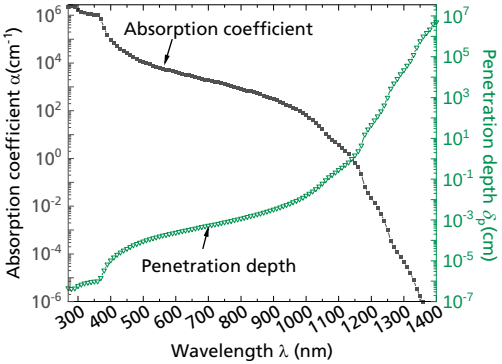


Fig. 2.3. The wavelength-dependent absorption coefficient α and the penetration depth δ_p of incident light in crystalline silicon at $T = 300$ K (data from Ref. [33]).

2.3 Basic functioning principle of silicon solar cells

The fundamentals of crystalline silicon solar cells and their operational principle are published in the following books [25, 27, 34], from which the content of the sections 2.4, 2.5, and 2.6 is derived (unless stated otherwise). For the functionality of the device, (i) generation, (ii) separation, and (iii) collection of charge carriers (i.e., electrons or holes) are required. The crystalline silicon solar cell is a diode featuring an emitter (in this case a highly-doped n-type n^+-emitter) and a base (in this case p-type); see Fig. 2.4. As mentioned, when light of sufficient energy hits the semiconductor, it is absorbed and an electron as well as a hole are generated. An antireflection coating, i.e., in this case silicon nitride (SiN_X), as well as textured surfaces decrease reflection aiming for higher photogenerated currents. However, the generated electrons and hole are in meta-stable states where recombination prior to any form of power generation occurs if no separation of charge carriers is induced (radiative and non-radiative charge carrier recombination types are discussed in section 2.5.2). The charge carriers are spatially separated at the pn-junction, particularly in the space charge region (SCR). As a result, charge carriers of different polarities flow in opposing directions. In case of solar cells with p-type base and n^+-emitter, electrons migrate to the front while holes flow to the rear. The charge carriers are then collected by the metal contacts (e.g., silver on the front and aluminum on the rear). Recombination after flowing through the electrical load occurs at the metal-silicon contact.

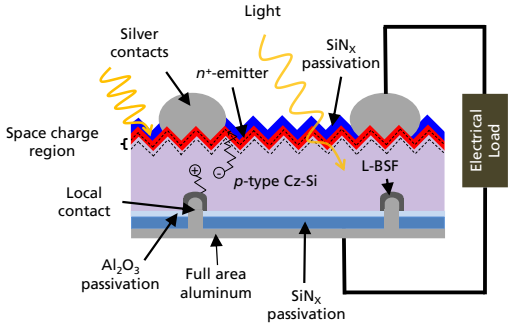


Fig. 2.4. Schematic cross-section of a crystalline silicon passivated emitter and rear cell (PERC) device connected to an electrical load. The cell features a p-type base, n^+-emitter capped by SiN_x passivation layer. The rear side consists of the dielectric layers silicon dioxide (SiO_2), aluminum oxide (Al_2O_3), and SiN_X. The rear side features a full-area aluminum that contacts the base locally creating a local back surface field (L-BSF). The PERC cell structure was first published in Ref. [8]. The front side is contacted by a silver metal contact grid.

The recombination of charge carriers prior to collection leads to drops in cell efficiencies.

2.4 Equivalent circuit of a real solar cell

2.4.1 One- and two-diode models

The similarity in the structure of the crystalline silicon solar cell to that of a pn-junction silicon diode allows the description of its electrical functionality in terms of diode current-voltage (IV) characteristics. In an illuminated ideal solar cell, the current density as a function of voltage $j(V)$ is described by the one-diode model

$$j(V) = j_0 \left[exp\left(\frac{qV}{n_{i1} k_B T} \right) - 1 \right] - j_{ph}, \tag{2.3}$$

where j_{ph} stands for the photogenerated current density. The variables q, k_B, and T correspond to the elementary charge, *Boltzmann* constant, and device temperature, respectively. In the case of an ideal diode, the ideality factor n_{i1} is equal to 1. When non-ideal injection-dependent losses are neglected, the recombination at the emitter and the base can be described by the diode's dark saturation current density j_0.

However, crystalline silicon solar cells encounter additional losses not described in the ideal one-diode model. These include parasitic electrical losses in series resistance r_S (briefly explained in section 2.5.3) in addition to shunt resistance (or parallel resistance) r_p losses. Additionally, non-ideal injection-dependent losses are neglected in the one-diode model and the SCR recombination losses are not described. For this reason, the two-diode model (described in Refs. [35, 36]) is derived, since it includes the aforementioned losses; see Fig. 2.5 for an equivalent electrical circuit diagram.

The inclusion of an additional second diode (D2) with a theoretical ideality factor of $n_{i2} = 2$ and the consideration of the area-decoupled r_S, r_p is translated in the $j(V)$ equation as follows,

$$j(V) = j_{01}\left[exp\left(\frac{q(V-jr_S)}{n_{i1}k_BT}\right)-1\right] + j_{02}\left[exp\left(\frac{q(V-jr_S)}{n_{i2}k_BT}\right)-1\right] + \frac{V-jr_S}{r_p} - j_{ph}. \tag{2.4}$$

Like the one-diode model j_0, the first diode's (D1) dark saturation current density j_{01} considers emitter and base recombination having $n_{i1} = 1$. Recombination losses different from "ideal behavior" are then designated in the D2 dark saturation current density j_{02}. These include injection-dependent and SCR defect recombination that are relevant at low voltage levels.

2.4.2 Solar cell output parameters

To obtain the energy conversion efficiency η of a solar cell, the IV characteristics of the device are required. The IV measurements are performed under well-defined standard test conditions (STC) [31], that specify the

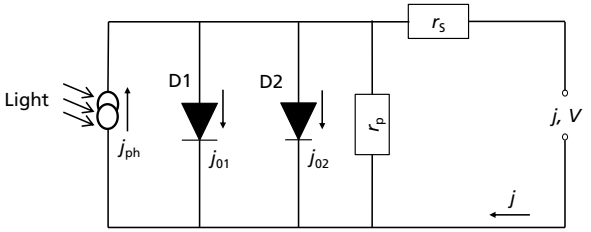


Fig. 2.5. The equivalent electrical circuit diagram of a solar cell device following the two-diode model shown in equation (2.4). The figure is redrawn and adapted from Ref. [25].

measurements conditions. From the illuminated IV measurement, STC-defined incident light features an air mass 1.5 global spectrum (AM1.5G) irradiance with a power density $G = 1000\ \mathrm{W/m^2}$ [37]. The measurement is done by determining the current as function of varying applied voltage. The temperature during the measurement is $T_{\mathrm{STC}} = 25°\mathrm{C}$. From the illuminated IV curve, output parameters like the open-circuit voltage V_{OC}, the short-circuit current density j_{SC}, and the maximum power point (mpp) are extracted; see Fig. 2.6. The dark IV measurement allows the derivation of the r_{S}, r_{p}, j_{01}, and j_{02} by fitting the two-diode model in equation (2.4) to the semi-logarithmic log(IV) curve. As a result, at lower voltages j_{02} and r_{p} values are extracted, while r_{S} and j_{01} are obtained at higher voltages.

Referring to equation (2.4), at an applied voltage $V = 0$ mV the device's j_{SC} (highest j value) is attained, where $j_{\mathrm{SC}} = -j_{\mathrm{ph}}$ (considering $r_{\mathrm{S}} = 0\ \Omega\mathrm{cm^2}$). The result can be switched to positive since the curve can also be drawn in the first quadrant. Conversely, at open-circuit voltage when $j = 0\ \mathrm{mA/cm^2}$, V_{OC} can be written as

$$V_{\mathrm{OC}} = \frac{k_{\mathrm{B}}T}{q} \ln\left(\frac{j_{\mathrm{SC}}}{j_{01}} + 1\right), \tag{2.5}$$

where j_{02} and r_{p} are considered negligible and infinite, respectively. Since the IV measurement temperature is well-defined at $T_{\mathrm{STC}} = 25°\mathrm{C} = 298$ K,

$$\frac{k_{\mathrm{B}}T_{\mathrm{STC}}}{q} = V_{\mathrm{Th}} = 25.8\ \mathrm{mV}. \tag{2.6}$$

Based on equation (2.5), the dependency of V_{OC} on j_{SC} and j_{01} is clear. In other words, for higher V_{OC} values higher photogenerated current and/or lower recombination levels are required.

An additional performance indicator of a solar cell is the fill factor *FF*. It is the ratio of the power density at maximum power point p_{mpp} to the product of j_{SC} and V_{OC}

$$FF = \frac{j_{\mathrm{mpp}} V_{\mathrm{mpp}}}{j_{\mathrm{SC}} V_{\mathrm{OC}}}. \tag{2.7}$$

The *FF* is deduced from the illuminated IV curve such that j_{mpp} and V_{mpp} stand for the current density and voltage at maximum power point, respectively.

An ideal fill factor FF_0 is derived such that the value is independent from parasitic resistance effects ($r_S = 0\ \Omega\text{cm}^2$), leakage currents (infinite r_p), and no second diode contribution ($j_{02} = 0\ \text{nA/cm}^2$) is considered [38]. Taking the normalized voltage $v_{OC} = V_{OC}/V_{Th}$ into account, the FF_0 is

$$FF_0 = \frac{v_{OC} - \ln(v_{OC} + 0.72)}{v_{OC} + 1}. \tag{2.8}$$

This empirically verified expression is dependent on V_{OC} and considers only the ideal diode dark saturation current density j_{01}.

Apart from illuminated IV measurement results, V_{OC} values can be attained by SunsV_{OC} measurements [39, 40]. This technique is practically a currentless method that leads to the open-circuit measurements of the device at varying irradiances. At 1 suns (around $G = 1000\ \text{W/m}^2$), the V_{OC} is extracted. The operating points at different irradiances of the decaying flashlight and an approximate j_{SC} value (i.e., given and not measured) form what is called, a pseudo IV curve. This curve describes the IV characteristics of the device without including r_S contributions, which also leads to the extraction of the r_S-free pseudo fill factor pFF. When compared to one another, the different fill factors: FF, pFF, and FF_0 are useful for the approximation of solar cell losses. For instance, FF losses caused by r_S can be estimated by the difference $pFF - FF$ [41]. Whereas fill factor losses due to $FF_0 - pFF$ can be attributed to low r_p and high SCR recombination. The latter is described by j_{02} values [42].

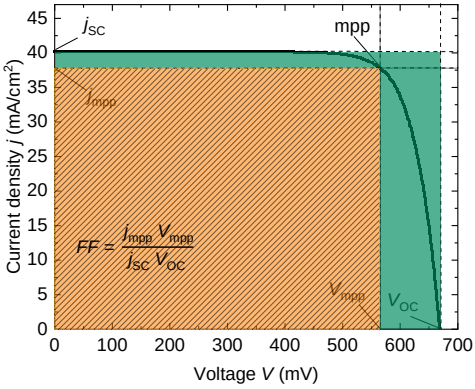


Fig. 2.6. Illuminated current-voltage (IV) curve of a measured solar cell in forward bias from which device performance output parameters are extracted. The performance output parameters are labeled in the figure. The fill factor is the ratio of $j_{mpp}\,V_{mpp}$ (orange area with a diagonally-dashed pattern) to $j_{SC}\,V_{OC}$ (orange and green area).

Returning to the main definition, energy conversion efficiency η of a solar cell signifies the ratio of generated electric power density (or maximum power point) p_{mpp} to the power density (or irradiance) G of the incident light. Equation (2.7) can be used to obtain η in terms of j_{SC}, V_{OC}, FF, and G.

$$\eta = \frac{p_{\mathrm{mpp}}}{G} = \frac{j_{\mathrm{mpp}} V_{\mathrm{mpp}}}{G} = \frac{j_{\mathrm{SC}} V_{\mathrm{OC}} FF}{G}. \tag{2.9}$$

In the case of bifacial solar cell devices (i.e., cells that capture light from both the front and rear sides), the term: output power density p_{out}, is used to express the device performance under bifacial illumination conditions. In this case, p_{out} includes both the front and the rear side measurement results. According to the explanation presented in Ref. [43], at a monofacial irradiance of 1000 W/m^2 the value of p_{out} is identical to η. Although no standard testing conditions for bifacial solar cells were published at the time of the dissertation start in 2017, the monofacial STC measurement can still be used to describe the performance of the cell from each the front and the rear side. Therefore, one side at a time is illuminated for the measurement of bifacial solar cells in this work. The approximation of the bifacial p_{out} is then attained by considering a scenario where the front side irradiance is $G = 1000$ W/m^2, while the rear side irradiance is $G = 100$ W/m^2 (10% of the front side irradiance). Such a calculation is also adopted in Ref. [44]. The p_{out} can then be calculated by adding the contributions of the front and the rear sides

$$p_{\mathrm{out}} = \eta_{\mathrm{FS}} + (0.1)\eta_{\mathrm{RS}} , \tag{2.10}$$

where η_{FS} and η_{RS} are the front side and rear side efficiencies attained at STC, respectively.

Another performance indicator commonly used for bifacial solar cells is the bifaciality factor β. It is obtained from the ratio of η_{RS} and η_{FS}

$$\beta = \frac{\eta_{\mathrm{RS}}}{\eta_{\mathrm{FS}}}. \tag{2.11}$$

The result of the ratio is commonly presented as a β percentage.

In this dissertation, the IV and the SunsV_{OC} measurement techniques are main electrical characterization methods accompanying the development of the solar cells.

2.4.3 Current-voltage measurements and contacting techniques

As discussed in section 2.4.2, IV characterization is necessary to determine solar cell output parameters, such as the energy conversion efficiency η. The IV measurements of solar cells of varying sizes takes place in an IV cell tester measurement setup that is illustrated in Fig. 2.7. In the case of full wafer-sized cells (i.e., pseudo square edge length of 156.75 mm) or half cells, the handling of the cells is automated. The cells are handled by means of vacuum suction pads from cell carriers onto a rotating round cell-holding table. The cell is then transported/rotated into the IV measurement chamber for electrical contacting; for details about the cell tester refer to Ref. [45]. Consequently, the n-type electrodes and the p-type electrodes of the cell are contacted separately by means of contacting probes. The measurement takes place by illuminating the cell and recording the cell's current and voltage. A reference cell monitors the incident irradiance, while a pyrometer monitors the temperature of the cell during the measurement. Measurements are taken at STC conditions featuring an irradiance $G = 1000\ \mathrm{W/m^2}$ and a spectrum with an air mass coefficient AM1.5G [37]. The setup ensures a negligible reflection back into the cell in the relevant wavelength range $300\ \mathrm{nm} \leq \lambda \leq 1100\ \mathrm{nm}$, making it suitable for the monofacial (i.e., one side illuminated) measurement of bifacial solar cells.

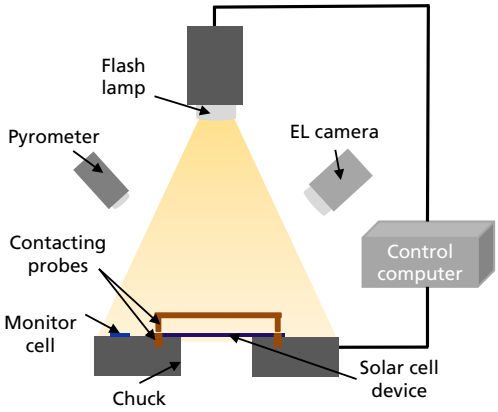


Fig. 2.7. An illustration of the IV measurement cell tester setup. The tool consists of a flash lamp to generate incident light with a defined spectrum and intensity. The contacting of the cell is performed by contacting probes. The reference cell monitors the irradiance levels during the measurement, while the pyrometer records the temperature. Additionally, a camera captures electroluminescence (EL) images for the detection of local defects. The figure is redrawn and adapted from Ref. [45].

For cells with front side and rear side contacts with opposing polarities, the measurement contacting takes place by IV-pin arrays on each of the sides. The number of used IV-pin arrays on each of the sides is dependent on the number of busbars on each side of the cell, such that each busbar is contacted by an IV-pin array. The pin array consists of 33 pins (22 for the current and 11 for the voltage). For busbarless cells, *Grid*$^{\text{TOUCH}}$ contacting units are used [46]. One of the cell sides (i.e., the illuminated side) is contacted by 35 contacting wires (i.e., 30 for the current, 5 for the voltage) inserted in a frame. The other side (i.e., non-illuminated side) is contacted by 35 conductive contacting strips built in a chuck.

Another characterization method that requires the electrical contacting of cells is the electroluminescence (EL) imaging [47, 48], which is also integrated in the cell tester. During the measurement, a forward-bias voltage is provided across the cell, making the cell act as a light-emitting diode. This allows the visual local characterization of recombination centers by means of an electroluminescence-detecting infrared camera (EL camera). Low detected EL signals imply regions with high defects. The detected defects can be caused by cell cracks and/or by metallization defects, such as finger breakages and inhomogeneities in the metal-semiconductor contacting or non-radiative recombination.

2.4.4 SunsV_{OC} measurements and contacting method

The SunsV_{OC} measurement technique is a characterization method used to provide solar cell parameters of metallized cells (i.e., cells after contacts are formed) [39, 40]. Throughout this work, the SunsV_{OC} measurement is used as a characterization method, since it provides V_{OC} and pseudo fill factor *pFF* values, which are necessary for the comprehension of process influence on fabricated cells at different post-metallization stages. The SunsV_{OC} measurement functions by measuring the V_{OC} of the cell at varying irradiances (i.e., irradiance-dependent V_{OC} measurement). The tool used throughout this work is the *Sinton Instruments* SunsV_{OC} stage [49]. A sketch of the measurement setup is illustrated in Fig. 2.8. It includes a flashlamp for the illumination, a point probe for contacting, a reference cell to monitor the irradiance, and a conductive chuck and stage on which the cells' non-illuminated sides are contacted. To obtain a measurement, the cell is illuminated by the flash lamp with decaying irradiance.

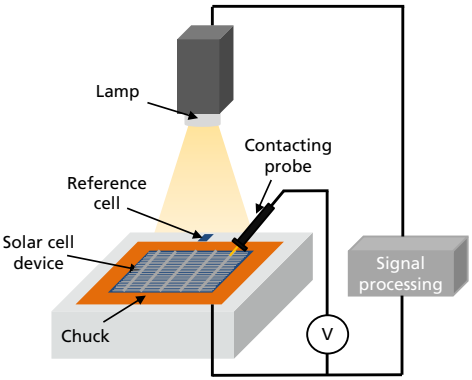


Fig. 2.8. An illustration of the SunsV_{OC} measurement setup. The tool consists of a flash lamp to generate excess charge carriers while the contacting probe and the chuck contact the solar cell and measure the voltage across it. The reference cell monitors the irradiance levels during the measurement. Sketched by referring to the setup photograph and information in Ref. [49].

During the measurement, the illuminated side of the cell is contacted by the contacting probe, while the rear side is contacted by the conductive chuck.

2.5 Loss mechanisms and their effects on solar cell output parameters

In this section, the common optical and electrical loss mechanisms in silicon solar cells are depicted alongside their main effect on solar cell output parameters. Charge carrier defect recombination at the surface receives extra focus for its relevance to explain the physical phenomenon behind edge recombination.

2.5.1 Optical losses

In addition to the optical losses derived from crystalline silicon properties (i.e., transmission and thermalization losses discussed in section 2.2), reflective losses due to the metallization are very predominant. Shading losses resulting from the presence of metal contacts (fingers and busbars) are a major source of optical losses. These structures cover active cell areas which are potential light capturing areas. Metal contact grids on the light trapping side (or sides) of cells are designed with a reduced metallization fraction (percentage of metal coverage to cell area) with the aim of reduc-

ing shading losses without contributing to electrical resistive losses (i.e., fingers with high aspect ratios [50–52]). On the other hand, light impinging on the cell might also get reflected from the metal-free active cell area. This occurs due to the radical change of refraction indices at the interface of air and silicon (including other additional thinner layers in between). As a method to increase light trapping, wafer surfaces are textured to form pyramidal structures [53, 54]. Additionally, antireflection coatings from dielectric materials such as SiN_X and SiO_X are deposited to create a more gradual transition of refractive indices (this is apart from their advantageous qualities in surface passivation that will be discussed in section 2.7).

For a common simplification, optical losses lead to lower short-circuit current density j_{SC} values. A low j_{SC} can in turn lead to a decrease in open-circuit voltage V_{OC} both of which reduce the energy conversion efficiency η of the solar cell.

2.5.2 Charge carrier recombination losses

During the generation process, excitation creates electrons and holes due to band-to-band transitions. A leading cause of the loss in cell efficiency is the recombination of electrons and holes that aims to restore the semiconductor's equilibrium state after generation. In other words, recombination is the opposing phenomena to the creation of photogenerated excess charge carriers. The properties of a semiconductor material such as the bandgap, impurities, doping level, and crystal lattice defects influence the type and rate at which excess charge carriers recombine (for a detailed explanation about charge carrier recombination please refer to Refs. [31, 55, 56] from which this section is derived). Understanding recombination mechanisms is possible by measuring the average time it takes for an electron and a hole to recombine after generation. This is referred to as recombination lifetime τ expressed as

$$\tau = \frac{\Delta n}{R_{\text{rec}}} = \frac{\Delta n}{R_{\text{tot}} - G_{\text{th}}}, \tag{2.12}$$

where R_{rec} stands for the net recombination rate (i.e., total recombination rate R_{tot} subtracted by the charge carrier generation in thermal equilibrium G_{th}). Additionally, excess carrier concentration of electrons Δn and holes Δp are equal at the equilibrium state.

The main recombination mechanisms present in crystalline silicon are either intrinsic: radiative [57, 58] and Auger recombination [59], or extrinsic: Shockley-Read-Hall (SRH) recombination [60, 61], also known as defect recombination. Moreover, surface recombination (also at the edge) is a particular type of an extrinsic SRH recombination.

Radiative recombination

Radiative band-to-band recombination is explained by the drop of a conduction band electron to an unoccupied state of the valence band by releasing the excess energy as an emitted photon; see Fig. 2.9(a). In other words, it is analogous to the direct reverse mechanism of the photogeneration. Since silicon is an indirect bandgap material, the energy-momentum conservation requires an additional contribution of a phonon. For that reason, radiative recombination is more common in direct bandgap materials. Nevertheless, it still is present in silicon and can be described by

$$\tau_{\mathrm{rad}} = \frac{1}{B_{\mathrm{rad}}(n_0+p_0+\Delta n)}, \tag{2.13}$$

where B_{rad} stands for the radiative recombination coefficient, n_0 and p_0 quantify the thermal equilibrium electrons and holes concentrations, respectively. Moreover, the expression implies that for a low excess carrier concentration (low injection) Δn, τ_{rad} depends on the doping concentration. Conversely, for high excess carrier concentration (high injection) the dependency of τ_{rad} shifts to be on Δn.

Auger recombination

The dominant intrinsic recombination in silicon is known as band-to-band Auger recombination. In this mechanism, excess energy from the electron-hole annihilation is transferred to another additional electron or a hole, which implies the participation of three charge carriers; see Fig. 2.9(b). In the case of the involvement of an additional electron, the third charge carrier is excited to a higher band level, where it releases excess energy as lattice vibrations (thermalization); specifically abbreviated as electron-electron-hole (eeh) interaction. Analogously, when the energy is transferred to a hole as the third carrier, the hole relaxes in a deeper band level of the valence band and the phenomena is abbreviated electron-hole-hole (ehh) interaction.

In high injection conditions, and referring to the traditional theory explained in Ref. [62], Auger lifetime $\tau_{\mathrm{Au,h}}$ is approximated by

$$\tau_{\mathrm{Au,h}} = \frac{1}{(C_n+C_p)\Delta n^2}, \tag{2.14}$$

where C_n+C_p is the sum of electron and hole Auger coefficients, respectively (values found in Ref. [63]). Moreover, under low injection conditions, taking the example of a p-type material, $\tau_{\mathrm{Au,l}}$ is expressed as

$$\tau_{\mathrm{Au,l}} = \frac{1}{C_p N^2}, \tag{2.15}$$

where N is the dopant concentration. Equation (2.14) shows that under high injection conditions the dependency of the Auger lifetime is on the variable Δn^2, whereas in low injection conditions it solely depends on the variable N^2. For an overview of the present Auger recombination theories in silicon please refer to Ref. [31].

Shockley-Read-Hall recombination

Shockley-Read-Hall (SRH) recombination is an extrinsic type of recombination that strongly depends on defects caused by the imperfection of the crystal. Defects include impurities in the bulk and lattice dislocations. These defects can create energy levels in the "forbidden" region of the bandgap known as traps or trap states with an energy level E_{t}, leading to the facilitated recombination; see Fig. 2.9(c). The charge carrier, e.g., free electron, is first trapped in the defect state thus increasing its probability of recombining with a carrier of the other type (e.g., hole). Excess energy is then released in the form of phonons and photons.

Based on SRH statistical theory, trap recombination rates can be calculated, from which the SRH lifetime τ_{SRH} is derived. τ_{SRH} in the bulk is expressed as

$$\tau_{\mathrm{SRH}} = \frac{\tau_{\mathrm{p0}}(n_0+n_1+\Delta n) + \tau_{\mathrm{n0}}(p_0+p_1+\Delta n)}{n_0+p_0+\Delta n}, \tag{2.16}$$

where τ_{n0} describes the time constant for electron's capture, having electron capture cross-section σ_{n}, average thermal velocity of carriers v_{th}, and traps density N_{t} (similarly τ_{p0}, σ_{p}, v_{th}, and N_{t} stand for the time

constant, capture cross-section, charge carrier thermal velocity, and traps density respectively for holes). τ_{n0} and τ_{p0} can be calculated by

$$\tau_{n0} = \frac{1}{\sigma_n \, v_{th} \, N_t}, \quad \text{and} \quad \tau_{p0} = \frac{1}{\sigma_p \, v_{th} \, N_t}. \tag{2.17}$$

Meanwhile n_1 and p_1 are obtained by

$$n_1 = N_C \, exp\left(\frac{E_t - E_C}{k_B T}\right) \quad \text{and} \quad p_1 = N_V \, exp\left(\frac{E_V - E_t}{k_B T}\right). \tag{2.18}$$

where N_C corresponds to the density of states for the conduction band and N_V represents the density of states for the valence band. The equation implies that a reduction in the trap density N_t causes an increase in τ_{SRH}. SRH recombination is the most relevant recombination mechanism present in terrestrially-deployed silicon solar cells.

Surface recombination

Apart from the SRH recombination that occurs in the bulk; surface recombination, as the name states, is a specific type of defect recombination that takes place at semiconductor surface defects. In the case of silicon, surface valence electrons are unable to form covalent bonds with neighboring atoms due to the discontinuity of the crystal lattice, which leads to defects known as "dangling bonds". These defects can be described

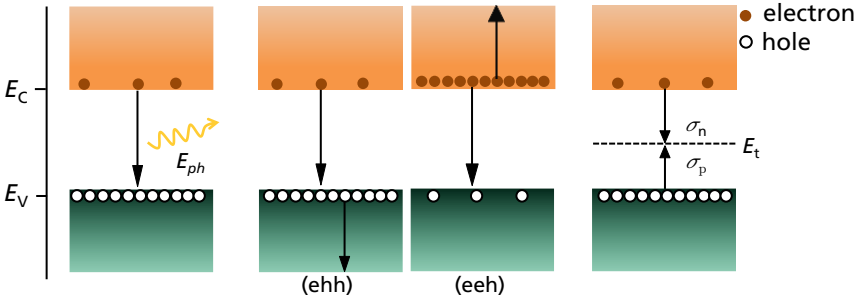


Fig. 2.9. Energy band diagram schematic in which conduction and valence band edges E_C and E_V are shown respectively; the main recombination mechanisms in crystalline silicon: (a) Radiative recombination where excess energy is released as a photon; (b) Auger where excess energy is transferred to an electron (*eeh*) or a hole (*ehh*), and (c) Shockley-Read-Hall recombination showing the capture cross-sections for electrons and holes including the energy level E_t created by the defect. The figure is redrawn from Ref. [31].

in terms of interface defect states $D_{it}(E)$ covering the wide range of energy defects within the bandgap. Assuming that defects are independent trapping centers, and according to the SRH formulism, *Eades* and *Swanson* calculate the surface recombination rate per unit area R_{sur} [64]. It is described in terms of the electron and hole concentrations at the surface denoted by n_s and p_s, respectively. R_{sur} is defined by

$$R_{sur} = v_{th}\,(n_s p_s - n_{ieff}^2)\int_{E_V}^{E_C} \frac{D_{it}(E)\,dE}{\dfrac{n_s + n_1(E)}{\sigma_p(E)} + \dfrac{p_s + p_1(E)}{\sigma_n(E)}}\,. \tag{2.19}$$

From R_{sur}, the surface recombination velocity S_r is approximated by

$$S_r = \frac{R_{sur}}{\Delta n}. \tag{2.20}$$

From the equations (2.19) and (2.20) it is evident that the reduction of surface recombination velocity is attained by the reduction of $D_{it}(E)$ commonly known as chemical passivation. Moreover, the reduction in n_s or p_s would also lead to the decrease of S_r by what is called the field effect passivation [65]. For the development of solar cells, decreasing SRH recombination is of vital relevance as it persistently affects solar cell output parameters, particularly the V_{OC}.

2.5.3 Resistive losses

As discussed in section 2.4.1, a real solar cell exhibits series and parallel resistances, r_S and r_p, respectively. The components of the ohmic r_S can be summarized by contributions from: (i) the base resistivity of the doped wafer base ρ_B, (ii) the emitter sheet resistance R_{sh}, (iii) the front and rear contact resistivity to the metal electrodes $\rho_{C,FS}$ and $\rho_{C,RS}$, in addition to (iv) lateral resistivity in the electrodes $\rho_{L,FS}$ and $\rho_{L,RS}$ (for details of series resistance calculation methods please refer to Ref. [22]).

It is commonly known that shunting losses or leakages at the *pn*-juntion reduce mainly the pseudo fill factor *pFF* and hence the energy conversion efficiency η. Developing a highly efficient solar cell requires the reduction

of r_S losses by adapting its components, while keeping r_p at acceptable high levels.

2.6 Charge carrier recombination characterization

As discussed in section 2.5.2, the lifetime of electrons and holes is a decisive parameter in determining and further developing the quality of solar cell devices. In semiconductors, the recombination mechanisms coexist and the total lifetime τ includes components of each mechanism. To describe measurement-based lifetime results, the term effective lifetime τ_{eff} is used. Knowing that the total recombination is the sum of recombination rates of each contributing mechanism, τ_{eff} is calculated by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Surface}}. \tag{2.21}$$

Splitting the contributions of the bulk and surface recombination mechanisms, as considered in Ref. [66] leads to the expression

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{Surface}}. \tag{2.22}$$

By the choice of a highly pure substrate such as Fz-Si (very high bulk τ_{SRH}), the reduction of τ_{bulk} to its intrinsic components is typically considered [59].

Especially in this work, $\tau_{Surface}$ is of high interest because the experimental work deals with reducing the surface recombination. *Sproul* [67] introduces the following expression

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W}, \tag{2.23}$$

where S_{eff} stands for the effective surface recombination velocity of one surface of a symmetrically-processed lifetime sample and W is the wafer thickness. This expression is commonly used to calculate S_{eff} particularly in cases where $S_{eff}W/D < 0.25$ and D being the minority carrier diffusivity.

Moreover, the effective diffusion length L_{eff}, which is the average distance a carrier covers from generation until recombination, can be calculated in relation to τ_{eff} and D,

$$L_{\text{eff}} = (\tau_{\text{eff}}\, D)^{1/2}\,. \tag{2.24}$$

A high L_{eff} indicates a higher probability of collection of the carrier also due to the higher τ_{eff}. Both τ_{eff} and L_{eff} are indications of material quality and are used as characterization measures for the development of solar cell materials and processes.

2.6.1 Photoconductance decay measurement technique

For the determination of τ_{eff}, the photoconductance decay measurement technique [68] is widely used. The method exploits the relation between the time-dependent excess carrier concentration $\Delta n(t)$ and the time-dependent excess photoconductance $\Delta\sigma(t)$. The relation is expressed as

$$\Delta n(t) = \frac{\Delta\sigma(t)}{qW(\mu_{\text{n}} + \mu_{\text{p}})}, \tag{2.25}$$

with q being the elementary charge, W being the wafer thickness, and $\mu_{\text{n}} + \mu_{\text{p}}$ being the sum of electron and hole mobilities (studied for different doping levels and carrier concentrations in Refs. [69–72]).

The measurements are performed using the *Sinton Instruments WCT-120* lifetime tester [73] which encompasses a flashlight and measurement chuck; see Fig. 2.10. An integrated radio frequency-bridge circuit, that operates in the MHz-range, including an inductive coil is built within the chuck. The sensor area has a diameter of 40 mm. During flashing, a calibrated reference solar cell monitors the light intensity; meanwhile the circuit's voltage signal is recorded in a contactless measurement.

Depending on the measured sample, if a short light pulse is used, excess charge carrier generation can be completed after the pulse decays. As a result, τ_{eff} for the so-called transient mode is calculated by using the time-dependent equation

$$\tau_{\text{eff}}(\Delta n(t)) = -\frac{\Delta n(t)}{\dfrac{d\Delta n(t)}{dt}}. \tag{2.26}$$

However, this transient measurement mode is more applicable to lifetime samples with rather high τ_{eff}. Moreover, τ_{eff} can also be measured by the quasi-steady state photoconductance (QSSPC) method in the generalized mode [74]. Different from the transient mode, measuring in the generalized QSSPC mode requires the determination of $G(t)$, which is done by monitoring the flash and having the material's absorption fraction [75]. This is to ensure that the generation still occurs during the data acquisition. τ_{eff} can then be expressed by keeping the generation term $G(t)$,

$$\tau_{\text{eff}}(\Delta n(t)) = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}}. \tag{2.27}$$

According to *Rein* [55], samples with $\tau_{\text{eff}} > 200$ µs can be accurately measured in the transient mode while the generalized mode yields accurate results for samples with $\tau_{\text{eff}} < 200$ µs.

From the QSSPC measurement, the implied open-circuit voltage $\text{i}V_{\text{OC}}$ of a *p*-type non-metallized precursors (wafer with passivation layers) can be acquired by an expression derived from *Sinton* and *Cuevas* [68],

$$\text{i}V_{\text{OC}}(\Delta n) = \frac{k_{\text{B}}T}{q} \ln\left(\frac{(N_{\text{A}} + \Delta n)\Delta n}{n_{\text{ieff}}^2}\right), \tag{2.28}$$

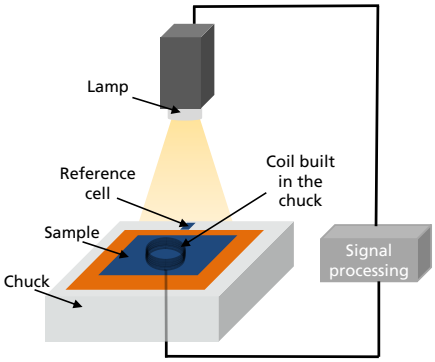


Fig. 2.10. Schematic illustration of the photoconductance decay measurement setup. The substrate is illuminated by a flash lamp thus generating excess charge carriers. This leads to a change in the sample conductance measured by the integrated coil. Meanwhile the reference cell detects the irradiance which is also used to deduce the generation rate. The figure is redrawn from Ref. [42].

where n_{ieff}^2 is the square of the intrinsic carrier concentration, N_{A} the doping concentration in the p-type substrate, and Δn the excess charge carrier density. The expression can be used analogously for n-type samples.

The iV_{OC} value offers an estimate of pre-metallization open-circuit voltage values at different injection levels. In the case where the iV_{OC} at equivalent irradiance of 1000 W/m^2 is extracted, the subtraction i$V_{\mathrm{OC}} - V_{\mathrm{OC}}$ estimates the V_{OC} loss induced by the metallization assuming no significant variations in material and pre-metallization processes' quality.

In this work, QSSPC measurements are often used to obtain τ_{eff} values. Additionally, precursors' iV_{OC} values are also determined by means of this measurement technique.

2.6.2 Photoluminescence imaging technique

The photoluminescence (PL) imaging technique is a method to capture the light emitted by radiative recombination in a sample after exiting it using a source [47, 76, 77]. Sample defects lead to high levels of recombination and low charge carrier densities. Consequently, the radiative recombination at those locations is also low. According to Refs. [78, 79], the decay of the excess carrier concentration Δn is related to the PL intensity φ_{PL} by

$$\varphi_{\mathrm{PL}} = A_{\mathrm{opt}} B_{\mathrm{rad}} \Delta n (\Delta n + N), \tag{2.29}$$

with a setup/sample dependent optical factor A_{opt}, radiative recombination coefficient B_{rad}, and doping concentration N.

The concept comes into practice in a PL measurement setup; see Fig. 2.11. The tool includes an illumination source (laser or a light emitting diode array), and a photodetector (i.e., charged coupled device (CCD) camera) responsible for measuring the PL signal. An additional detector monitors the generation rate. The *Fraunhofer ISE* "*PL–Modulum*" is the tool used in this work and it features a laser with a wavelength $\lambda = 808$ nm and rated power $P_{\mathrm{r}} = 120$ W. The long-pass filter ensures that no laser radiation is captured by the CCD. Further details about the setup can be found in Ref. [80]. The method allows for the determination of local defects in the substrate bulk or the surface, corresponding to detected low PL signal counts $\varphi(\mathrm{x})$, whereas regions with high signals are attributed to regions with lower defects.

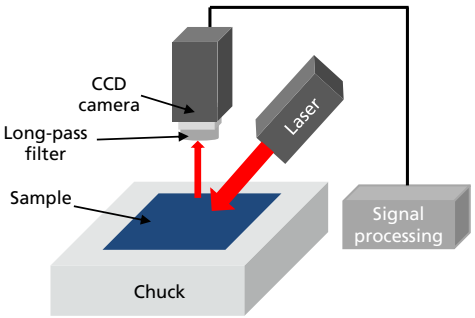


Fig. 2.11. Schematic illustration of the PL imaging measurement setup. The substrate is first illuminated by an excitation laser beam. The CCD camera then detects the filtered photons emitted (radiated) from the substrate at a specific period of time. The figure is redrawn by referring to Refs. [47, 76].

2.7 Crystalline silicon surface passivation fundamentals

As discussed in section 2.5.2, surface recombination is a specific case of SRH recombination when an abrupt disorder in the silicon crystal lattice is present. These defects create recombination centers at the semiconductor surface that are quantified by an increase in D_{it} distributed over the bandgap. Fig. 2.12(a) shows a schematic bandgap diagram of p-type silicon exhibiting surface defects and high D_{it}. According to the SRH-formulation, two components of equation (2.19) can be targeted to reduce surface recombination. The first component is D_{it}. Reducing it requires the saturation of the dangling bonds by hydrogen or oxygen usually present in dielectric passivation layers such as silicon dioxide (SiO_2) and aluminum oxide (Al_2O_3); see Fig. 2.12(b). This mechanism is called chemical passivation. By referring to the same equation (2.19), the surface recombination can also be reduced by decreasing either n_s or p_s. This phenomenon is known as field effect passivation. It takes place by reducing carriers of one type from reaching the surface and diminishing surface recombination. This can be technically achieved by introducing fixed charges Q_f. Taking the example of p-type silicon, passivation layers that introduce negative Q_f, such as Al_2O_3, lead to band bending and the depletion of minority carriers (i.e., in this case electrons) from the surface. Fig. 2.12(c) shows a schematic band diagram of the field effect passivation in p-type silicon. Alternatively, field effect passivation can be induced by doping surfaces creating surface

fields [19], depleting carriers of a kind and reducing recombination. Apart from the surface passivation quality, passivation layers of solar cells are considered for their optical properties, stability against further processes (for e.g., firing) and durability after possible deployment [31, 81]. Some of the most studied silicon solar cell passivation layers are discussed in the following subsection.

Surface passivation materials for silicon solar cells

One of the most studied dielectric layers for the passivation of silicon is silicon dioxide (SiO_2) [31, 82] (i.e., also relevant for microelectronic transistor devices [83]). In an ambient environment, a so-called native SiO_2 grows on bare silicon following the dry oxidation reaction [25, 84, 85]

$$Si + O_2 \rightarrow SiO_2 . \tag{2.30}$$

This growth occurs at room temperature air, where the growth is logarithmic as a function of exposure time in air as reported in Ref. [86]. The thickness of the layers in room temperature reaches a practical maximum of around 2 nm. The reaction rate decreases with the growth of the oxide since the oxygen encounters an increasing oxide barrier for the reaction to take place [84]. Layer thicknesses of approximately 100 nm are attained during a 100 min dry oxidation at elevated temperatures of around 1050°C [84]. The growth of SiO_2 can be accelerated in a wet oxidation process by including hydrogen as a process gas leading to the reaction

$$2Si + O_2 + 2H_2O \rightarrow 2SiO_2 + 2H_2 \tag{2.31}$$

as shown in Refs. [25, 84, 85]. This type of oxidation reduces the process temperature to around 800°C that protects from the damage of the silicon bulk [87].

SiO_2 layers contribute to the silicon surface passivation mainly due to the high quality of the interface featuring D_{it} values of around $10^{10} - 10^{11}$ $eV^{-1}cm^{-2}$ [31, 64, 88–90]. The field effect passivation as a result of SiO_2 layers is rather observed to be secondary as a result of the low positive fixed charge density Q_f with values less than 5×10^{11} cm^{-2} [31, 88–90]. Very low effective surface recombination velocities S_{eff} less than 10 cm/s prove the excellent surface passivation of thermally-grown SiO_2 [31, 64, 91–93]. High quality passivation on n-type and p-type substrates with low and high doping concentrations is

proven [92, 94, 95]. It is also shown that an alneal process (i.e., combination of aluminum on SiO_2 and annealing) can attain additional improvement of the surface passivation quality of SiO_2 [96].

Amorphous silicon nitride (SiN_X) layers are commonly used dielectric materials acting as antireflection coatings (ARC) of silicon solar cell illuminated sides [31, 56]. Moreover, the SiN_X acts as an excellent surface passivation for highly-doped n^+ surfaces (i.e., common phosphorous n^+-emitters). The SiN_X layers are deposited on silicon by means of plasma enhanced chemical vapor deposition (PECVD) which is a common technique in the industry. SiN_X layers passivate n-type (i.e., low and highly-doped) and lowly-doped p-type substrates mainly due to the positive Q_f in the order of 10^{12} cm^{-2} and an enhanced interface quality quantified by D_{it} in the order of 10^{11} $eV^{-1}cm^{-2}$ [88, 97–100]. SiN_X layers are not suitable for highly-doped p^+ surfaces [31].

Hydrogenated amorphous silicon (a-Si:H) is also used for the silicon surface passivation. The a-Si:H layers are usually deposited by PECVD technique. As a result of the very low attained D_{it} of around 10^{10} $eV^{-1}cm^{-2}$, chemical passivation is the dominating surface passivation phenomenon (i.e., no significant field effect passivation is observed) [31, 102, 103]. The functionality of a-Si:H as a passivation layer is proven on lowly and highly-doped p-type and n-type substrates [104, 105]. Nevertheless, a-Si:H layers

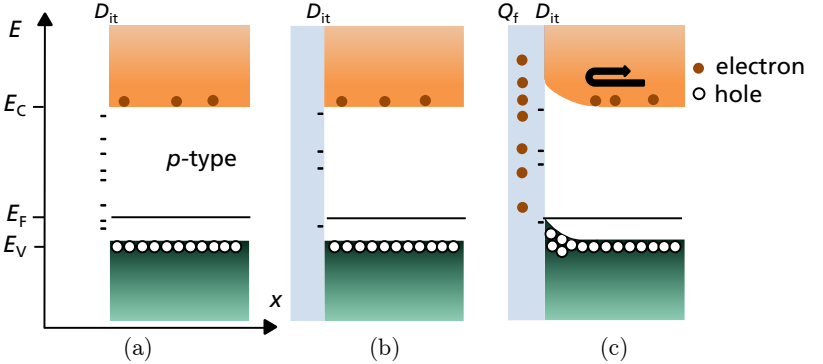


Fig. 2.12. Band diagram sketches of p-type silicon surface with (a) defects and recombination traps shown by the sign "-" and a high D_{it}. (b) chemical passivation, shown by the light blue region, occurring due to hydrogen or oxide-rich passivation layers. This leads to the reduction of D_{it}. (c) field effect passivation by the introduction of negative fixed charges Q_f using an Al_2O_3 layer at the interface leading to the depletion of electrons and accumulation of holes. E_F refers to the Fermi level. The figure is redrawn and adapted from Ref. [101].

degrade at elevated temperatures limiting their applicability in high temperature processes [106]. In addition, a-Si:H layers also feature a higher absorption coefficient compared to crystalline silicon, leading to light coupling losses in case applied on the illuminated side [107].

Surface passivation by means of Al_2O_3 dielectric layers is also very common in the fabrication of silicon solar cells [31, 108, 109]. Al_2O_3 layers can be deposited by means of atomic layer deposition (ALD), PECVD, sputtering, and atmospheric pressure chemical vapor deposition [110–113]. Still, low S_{eff} are typically attained after post-deposition annealing (also known as "activation") usually at temperatures above 400°C [105, 106]. The acceptable interface quality quantified by D_{it} values of around 10^{11} $eV^{-1}cm^{-2}$ as well as the very high negative Q_f in the order of negative 10^{13} cm^{-2} ensure excellent chemical and field effect passivation of silicon substrates [88, 97, 111, 114, 115]. Usually, this is the case for p-type and n-type samples with low doping concentrations as well as p^+-doped ones [111, 114, 116, 117]. The charge accumulation at the surface of p-type samples because of the negative Q_f of Al_2O_3 layers leads to the reduction of surface minority carrier (i.e., electrons) as shown in the schematic band diagram Fig. 2.12(c). Conversely, the negative Q_f on the lowly-doped n-type silicon leads to the depletion of majority carriers (i.e., holes) known as the surface inversion, which also leads to an effective surface passivation. Al_2O_3 layers within the necessary thicknesses are transparent in the wavelength ranges relevant for solar cells, making it suitable for deployment [118]. Apart from the application for solar cell surface passivation, Al_2O_3 is also investigated for its functionality as dielectric material in microelectronic devices [119].

Based on Refs. [88, 120], *Preu et al.* [81] provides a summary of the dielectric layers used for silicon surface passivation of solar cells. The passivation layers' D_{it} and Q_f values are shown in Fig. 2.13.

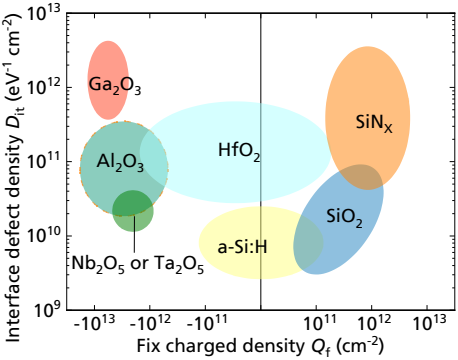


Fig. 2.13. Summary of silicon surface passivation layers and their corresponding interface defect density D_{it} and fix charge density Q_f values. Abbreviations: gallium oxide (Ga_2O_3), aluminum oxide (Al_2O_3), hafnium dioxide (HfO_2), tantalum pentoxide (Ta_2O_5), niobium pentoxide (Nb_2O_5), amorphous silicon (a-Si:H), silicon nitride (SiN_X), and silicon dioxide (SiO_2). The figure is from Ref. [81].

As an essential topic of this dissertation, chapter 6 is dedicated to the low temperature silicon surface passivation by ALD-deposited Al_2O_3 layers.

3 State-of-the-art Solar Cells and the Shingle Approach

3.1 Introduction

The first section in this chapter reviews a number of the full wafer-sized silicon solar cell device structures in industrial mass production at the start of this work in 2017. Special emphasis is put on *p*-type Czochralski-grown (Cz-Si) passivated emitter and rear cell (PERC) architectures in monofacial or bifacial design. They feature diffused emitters, screen-printed metal contacts, and dielectric layers for the passivation of the silicon surface. Additionally, commonly known cell fabrication routes and technologies are discussed. The chapter also sums up the state-of-the-art of separated and shingled silicon solar cells, known prior to the starting date of this work. Moreover, a literature review on published/available edge recombination models and characterization methods provides useful knowledge for the development and characterization of the edge-passivated bifacial shingle solar cells in this work.

3.2 PERC solar cell concepts and fabrication routes

The silicon-based photovoltaic solar cell technology has come a long way since the first diffused emitter solar cell that was demonstrated in 1954 by *Bell Laboratories* [121]. This lab-scale device that presented an energy conversion efficiency of about 6% was fabricated on an *n*-type silicon wafer featuring a boron-diffused emitter.

Throughout the decades since then, the innovative advancements in cell structures, modules, and efficiencies as well as production technologies have launched the transition of silicon-based solar cell devices from niche applications, like satellites in space, towards affordable terrestrial mainstream products. As published in the 8th edition of the *International*

Technology Roadmap for Photovoltaics (*ITRPV*) [122], at the start of this dissertation in 2017, the most widespread industrially-produced solar cell was the aluminum back surface field (Al-BSF) solar cell [123]. Nevertheless, the passivated emitter and rear cell (PERC) [8] concept was already in mass production with projections highlighting an expected yearly increase of its market share. The PERC cell architecture was first introduced in 1989 on a p-type floatzone silicon (Fz-Si) substrate with a lab-scale cell area of 4 cm^2 [8]. The cell fabrication technologies have remarkably advanced ever since, eventually paving the way for PERC cells to enter mass production [124, 125]. Different from the Al-BSF solar cell architecture, the rear side of the PERC cell includes dielectric passivation layers, such as, e.g., silicon dioxide (SiO_2) [126] already used in 1989, and later aluminum oxide (Al_2O_3) [127] capped by silicon nitride (SiN_X) [100]. Alternatively, a layer stack consisting of silicon oxynitride [128] and SiN_X have also been used as rear side passivation layers [129]. In other words, the PERC structure includes dielectric passivation layers both on the front side and the rear side. The presence of these passivation layers reduces the recombination of charge carriers at the wafer surfaces leading to increased cell efficiencies. Fig. 3.1(a) depicts a typical cross-section of a p-type silicon PERC solar cell, featuring a front side diffused n^+-type phosphorous emitter passivated by a SiN_X layer. The rear side is passivated by an Al_2O_3/SiN_X layer stack. Directly at the interface between silicon and the passivation layers, a thin SiO_2 layer is present (not shown in the figure). The front side features screen-printed and fired silver contacts that are in direct contact to the emitter, while the rear side full-area contact consists of screen-printed and fired aluminum. However, unlike the Al-BSF solar cell in which the total rear area is contacted, the rear side contacting in PERC is performed only locally. The local contact is attained by keeping the vast majority of the rear side dielectric under the metal-covered area intact. This is achieved by forming only local laser contact openings in the passivation layer stack that result in local back surface fields (L-BSF) after contact firing [125].

Bifacial solar cells (and modules) offer the opportunity to increase the output power density p_{out} by making use of the rear side irradiance (i.e., albedo light) [130]. Since the PERC cell architecture encompasses a local contacting on the rear side, the concept allows the fabrication of bifacial PERC cells by applying a rear side aluminum finger grid as shown in Fig. 3.1(b). The terms biPERC and PERC+ are used in the literature to

describe bifacial PERC solar cells [9, 131]. In this work, the term biPERC is used to refer to bifacial PERC cells. The bifacial approach replaces the rear side full-area aluminum contact and permits the additional absorption of light impinging on the non-metallized spacing between the rear side contacts.

Boosting bifaciality to levels higher than that of biPERC is possible by fabricating other derivatives of PERC cell structures [132] (also known as PER-X structures), such as passivated emitter and rear totally diffused (PERT) solar cells [133] or passivated emitter and rear locally diffused (PERL) [134] devices.

Other cell concepts already produced in the industry in 2017 include the silicon heterojunction (SHJ) solar cells [135] and interdigitated back contact (IBC) solar cells [136]. Tunnel oxide passivated contact (TOPCon) [137] solar cells, which was just in research and development at the time of this dissertation start in 2017, entered mass production in 2019 [138].

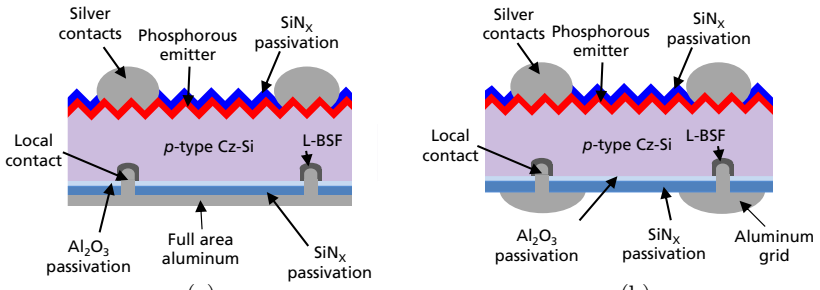


Fig. 3.1. Schematic cross-sections of two *p*-type Cz-Si solar cell architectures: (a) monofacial PERC and (b) biPERC. Although the structures on the front side are identical, the main difference lies in the rear side aluminum metal contact. The monofacial PERC features a full-area aluminum layer with local base contacts and the so-called local BSF (L-BSF), while the biPERC has a rear side aluminum finger grid. For both cell architectures, a thin SiO_2 layer present at the interfaces between the sketched passivation layers and the silicon on both sides are not shown for simplicity reasons. In addition, the rear side external silver contacts are not shown for simplicity reasons. The figure is redrawn and adapted from Ref. [57].

Fabrication process routes for monofacial and bifacial PERC cells

This dissertation mainly focuses on the *p*-type Cz-Si biPERC cell architecture and an industry-typical process flow as basis for the further development of the shingle cells. At the *Fraunhofer ISE Photovoltaic Technology Evaluation Center* (*PV–TEC*) [139], the pilot-line follows the PERC process sequence shown in Fig. 3.2 for the PERC [140] and biPERC cells. The fabrication of the PERC cells starts with as-cut *p*-type Cz-Si wafers with an edge length of 156.75 mm (also known as 6-inch cells, or M2 format cells in case the wafer has a 210 mm diameter). The wafers undergo alkaline texturing followed by the formation of the n^+-emitter in a phosphorous oxychloride ($POCl_3$) tube diffusion process. Next, the rear side emitter is removed, and the front side phosphosilicate glass (PSG)/SiO_2 layer stack is etched in an inline wet-chemical process. To passivate the rear side, the wafer surfaces are then wet-chemically cleaned and an around 6 nm-thin Al_2O_3 layer is formed by means of atomic layer deposition (ALD). Then, an outgassing process is performed in a tube furnace with nitrogen (N_2) gas ambient at around 550°C. The rear side SiN_X deposition of the capping layer is conducted by plasma enhanced chemical vapor deposition (PECVD). The thickness of the rear side capping layer is optimized depending on whether the cells are intended to be monofacial or bifacial. For monofacial cells, a SiN_X layer thickness of around 150 nm is intended while for bifacial ones an about 75 nm-thick SiN_X layer, and thus thinner layer, is deposited. This explains the rather "yellowish" color of the rear side of PERC precursors optimized for monofacial use, while that of the bifacial cells are "blueish". A similar process is used to coat the front side by a 75 nm-thick SiN_X layer to passivate the emitter and act as an antireflection coating (ARC). By that, the "frontend" process steps are completed.

The following "backend" processes are necessary for the formation of the contacts and the activation of the passivation properties. The completely passivated PERC precursors are subjected to the local laser contact opening (LCO) which is performed by a pulsed infrared laser that locally ablates the rear side passivation. Next, the external rear side silver contacts, i.e., the "solder pads" are screen printed. For the fabrication of monofacial cells, a full-area screen printing of aluminum (Al) paste is performed while the rear side is printed with a grid layout (fingers and busbars) for bifacial cells. Commercial Al pastes optimized for the respec-

tive application are used. The printed rear side metal paste covers the LCO. Following the screen printing on the rear side, the front side silver (Ag) grid is printed. The metal-semiconductor contact formation occurs during the contact firing step that takes place in an industrial conveyor belt furnace [141]. The ultrafast regeneration process [142, 143] boosts and stabilizes efficiencies of especially boron-doped *p*-type Cz-Si wafers (Cz-Si:B), discussed in detail in the upcoming paragraph. Front side and rear side photographs of PERC and biPERC solar cells are shown in Fig. 3.3. The "backend" processes are finished after cell characterization by means of current-voltage (IV) measurements.

For boron-doped *p*-type Cz-Si wafers (Cz-Si:B) a common bulk defect is the boron-oxygen (B-O) defect that leads to cell efficiency drops when activated [144, 145]. The defect is observed under excess charge carrier density (e.g., irradiance) leading to the commonly known light-induced degradation (LiD) [146, 147]. Some post-firing thermal photonic processes stabilize the cells on high levels [148]. The combination of heat and

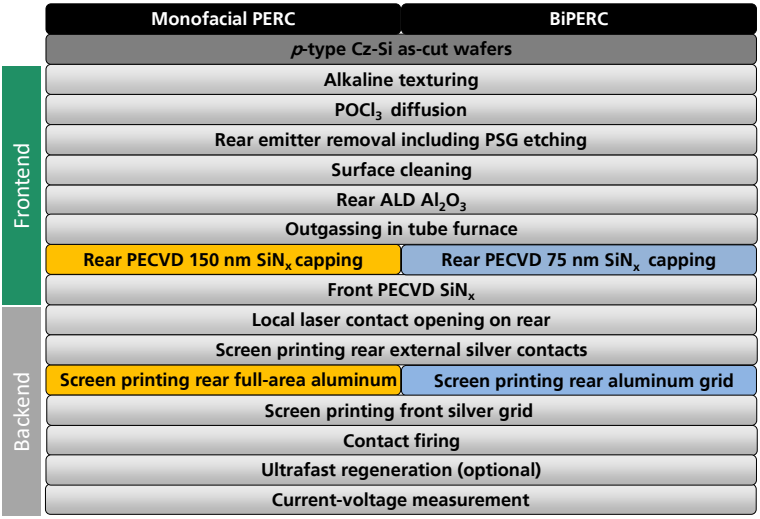
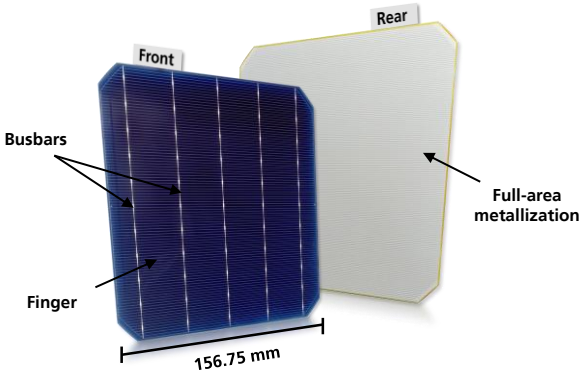


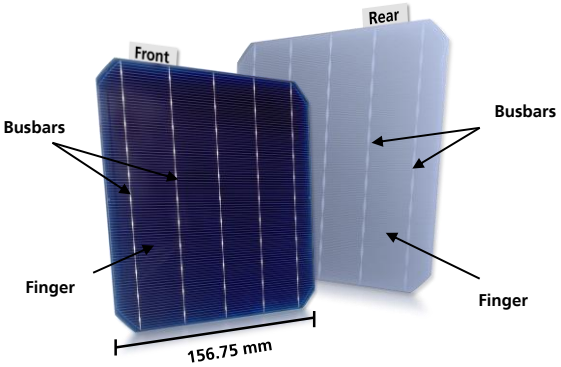
Fig. 3.2. Example of a baseline process flow for the fabrication of PERC and biPERC solar cells at the *Fraunhofer ISE* pilot-line using as-cut *p*-type Cz-Si wafers. Although the process sequence is almost identical, the main difference between the fabrication of the monofacial and bifacial PERC cells lies (i) in the rear side passivation layers optimized for the defined application and (ii) in the rear side screen printing layouts. The monofacial device features full-area aluminum while the bifacial one has an aluminum grid.

irradiance leads to the regeneration of the cells in a stable state with high efficiencies. The laser-based ultrafast regeneration (UFR) process is an industrial method dedicated for the regeneration [142, 143].

In this work, the state of the B-O defect is given for the experiments done on Cz-Si:B wafers. The states are based on the processing stage of the wafer: (i) the as-processed state directly after contact firing being possibly unstable, (ii) the degraded state after LiD by light exposure being stable, and (iii) the regenerated state after the mentioned post-firing treatment being ideally stable. However, the defect is also seen to be of minor



(a) Monofacial PERC



(b) biPERC

Fig. 3.3. Photographs of industrial 6-inch H-pattern p-type Cz-Si solar cells with screen printed contacts: (a) monofacial PERC and (b) biPERC. The front side of both cells has a five-busbar contact grid. The rear side of monofacial PERC cell features a full-area metallization while that of the biPERC cell has a contact grid layout (rear side external silver contacts are not shown).

importance in magnetically-cast Cz-Si:B [42]. Additionally, B-O-related LiD is not seen to be relevant in gallium-doped wafers (Cz-Si:Ga), which are used in some of the investigations in the upcoming sections.

3.3 Separated and shingle solar cells

Aiming towards higher module output power densities p_{out}, advancements in cell-to-module architectures are required. Integrating half cells separated after contact formation into modules is an approach to boost p_{out} [11]. One of the main advantages lies in the reduction of the current generated per cell, leading to the possibility of reducing the current per string. By that, the losses on the interconnection level are reduced as the dissipated resistive power loss P_{loss} is proportional to the total resistance R_{T} (i.e., that of the cells and the interconnection) multiplied by the square of the string current I_{str},

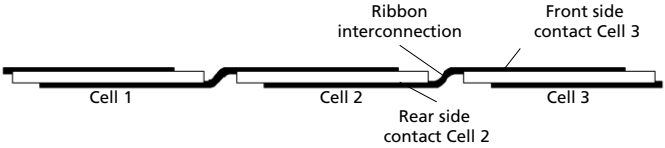
$$P_{\mathrm{loss}} = R_{\mathrm{T}} I_{\mathrm{str}}{}^{2}. \tag{3.1}$$

Additionally, optical improvements are also recorded, mainly caused by the reflection from the backsheet. The reflection then leads to current gains. Since the separation process is completed in a late stage of the cell fabrication, conventional copper-based ribbon module interconnection can be used; see Fig. 3.4(a). The approach of conventionally interconnecting separated cells is already shown in half cell modules [11].

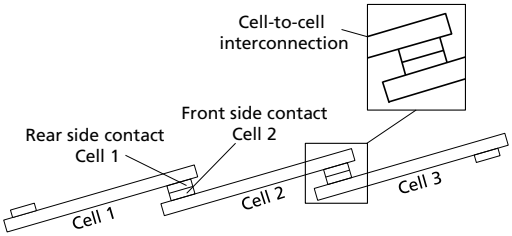
The concept of shingling was first proposed in a patent application from 1956 [14]; see Fig. 3.4(b). The photovoltaic devices are placed in a "stepped" relationship with respect to each other. The patent also briefly explains the feasibility of a low ohmic electrical series connection. In 1969, *Baron*' s patent titled "Solar cells with flexible bifurcated connectors" [149] explained the possibility of connecting solar cells using clips accompanied to the overlapping architecture of the cell assembly. The bowed bifurcated clips mechanically and electrically interconnect the bottom contact strip of one solar cell to the top contact strip of the other. This approach aimed to solve the fixed and direct bonding of the overlapped cells thus relieving thermal expansion/contraction stress while at the same time simplifying the interconnection approach considered by *Nielson et al.* [150] (a patent prior to *Baron*' s). In 1972, *Leinkram et al.* proposed the use of stepped spaced platens in combination with adhesives to bond solar cells on a panel in a shingle assembly [151]. The idea behind the invention is to

create higher thermal dissipation capacity to make the solar panel appropriate for deployment in satellite missions. Shingling is also seen as interesting for applications that include rather unusual deployment geometries requiring curvatures within the modules; such as domes [152, 153].

In the 1996 *World Solar Challenge*, shingling interconnection was used to interconnect PERL solar cells on a vehicle with limited-area aiming for very high p_{out} [154]. At *Fraunhofer ISE*, the shingle technique was used back in 2002 to interconnect monofacial PERC cells for the purpose of high conversion efficiency at low illumination intensity applications on electronic devices [16]. The product was integrated in the *Siemens S25* mobile phone. In a 2016 publication, *Beaucarne* showed the use of electrically conductive adhesives (ECA), replacing the ribbons for the interconnection of separated cells by shingling [155]. The work also introduced an analytical model explaining the thermomechanics of shingled cells interconnected by ECA.



(a) Conventional ribbon-based cell interconnection



(b) Shingle cell interconnection

Fig. 3.4. Schematic depiction of the cross-section view of three interconnected solar cells based on (a) the conventional copper-based ribbon interconnection approach, and (b) the shingle interconnection method. In the conventional approach, the front side of a cell is interconnected to the rear side of the neighboring one by means of conductive ribbons. That is different from shingled solar cells where the rear side of the cell is interconnected to the front side of a neighboring cell by overlapping. One of the approaches includes electrically conductive adhesives (ECA) in between the busbars to further ensure the electrical and mechanical interconnection.

Sunpower has been the first company to offer the monofacial shingled cells as the *Performance P–Series* module in 2015 [156]. The monofacial module has achieved a nominal power of 350 Wp for 2.06 m^2 module area at standard testing conditions (STC) [37] (data from 2017). As expected, the company also holds recent patents in the subject [157–159]. One of the main claims is the shingled connection of cells using electrical and thermal conductive adhesives confined by the metallization pattern on the cells. The encapsulation thought of in the patent allows the possibility of bifacial solar cell integration. In 2016 the company *Seraphim* also offered the *Eclipse* module based on shingled monofacial solar cells [160].

In 2017 the shingling interconnection of monofacial Al-BSF cells was published by *Rudolph et al.* [161], who fabricated mini-modules (i.e., approximately wafer-size equivalent modules) and showed the performance advantage of shingled cells in comparison to conventionally interconnected references. *Tonini et al.* also published an approach where ECA was used to interconnect monofacial separated PERC cells [162]. The results showed a $10\%_{rel}$ output power gain in comparison to reference 60 cell-equivalent modules even after module thermal cycling tests. Therefore, it is evident that shingling is an approach to achieve higher p_{out}. Hence, in 2017, shingle modules using monofacial cells were already fabricated to make use of the electrical, optical, and aesthetic advantages. However, no record of bifacial shingle solar cells and bifacial shingle modules was known to the author up to the start of this work in 2017.

Independent from the chosen cell interconnection technology (whether conventional, shingled, etc.), the cell separation process leads to charge carrier recombination at the newly formed edges. This type of surface recombination, also known as edge recombination, causes drops in cell efficiency. For improved p_{out} results of separated cell approaches on module level, the overall gain on the module p_{out} must overcome the edge recombination losses on the cell level. This raises concerns of the importance of modeling and characterizing edge recombination and its effect on solar cell output parameters. The characterization of edge recombination also allows the understanding of further edge passivation processes that exhibit a possible improvement in the electrical performance of edge-passivated cells. As the separation and edge passivation are core topics in this dissertation, an overview about existing edge recombination characterization and modeling methods follows next.

3.4 Edge recombination models and characterization methods

Edge recombination in silicon solar cells exists whenever the periodic structure of the crystal lattice is interrupted by the formation of an edge. In the fabrication of full wafer-sized cells, the wafer edges are passivated by the wrap around of dielectric layers deposited during the front and rear passivation processes; see ,e.g., Fig. 3.2. Consequently, the impact of edge recombination on full wafer-sized cells is low. However, separating cells at a later stage commonly after contact formation, creates new "unpassivated" edges with exposed *pn*-junction (i.e., edges without surface passivation).

Edge recombination and its impact on silicon solar cell performance is discussed extensively in the silicon solar cell characterization community. In 1993, *Luque* and *Tobias* describe the effect of edge (or perimeter) recombination as a function of illumination concentration and fabricated cell size [163]. Their model, also verified by experiments, shows that the cell open-circuit voltage V_{OC} drops due to edge recombination. This effect is mostly visible at low illumination intensity and smaller cell-sizes. *Aberle et al.* state that an efficiency loss of $3 - 4\%_{\mathrm{rel}}$ is likely due to the high surface recombination velocity at the edges of 4 cm²-large PERL cells [164]. Therefore, the lab-scale cells are left embedded in the substrate wafer to drastically reduce this loss. In 1996, *Altermatt et al.* have published a numerical model to analyze the reduction in cell efficiency as a result of edge losses [165]. The work reveals that surface recombination velocities lower than 2000 cm/s should be achieved to restrict the effects of edge recombination and observe efficiency improvements. *Kühn et al.* reported a simulated edge-related dark saturation current per length $j_{02,\mathrm{edge}} = 20$ nA/cm for cleaved solar cells [166].

In the dissertation of *Dicker* [21], the behavior of the edge recombination for different separated cell sizes and at different irradiances is incorporated into the two-diode model. In the work, the perimeter-to-area ratio k is particularly defined as the perimeter fraction of the "unpassivated/separated" edge P_{sep} over the total cell area A_{tot} such that

$$k = \frac{P_{\mathrm{sep}}}{A_{\mathrm{tot}}}. \tag{3.2}$$

Experimentally, illuminated current-voltage (IV) curves are obtained for different irradiances G ranging from 1 W/m² to 1000 W/m² by considering the one-diode model equation (2.5). The terms can also be expressed as

$$V_{\mathrm{OC}} = n_{\mathrm{id}} V_{\mathrm{Th}} \ln\left(\frac{G\, j_{\mathrm{SC,1Sun}}}{j_{01}}\right), \tag{3.3}$$

where n_{id} is the ideality factor, j_{01} is the dark saturation current density, $j_{\mathrm{SC,1Sun}}$ is the short-circuit current density at an irradiance of $G = 1000$ W/m², and V_{Th} is the thermal voltage as shown in equation (2.6).

V_{OC} as a function of the logarithmic irradiance values are plotted for each of the separated cells. The slope of the fitted line provides the n_{id} for each of the cell sizes. The results of the parametrization, also discussed in Refs [15, 16], show an increase of n_{id} reaching values close to $n_{\mathrm{id}} = 2$ with the increase of k. This indicates that the recombination current at the space charge region is higher for cells with higher k. A two-diode model including a second diode with total edge-related saturation current density $j_{02,\mathrm{tot,edge}}$ is done by scaling the space charge recombination current density per length $j_{02,\mathrm{edge}}$, with k.

$$j_{02,\mathrm{tot,edge}} = j_{02,\mathrm{edge}} \cdot k \ . \tag{3.4}$$

The first diode then represents n_{id} of the non-separated cell with the dark saturation current density j_{01}. As previously mentioned, these values are determined from the G and k variation in the one-diode model. Using them in the two-diode model, leads to $j_{02,\mathrm{edge}}$ and n_{edge} after considering the best fit. By this method $j_{02,\mathrm{edge}} = 13$ nA/cm and $n_{\mathrm{edge}} = 2$ is determined in Refs. [16, 21]. As a visual characterization method, thermography infrared image shows the higher detected signals for the separated edge where the *pn*-junction is exposed.

To date, edge recombination characterization methods are shown by numerous authors. *Chen et al.* [167] introduce a contactless technique that quantifies edge recombination by means of quasi-steady state photoconductance (QSSPC) and quasi-steady state photoluminescence measurements. This is realized by observing the carrier lifetime at different injection levels for samples with different "artificial" edge lengths, meaning formed trenches exposing the *pn*-junction. The method offers the advantage of characterizing edge recombination prior to the formation of the cell metal contacts. *Fong et al.* present a method to extract edge recombi-

nation by using photoluminescence imaging in addition to electroluminescence imaging [168]. In *Bertrand et al.*, edge recombination losses in separated Al-BSF cells are extracted by characterizing cells of different sizes [169]. Apart from showing the effect of the separation on V_{OC} and pseudo fill factor *pFF* values, methods based on the two-diode model are introduced to extract the saturation current density at the edge.

In 2017*, Quokka3* cell simulation software incorporated a "multidomain modelling" approach that allows the possibility of simulating shingle cell performance by considering edge recombination effects as well [170].

At the beginning of this dissertation work, simulations performed by *Wöhrle et al.* aimed to understand the impact of edge recombination on fabricated PERC-based shingle solar cells [171]. The obtained results were planned to be used as a starting point for the fabrication of the shingle cells in this dissertation. Referring to previous publications, the recombination losses at the edge discussed in this work are divided into three-subclasses: (i) The bulk region where surface recombination with an ideality factor $n_{i1} = 1$ is considered, (ii) the highly-doped emitter region at the edge with $n_{i1} = 1$, and (iii) the space charge region (SCR) that includes the non-ideal recombination with an ideality factor $n_{i2} \approx 2$. The bulk and the SCR are considered to have an equal contribution to the total edge recombination. The modeling defines the extreme cases of maximum and minimum edge recombination. An unpassivated separated edge, according to Ref. [16], has an effective surface recombination velocity $S_{eff,edge} = 5 \times 10^6$ cm/s (with $n_{i1} = 1$) and a $j_{02,edge} = 19$ nA/cm (value from Ref. [170]). The simulation which considers not only edge recombination (for e.g., resistive losses are also included) reveals an optimum cell width of around 25 mm. For the minimum edge recombination, a passivated edge condition is modeled with an effective surface recombination velocity $S_{eff,edge} = 10$ cm/s and a $j_{02,edge} = 0$ nA/cm. At a simulated bifacial illumination of 1100 W/m² (i.e., front irradiance $G_{front} = 1000$ W/m² and rear side irradiance $G_{rear} = 100$ W/m²) the edge-passivated cell shows a p_{out} performance advantage of around 1 mW/cm² compared to the non-passivated separated cell. All realistic edge recombination cases should be positioned somewhere in between these extremes depending on the passivation quality at the edge. A parallel dissertation work in progress by *Stolzenburg* is ongoing, aiming towards the advanced characterization of edge recombination, with initial modeling results already published in Ref. [172].

In terms of solar cell output parameters, edge recombination is characterized mainly by losses in V_{OC} and *FF*. Both values are obtained by IV measurements showing the drop in η values. However, the *FF* also includes shunt and resistive losses, making it inappropriate for determining edge recombination losses. The *pFF* values derived from the SunsV_{OC} measurements [39, 169] provide a useful method to characterize edge-related losses. IV measurements and SunsV_{OC} measurements are explained in section 2.4, while the specific adaptations for the characterization of the developed shingle cells are discussed in section 4.4.

3.5 Chapter summary

This chapter focuses mainly on describing PERC cells that were relevant at the start of the dissertation in 2017. The process sequence starting from *p*-type Cz-Si as-cut wafers up to the full wafer-sized cell characterization is provided by introducing the "frontend" and "backend" process steps. The local rear side contacting of the PERC cell architecture allows the fabrication of biPERC devices with the same number of process steps as their monofacial counterpart. Monofacial PERC cells feature a full-area screen-printed and fired aluminum rear side contact while that of biPERC cells are formed by an aluminum grid. An additional difference between the two cell structures lies in a thinner rear side SiN_X passivation layer thickness for the biPERC cell optimized for bifacial application.

Based on the literature review provided in this chapter, previous studies already confirm the advantage of separated cells (particularly the shingling interconnection) especially on the module level reaching around $10\%_{rel}$ output power gain in comparison to modules with conventionally interconnected cells. However, no record of bifacial shingle cells or bifacial shingle modules is found in the works preceding the start of this dissertation. On a separated cell level, previous studies quantify the edge recombination losses for silicon solar cells with an effective dark saturation current at the emitter, space charge region, and bulk recombination to a *k*-dependent j_{02} and an ideality factor $n_{i2} \approx 2$. As a takeaway message, edge recombination reduces mainly the solar cell output parameters V_{OC} and *pFF* and therefore *FF*.

4 The p-Type Shingled Passivated Edge, Emitter, and Rear Solar Cell

4.1 Introduction

This chapter introduces the p-type shingled passivated edge, emitter, and rear (pSPEER) solar cell concept which stands in focus within this dissertation. The pSPEER cell structure and fabrication process flow are discussed. The terminology related to the device components is defined. Additionally, the "passivated edge technology" (PET) approach is introduced for its application on separated silicon solar cells. The application of PET on pSPEER cells results in a cell architecture named $p\text{SPEER}^{\text{PET}}$, which is also portrayed and clarified. The current-voltage setup for the measurement of shingle cells is described and includes specific adaptations to measure shingle solar cells. The SunsV_{OC} measurement and the contacting approach for characterizing shingle cells is also depicted.

4.2 The pSPEER solar cell[1]

4.2.1 Cell structure and process flow

The shingling interconnection of solar cells leads to a reduction of cell-to-module losses by mainly reducing electrical interconnection losses within the module. This approach leads to optical light coupling gains as a result of the omitted cell spacing. The visually busbarless module also gives it an appealing appearance. Using bifacial cells leads to an additional boost in output power densities p_{out} by profiting from rear side irradiance. The approach adopted at *Fraunhofer ISE* joins the notions of bifaciality and

[1] Parts of this section are based on the publication stated in Ref. [173]. The author of this dissertation is also the first author of the referenced paper.

shingling interconnection by introducing the bifacial p-type shingled passivated edge, emitter, and rear (pSPEER) solar cell developed and characterized in this dissertation. Furthermore, the pSPEER concept was first published in Ref. [173] at the beginning of the work in which the structure and the proof-of-concept was shown. The pSPEER solar cell is a derivative of the p-type bifacial passivated emitter and rear cell (biPERC) structure shown in Fig. 3.1(b) of section 3.2. The name includes the term "shingled", which refers to the intended interconnection technique the cells undergo after manufacturing. The pSPEER cell architecture is shown in Fig. 4.1(a). Like the biPERC cell architecture, the pSPEER solar cell also encompasses a p-type Cz-Si base and an n^+-type phosphorous diffused emitter that is passivated by SiN_X. The rear side features dielectric passivation layers (usually an Al_2O_3 layer capped by a SiN_X layer). As discussed in chapter 3, a thin silicon dioxide (SiO_2) layer is additionally present directly at the silicon interfaces on the front and the rear sides (not shown in the sketch). The main difference in the structure rises at the separated edges which in the case of the pSPEER cell is sustained by natively-grown SiO_2 layers known to grow on silicon exposed to air ambient [86]. The term "passivated edge" within the naming of pSPEER solar cell thus refers to this native SiO_2 layer grown on the cell edge that passivates the edge to a certain extent.

The process sequence for the fabrication of the pSPEER solar cell is shown in Fig. 4.1(b). In comparison to the fabrication steps of biPERC cells, one additional post-metallization backend process step, i.e., the laser-assisted separation, is required to obtain pSPEER solar cells. Additionally, the rear side laser local contact opening patterns as well as the metallization layouts are adapted according to the intended shingle cell design.

This implies that the pSPEER cell also benefits from advancements in the baseline PERC technology. Since the separation comes at the end of the cell fabrication process sequence, this separation process step can be integrated to already existing PERC routes. The separation of full wafer-sized cells into shingle strip cells is performed by adding a separation unit to the production line. Changes in the frontend process steps are not required.

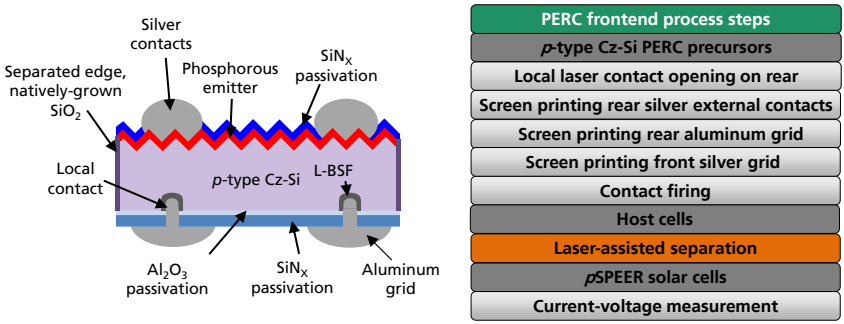
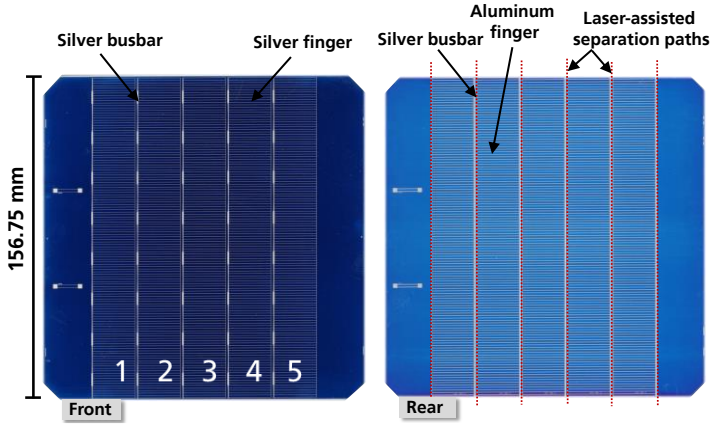


Fig. 4.1. (a) Schematic cross-section of a *p*SPEER solar cell. As a derivative of the biPERC cell, the principal *p*SPEER cell structure is almost identical except for the natively-grown SiO_2 layer on the separated edges. The SiO_2 layers at the interfaces between the passivation layers and the silicon are not shown in this figure except at the edges. In addition, the rear side external silver contacts are not shown for simplicity reasons. (b) Process sequence for the fabrication of *p*SPEER cells starting from full wafer-sized *p*-type Cz-Si passivated precursors (only backend process steps shown). The only additional process step in comparison to the fabrication of biPERC cells is the laser-assisted separation. (Of course, the metallization layouts are also adapted for the fabrication of shingle cells). The figure is redrawn and adapted from Ref. [173].

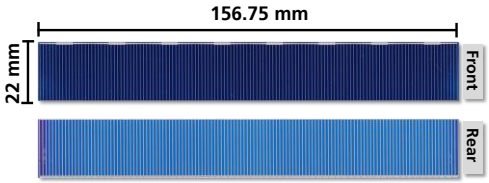
Eventually, a full wafer-sized *p*-type Cz-Si PERC precursor from a production line is used as a starting material. This also implies that the frontend process sequence is kept unaltered. The precursors feature the front and rear side passivation layers, and the fabrication can start from the backend processes. To start with, the rear side local contact openings (LCOs) are formed by means of laser ablation. Next, the rear side external busbar contacts are screen printed using a non-fire-through silver paste (also referred to as "floating busbars"). Ideally, the non-fire-through paste does not etch through the passivation layer and does not contact the silicon. Following that, the rear side finger grid is screen printed by an aluminum paste covering the LCOs and interconnecting the aluminum grid to the rear side silver busbars. Consequently, the front side silver busbars and fingers are also screen printed. The metal-semiconductor contact formation takes place in a conveyer belt fast firing oven. With this method, five or six shingle cells are obtained from each host cell depending on the design of the metallization layouts (five cells are obtained in the case shown in Fig. 4.2(a)). The design also includes metallization gaps as paths for the laser-assisted separation process that takes place as the last

fabrication step before the current-voltage (IV) measurement. By that, pSPEER solar cells are obtained as shown in Fig. 4.2(b).

As discussed above, adaptations in the rear and front metallization layouts must be taken into consideration. This takes into account that no significant series resistance losses rise in comparison to the standard full-wafer size PERC solar cells. Moreover, the rear and front side busbar designs allow the shingled interconnection on a module level, by considering cell-to-cell interconnection requirements.



(a) Host cell



(b) pSPEER solar cell

Fig. 4.2. Photographs of the front and rear sides from: (a) A metallized host cell with the metallization layouts adapted such that five pSPEER cells can be obtained. (b) A pSPEER solar cell after laser-assisted separation with the dimensions of 22 mm x 156.75 mm. In this case, the additional strips to the left and the right of the numbered strips are not used as shingle cells because of their pseudo square edges.

Additional attention is needed for the silver busbar widths as well as the interconnection regions between the fingers and the busbars that are screen printed separately. Such design considerations effect the cell performance and play a role in the intended cell-to-cell interconnection. Moreover, the design of the metallization layouts also considers distance accuracy tolerances during processes. For example, the accuracy of the alignment between the LCO formation and the rear side finger screen printing processes is considered. The design also accounts for possible minor deviations in laser-assisted separation processes.

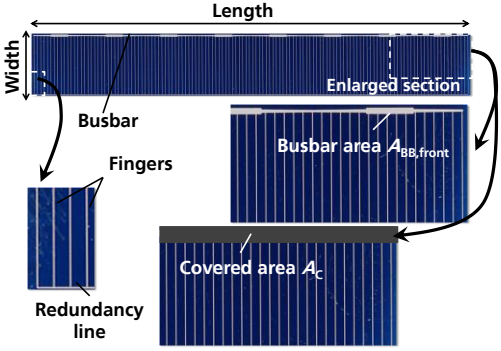
Throughout the progress of the work, seven metallization layout generations have been developed that address cell and module performance concerns as well as cell measurement purposes. Appendix A.3 includes details about the metallization layout designs. The metallization layout generation used for each discussed cell batch within the upcoming chapters is provided in the respective experiment description sections.

4.2.2 Terminology for *p*SPEER solar cells

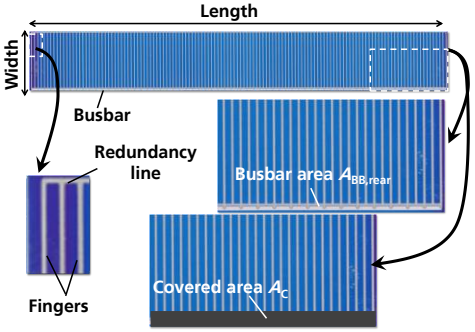
The frequently used terms referring to the *p*SPEER cell structures and components are defined in this section. Fig. 4.3(a) and (b) show the top view photographs of a *p*SPEER solar cell's front and rear side, respectively. After separation, the separated cell's length and width define the total area A_{tot}. Like the standard full wafer-sized solar cells, the *p*SPEER cell encompasses the fingers and busbars as metal contacts. The fingers are responsible for the collection and the lateral transport of the charge carriers, while the busbars are necessary for the cell-to-cell interconnection. Since the cells are intended to be interconnected by shingling, a busbar to busbar contact within the module is foreseen. The redundancy line is included in the metallization design to ensure that possible finger interruptions/breakages during processing are compensated by an additional contact structure that is perpendicular with respect to the fingers. Accordingly, the total front side metal coverage area of the cell $A_{\mathrm{met,front}}$ is defined as the summation of the area covered by the front side fingers $A_{\mathrm{f,front}}$ (i.e., including that of the redundancy line) and the area of the front side busbar $A_{\mathrm{BB,front}}$.

Similarly, the rear side total metallization fraction $A_{\mathrm{met,rear}}$ is defined by the summation of the rear side finger $A_{\mathrm{f,rear}}$ and the rear side busbar area

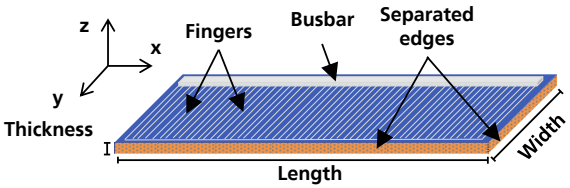
$A_{BB,rear}$. Since the shingling concept requires the overlap of neighboring cells, a new apparent area is obtained after an intended overlap.



(a) Front side (top view)



(b) Rear side (top view)



(c) Sketch (side view)

Fig. 4.3. pSPEER solar cell (a) top view illustration of the pSPEER cell front side and its components. The busbar area $A_{BB,front}$ and the covered area A_C are defined. (b) Top view illustration of the pSPEER cell rear side and its components. The busbar area $A_{BB,rear}$ and the covered area A_C are defined. (c) Three-dimensional sketch defining the edges of the pSPEER cell obtained after separation (in orange, not to scale). In this example, the separation is done in x- and y-directions.

The overlap by a neighboring cell covers the busbar and a portion of the non-metallized active cell area between the busbar and the cell perimeter. This covered area A_C is solely defined by the overlap. In this work, the designated area A_{des} is the remaining area after the exclusion of the covered metallization area (i.e., in this case the busbar area) such that the front side designated area is $A_{des,front} = A_{tot} - A_{BB,front}$. Analogously the rear side designated area is $A_{des,rear} = A_{tot} - A_{BB,rear}$. In other words, the designated area metallization fraction excludes the metallization-related shading contribution of the busbars and allows the "busbarless comparison" of the cells with different metallization layouts.

Fig. 4.3(c) shows a three-dimensional sketch of the *p*SPEER solar cell with edge surfaces (commonly named as "edges" in this work) obtained after separation. In this case, the edges are in the x- and the y-direction, due to the separation in both directions. The thickness of the cell is defined by the thickness of the used wafer for the cell fabrication.

4.3 Passivated edge technology (PET) for separated silicon solar cells[2]

4.3.1 Motivation

For the fabrication of separated solar cells, whether half cells, third cells or shingle cells, the separation process usually takes place after the full wafer-sized cell is fabricated. Separating the samples at earlier stages in the production requires production line machine upgrades along with the difficulty/cost inefficiency to handle separated cells from earlier stages in the process flow. Although the separation process fits in the fabrication sequence, it creates unpassivated edges and induces edge recombination; discussed in section 3.4. The recombination increases with the increase of defects alongside the absence of intended passivation layers on the newly formed edges because of the separation process [174]. As studied in Ref. [15], the native SiO_2 layer grown on the cell edge might improve the solar cell performance especially at low illumination conditions

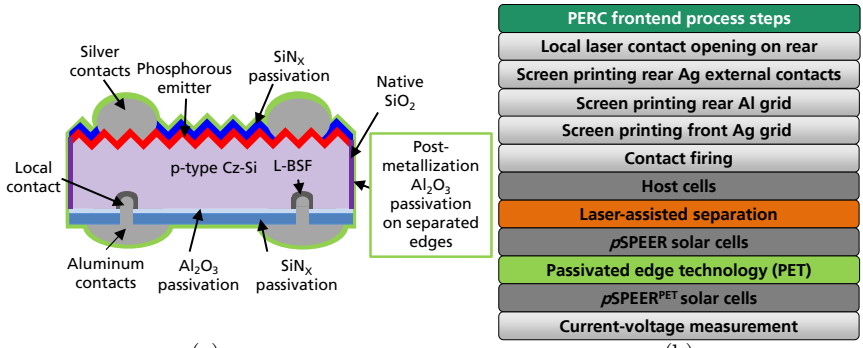
[2] Parts of this section are based on the publication stated in Ref. [175]. The author of this dissertation is the first author of the referenced paper. The first investigations of the the PET were performed in M. Al-Akash's master thesis, stated in Ref. [176], supervised by the author of this dissertation.

($G \approx 1$ W/m^2). However, additional edge passivation approaches are required to obtain enhanced cell performances by further decreasing the surface recombination velocity at the separated edge.

4.3.2 Concept and fabrication route of the pSPEER^{PET} solar cell

The passivated edge technology (PET), introduced in Ref. [175], is a post-metallization and separation edge passivation technique to boost the efficiency of separated silicon solar cells. In the PET, the absence of intended passivation layers is compensated by (i) dielectric passivation layer deposition and (ii) post-deposition annealing (PDA) activation processes. The passivation layer Al_2O_3 is known to provide excellent chemical passivation as well as a field effect passivation by its fixed negative charges [114]. This then aims to act as a repassivation of the separated edges. Performing PET on pSPEER cells, forms an upgraded cell architecture called the pSPEER^{PET} solar cell; see Fig. 4.4(a). In fact, the cell architecture is similar to that of the pSPEER solar cell shown in Fig. 4.1(a), with the addition of the post-metallization Al_2O_3 layer conformally-deposited all over the cell most importantly the edges. As a derivative of the PERC cell technology, the fabrication of pSPEER^{PET} solar cells includes identical process steps with the additional laser-assisted separation process and then the PET. Any pSPEER solar cell undergoing PET turns it into a pSPEER^{PET} solar cell; as shown in the process sequence in Fig. 4.4(b).

However, the deposition and annealing processes are required to take place at relatively low temperatures ($T < 200$°C) to avoid any side-effect damage on the already existing cell metallization and passivation. This also depends on the cell type and components used. Therefore, chapter 6 of this work focuses mainly on investigating low temperature surface passivation by means of ALD. Experimental investigation of PET on pSPEER cell performance is thoroughly studied in chapter 7.



(a) (b)

Fig. 4.4. (a) Schematic cross-section of a pSPEER$^{\mathrm{PET}}$ solar cell. As an adaptation of the pSPEER cell structure, the pSPEER$^{\mathrm{PET}}$ cell features an additional post-metallization Al_2O_3 passivation layer on the cell surfaces including separated edges. SiO_2 layers in the interfaces between deposited passivation layers and silicon are not shown except at the edge. In addition, the rear side external silver contacts are not shown for simplicity reasons. (b) Process sequence for the fabrication of pSPEER$^{\mathrm{PET}}$ cells starting from p-type Cz-Si passivated precursors with edge length of a wafer (only backend process steps). In comparison to the pSPEER cells, the fabrication of pSPEER$^{\mathrm{PET}}$ requires an additional passivated edge technology (PET) after the laser-assisted separation. The figure is redrawn from Ref. [175].

4.4 Characterization of *p*SPEER solar cells

4.4.1 Current-voltage measurement setup[3]

In contrast to the measurements of full wafer-sized cells, or half cells, the IV measurement of shingle cells in general and pSPEER cells in particular require (up to the current status) an offline or a semi-automatic system. For that purpose, special handling nests with custom-made dimensions of the separated cell perimeters are used to place the separated cells within; see Fig. 4.5(a). The shingle cell within the nest is then rotated into the IV measurement contacting chamber where each of the front and the rear side busbars is contacted by IV-pin arrays as shown in Fig. 4.5(b) and (c). To obtain, accurate measurements, the cell tester is calibrated by shingle cells measured at *Fraunhofer ISE CalLab PV cells*. Details about the *CalLab* measurement are discussed in Appendix A.1. The calibration of the cell

[3] N. Wöhrle, P. Baliozian, A. Krieg, and M. Rauer, "Measurement of Strip Solar Cells", *Unpublished work*, 2021.

tester is mainly done by adjusting the irradiance of the incident lamp, such that a similar short-circuit current I_{SC} to the one obtained in the *CalLab* measurement is attained.

In other words, the I_{SC} obtained at the cell tester is corrected such that shading due to the IV measurement contacting units is compensated. The measurements performed in the cell tester are A_{tot} measurements. A conversion to A_{des} (excluding the busbar) values is done by first calculating the designated area short-circuit current density $j_{SC,des}$ as follows

$$j_{SC,des} = \frac{I_{SC}}{A_{tot} - A_{BB}}. \tag{4.1}$$

After obtaining $j_{SC,des}$, it can be replaced instead of j_{SC} in equation (2.9) to obtain the designated area energy conversion efficiency η_{des}. The V_{OC} and

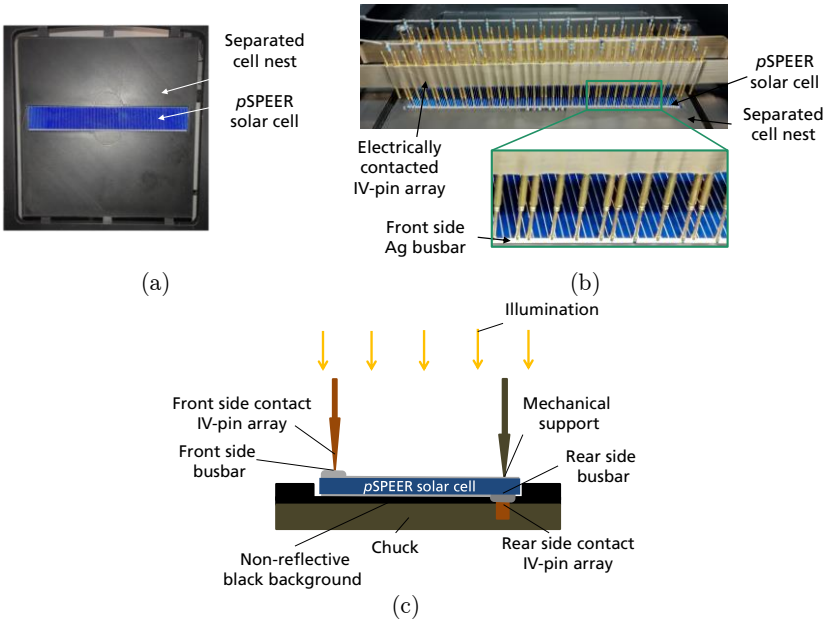


Fig. 4.5. Photographs of (a) the nest with the dimensions holding a pSPEER solar cell for the semi-automatic IV measurement handling (b) the busbar contacting of the shingle cell by means of an IV-pin array. (c) Schematic illustration of the IV measurement contacting unit. The cell is measured monofacially, and only the busbars are electrically contacted by IV-pin arrays. To measure the other side, the cell is then flipped and contacted and measured again. Figures (a) and (b) are adapted from Ref. [174].

FF are taken from the IV measurement since no significant changes to these value is expected as a result of the A_{des} consideration. Since the designated area mainly excludes the metallized A_{BB}, the $j_{\mathrm{SC,des}}$ is higher than the total area j_{SC}. Consequently, η_{des} is also higher than the total area η. However, this allows a fair comparison between cells having different busbar designs fabricated throughout the course of this work. In addition, since the cells are already contacted during the IV measurements, the tool also provides SunsV_{OC} measurement results analyzed during the flash lamp irradiance decay. This permits the extraction of *pFF* values alongside the rest of the cell parameters during the IV measurement. Nevertheless, the offline SunsV_{OC} measurement has the advantage of flexibility in the contacting positions, that would not be possible in the cell tester contacting scheme.

4.4.2 SunsV_{OC} measurement approach

Since the influence of processes is of most interest in the attempt to characterize changes, SunsV_{OC} measurements before and after processing are done. For instance, the impact of the separation process on host cells can be obtained by extracting the V_{OC} and the *pFF* before and after separation. To consider possible measurement setup or cell inhomogeneities into account, the cells are placed on the chuck in a matching position before and after processing; see Fig. 4.6(a) for the host cell and (b) for the shingle cell measurements, respectively. The probing is also performed in a similar manner before and after processing.

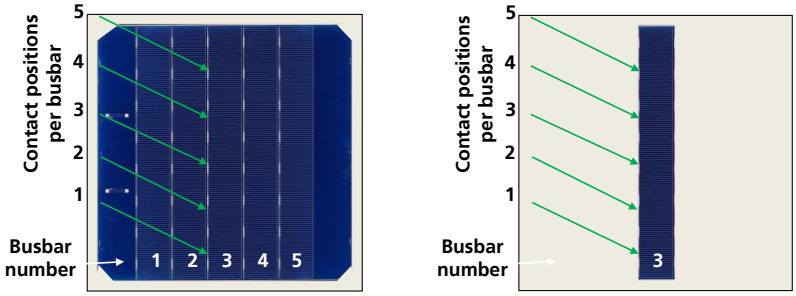


Fig. 4.6. (a) A sample schematic depiction of SunsV_{OC} contacting positions of a host cell placed on the measurement chuck. In this case the cell features five busbars and each busbar is contacted at five positions by a probe. (b) Schematic separated shingle cell is also measured at five positions, which are identical to that of their original positions within the host cell.

4.5 Chapter summary

This chapter introduces the p-type shingled passivated edge, emitter, and rear (pSPEER) solar cell as a cell concept. It is a derivative of the biPERC architecture that merges the notions of bifaciality and the ability to be connected to neighboring cells by shingling interconnection. By introducing one additional laser-assisted separation process at the end of the full wafer-sized PERC cell fabrication process sequence, pSPEER cells can be obtained. This allows the convenient addition of the separation process to the already existing process sequence. In comparison to the biPERC cell architecture, the pSPEER features an additional silicon dioxide (SiO_2) layer natively-grown on the separated edge in ambient air after separation. Within the period of the dissertation, seven generations of metallization layouts are designed to metallize host cells. These designs include considerations of the number of cells per host cell, different cell sizes (i.e., lengths and widths) as well as busbar and finger dimensions.

Since edge recombination is evident in post-metallization separated silicon cells, in this chapter, the "passivated edge technology" (PET) is introduced as a post-metallization and separation edge passivation technology. PET is a combination of (i) dielectric passivation layer deposition and (ii) post-deposition annealing (PDA) activation processes. The pSPEER$^{\mathrm{PET}}$ cell is shown to be an upgrade of the pSPEER cell by having an additional aluminum oxide Al_2O_3 deposition coating the cell, including the separated edges. Low temperature deposition and annealing processes (i.e., $T < 200°C$) are intended to prevent side-effects that harm already existing device components such as contacts and passivation layers. In other words, the chapter introduces the cell concepts along with core additional fabrication process steps which are addressed experimentally in depth in following chapters.

For the IV measurements of separated shingle cells, IV-pin array contacting of the front and rear side busbars are performed after placing the separated cell in the cell nest designed for that purpose. Although total area IV measurements are usually performed, the results are converted to designated area measurement results by excluding the metallization area expected to remain under the intended overlap (i.e., covered by shingling interconnection). This facilitates the comparison among cells independent from the chosen busbar designs. SunsV_{OC} contacting is done by choosing positions on the busbars and using a contacting probe.

5 Separation Processes for Silicon Solar Cells

5.1 Introduction

The advancement in separated solar cell concepts is made possible by the deployment of industrial separation processes. This chapter first provides an overview of existing techniques for the separation of semiconductors with a focus on industrial methods used for solar cells. Moreover, the functioning principle of the thermal laser separation (TLS) and the equipment used for the process are described. By emphasizing on the TLS, a new method for process optimization is introduced that is based on photoluminescence imaging. Using this technique, the influence of an optimized TLS process is distinguished from the impact of edge recombination by experimental investigations on PERC and silicon heterojunction solar cells. A comparison between conventional laser scribing and mechanical cleaving and TLS for singulation shows the influence of the different processes on electrical properties of host cells and *p*SPEER solar cells. Moreover, separated cells with much smaller sizes, where edge recombination becomes more dominant, are characterized from which conclusions about the separation impact are derived.

5.2 Separation techniques for semiconductor devices

In the semiconductor industry, separation, more commonly known as dicing, is an essential process step to obtain multiple fabricated chips from substrate wafers [177]. In his dissertation, *Koitzsch* summarizes the different requirements for the separation of semiconductor devices [29]. The focus is placed on (i) the quality of the separated edge (i.e., perpendicularity with respect to the wafer plane and surface roughness), (ii) throughput (i.e., separated units per hour), (iii) process costs, (iv) process yield, (v) temperature load on the substrate during processing, and

(vi) cleanliness of the substrate after processing (e.g., no metal contamination on the separated edges). Depending on the semiconductor device and the application constraints, the listed requirements can be ranked with the order of their importance.

A brief review of available semiconductor dicing methods is provided in this section by relying on Refs. [29, 30, 178]. The most commonly used dicing method in the semiconductor industry is the disc (or blade) dicing [179, 180]. In this technique, a rotating disc separates the substrate in desired directions, while being cooled by water spraying through a nozzle. The dicing takes place independently from the crystallographic orientations (i.e., Miller indices discussed in section 2.2). However, the process leads to kerf losses and rough edges.

Another separation method is the two-step mechanical scribing and cleaving technique. The scribing usually takes place by using a diamond scriber (or a disc) along the separation path and then the cleaving is done by applying a mechanical torque [180, 181]. A very high edge smoothness is attained in case a minor scribe is initiated, for e.g., by using a diamond scriber, followed by mechanical cleaving in the favored lattice orientation.

Laser-assisted separation techniques are also used to dice semiconductor chips. One method is the ablation process by means of pulsed laser beams [182]. In this technique, the laser that is focused on the substrate leads to the melting and/or evaporation of the semiconductor material. The use of lasers allows higher throughputs in production. However, the high temperatures occurring (i.e., higher than the silicon melting point of 1414°C) might harm already existing device structures. Furthermore, depending on the substrate thickness and the used laser, processes with several runs (or passes) are required to ablate the whole substrate thickness. The separation that occurs is independent from the crystallographic directions. Rough edges are attained because of the ablation.

Another laser-based method is the water-guided laser technology, also known as *MicroJet* separation [183, 184]. In this technique, the laser beam is guided by a high-pressure water/air beam, by exploiting the optical total internal reflection within the water jet. Like the laser scribing discussed above, the laser in this method leads to the ablation of the material. The presence of water during the separation reduces the possibly destructive influence of high temperatures. However, devices sensitive to

water require additional protective measures prior to processing in case this method is used.

Plasma etching separation is a chemical reaction-based method to dice chips [185]. The substrate is initially masked by inks (e.g., photolithography photoresist inks), keeping mask-free separation paths. The chemical reaction by the created plasma etches the mask-free regions: a very high separated edge quality is obtained from this process. Still, several additional steps are required for this process. Chips with a combination of different materials feature different material-dependent etching rates. This makes the separation of such devices by plasma etching technique challenging.

Another non-ablative method is the stealth laser dicing technique [186, 187]. In contrary to the laser ablation method, the laser induces internal material modifications and does not affect (i.e., does not ablate) the substrate surface. The permeable pulsed laser beam is partially transmitted through the substrate surface and creates a modification layer of amorphized material. In a subsequent step, a mechanical torque is created to separate the substrate. Although a high edge quality is attained, the success of the stealth laser dicing method strongly depends on the substrate material. The existence of device components such as metal contacts, might lead to the difficulty in creating a focused permeable beam within the material. Highly-doped materials are also difficult to process due to the high absorption that does not allow the laser to create the modification layer in the intended focus plane.

Other separation processes also used in the semiconductor industry are laser scribing and mechanical cleaving (LSMC) [11, 188], thermal laser separation (TLS) [23, 189], and laser direct cleaving (LDC) [190]. The latter is comparable to the laser-induced cutting (LIC) [191, 192]. These technologies are discussed in more detail in the next section due to their relevance in the separation of silicon solar cells.

5.2.1 Separation processes for silicon solar cells

For the industrial fabrication of separated silicon solar cells (e.g., half cells or shingle cells), the separation processes must fulfill high production throughput, mechanical strength of the separated product, as well as electrical performance requirements of the final device. Since the separa-

tion usually takes place in a late stage of the cell fabrication, mainly after contact firing as shown in Fig. 4.1(b), separation processes that lead to few/no defects are desired. Before laser-assisted separation processes were deployed for the separation of silicon solar cells, blade dicing was used to obtain chip-sized cells [19]. With the advancement of lasers for the material processing of silicon, laser-assisted processes for the separation of silicon solar cells have been introduced in the industry.

Laser scribing and mechanical cleaving (LSMC) is a common approach for the separation of silicon solar cells [188]. It is conducted by the ablation of a significant portion of the cell's thickness, (e.g., one-third), by means of a pulsed laser and subsequently mechanically cleaving of the device; see Fig. 5.1(a) and (b). Separation independent from the crystallographic orientations can be performed. On a solar cell level, *Eiternick et al.* studied the electrical output parameter losses as a result of the separation process by means of LSMC [193]. The main electrical loss is seen to be in the ablation (laser scribe) process step while the cleaving step has a relatively minor contribution in the total loss. The separation loss is quantified by an increase in the second diode dark saturation current density j_{02} as well as a decrease in the cells' parallel (shunt) resistances r_{p}.

Laser direct cleaving (LDC) is a kerfless non-ablative separation process commercialized in a laser machine by *Innolas Solutions GmbH* [190]. It is similar to the laser-induced cutting (LIC) [191, 192]. These separation techniques function by first inducing an initial crack that is then guided through the material by local heating. The laser-induced tension within the material leads to the separation. These processes do not require additional coolants. The exact functioning principle of the LDC is not yet

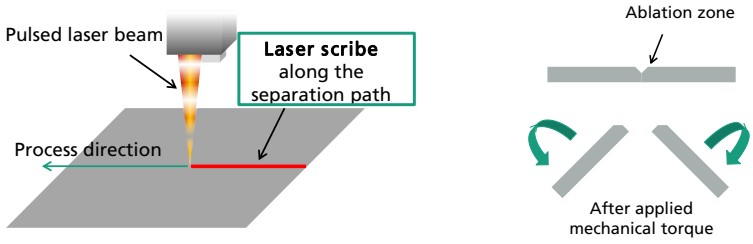


Fig. 5.1. Schematic depiction of the LSMC separation technique. (a) Laser scribing process by means of a pulsed laser beam and the (b) side view of the mechanical cleave process step by means of an applied torque. Figure (a) is adapted from Ref. [194].

published. On the other hand, the LIC is shown to have a narrower process window compared to that of the TLS [195]. It is expected that the separation can be done independent from the crystallographic directions.

The TLS is an alternative non-ablative dicing technique [23, 189]. The separation takes place in two process steps. First a crack (or scribe) of typically a few hundred micrometers is initiated by means of a pulsed laser or a diamond scriber. In a second step, the crack is propagated starting from the initial scribe position by a continuous wave laser heating and a simultaneous water/air cooling process (active cooling as an addition to LIC). The evolving thermal gradient guides the crack in the desired separation path independent from the crystallographic orientation. TLS leads to the creation of substrate edges with very low surface roughness. However, crack deviations in the separation of up to a few hundred micrometers are possible [196].

In *Eiternick et al.* [195], a comparison between TLS-separated and LSMC-separated half cells is done on multicrystalline three-busbar PERC solar cells. The electrical characterization by current-voltage (IV) measurements in the paper shows a minor advantage of TLS-separated solar cells in terms of electrical performance. The main advantage of TLS-separated half cells is seen to be in the four-point-bending mechanical stability tests. The results show that TLS-separated cells have comparable mechanical stability results to reference full wafer-sized cells in terms of Weibull modulus and characteristic fracture stresses. The LSMC-separated cells, in contrary, experience a significant strength reduction by around 33 $\%_{\mathrm{rel}}$. In *Röth et al.*, the mechanical stability of TLS-separated half cells is again confirmed [196]. Even after module integration, TLS-separated cells show mechanical stability advantages compared to LSMC-separated cells [197]. Based on the best knowledge of the author of this dissertation, there is no record of electrically characterized TLS-separated shingle cells (strip cells) published prior to the start of this dissertation work in 2017.

Since the TLS is experimentally investigated in this dissertation a more detailed explanation of its concept, functional principle and the used equipment is provided now.

5.2.2 Thermal laser separation

This subsection is dedicated to the detailed explanation of the thermal laser separation (TLS) functioning principle and equipment. The TLS technique is commercialized by the *3D-Micromac AG* in a machine named *microDICE* [198]. With the start of the dissertation, a *microDICE* tool was also acquired and commissioned in the *Fraunhofer ISE Photovoltaic Technology Evaluation Center* (*PV–TEC*) backend laboratory. Both separation processes, LSMC and TLS, investigated within this dissertation are performed in this *microDICE* machine.

Functioning principle and equipment

As mentioned in the previous section, the TLS process consists of two essential process steps: (i) the crack initiation and (ii) the crack propagation [23]. Fig. 5.2(a) shows a schematic illustration of the TLS process steps. A crack of typically up to several hundred micrometers in length is initiated using a pulsed scribe laser. The crack propagation is accomplished by laser heating using a continuous wave laser and consequent water/air aerosol jet cooling. Moreover, this thermal cleave process takes place by heating the substrate with a continuous wave beam spot in the form of an ellipse; see Fig. 5.2(b). The heating creates a radial compressive stress from the ellipse center, whereas the edges of the ellipse encounter tangential tensile stress as explained in Ref. [30]. During the simultaneous active cooling by means of the water/air nozzle, an additional tensile stress is induced. For a successful crack propagation, it is required that the total tensile stress at the tip of the initiated (i.e., scribed) crack surpasses the critical fracture point at the hot and cool transition zone. In other words, the thermal gradient induced by the heating and cooling cycles guides the crack in pre-defined separation paths that can take place independent from the crystallographic orientation of the crystalline semiconductor substrate. Apart from the initial laser scribing process, ideally the cleave process does not lead to the melting of the substrate. The temperatures attained during the cleave process are several hundred degrees Celsius and, therefore, much lower than the melting point of silicon.

The *microDICE* tool used in this work includes two integrated laser sources (one for each of the laser processes). In the machine's process chamber, the z-axis setup includes both scribe and cleave laser beam paths. The laser for the scribe process is a nanosecond pulsed infrared laser with a wavelength $\lambda = 1070$ nm. A maximum output power of $P_S = 60$ W and a frequency of up to $f_S = 1000$ kHz can be attained with it. It is used for the fabrication of the initial scribe (i.e., crack initiation) for TLS as well as for the scribe process of LSMC.

The laser for the cleave process is a continuous wave infrared laser with $\lambda = 1070$ nm that reaches a maximum output power $P_C = 850$ W. Additionally, the water nozzle and the air jet are also mounted on the z-axis. Two cameras (wide and zoom) are also integrated to provide images that are necessary for the alignment of the substrate by the alignment algorithm. They are also used to measure device structures, for e.g., metal contacts or separation path widths, on substrates. The machine also encompasses a distance measurement sensor to monitor the distance between the work piece and the z-axis setup, while the sensor is also used to measure substrate thicknesses.

To process the substrate, it is placed on the chuck positioned on the x-y-plane. The chuck, in our case made up of aluminum, features holes for the vacuum suction of the substrate during processing. It is also mounted on a rotary table allowing a spin along the rotation axis (i.e., c-axis). Depending on the processed substrates, foils are used to ensure an additional adhesion apart from the vacuum suction of the sample to the chuck.

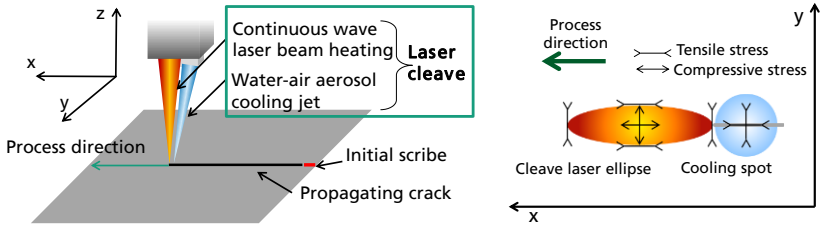


Fig. 5.2. (a) Schematic illustration of the TLS process showing the crack initiation (initial scribe) in red and the crack propagation by the heating and simultaneous cooling (cleave) in black. The scribe laser is not shown in the figure. (b) Depiction of the thermal stresses induced in the substrate during the crack propagating cleave process. Figures (a) and (b) are redrawns from Ref. [194] and Ref. [30], respectively.

For monitoring purposes before processing, a sensor integrated in the setup measures the laser power values. Moreover, for a qualitative control of the cleave process, an infrared thermocamera with an angle of around 45° to the chuck can be used, as shown in Ref. [30]. The infrared camera *Optris PI400* features a measurement spectral range from 7.5 µm to 13 µm, with a detector resolution of 382 x 288 pixels, and a frame rate of 80 Hz [199]. Obtaining accurate absolute quantitative temperature values is not possible due to the strong dependency of the emissivity of silicon on the temperature [200, 201] and the doping concentration [202]. Nevertheless, the temperature profiles attained from the camera measurement can clearly identify changes in the setup where similar temperature profiles (i.e., ellipse shapes) for similar samples are expected; see Fig. 5.3(a) for a sample image. From the obtained two-dimensional image, position-dependent thermal gradients can be visualized; see Fig. 5.3(b). For a detailed explanation about the TLS process monitoring by thermography please refer to Ref. [203].

Overview of process parameters

The TLS process parameters are numerous and often inter-reliant [29]. Therefore, it is difficult to change single parameters without affecting others. The research done on the TLS process has come a long way with in-depth studies aiming to optimize the crack initiation and propagation processes especially on silicon substrates [29]. Additional investigations are

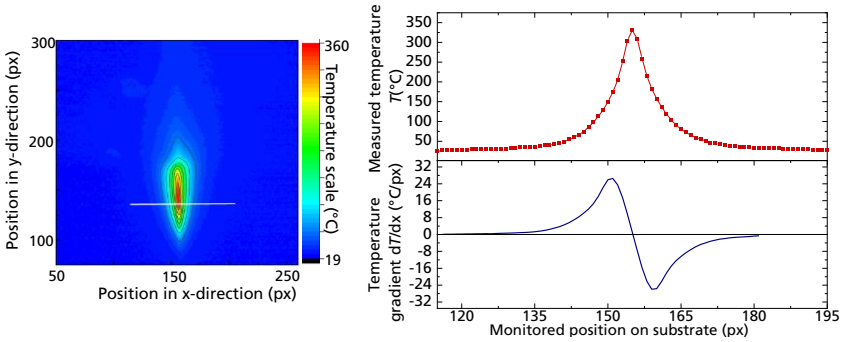


Fig. 5.3. Example of an infrared camera measurement result during the cleave process on a silicon substrate showing (a) the two-dimensional temperature distribution and (b) a plot of the position-dependent temperature profile and gradient along a chosen position (i.e., white line) shown in (a). Absolute temperature values are not accurate since no emissivity correction is performed.

also conducted to minimize the crack propagation deviation [30]. For the scribe process, the scribe laser power P_S, the scribe process velocity v_S, and frequency f_S can be considered as some of the essential parameters. A few of the key cleave process parameters are the cleave laser power P_C, cleave process velocity v_C, water flow w_C, air flow a_C as well as cleave laser ellipse length e_l and cleave laser ellipse width e_w. The ellipse can be adjusted by the cleave laser focus and the lens position. Additionally, the distance between the center of the ellipse and the cooling spot can be adjusted by the cooling nozzle position.

Variations of specific cleave process parameters are always to be considered in relation to others. For instance, as also mentioned in Ref. [30], the increase of e_w requires the increase of the P_C to achieve a successful crack propagation. The main functioning process parameters have been provided by the *3D-Micromac AG* with the commissioning of the machine in the *PV–TEC* laboratory.

Exemplary TLS parameter variation

As an exemplary investigation, the influence of the two process parameters initial scribe length l_S and P_C on the physical separation of PERC solar cells is performed. This is possible by varying each of them separately, while keeping the rest of the scribe and cleave process parameters constant. Apart from the successful physical separation, light microscope images show the structure of the obtained cell edges.

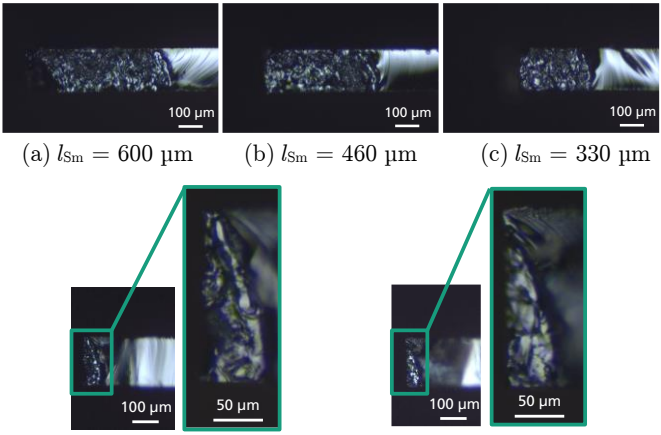
To investigate the impact of the l_S variation, the scribe process parameters $P_S = 10$ W, $f_S = 30$ kHz, and $v_S = 50$ mm/s are kept constant while l_S is varied prior to the cleave laser process. Five l_S values are considered for the variation, while the cleave process parameters are kept constant.

As a result, successful thermal cleaving (i.e., physical separation) is demonstrated independent from the studied l_S values. The measured scribe lengths $l_{Sm} = \{600\ \mu m, 460\ \mu m, 330\ \mu m, 65\ \mu m, 56\ \mu m\}$ can be seen in Fig. 5.4. This indicates that the crack intiation of even $l_{Sm} = 56\ \mu m$ is enough for a successful cleave process to take place for the considered set of parameters.

In the next investigation, the scribe and the cleave process parameters are kept constant, while P_C is varied. In total, five P_C values are considered.

As an outcome, the lowest tested P_C value (i.e., $P_C = 81$ W) does not lead to successful cleave processes considering the chosen set of parameters. In other words, no separation takes place. However, for $P_C = \{88\text{ W}, 112\text{ W}, 120\text{ W}\}$ the power is high enough for the successful separation leading to smooth solar cell edges; as shown in Fig. 5.5(a), (b), (c). In the case of $P_C = 170$ W, the very high laser power leads to the destruction of the solar cell as shown in the increased cell edge roughness in Fig. 5.5(d).

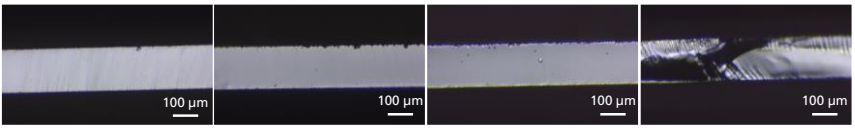
Considering their large impact on the thermal budget, the main process parameters that are varied in the following sections of the work are mainly P_C and v_C. The upcoming section deals with the impact of the TLS on the electrical performance of silicon solar cells.



(a) $l_{Sm} = 600$ µm (b) $l_{Sm} = 460$ µm (c) $l_{Sm} = 330$ µm

(d) $l_{Sm} = 65$ µm (e) $l_{Sm} = 56$ µm

Fig. 5.4. Light microscope images of silicon solar cell edges at the scribed position (initial crack). The scribe length l_S is varied from (a) to (e). Approximate measured l_{Sm} values are provided. All obtained l_{Sm} values lead to successful physical separation when followed by the cleave process.



(a) $P_C = 88$ W (b) $P_C = 112$ W (c) $P_C = 120$ W (d) $P_C = 170$ W

Fig. 5.5. Light microscope images of silicon solar cell edges because of the cleave power P_C variation in (a) to (d). Lower tested $P_C = 81$ W value does not lead to a separation. The highest $P_C = 170$ W leads to rough cell edges.

5.3 Thermal laser separation on passivated non-metallized precursors[4]

Although the TLS cleave process causes local heating that reaches temperatures below the melting point of crystalline silicon, the process can still have an impact on the already existing cell structures. High temperature laser-assisted processes that reach a few hundred degrees Celsius could degrade the surface passivation sustained by layers such as aluminum oxide (Al_2O_3), silicon nitride (SiN_X), silicon dioxide (SiO_2) for PERC solar cells, or hydrogenated amorphous silicon (a-Si:H) for silicon heterojunction (SHJ) solar cells [206, 207]. In this section, which is based on Refs. [204], the impact of the cleave laser process on non-metallized PERC and SHJ precursors is investigated with the aim of a substrate-tailored process optimization.

5.3.1 Method description for the cleave process optimization

For the complete separation of substrates by TLS, both the scribe and the cleave are required. If the scribe is not performed (i.e., a crack is not initiated), the cleave process by itself does not lead to separation. This allows the investigation of the cleave process without the additional contribution of edge-related defects. In other words, only the impact of the cleave process is observed while no influence of newly formed edges is present. The aim of the optimization is to have the least cleave process-induced degradation, with the main condition of having an effective

[4] Parts of this section are based on the publication stated in Ref. [204]. The author of this dissertation is the first author of the referenced paper. The cleave process optimization method is developed in the master thesis of A. Nair, stated in Ref. [205], that is co-supervised by the author of this dissertation.

mechanical separation. Taking the P_C parameter variation as an example, Fig. 5.6 shows a sequence considered for the parameter optimization.

For the spatially-resolved characterization of the local defects in silicon substrates, photoluminescence (PL) imaging technique is a suitable method; details about the technique and measurement setup are described in section 2.6.2. Since the cleave process induces a spatial local temperature increase (in the range of mm), PL imaging can detect and visualize the cleave process impact on the surface passivation properties. For a defined excitation irradiance at a fixed position on the substrate, PL signal counts $\varphi(x)$ are obtained.

Performing PL imaging before and after the cleave process variations on a precursor shows the impact of the process on $\varphi(x)$. Considering regions of interest (ROIs) at positions without non-cleave process-related defects allows the investigation of the cleave process itself; see Fig. 5.7. Averaging line scan ROIs before and after the cleave process provide the average $\varphi(x)$ before and after processing $\varphi_b(x)$ and $\varphi_a(x)$, respectively. The difference $\Delta\varphi(x)$ resulting from the cleave process is calculated by using

$$\Delta\varphi(x) = \varphi_a(x) - \varphi_b(x). \tag{5.1}$$

High $\Delta\varphi(x)$ values correspond to high drops visualized by lower signals after processing. Fig. 5.7 is a sample PL-based investigation of the P_C optimization keeping the rest of the process parameters unchanged. This method can also be used to optimize the rest of the cleave process parameters such as v_C, e_l, e_w, w_C, or a_C etc.

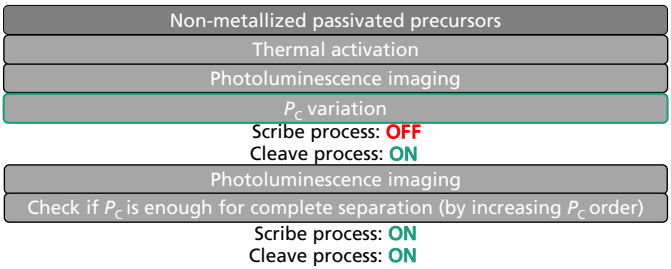


Fig. 5.6. Description of the cleave process development sequence taking the example of the P_C variation. Non-metallized passivated precursors that have undergone an intended passivation layer activation process (firing for PERC, curing for SHJ) are used. The figure is redrawn from Ref. [204].

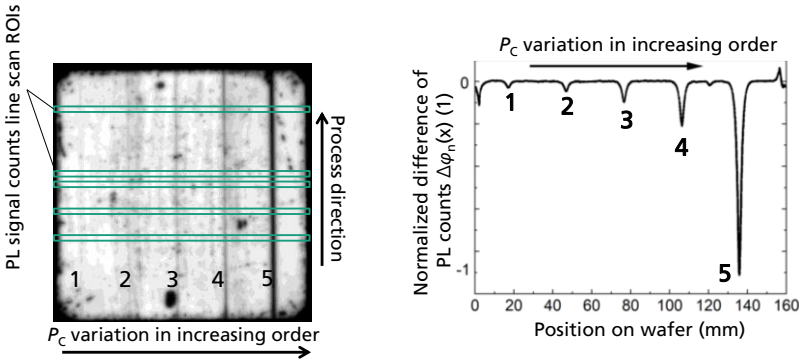


Fig. 5.7. Example of a cleave process optimization method (in this case P_C variation) for a SHJ passivated precursor. (a) A PL image of a sample after variation of the cleave process. The sample is measured at an irradiance of 0.75 suns that is equivalent to 461 W/m^2. The used suns equivalent is defined by a photon flux $\Phi = 2.5 \times 10^{17}$ photons(808 nm)/cm^{2}s^{-1}. Line spacing of 30 mm is considered between each of the five cleave lines 1 to 5. Noting that since only a cleave process is performed (i.e., no scribe process), the precursor is not separated and kept in a full wafer-sized format. (b) The position-dependent drops in the normalized PL signal counts $\Delta\varphi_n(x)$. The normalized drop of -1 corresponds to the highest signal drop among all the cleave lines, in this case for line 5. The figures are adapted from Ref. [204].

5.3.2 Sample preparation and experimental process flow

The method explained in the previous section is used to experimentally study the impact of the cleave process on PERC and SHJ passivated and non-metallized precursors.

The process flow is depicted in Fig. 5.8. The PERC precursors used in this experiment feature a *p*-type boron-doped Czochralski-grown silicon (Cz-Si:B) base. The rear side is passivated by an aluminum oxide (Al_2O_3) and silicon nitride (SiN_X) stack. The phosphorous-diffused *n*-type emitter is passivated by a SiN_X passivation layer. The activation of the passivation layers takes place in a fast firing oven with a typical temperature profile for PERC cells [141]. The samples are then treated with an ultrafast regeneration (UFR) process [142, 143]. Since the used UFR process does not lead to a 100% stable regeneration, an intended light-induced degradation under illumination is then perfomed. This stabilizes the boron-oxygen (B-O) state prior to the cleave laser processing. PL imaging is then performed before and after P_C variation. Only P_C values are varied while the other process parameters are kept constant. Five P_C values are consid-

ered ranging from 73 W to 103 W, at $v_C = 200$ mm/s. The characterized samples undergo a second UFR process followed by PL imaging.

A similar approach is adopted for the industrial SHJ precursors. These samples are fabricated on n-type Cz-Si wafers and feature a p-type emitter on the rear side. The precursors are coated by transparent conductive oxide layers on both sides. To see a schematic cross-section of the SHJ sample please refer to Ref. [208]. The passivation layer activation occurs in a curing process in an inline oven. PL imaging is performed before and after P_C variation. In this case also five P_C levels are considered ranging from 59 W to 88 W at $v_C = 250$ mm/s. The differences in the chosen P_C and v_C values for the two different cell architectures is a result of experience values from coarser parameter variations in previous experiments.

5.3.3 Results and discussion

As an exemplary result of the experiment, the PL image of a processed PERC precursor with five cleave lines is shown in Fig. 5.9. Part (a) of the figure, which is the upper half, shows the result right after the cleave process P_C variation. Part (b), the bottom half, shows the result after the additional UFR process. The cleave process induces lower $\varphi(x)$ values on the wafer in (a) shown by the darker lines (i.e., drop in the PL signal counts $\Delta\varphi(x)$). The drop $\Delta\varphi_n(x)$ is proportional to the P_C values; see

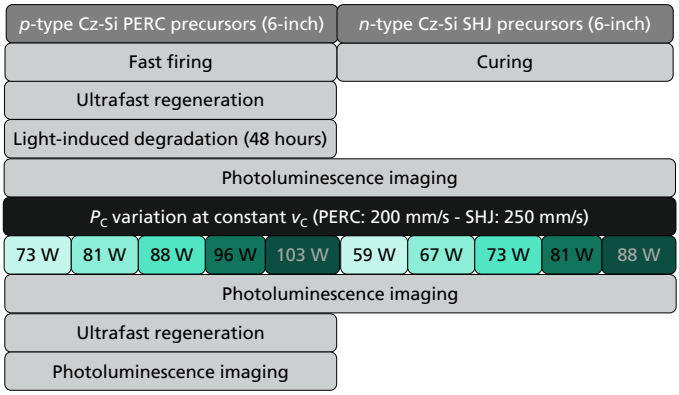


Fig. 5.8. Experimental process flow for the investigation of the cleave process impact on p-type Cz-Si:B PERC and n-type Cz-Si SHJ precursors without metallization. The cleave process is performed on the emitter-free sides, i.e., the rear side for the PERC precursors and the front side of the SHJ precursors. The figure is redrawn from Ref. [204].

Fig. 5.9(c). However, the PL image shown in (b), which is obtained after the second UFR process, shows that the dark lines have disappeared. The line scan profile shown in Fig. 5.9(d) also depicts a more or less constant normalized PL signal counts $\varphi_n(x)$ after UFR.

From the chosen P_C values in this experiment, a successful separation process is attained at 88 W, 96 W, and 103 W in case the scribe process is performed. These P_C values are marked in green rectangle borders in Fig. 5.9. Although each of the three P_C levels can be considered for further processing, the $P_C = 88$ W is chosen as the optimum one (used in the upcoming section to process metallized PERC host cells).

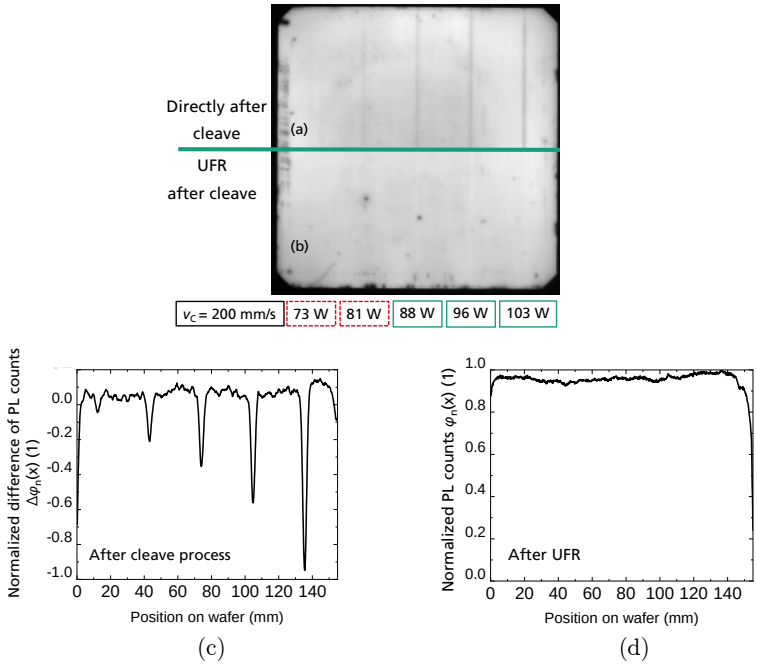
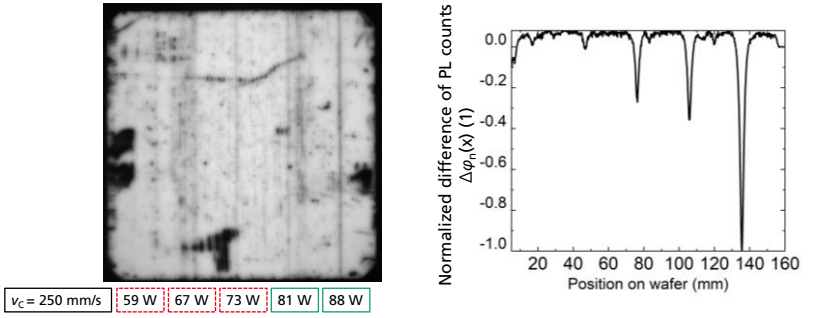


Fig. 5.9. (a) PL image of a processed passivated *p*-type Cz-Si:B PERC precursor directly after the cleave process (top part of the image), (b) PL image of the same wafer after the additional UFR process (bottom part of the image). The measurements are conducted at an irradiance of 1 suns equivalent to 651 W/m^2. The P_C values leading to a complete separation in case the scribe process is performed are marked in green rectangle borders, the rest are marked in red with dashed rectangle borders. (c) Position-dependent $\Delta\varphi_n(x)$ after the cleave process. (d) Average position-dependent $\varphi_n(x)$ after the additional UFR process. The figures are adapted from Ref. [204].

Possible explanations for the reversible signal reduction induced by the cleave process are: (i) The activation of the B-O complex by the cleave laser process leading to light-induced degradation (LiD), (ii) temporary reduction in the surface passivation quality, or (iii) a combination of both. This also implies that the additional UFR process after the cleave either (i) regenerates the LiD-projected zones, (ii) locally improves the surface passivation or, (iii) results in a combination of regeneration of the bulk and repassivation of the surface. Further experimental investigations are required to understand the nature of the reversible signal reduction because of the cleave process. Nevertheless, there are no cleave process-induced permanent defects present on PERC precursors with the chosen cleave process parameters.

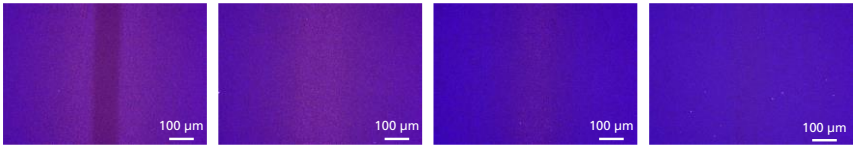
In the case of the SHJ precursor, Fig. 5.10(a) and (b) show the impact of the cleave process in the PL image and the drop $\Delta\varphi_n(x)$ as a function of the position on the substrate, respectively. The results show higher local $\varphi_n(x)$ drops with higher P_C values. P_C values below 81 W do not lead to a complete mechanical separation in case the scribe process is also performed. For that reason, within the considered variation, $P_C = 81$ W is chosen as the optimum value at $v_C = 250$ mm/s.

The light microscope images in Fig. 5.11(a) to (d) show the impact of cleave processes performed with different P_C values. The process optimization leads to the reduction of cleave process-induced damage.



(a) (b)

Fig. 5.10. (a) PL image of a processed *n*-type Cz-Si passivated SHJ precursor measured after the cleave process variation. The SHJ passivated precursor is measured at an irradiance of 0.75 suns equivalent of 461 W/m². The P_C values leading to a complete separation in case the scribe process is performed are marked in green rectangle borders, the rest are marked in dashed red rectangle borders. (b) Position-dependent drops $\Delta\varphi_n(x)$ after the cleave process. The figures are adapted from Ref. [204].



(a) (b) (c) (d)

Fig. 5.11. Light microscope images of cleave lines displaying the impact of the cleave laser process on SHJ precursors. Specific examples of cleave lines as a result of (a) a non-optimized cleave process with a very high thermal budget, (b) a non-optimized cleave process with reduced thermal budget, (c) an optimized cleave process, and (d) a cleave process with a very low resultant thermal budget. The very low thermal budget does not lead to a separation in case the scribe process is also performed. The analysis based on PL images, not shown in these images, allows the deeper investigation of the cleave process impact on the possible laser-induced defects.

As an explanation of the observed results, the a-Si:H passivation layers in the SHJ samples are known to degrade at temperatures above 200°C [106]. This degradation because of the cleave process is proportional to the increase in the local temperature with increasing P_C. Regardless of the degradation shown in the results, the optimum P_C is obtained and used also as a process parameter for further processing of metallized host cells.

5.4 Thermal laser separation on solar cells[5]

The aim of this section is to demonstrate the impact of the cleave process and the impact of the complete TLS process on solar cell output parameters.

5.4.1 Method description

To study the influence of the cleave process only, the scribe is not performed at all, meaning the scribe laser is kept off and only the cleave process is performed; see also Fig. 5.12. To study the impact of the complete TLS process (i.e., after the formation of the new edges), measurements before and after the scribe and cleave processes are performed. As discussed in section 2.4.4, the SunsV_{OC} measurements provide the pseudo fill factor *pFF* and the open-circuit voltage V_{OC}. Measuring host cells before and after processing provides *pFF* before and after processing,

[5] Parts of this section are based on the publication stated in Ref. [204]. The author of this dissertation is the first author of the referenced paper.

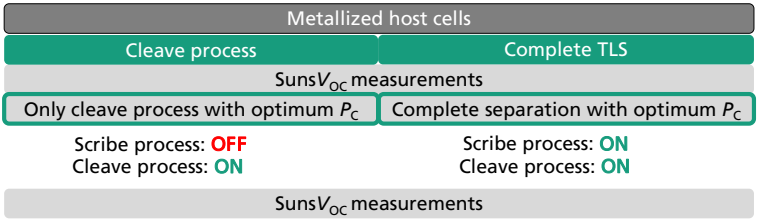


Fig. 5.12. Description of the method to examine the impact on metallized host cells from (left) the cleave process only (no scribe) in comparison to the (right) complete TLS process (scribe and cleave) that leads to separated cells. Cells with the complete TLS process feature also the newly formed edges. For the cleave process in both groups, the optimum is considered, for example the cleave power P_C, determined in the previous section (from Fig. 5.7), is used. The figure is redrawn from Ref. [204].

the mean values are denoted as pFF_b and pFF_a, respectively. The change in pFF, i.e., ΔpFF, is then obtained by the difference of the mean values after and before processing,

$$\Delta pFF = pFF_a - pFF_b. \tag{5.2}$$

Analogously, the impact on V_{OC} can be obtained by calculating the difference

$$\Delta V_{OC} = V_{OCa} - V_{OCb}, \tag{5.3}$$

where V_{OCa} and V_{OCb} are the mean open-circuit voltage values after and before processing, respectively.

5.4.2 Cell fabrication and experimental process flow

An experiment considering the optimized cleave processes, for the two cell architectures PERC and SHJ from section 5.3, is performed. Both the cleave process (without the initial scribe), and the complete TLS (with both laser processes) are considered in the experiment. To start with, a cell batch considering half cell and shingle cell layouts are considered for each of the two cell types.

Host cell fabrication

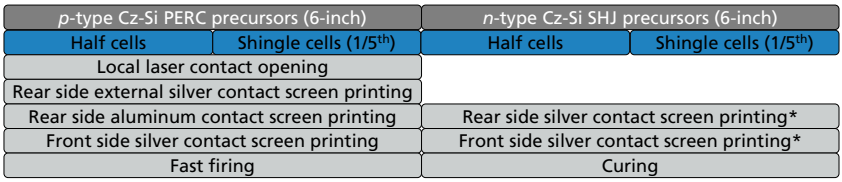
For the fabrication of monofacial PERC host cells for both half cell and shingle cell formats, industrial 6-inch p-type Cz-Si:B PERC precursors with passivation layers on both sides are used. These precursors are like the ones used in section 5.3.2. The process flow for the PERC host cell

fabrication is shown in Fig. 5.13(a). The first step is the local laser contact opening followed by the rear side screen printing processes of the external silver contacts and the full-area aluminum cell contacts. The front side silver finger grid is then screen printed afterwhich the metallized samples undergo the firing process. The host cell with the half cell metallization grid is a twelve-busbar layout and features a metal-free gap in the wafer center; see Fig. 5.14(a). The host cell with the shingle metallization grid features a metallization layout to obtain five shingle cells with 31.35 mm widths (i.e., also called $1/5^{\text{th}}$ format shingle cells). Four metal-free gaps are kept as separation paths; see Fig. 5.14(b). Three cells out of the five are identical with designed areas of 31.35 mm x 156.75 mm, while the other two feature pseudo square edges.

For the fabrication of bifacial SHJ host cells for both half and shingle formats, industrial precursors similar to the ones used in section 5.3 are considered. The fabrication process flow is shown in Fig. 5.13(b). The rear side and the front side metallization finger grids are screen printed using low temperature silver pastes [209]. The metallization layout for the half cell format features a six busbar layout on the front and rear; see Fig. 5.14(c). The shingle format features an identical metallization layout for the front and the rear. The finger grid layout used for the PERC front side is used in this case. Five strip cells are obtained from each fabricated host cell (i.e., $1/5^{\text{th}}$ shingle layout); see Fig. 5.14(d).

Experimental process flow

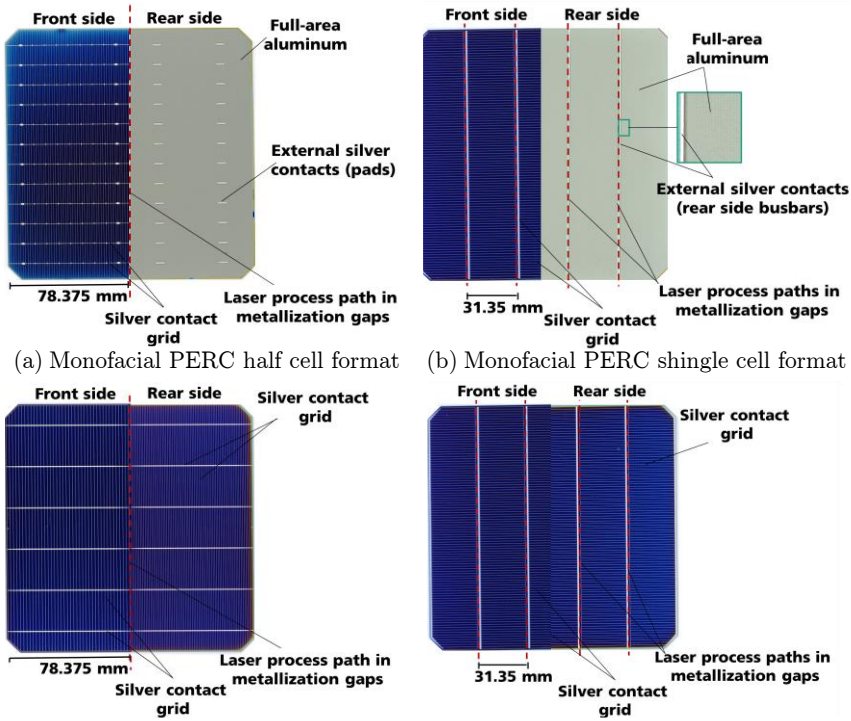
Considering the introduced method of section 5.4.1, an experiment is designed in which the PERC and SHJ host cells are processed; see Fig. 5.15. For each of the cell metallization formats and cell architectures, SunsV_{OC} measurements are performed before and after processing.



(a) (b)

Fig. 5.13. Process flow for the fabrication of monofacial p-type Cz-Si PERC and bifacial n-type Cz-Si SHJ host cells starting from 6-inch industrial passivated precursors. The figure is redrawn from Ref. [204].

The busbars are contacted at identical positions before and after processing and a reference cell not undergoing any process steps is measured to monitor the reproducibility of the results (i.e., not shown in the process flow).



(a) Monofacial PERC half cell format (b) Monofacial PERC shingle cell format

(c) Bifacial SHJ half cell format (d) Bifacial SHJ shingle cell format

Fig. 5.14. Front side and rear side photographs of the fabricated Cz-Si host cells. Monofacial *p*-type PERC solar cell with (a) a half cell format and (b) a shingle cell format. Bifacial *n*-type SHJ solar cell with (c) a half cell format and (d) a shingle cell format. The figures are adapted from Ref. [204].

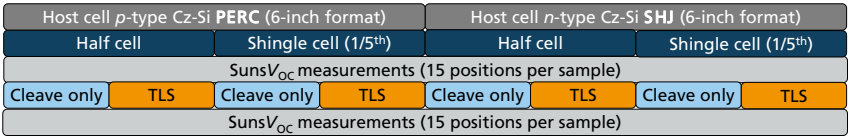


Fig. 5.15. Experimental process flow investigating the impact of: (i) only the cleave process and (ii) the complete TLS on PERC and SHJ host cells with half cell and shingle cell metallization formats. SunsV_{OC} measurements are performed before and after processing at 15 measurement positions. The figure is redrawn from Ref. [204].

5.4.3 Results and discussion

In the case of PERC solar cells, the V_{OC} and pFF values extracted from the SunsV_{OC} measurements are plotted in Fig. 5.16(a) and (b), respectively.

The results before and after processing are shown for both the half cell and the shingle cell formats. Before processing, the host cells with half cell metallization layout feature a mean $V_{OC} = (672 \pm 3)$ mV and a mean $pFF = (83.3 \pm 0.3)\%$. The cleave process leads to mean drops in V_{OC} and pFF of only $\Delta V_{OC} = -1$ mV and $\Delta pFF = -0.1\%_{abs}$. After separation, the cells that undergo the complete TLS process show $\Delta V_{OC} = -2$ mV and $\Delta pFF = -0.2\%_{abs}$. Considering the PERC cells with shingle formats, the group of cells that undergo only the cleave process show no drop in V_{OC} and only a slight reduction in pFF of $\Delta pFF = -0.1\%_{abs}$. The complete TLS leads to the formation of separated shingle cells and the drops are found to be $\Delta V_{OC} = -1$ mV and $\Delta pFF = -0.3\%_{abs}$.

As a result of the investigation on PERC cells, it is shown that the cleave process itself has a lower impact on the reduction in pFF in comparison to the impact of the complete TLS process. This is demonstrated especially in the case of the shingle cells where around $67\%_{rel}$ of the pFF loss is attributed to the creation of newly formed cell edges.

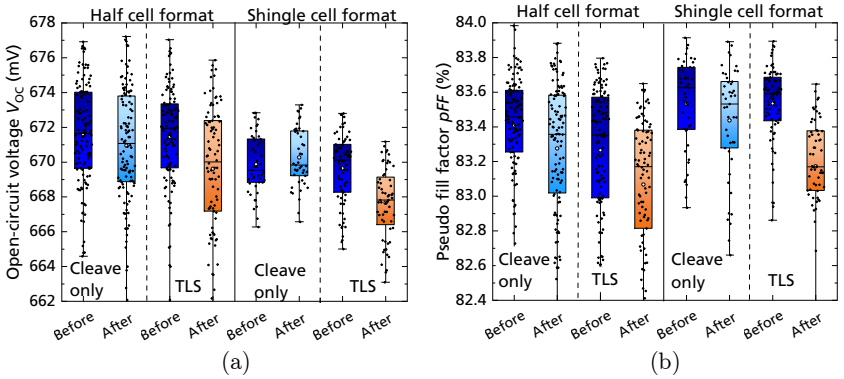


Fig. 5.16. SunsV_{OC} measurement results showing the (a) V_{OC} values and the (b) pFF values of PERC cells. The median is shown by a horizontal dash while the mean is depicted by a point. The highest and lowest data point values (i.e., box plot boundaries) represent the maximum and the minimum, respectively. Data from Ref. [204].

For the SHJ cells, the SunsV_{OC} measurement results are plotted in Fig. 5.17(a) and (b). It is well-known that SHJ solar cells feature generally higher V_{OC} and *pFF* values compared to PERC cells [210]. The mean V_{OC} and *pFF* values of the half cell format host cells before processing are (738 ± 2) mV and (84.2 ± 0.3)%, respectively. The cleave process results in drops of $\Delta V_{OC} = -2$ mV and $\Delta pFF = -0.1\%_{abs}$. The complete separation shows a higher drop quantified by $\Delta V_{OC} = -4$ mV and $\Delta pFF = -0.4\%_{abs}$. In the case of host cells with shingle cell format, the cleave process leads to $\Delta V_{OC} = -2$ mV and $\Delta pFF = -0.3\%_{abs}$. In contrast, the complete TLS results in a severe reduction with $\Delta pFF = -2.1\%_{abs}$, whereas $\Delta V_{OC} = -3$ mV is comparable to the drop measured for the only cleave-processed group.

Although the drops in V_{OC} are comparable among the only cleaved and complete TLS-processed cells, the *pFF* values of half cells and shingle cells are lower. This drop is attributed to edge recombination losses because of the newly formed unpassivated edges. In the case of the shingle cells, the drop in *pFF* is even more severe in comparison to that of the half cells. That is the case due to the higher separated perimeter-to-cell area ratio (i.e., smaller cell sizes). The loss is more noticeable on the *pFF* value where non-ideal recombination quantified by j_{02}-related losses are accounted for.

As a general outcome, the highest cleave process-related losses are recorded in the SHJ cells with the shingle format that encompass four processed

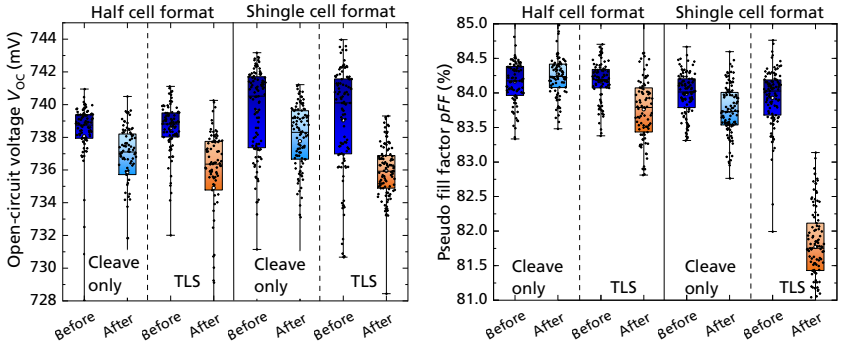


Fig. 5.17. SunsV_{OC} measurement results showing the (a) V_{OC} values and the (b) *pFF* values of SHJ cells. The median is shown by a horizontal dash while the mean is depicted by a point. The highest and lowest data point values (i.e., box plot boundaries) represent the maximum and the minimum, respectively. Data from Ref. [204].

cleave lines. The losses because of the only cleave process can be attributed to the surface passivation degradation of temperature-sensitive a-Si:H layer passivation. Moreover, the complete separation by TLS leads to around 86%$_{\mathrm{rel}}$ of the measured *pFF* loss. This loss is attributed to the creation of the new unpassivated edges. The larger drops in the SHJ-separated cells (in comparison to PERC-separated ones) can be clarified by three possible causes. The first one is the initial V_{OC} level differences between the two cell concepts indicating higher relative losses for SHJ cells. The higher V_{OC} levels of SHJ solar cells imply that they feature a lower saturation current density j_0. The edge recombination represented by an edge-related recombination current per length $j_{0,\mathrm{edge}}$ has a higher share on the overall performance for cells with initially lower j_0. The second reason might be the structural differences of the cell architectures. An example of such a structural difference is that SHJ solar cells feature transparent conductive oxide (TCO) layers which, apart from the metallization, are responsible for the lateral conduction of charge carriers (also to the separated newly formed edges). This is different from the PERC cell with a diffused emitter which is also highly conductive leading to the flow of charge carriers to the separated edge. The structural differences of the conductive layers might lead to different edge recombination mechanisms which have unalike impacts. The reason behind the different drops might also be, thirdly, a combination of both previously mentioned causes. This research topic is being further investigated in a running dissertation work by *Stolzenburg* aiming towards the advanced characterization of edge recombination [211].

The SunsV_{OC} measurements serve the purpose of characterizing changes caused by the separation processes. The approach also considers cell position-dependent measurement contacting points. However, illuminated IV measurements of solar cells are necessary to observe energy conversion efficiencies η, which unlike SunsV_{OC} measurements take series resistance r_{S} losses into account. For the IV measurements, only completely separated PERC and SHJ shingle cells are measured, due to the identical front side metallization layout of the cells. The identical shingle cell layout gives the possibility of measuring the cells by using the same contacting scheme; as shown in section 4.4.1. The measurements are conducted monofacially at an irradiance $G_{\mathrm{front}} = 1000\ \mathrm{W/m^2}$, by contacting the rear side and front side busbars by IV-pin arrays.

Table 5.1. IV data for the fabricated p-type Cz-Si PERC and n-type Cz-Si SHJ shingle solar cells. The monofacial measurements are performed from the front side. Measurement results of the designated area (i.e., excluding the busbar area) are given since the busbars are intended to be covered by shingling. Measured total cell area is $A_{\mathrm{tot}} = 4918$ mm^2. The cell tester is calibrated by using a reference PERC shingle cell measured at *Fraunhofer ISE CalLab PV cells*. Data from Ref. [204].

Cell type	η_{des} (%)	V_{OC} (mV)	$j_{\mathrm{SC,des}}$ (mA/cm^2)	FF (%)	pFF (%)	r_{S} (Ωcm^2)
Monofacial p-type Cz-Si PERC shingle solar cell						
Mean	21.1 ± 0.1	665 ± 2	39.6 ± 0.1	80.0 ± 0.2	82.5 ± 0.2	0.60 ± 0.00
Highest	21.2	668	39.8	79.9	82.7	0.58
Bifacial n-type Cz-Si SHJ shingle solar cell						
Mean	21.4 ± 0.1	732 ± 1	37.5 ± 0.0	78.0 ± 0.2	81.8 ± 0.2	0.90 ± 0.00
Highest	21.5	734	37.6	78.1	81.7	0.92

The non-reflective background ensures that no additional reflection from the rear side contributes to the measurement. The IV measurement results are shown in Table 5.1.

In case of the PERC shingle cells, a peak front side designated area efficiency of $\eta_{\mathrm{des}} = 21.2\%$ with a mean value of $(21.1 \pm 0.1)\%$ is attained. In this batch, SHJ shingle solar cells achieve a maximum $\eta_{\mathrm{des}} = 21.5\%$ with a mean value being $(21.4 \pm 0.1)\%$. Improvements in the pFF values are expected with the integration of edge passivation methods.

5.5 Comparison of separation processes

As mentioned in section 5.2, TLS-separated half cells are mechanically more stable than LSMC-separated ones [195, 196]. In this dissertation, the process impact on the electrical performance of silicon solar cells is investigated. This section examines the differences between the separation processes by fabricating pSPEER solar cells as well as small-sized cells with various sizes.

5.5.1 Laser-assisted separation of *p*SPEER solar cells[6]

The impact of the LSMC and the TLS separation technique are studied on *p*SPEER solar cells. This subsection is based on the publication in Ref. [194]. In the LSMC process, the laser scribing along the separation path is the main laser process involved. In the case of the TLS, the scribe laser process is responsible for the crack initiation (i.e., typically up to a few hundred micrometers in length). Then, the cleave process along the whole separation path is the main laser process that leads to the crack propagation and separation.

Cell fabrication and experimental process flow

For the investigation, a cell batch is conducted starting from industrial *p*-type 6-inch Cz-Si:B PERC precursors. Fig. 5.18(a) shows the experimental process flow. First the local laser contact opening is performed on the rear side, followed by the rear side screen printing of the external silver busbars and the aluminum finger grid. Then, the front side silver grid is screen printed. The metal-semiconductor contact is then formed in an industrial fast firing oven. The metallization layout used in this batch is the *Gen5* layout. Details about the metallization layout can be found in Appendix A.3. Fig. 5.18(b) shows photographs of the host cell's front and rear side.

Each host cell includes five *p*SPEER solar cells with the perimeter dimensions 22 mm x 156.75 mm. The host cells then undergo ultrafast regeneration followed by light-induced degradation (LiD), to end up in a stable B-O complex-related state. The host cells are then characterized by SunsV_{OC} measurements using a *Grid*$^{\mathrm{TOUCH}}$ contacting unit. Finally, the host cells are sorted such that in all the groups in the experiment the average *pFF* values of the host cells are similar.

[6] Parts of this section are published in Ref. [194]. The author of this dissertation, as the second author of the paper, contributed to the scientific advancement by co-designing the experiment.

The main laser process in the LSMC technique is the scribe laser process, while the main one in the TLS is the cleave laser process. To study the impact of the main laser processes in Group 1, only the scribe or only the cleave is performed on host cells. Group 2 investigates the impact of the complete separation processes from the front and the rear side. After processing, all cells again undergo LiD for 48 hours. Since the IV-pin contacting is not compatible to the host cell's metallization layout, the processed host cells from Group 1 undergo SunsV_{OC} measurements using a *Grid*^{TOUCH} contacting unit. Reference host cells that do not undergo laser processing are also measured to monitor the reproducibility of the measurement. The completely separated cells of Group 2 undergo illuminated IV measurements. The front side and rear side busbars are contacted by IV-pin arrays. With the available setup, the contacting of separated shingle cells by means of *Grid*^{TOUCH} is not possible. The IV measurements are performed monofacially at an irradiance $G_{front} = 1000\ W/m^2$.

Results and discussion

The SunsV_{OC} measurement results of Group 1 are shown in Fig. 5.19(a) and (b). The cells that undergo the cleave process from the front side or the rear side show no changes in V_{OC}. For the cells cleaved from the front side $\Delta pFF = -0.2\%_{abs}$ is shown, while the ones cleaved from rear side record $\Delta pFF = -0.1\%_{abs}$ after processing. In the case of the cells that are

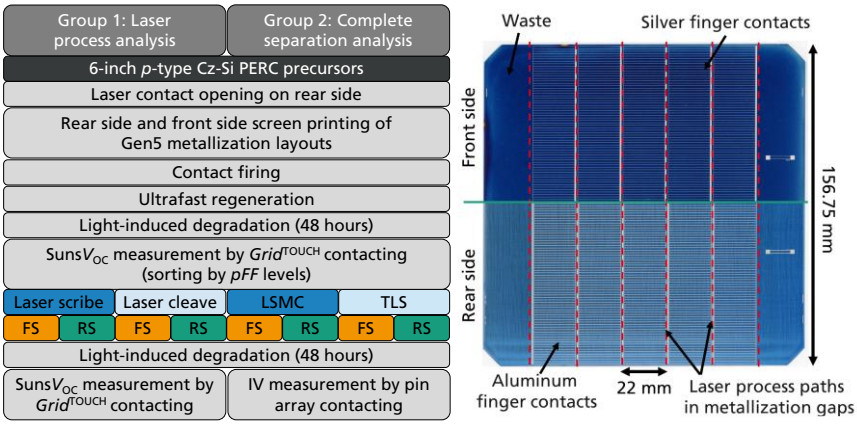


Fig. 5.18. (a) Schematic process sequence for the comparison of the laser-assisted separation processes. (b) Photograph of the front side (FS) and rear side (RS) of the host cell metallized with the *Gen5* metallization layout. The figures are redrawn from Ref. [194].

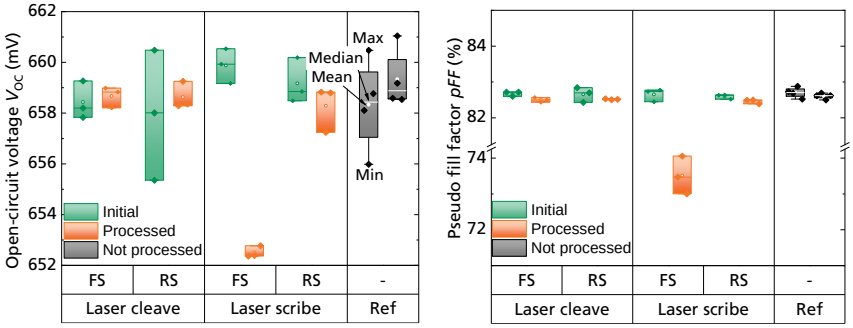


Fig. 5.19. SunsV_{OC} measurement data for the investigation of the impact of the laser processes on fabricated host cells showing (a) V_{OC} and (b) pFF before and after processing. Reference cells (Ref) are measured to monitor the reproducibility of the measurement. The SunsV_{OC} measurements are performed using the *Grid*^{TOUCH} contacting unit. FS and RS indicate the side from which the host cells are processed. The figures are redrawn from Ref. [194].

laser-scribed from the front side, drops quantified by $\Delta V_{OC} = -7$ mV and $\Delta pFF = -9.1\%_{abs}$ are measured. The cells that are scribed from the rear side show only $\Delta V_{OC} = -1$ mV and $\Delta pFF = -0.1\%_{abs}$. The reference cell shows changes of ΔV_{OC} and ΔpFF being 2 mV and $-0.1\%_{abs}$, respectively.

In the case of cells processed by laser scribing from the front side (i.e., emitter side), the substantial drops in V_{OC} and pFF are caused by the destruction of the *pn*-junction. The impact of the laser scribing process is much lower when the processing is done from the rear side. However, a damage of the rear side passivation layers still leads to the minor drops. The cleave process from both sides show minor reduction in pFF. Hence, this experiment shows that the cleave process itself has low impact on the surface passivation of the PERC host cells. The result is independent from the processed cell side.

The IV data of separated cells from Group 2 are plotted in Fig. 5.20. Since the contacting methods before and after processing are not identical, only the results among the separated cells can be compared. Independent from the separation process used, the designated area short-circuit current density and the series resistance (not shown) are measured to be around $j_{SC,des} = 40.6$ mA/cm^2 and $r_S = 0.4$ Ωcm^2, respectively.

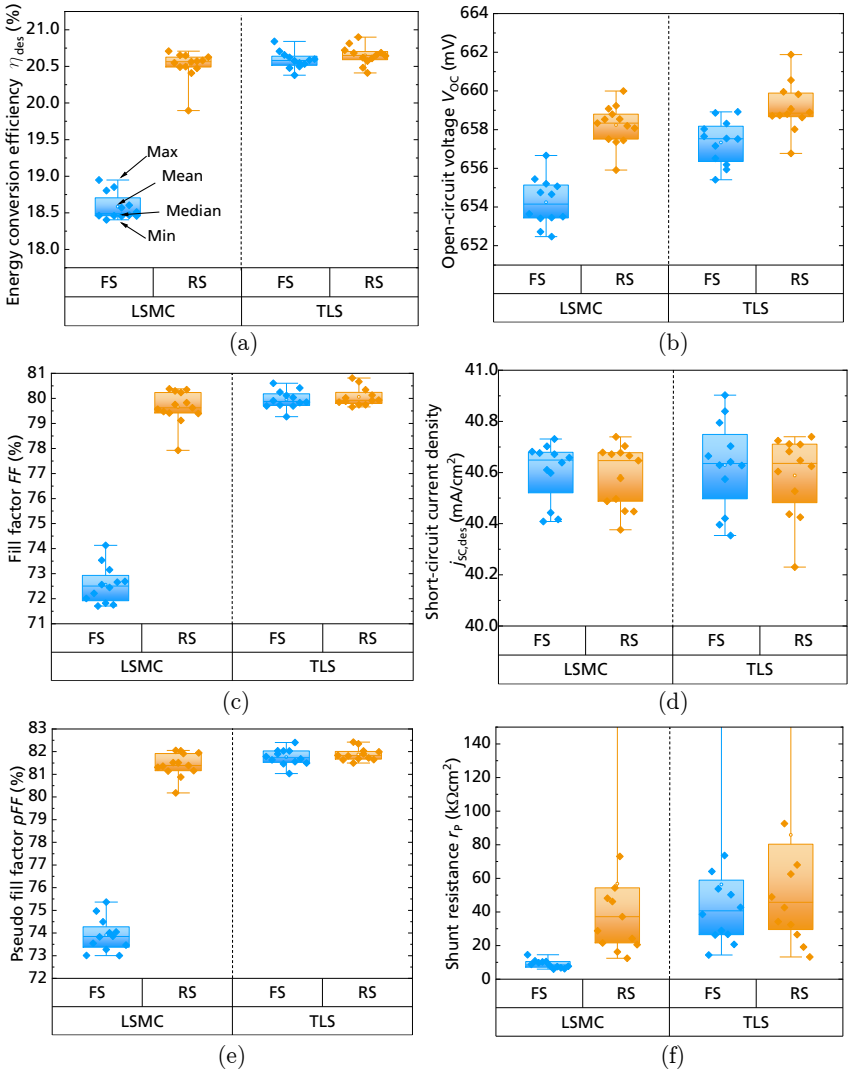


Fig. 5.20. IV data showing the results of Group 2: (a) Designated area energy conversion efficiency η_{des}, (b) open-circuit voltage V_{OC}, (c) fill factor *FF*, (d) designated area short-circuit current density $j_{SC,des}$, (c) pseudo fill factor *pFF*, and (f) parallel (shunt) resistance r_p. For the designated area data, the busbar area is excluded. The total cell area is $A_{tot} = 3449$ mm^2. FS and RS stand for the front side and rear side laser processing sides, respectively. The figures are redrawn from Ref. [194].

The cells separated by LSMC from the front side show the lowest designated area cell efficiencies with a mean value of $\eta_{\mathrm{des}} = 18.5\%$. These cells feature the lowest mean $pFF = 73.9\%$. The low pFF is the main reason for the low FF results, despite the relatively low $r_{\mathrm{p}} = 9\ \mathrm{k\Omega cm^2}$ among the separated cell groups. The cells separated by LSMC from the rear side and by TLS from either side have mean η_{des} values ranging between 20.5% and 20.7%. Mean pFF values range between 81.4% and 81.9%. Still, it is explicit that the TLS process can be processed from both the front and the rear side. That is due to the non-ablative nature of the process that has a very low impact on the *pn*-junction and/or the surface passivation of PERC host cells. Whereas to have lower recombination, the ablative scribing of the LSMC process should be conducted from the rear side, i.e., the emitter-free side.

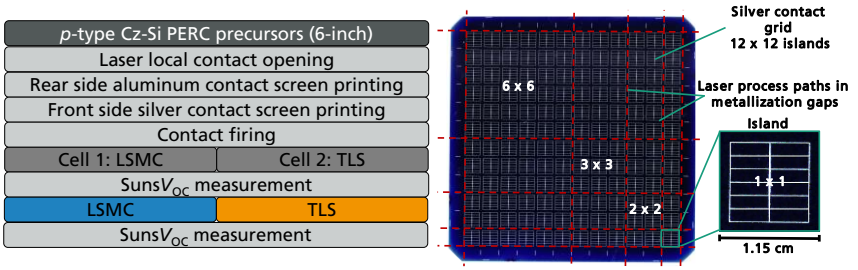
5.5.2 Small-sized solar cells with large perimeter-to-area ratios[7]

A more accurate comparison between the separation processes can be done by the fabrication of cells with different separated perimeter-to-area ratios k, that is calculated by equation (3.2). As explained in section 3.4, an increase of k strongly influences the impact of edge recombination on the global cell output parameters. Additionally, edge recombination is detected on the open-circuit voltage $V_{\mathrm{OC,low}}$ measured at low illumination (e.g., at around $G_{\mathrm{front}} = 100\ \mathrm{W/m^2}$). An experiment is conducted by fabricating cells with different sizes using each of the separation processes.

Host cell fabrication and experimental process flow

For the investigation, industrial 6-inch gallium-doped Cz-Si (Cz-Si:Ga) PERC precursors are used. The fabrication process sequence is illustrated in Fig. 5.21(a). After the local laser contact opening on the rear side, the rear side aluminum and front side silver contacts are screen printed, followed by the contact firing step. For this experiment, the rear side external silver contacts are not required. The metallization layout is designed to obtain 12 x 12 identical contacted "islands" on each host cell; as shown in Fig. 5.21(b). Each island has a designed area of $A_{\mathrm{tot}} = 1.15\ \mathrm{cm} \times 1.15\ \mathrm{cm} \approx 1.32\ \mathrm{cm^2}$ (i.e., around 0.5% of the host cell

[7] The approach and results are presented in PV magazine webinar "Cutting out the cracks: Advantages of thermal stress cutting" on June 3rd, 2021.



(a) (b)

Fig. 5.21. (a) Schematic process sequence for the comparison of the laser-assisted separation processes for the fabrication of small-sized solar cells. (b) Photograph of the host cell's front side with a "12 x 12 island" metallization layout. Each island has a total area A_{tot} = 1.15 cm x 1.15 cm ≈ 1.32 cm².

area). Separation path gaps are also considered between the islands. Since Cz-Si:Ga material is used for the cell fabrication, B-O complex-related LiD does not have to be considered.

To perform the comparison analysis, the host cells are measured by SunsV_{OC} measurements before processing using the offline setup and the contacting probe; see the setup explanation in section 2.4.4 and the measurement approach in section 4.4.2. For each of the separation processes, identical separation patterns are considered to obtain the same cell sizes from each of the LSMC and TLS-processed host cells. In total, four smaller cell sizes, that correspond to four k values, are obtained from each host cell as shown in Table 5.2. The separation takes place from the rear side. After the separation, the separated cells are measured again by the SunsV_{OC} technique.

Results and discussion

The SunsV_{OC} measurement results showing the reduction in $V_{OC,low}$, i.e., $\Delta V_{OC,low}$, and ΔpFF are depicted in Fig. 5.22(a) and (b), respectively. For the smallest cell size that features k = 0.347 mm^{-1}, the LSMC-separated cell shows a $\Delta V_{OC,low}$ = – 29 mV and ΔpFF = – 5.3%$_{abs}$, while the TLS-separated one yields lower losses, namely $\Delta V_{OC,low}$ = – 23 mV and ΔpFF = – 3.2%$_{abs}$. This indicates that for the case of the LSMC-separated cell, the $V_{OC,low}$ drop of around 5%$_{rel}$ and the pFF drop of around 6%$_{rel}$ from the host cell is recorded. The TLS-separated one shows lower drops of 4%$_{rel}$ in V_{OC} and 4%$_{rel}$ in pFF. For those cells, the TLS-separated cell shows

Table 5.2. Details about the fabricated cell patterns obtained for the separation process comparison. The host cell dimensions are provided for comparison purposes. The given values are nominal layout designed values.

Cell pattern	Host cell	1	2	3	4
Number of cell "islands"	12 x 12*	6 x 6	3 x 3	2 x 2	1 x 1
Edge length (cm)	156.75	6.9	3.45	2.3	1.15
Total cell area A_{tot} (cm^2)	244.32	47.61	11.90	5.29	1.32
Perimeter-to-area ratio k (cm^{-1})	-	0.58	1.16	1.74	3.47

*In total 144 islands are printed on the host precursor leaving non-metallized areas. The measurement of the host is not included in the analysis.

an advantage in comparison to the LSMC-separated one, quantified by the 6 mV and 2.1%$_{abs}$ higher values.

As thoroughly investigated in previous works [15, 16, 21, 169], also discussed in section 3.4, the increase of the k value leads to drops in V_{OC} and pFF as a result of edge recombination. The comparison between both separation processes shows that for the PERC cells considered in this experiment, TLS-separated cells show a lower drop in V_{OC} and pFF. This behavior is shown especially on the smallest cell sizes with the highest k. This difference in results comparing the two separation techniques implies the higher defects induced by the LSMC. Scanning electron microscope (SEM) images in Fig. 5.23(a) and (b) show the structure of cell edges separated by LSMC and TLS respectively.

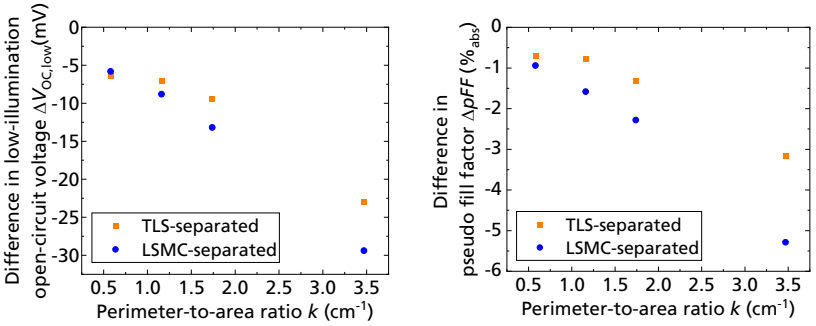
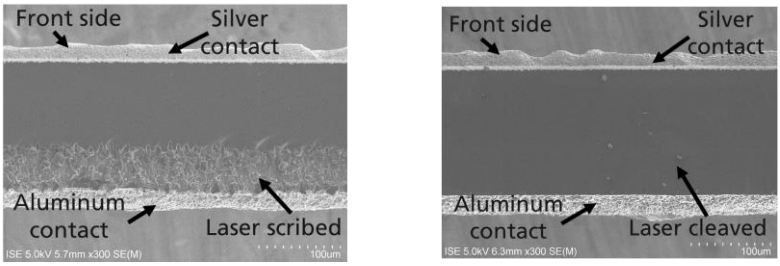


Fig. 5.22. Analyzed Suns V_{OC} measurement results showing (a) $\Delta V_{OC,low}$ and (b) ΔpFF obtained for PERC cells separated by either LSMC or TLS. Four cell sizes are considered.



(a) (b)

Fig. 5.23. SEM images of: (a) an LSMC-separated cell edge and (b) a TLS-separated cell edge. Both cells are laser-processed from the rear side. Figures are adapted from Ref. [194].

The LSMC-separated cell shows around one-third of the cell edge to be 'rough' as a result of the ablative process. The remainder of the edge is smooth due to the mechanical cleaving step. The 'rough' scribed region creates a larger recombinative surface area with edge defects. In contrast, the TLS-separated cell edge shows a rather smooth edge obtained from the non-ablative process, which leads to a smaller surface area and subsequently less recombination. It is evident that the question of silicon solar cell edge defects becomes more critical with the decrease in cell sizes.

5.6 Chapter summary

For the fabrication of separated silicon solar cells, such as half cells and shingle cells, the separation process is commonly performed after contact formation. This chapter provides an overview of separation techniques in the semiconductor industry in general and for solar cell fabrication in particular. Two of the common laser-assisted processes for the separation of silicon-based solar cells are laser scribing and mechanical cleaving (LSMC) and thermal laser separation (TLS). LSMC encompasses two process steps involving the ablation of, e.g., around one-third of the substrate thickness by means of a pulsed laser while the rest is mechanically cleaved. The TLS process also takes place in two process steps including the crack initiation by a scribe laser (i.e., a few hundred micrometers in length) and a subsequent cleave process along the desired separation path by means of a continuous wave laser heating and water/air cooling. The thermal gradient leads to the kerfless, non-ablative separation. The physical separation takes place even by having a scribe (crack initiation)

length as short as $l_{Sm} = 56$ µm. Too high cleave power P_C leads to rough solar cell edges with high defects.

The TLS cleave process window for the physical separation of cells is large, where a wide range of parameters lead to a physical separation. The temperatures attained during the cleave processes are well-below the melting point of silicon. However, in some non-optimum cases, it can still be critical causing damage of surface passivation (electrical performance reduction) of silicon solar cells such as PERC and SHJ. The chapter introduces a photoluminescence-based approach to optimize the cleave process that aims to obtain cell-tailored processes. Performing the cleave process without initiating a crack by the scribe process does not lead to separation and keeps the substrate in its full wafer-sized format. This allows the investigation of the cleave process impact in an experiment by using *p*-type Cz-Si PERC and *n*-type Cz-Si SHJ non-metallized industrial precursors. Knowing the large process window of the TLS cleave process, only a P_C variation is performed keeping the rest of the process parameters constant. In the case of the PERC substrate, the results show drops of the PL signal $\varphi(x)$ that are proportional to the increase in P_C. However, after performing an additional ultrafast regeneration process, the drops disappear, showing that no permanent damage of the surface passivation has resulted from the cleave process on PERC. This indicates possible B-O complex regeneration of degraded cleave lines and/or a surface repassivation. An optimum $P_C = 88$ W at a process velocity $v_C = 200$ m/s is found. In the case of SHJ substrates, the increase of P_C leads to a proportional $\varphi(x)$ drop that is attributed to surface passivation degradation. A regain of the $\varphi(x)$ is not observed. From the parameter variation an optimum process at $P_C = 81$ W and $v_C = 250$ mm/s is chosen.

The processes chosen from the P_C optimization experiment are used to investigate the impact of the cleave process as well as the complete TLS process (i.e., complete separation) on PERC and SHJ host cells with half cell and shingle cell formats. The solar cells that undergo only the cleave process without undergoing the scribe show a loss in *pFF* of $\Delta pFF = -0.1\%_{abs}$ in case of PERC and of $\Delta pFF = -0.4\%_{abs}$ in case of SHJ. For the complete TLS process, the scribe and cleave processes are both conducted, a mean *pFF* drop of, e.g., $\Delta pFF = -0.3\%_{abs}$ is shown in the case of PERC shingle cells. Whereas, in the case of SHJ shingle cells a reduction $\Delta pFF = -2.1\%_{abs}$ is found after complete separation. The investigation suggests that the highest share of V_{OC} and mainly *pFF* losses are

caused by recombination at the newly formed edges and not from the optimized TLS cleave process.

The chapter also shows that the TLS cleave process can be done from the front and the rear side of PERC host cells with similar V_{OC} and pFF losses. On the contrary, the laser scribing process performed from the front side (i.e., side of the emitter) shows severe drops in V_{OC} and pFF reaching $\Delta V_{OC} = -7$ mV and $\Delta pFF = -9.1\%_{abs}$. That is without performing the mechanical cleave step. Moreover, the complete separation of host cells into pSPEER solar cells shows comparable results among cells separated by TLS as well as LSMC from the rear side. To further observe the impact of the two separation techniques, even smaller cells with higher separated perimeter-to-area ratios k are fabricated by using each of the processes. V_{OC} and pFF differences from the host cell to the separated cells becomes larger with the increase of k (decrease of cell size). For the smallest cell with $A_{tot} = 1.15$ cm x 1.15 cm ≈ 1.32 cm² (i.e., around 0.5% of the host cell area), the LSMC-separated cell shows a drop in V_{OC} measured at low illumination (i.e., $\Delta V_{OC,low} = -29$ mV) from the host cell to the separated state. This corresponds to a reduction of around $5\%_{rel}$. The TLS-separated one shows only a drop of $4\%_{rel}$ (i.e., $\Delta V_{OC,low} = -23$ mV). Moreover $\Delta pFF = -5.3\%_{abs}$, corresponding to a $6\%_{rel}$ pFF reduction, is measured in the case of the LSMC-separated cell. A lower reduction $\Delta pFF = -3.2\%_{abs}$, $4\%_{rel}$ pFF reduction is measured in the case of the TLS-separated cell. The advantage of the TLS-separated cell can be explained by the smoother (i.e., possibly defect poorer) cell edges that lead to lower edge recombination losses in comparison to the LSMC-separated cell. The influence of a defect edge rises with the decrease of cell sizes.

In general, the results in this chapter also demonstrate the necessity of edge passivation techniques to avoid or regain cell output parameter drops resulting from cell separation. The separation process utilized also has an impact on further post-separation edge passivation processes to be discussed in chapter 7.

6 Silicon Surface Passivation by Low Temperature Aluminum Oxide

6.1 Introduction

Reducing charge carrier recombination at the surfaces by passivation is crucial towards achieving efficient silicon solar cells. This chapter emphasizes on the atomic layer deposition (ALD) technique of aluminum oxide (Al_2O_3) for silicon surface passivation. The motivation behind surface passivation by low temperature deposition ($T \leq 200°C$) and annealing ($T \leq 300°C$) is discussed. Then, the capability for surface passivation of Al_2O_3 layers formed by thermal ALD at low deposition temperatures is demonstrated on lowly-doped p-type and n-type silicon substrates. Charge carrier lifetime measurements are used to explore the dependency between surface passivation quality and Al_2O_3 layer deposition, in addition to the annealing temperatures. Moreover, the stability of the achieved surface passivation over storage time is also examined. The last segment of the chapter deals with an alternative laser-based post-deposition annealing process for the rapid activation of the Al_2O_3 surface passivation.

6.2 Review of aluminum oxide passivation for solar cells

To reduce the surface recombination in silicon solar cells, thin dielectric films are used with the aim of (i) reducing the density of interface traps (chemical passivation) and/or (ii) creating a field effect passivation (physical passivation). For the fundamentals of surface passivation, please refer to section 2.7. In 1989, *Hezel* and *Jäger* used Al_2O_3 as a passivation layer for silicon substrates in the application for solar cells [97]. Effective surface recombination velocities S_{eff} of around 200 cm/s were achieved on p-type silicon substrates. The coating was done by pyrolysis of aluminum-

triisopropoxide at atmospheric pressure and at process temperatures ranging between 290°C and 460°C. In 2006, *Agostinelli et al.* revived the use of Al_2O_3 for the surface passivation of silicon substrates [111]. They demonstrated a high quality surface passivation that was quantified by very low $S_{eff} = 10$ cm/s on lowly-doped *p*-type silicon substrates. *Hoex et al.* also showed very low $S_{eff} = 2$ cm/s and $S_{eff} = 6$ cm/s for lowly-doped *n*-type and *p*-type silicon substrates, respectively [117]. *Richter et al.* investigated the outcome of Al_2O_3 passivation on highly-doped *p*-type surfaces (i.e., boron-diffused emitters) [212]. In 2011, a very low emitter saturation current density of 45 fA/cm^2 was achieved. Even for a very low Al_2O_3 layer thickness of only $d_{Al2O3} = 1$ nm, the work published by *Werner et al.* reported an $S_{eff} < 100$ cm/s on *p*-type silicon substrates [213]. For Al_2O_3 layers thicker than $d_{Al2O3} = 10$ nm, they also confirmed the high negative fixed charge density Q_f and low density of traps D_{it} in the orders of 10^{12} cm^{-2} and 10^{11} eV^{-1}cm^{-2}, respectively. In other words, excellent surface passivation is already demonstrated on lowly-doped *p*-type, lowly-doped *n*-type, as well as highly boron-doped silicon substrates by deposited Al_2O_3 dielectric layers [108].

Annealing after the plasma-assisted ALD of Al_2O_3 on substrates, resulted in the reduction of D_{it} from around 10^{13} eV^{-1}cm^{-2} to 10^{11} eV^{-1}cm^{-2} [214]. The reduction in D_{it} after post-deposition annealing (PDA) was mainly explained by the diffusion of hydrogen to the silicon/Al_2O_3 interface, shown in the particular case of a substrate featuring 30 nm-thick Al_2O_3 coating and thermally-grown silicon dioxide (SiO_2) [215]. In the case of Al_2O_3 layers deposited by thermal ALD, low D_{it} was attained even in the as-deposited state [108]. It was determined that the PDA after thermal ALD enhances the Q_f values by an order of magnitude for Al_2O_3-coated substrates [108, 216].

Practically, common annealing processes were performed in nitrogen (N_2) or forming gas ambients (H_2/N_2) at annealing temperatures of around 425°C for annealing durations t_{ann} longer than 10 minutes [212]. As an approach to reduce t_{ann} to less than a minute, microwave-based PDA was also demonstrated [217]. Very high effective minority carrier lifetime $\tau_{eff} = 3.7$ ms was achieved, showing the functionality of the technique.

A fast firing process (in the order of seconds) at much higher temperatures above 700°C was performed to attain acceptable surface passivation by Al_2O_3 layers [218]. The advantage of the firing process-based PDA was

(and still is) the applicability of the passivation activation as well as the metal-semiconductor contact formation in one process. Post-deposition firing processes above 800°C lead to very low S_{eff} values on Al_2O_3-deposited silicon substrates also on silicon substrates featuring Al_2O_3 and silicon nitride (SiN_X) stacks [219]. In turn, *Schmidt et al.* demonstrated that Al_2O_3 layers and Al_2O_3/SiN_X stacks are activated by high temperature firing processes leading to excellent surface passivation quality on *p*-type silicon substrates [220]. The stability of the results of Al_2O_3/SiN_X stacks, also on screen-printed silicon solar cells, showed the applicability of the stack configuration and the firing process industrially [81].

For low deposition temperatures of 100°C, *Frascaroli et al.* demonstrated $\tau_{eff} = 500$ µs after PDA at 250°C in nitrogen ambient [221]. The *p*-type substrates showing such τ_{eff} levels featured deposited thicknesses greater than 6 nm. In *Richter*'s dissertation, very low S_{eff} values of around 4 cm/s were attained for samples deposited at temperatures of 130°C and annealed at 200°C on *p*-type silicon substrates [31]. Surface passivation quality by Al_2O_3 at deposition and annealing temperatures below the mentioned ones were not investigated in the literature up to the start of this work in 2017.

Within the time frame of this work, experiments done by *Veith-Wolf* and *Schmidt* showed results on lowly-doped *p*-type substrates deposited at temperatures of 200°C and 260°C with PDA temperatures between 200°C and 425°C [222]. Results of thermal ALD of Al_2O_3 proved that $\tau_{eff} > 1$ ms can be achieved after annealing durations of more than a few hours. The introduction of an additional corona charge in combination with PDA for 1 hr at 300°C resulted in an improved surface passivation quality quantified by $\tau_{eff} = 2.24$ ms. Annealing at 200°C in combination with corona charge coating showed $\tau_{eff} = 1.5$ ms. They also demonstrated that by only corona charge deposition without PDA, an $S_{eff} = 15$ cm/s can be achieved.

As discussed in section 2.7, in practice, several deposition methods can be used to form Al_2O_3 layers on substrates. Since Al_2O_3 deposition by ALD is the focus of this dissertation, the process is now further explained.

Aluminum oxide atomic layer deposition: setup and reactions

The explanations provided in this section are based on Refs. [31, 223, 224] unless stated otherwise by including additional references. The chemical

vapor deposition ALD allows the deposition of sub-monolayer thicknesses of dielectric inorganic materials on substrates. The deposition with very high conformality is attained in sequential self-limiting gas-solid reactions. One ALD cycle includes four essential steps: (i) Reaction of the first reactant, (ii) removal of reaction byproducts and non-reacted remaining reactants by purging using inert gases and/or evacuation, (iii) reaction of the second reactant, and again the (iv) removal of reaction byproducts and non-reacted remaining reactants by purging using inert gases and/or evacuation. In other words, in a single ALD cycle, gas precursors (i.e., reactants) are introduced separately by having purge steps in between [225]. The ALD cycle is repeated until a desired thickness is attained. The added dielectric material thickness per ALD cycle is called growth per cycle (GPC). Since the technique features two surface-dependent self-limiting reactions, the layer growth depends mainly on the substrate and some process parameters like e.g., substrate temperature, reaction gas doses, and purge durations. A linear relation between the GPC and the number of ALD cycles $N°$ is expected. To determine a completely saturated ALD process where no parasitic components remain, the purge durations are varied for process optimization [108].

For the formation of Al_2O_3 layers, a highly-purified pyrophoric compound trimethylaluminum $Al(CH_3)_2$, known as TMA, is commonly used as the aluminum source. The oxidation reaction either by plasma assistance or by thermal oxidation are common methods. The plasma-assisted oxidation takes place by using a plasma of oxygen radicals, while the thermal ALD requires either water vapor $H_2O_{(g)}$ or ozone as depicted in Fig. 6.1.

This work focuses mainly on the thermal ALD of Al_2O_3 by using $H_2O_{(g)}$ as an oxidant. The surface chemistry during the process steps can be explained by the (i) TMA exposure reaction and (ii) the oxidation reaction. The TMA exposure is described by

$$|| \text{Al–OH} + \text{Al(CH}_3)_{3(g)} \rightarrow || \text{Al–O–Al(CH}_3)_2 + \text{CH}_{4(g)} \tag{6.1}$$

where the surface species "||" of || hydroxyl Al–OH reacts with TMA to form chemisorbed || Al–O–$Al(CH_3)_2$ and methane $CH_{4(g)}$.

The oxidation reaction is expressed as follows

$$|| \text{Al(CH}_3)_2 + \text{H}_2\text{O}_{(g)} \rightarrow || \text{Al–OH} + \text{CH}_{4(g)}. \tag{6.2}$$

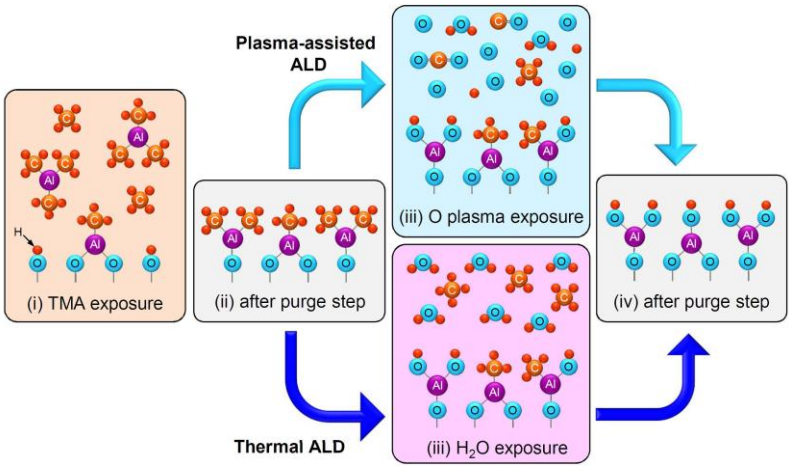


Fig. 6.1. Schematic illustration of a plasma-assisted and a thermal ALD cycle for the deposition of Al_2O_3 layers. The figure is from Ref. [31].

Lower GPC values at low temperatures are attained for H_2O-based thermal ALD oxidation reactions compared to plasma-assisted ALD reactions. That is mainly due to the decrease of the reaction efficiency at lower temperatures in the thermal ALD. A decrease of GPC is also observed at high temperatures. However, the GPC decrease at high temperatures is attributed to the reduction of TMA adsorption caused by dehydroxylation reactions.

ALD reactor and deposition process

Within this work, ALD is performed in the *FlexAL* reactor from *Oxford Instruments* [226]. A schematic illustration of the deposition setup and the involved gases in a single thermal ALD of Al_2O_3 are shown in Fig. 6.2(a) and (b), respectively. The tool offers the possibility of both plasma-assisted and thermal ALD processes. A plasma source is necessary for the oxidation reaction during the plasma-assisted processes. For the evacuation, a turbo pump is used. Moreover, the inert gases during the purge steps can be introduced in the reaction chamber through either the plasma source inlet or through the separate gas inlet valves (i.e., depending on the process parameters). The temperatures of the substrate as well as that of the precursor gases can be controlled independently. In general, substrates with diameters of up to 200 mm can be processed in this

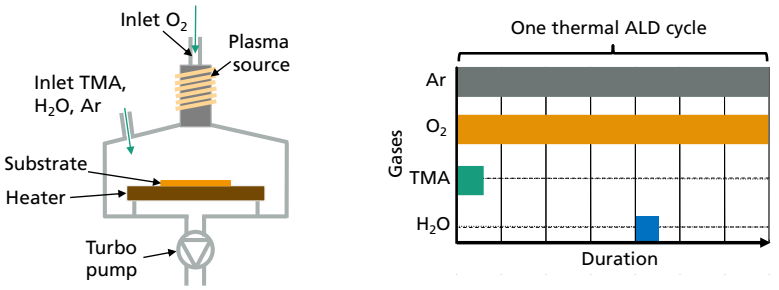


Fig. 6.2. (a) Schematic illustration of the reactor chamber in the *FlexAL* setup. (b) Schematic illustration of involved gases in one thermal ALD cycle of Al_2O_3 deposition. The figures are redrawn from Ref. [31].

reactor. The growth and material properties of Al_2O_3 deposited by the tool is thoroughly described in Ref. [224].

6.3 Motivation for low temperature surface passivation

In this work, deposition and annealing temperatures below 200°C are considered as low temperature processes in comparison to state-of-the-art surface passivation processes discussed in section 6.2.

Previous publications have investigated the impact of post-firing thermal processes on silicon solar cells, which are discussed in this section. *Kontermann et al.* investigated the influence of post-metallization annealing (PMA) temperature and duration on aluminum back surface field (Al-BSF) solar cells [227]. The results showed that for each of the gaseous atmospheres, (i) forming gas or (ii) nitrogen gas, the solar cell series resistance r_S increases (i.e., the fill factor *FF* decreases) with increasing thermal annealing budget. This result was already noticeable for temperatures higher than 300°C [227, 228]. Additionally, *Chan et al.* determined the outcome of PMA thermal processes on PERC solar cell structures [229]. At the lowest furnace temperature of 400°C, reduction in *FF* was already recorded. For temperatures below 650°C, the reduction in *FF* was attributed to the increase in r_S, while at temperatures above 650°C a drop in pseudo fill factor *pFF* was also recorded. The results showed possible metal-semiconductor degradation as well as degradation of surface passivation at higher temperature ranges. Similar investigations had been

reported showing an increase in contact resistance and thereby a reduction in *FF* values after PMA at relatively high temperatures [230, 231]. Temperatures higher than 200°C lead to the degradation of amorphous silicon passivation in silicon heterojunction (SHJ) solar cells [75, 106]. Apart from possible detrimental impact on existing contacts, low temperature surface passivation prevented possible bulk defects proven at higher temperatures [232].

As explained in 4.3, the passivated edge technology (PET) requires post-metallization deposition and annealing after separation. The necessity of low temperature processes is evident to avoid possible damage of already existing cell structures such as metal contacts and surface passivation layers. The low temperature surface passivation processes are also of interest for emerging solar cell technologies, such as III-V compound/silicon tandem solar cells as shown in Ref. [233]. Moreover, low temperature Al_2O_3 layers might also be valuable for substrate material characterization where a low thermal budget is required.

6.4 Investigation of thermally deposited Al_2O_3 layers

The experiment, based on Ref. [234][8], aims mainly to understand the possibility of attaining surface passivation properties of Al_2O_3 for deposition temperatures $T_{dep} \leq 130°C$ and annealing temperatures $T_{ann} \leq 300°C$ on *p*-type and *n*-type floatzone silicon (Fz-Si) substrates. Thermal ALD is used as the deposition process of choice to avoid possible detrimental plasma-metal interactions in case performed on metallized solar cells.

6.4.1 Sample preparation and experimental process flow

For the investigation of surface passivation properties of dielectric layers, symmetrically deposited lifetime samples are considered [67]. In other words, both the front and rear sides of each substrate must ideally feature identical surface properties including the same dielectric layer (or layer stacks). The substrates used in this experiment are high quality Fz-Si wafers that feature a (100) surface orientation and polished sides. Both, lowly-doped *p*-type and *n*-type Fz-Si wafers with base resistivities $\rho_B = 1\ \Omega cm$, are used. The *p*-type and *n*-type substrates feature wafer

[8] Master thesis of A. Bhandary supervised by the author of this dissertation.

thicknesses $W = 250$ µm and $W = 200$ µm, respectively. Fig. 6.3(a) shows the schematic cross-section of a Fz-Si wafer deposited symmetrically by Al_2O_3 layers, which is also referred to as lifetime sample in this work. Fig. 6.3(b) shows an illustration of the substrate and the separated labeled quarters. Before the deposition processes are performed, the wafers undergo surface cleaning by using first nitric acid (HNO_3) solution followed by hydrofluoric acid (HF) dipping.

For the deposition process, substrates are loaded in the handling loadlock compartment manually. The stage on which the substrate is placed is then automatically driven to the reaction chamber for the instigation of the deposition process. Next, the substrate is heated to the substrate temperature which is referred to as deposition temperature T_{dep} in the rest of the work. In this experiment, a variation of three T_{dep} values with $T_{dep} = \{60°C, 95°C, 130°C\}$ is performed. Fig. 6.4 illustrates the experimental process flow. To accomplish chosen average thicknesses for each of the deposition temperatures, several deposition recipes are tested. Main requirements for the final recipe choices are the conformality in d_{Al2O3} values as well as indices of refraction of the deposited layer n_{Al2O3} for both the front and rear sides of the deposited Fz-Si wafers.

For that reason, based on a coarse parameter variation, specific deposition processes are chosen. For the sample groups deposited at $T_{dep} = 130°C$, the deposition of the front and rear are performed simultaneously. This is possible by placing the lifetime samples on 800 µm-thick silicon spacers, which lift the substrate and allow the reaction on the rear side too.

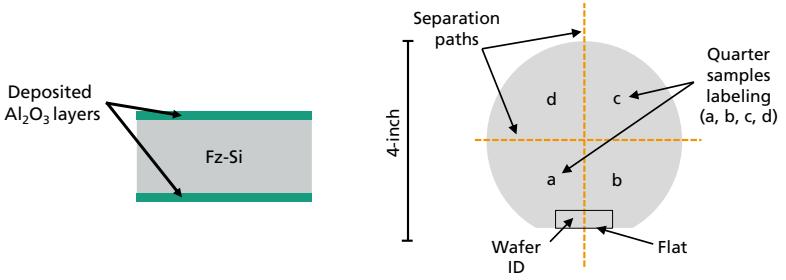


Fig. 6.3. (a) Schematic cross-section of a Fz-Si lifetime sample deposited symmetrically by Al_2O_3. The symmetry is necessary for the approximation of the further characterization of the surface passivation quality, i.e., the effective surface recombination velocity in particular. (b) Fz-Si substrate (4-inch) separated into four approximately equal quarters. The quarters featuring side lengths of around 2-inchs are used for further processing.

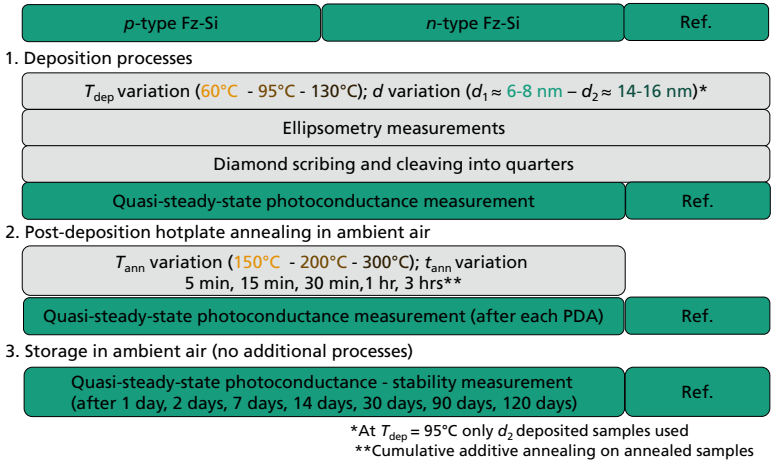


Fig. 6.4. Experimental process flow for the investigation of surface passivation on *p*-type and *n*-type Fz-Si by Al_2O_3. A reference sample with a known effective lifetime value is measured at each characterization step to ensure measurement setup reproducibility. (*for the case of T_{dep}= 95°C only d_2 is considered).

In the sample groups deposited at $T_{dep} = 95°C$ and $T_{dep} = 60°C$, pretest deposition runs do not show conformal simultaneous deposition of the front and the rear side. For that reason, the front and the rear side are deposited separately, to obtain symmetric lifetime samples.

The recipes for the deposition processes conducted at $T_{dep} = 95°C$ and $T_{dep} = 60°C$ feature longer purge durations than the deposition done at $T_{dep} = 130°C$. Both processes have similar gas inlet doses and purge durations, with the only difference being the substrate temperature during deposition. Moreover, the d_{Al2O3} are also varied in two groups. The first group includes thin layers having average thicknesses ranging between $6\ nm \leq d_1 \leq 8\ nm$, while the second group includes thicker layers with $14\ nm \leq d_2 \leq 16\ nm$. After the deposition is completed, d_{Al2O3} and n_{Al2O3} are determined by spectroscopic ellipsometry measurements.

For the measurement setup details please refer to Appendix A2. Each deposited wafer is then separated into four equal quarters by diamond scribing and mechanical cleaving. This increases the number of samples used for the further investigation without compromising the quality of the electrical characterization. From the generalized mode quasi-steady-state

photoconductance measurement (QSSPC) [74], the effective minority carrier lifetime τ_{eff} is extracted at an excess carrier density $\Delta n = 1 \text{ x } 10^{15} \text{ cm}^{-3}$.

To perform the PDA, a hotplate is used. The homogeneity of the spatial temperature distribution attained by the hotplate is verified by an infrared thermometer (laser pointer). For each of the deposition sample groups with the differences in the base doping type, T_{dep}, and/or d_{Al2O3}, an annealing variation is performed. The PDA takes place isothermally at various annealing temperatures in groups with $T_{\text{ann}} = \{150°\text{C}, 200°\text{C}, 300°\text{C}\}$. The annealing is conducted in ambient air. The samples undergo lifetime measurements by QSSPC in between each annealing step. Whereas the cumulative annealing steps are done in increasing durations $t_{\text{ann}} = \{5 \text{ min}, 15 \text{ min}, 30 \text{ min}, 1 \text{ hr}, 2 \text{ hrs}, 3 \text{ hrs}\}$.

To investigate the stability of the surface passivation in relation to storage time t_{S}, QSSPC measurements are repeated. The stability measurements are performed after about a day and reaching up to 120 days starting from the last as-annealed measurement. The storage environment is not controlled, meaning that the lifetime samples are kept in the dark with air as an ambient. A reference sample with a known τ_{eff} result is measured at each characterization step to ensure the reproducibility of the measurement.

6.4.2 Deposition process results

As a result of the differences in the chosen processes, GPC values are attained for each of the processes at $T_{\text{dep}} = \{60°\text{C}, 95°\text{C}, 130°\text{C}\}$; see Fig. 6.5(a). The processes at $T_{\text{dep}} = 60°\text{C}$ and $T_{\text{dep}} = 95°\text{C}$ attain similar GPC values of 0.06 nm/cycle, while the deposition at $T_{\text{dep}} = 130°\text{C}$ leads to a GPC = 0.11 nm/cycle. These GPC results are deduced from the slope of the linear relation between the d_{Al2O3} and the ALD cycle number. An illustrative example of that for the process at $T_{\text{dep}} = 95°\text{C}$ is shown in Fig. 6.5(b).

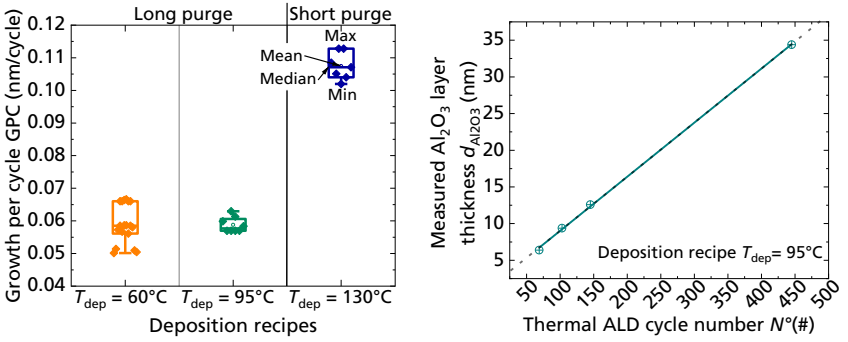


Fig. 6.5. (a) GPC values for each of the processes at $T_{dep} = \{60°C, 95°C, 130°C\}$. Longer purge processes are chosen for deposition runs at $T_{dep} = 60°C$ and $T_{dep} = 95°C$ in comparison to that at $T_{dep} = 130°C$. (b) Al_2O_3 thickness per thermal ALD cycle taking the example of ellipsometry results of Fz-Si samples deposited at $T_{dep} = 95°C$. The slope of the linear fit is the deduced GPC = 0.07 nm/cycle for this specific deposition process, while the y-intercept approximates the silicon dioxide thickness at the interface $d_{SiO2} = (1.64 \pm 0.3)$ nm. Data from Ref. [234].

6.4.3 Effective lifetime results

The QSSPC measurement results are first explained by focusing on each of the T_{dep} processed groups, separately. τ_{eff} in relation to t_{ann} is discussed for lifetime samples featuring the deposition layer thickness 6 nm $\leq d_1 \leq$ 8 nm for substrates with both doping types. After that, measurement results on samples featuring the thicker 14 nm $\leq d_2 \leq$ 16 nm layer are explained, also on substrates with both base dopings.

Lifetime samples deposited at T_{dep} = 60°C

For the p-type samples featuring d_1, the as-deposited τ_{eff} values range between 255 µs $\leq \tau_{eff} \leq$ 270 µs, as shown in Fig. 6.6(a). After 5 min of annealing, τ_{eff} values for all samples drop, where the highest drop of around 96%$_{rel}$ is recorded at the highest annealing temperature $T_{ann} = 300°C$. The samples annealed at lower temperatures experience lower drops. Interestingly, the successive annealing leads to a regain even after $t_{ann} = 3$ hrs. In the case of the sample annealed at $T_{ann} = 200°C$, the initial regain is followed by a drop after the 2 hrs annealing. The stability measurement results in Fig. 6.6(b) show that the sample annealed at the

highest annealing temperature $T_{ann} = 300°C$ is the least stable one. After the 120th day of storage, the highest drop of $72\%_{rel}$ from the annealed state is recorded. Nevertheless, the lowest annealing temperature leads to the lowest drop of around $26\%_{rel}$ and a stable $\tau_{eff} = 155$ µs.

For the n-type samples featuring d_1, the as-deposited τ_{eff} values range between 440 µs $\leq \tau_{eff} \leq$ 567 µs, as shown in Fig. 6.6(c). The changes in relation to T_{ann} and t_{ann} are similar to the p-type case. That is except for the $T_{ann} = 200°C$ having the lowest τ_{eff} value after 3 hrs annealing. After the 120th day of storage, see Fig. 6.6(d), the sample annealed at the lowest temperature shows the most stable result having the highest value of $\tau_{eff} = 321$ µs.

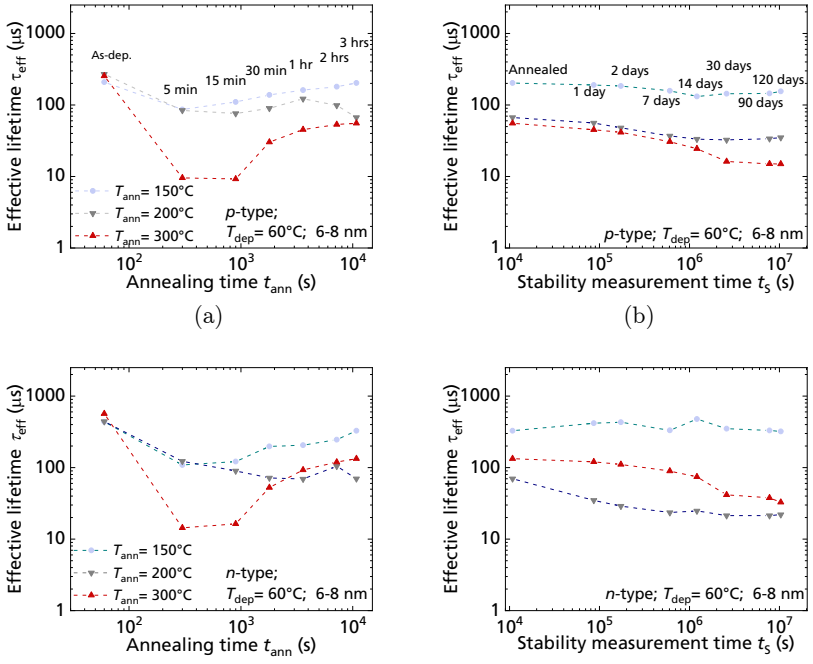


Fig. 6.6. (a) Effective minority carrier lifetime τ_{eff} measurement in relation to annealing time t_{ann} on symmetric p-type lifetime samples. (b) Stability of τ_{eff} in relation to ambient air storage time t_S in the dark for the p-type substrates. (c) τ_{eff} measurement in relation to t_{ann} on symmetric n-type lifetime samples. (d) Stability of τ_{eff} in relation to ambient air t_S in the dark for the n-type substrates. All Fz-Si samples are coated by Al_2O_3 layers at $T_{dep} = 60°C$. The deposited Al_2O_3 layer thickness is 6 nm $\leq d_1 \leq$ 8 nm. τ_{eff} is extracted at $\Delta n = 1 \times 10^{15}$ cm^{-3}. The dashed lines are a guide to the eye. Data from Ref. [234].

Samples annealed at higher temperatures experience τ_{eff} value drops and their τ_{eff} values are not stable in relation to t_{S}.

For the p-type samples featuring d_2, the as-deposited τ_{eff} values range between $60\ \mu\text{s} \leq \tau_{\text{eff}} \leq 198\ \mu\text{s}$, as shown in Fig. 6.7(a). After 5 min of annealing, τ_{eff} values of samples annealed at $T_{\text{ann}} = 200°\text{C}$ and 300°C show an increase. A $\tau_{\text{eff}} = 698\ \mu\text{s}$ for the sample annealed at $T_{\text{ann}} = 200°\text{C}$ is attained. The samples annealed at the highest temperature $T_{\text{ann}} = 300°\text{C}$ show a drop in τ_{eff} after the first annealing step. The highest drop of around $87\%_{\text{rel}}$ is recorded at the highest annealing temperature $T_{\text{ann}} = 300°\text{C}$. With the successive annealing steps, the samples annealed at the lowest temperature $T_{\text{ann}} = 150°\text{C}$ show an increase reaching in the best case a maximum of $\tau_{\text{eff}} = 995\ \mu\text{s}$ after 3 hrs. Interestingly, the successive annealing leads to a regain of τ_{eff} for the samples annealed at $T_{\text{ann}} = 300°\text{C}$, whereas a redrop in initially gained τ_{eff} is seen in the $T_{\text{ann}} = 200°\text{C}$. The stability measurement results show that the sample with highest τ_{eff} values ($\tau_{\text{eff}} > 171\ \mu\text{s}$) are the least stable results with the highest drop of $75\%_{\text{rel}}$ after the 120^{th} day of storage in comparison to the last as-annealed value; see Fig. 6.7(b).

For the n-type samples featuring d_2, the as-deposited τ_{eff} values range between $65\ \mu\text{s} \leq \tau_{\text{eff}} \leq 206\ \mu\text{s}$, as shown in Fig. 6.7(c). The changes as a result of annealing show similar trends to that of the p-type samples. The stability measurement results show that the sample with highest τ_{eff} values ($\tau_{\text{eff}} > 133\ \mu\text{s}$) are the least stable results with the highest drop of $62\%_{\text{rel}}$ after the 120^{th} day of storage in comparison to last as-annealed value; see Fig. 6.7(b).

As a general outcome of the lifetime samples deposited at $T_{\text{dep}} = 60°\text{C}$ with thin layers d_1, the as-deposited value is usually the highest compared to the values after annealing. For samples deposited with d_2, highest τ_{eff} values are attained at $T_{\text{ann}} = 150°\text{C}$. The results are mainly independent from the base doping type. Already after the first stability measurement (after one day), strong τ_{eff} drops are recorded for samples deposited with d_2. Although the attained τ_{eff} values after PDA are lower, measurements performed on samples deposited by d_1 show more stable results.

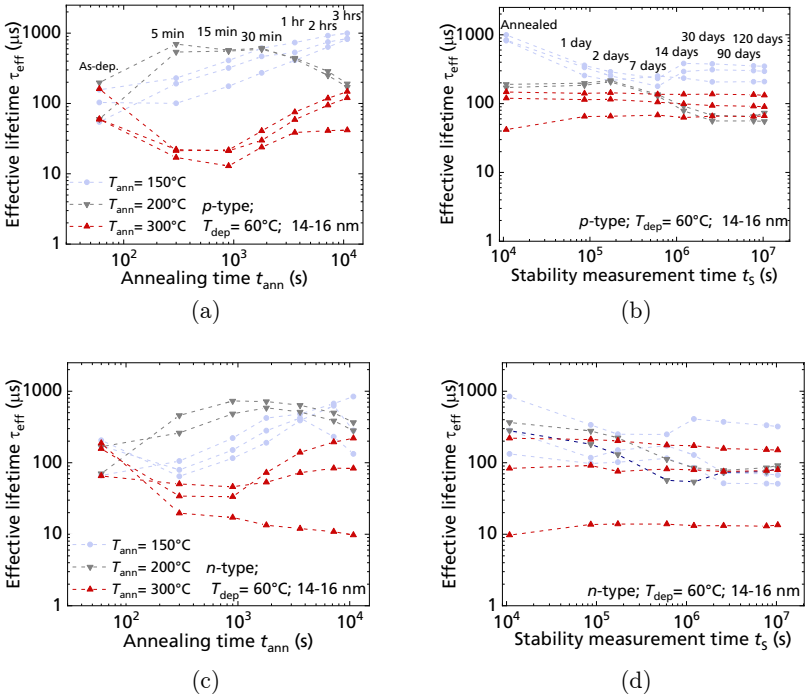


Fig. 6.7. (a) Effective minority carrier lifetime τ_{eff} measurement in relation to annealing time t_{ann} on symmetric p-type lifetime samples. (b) Stability of τ_{eff} in relation to ambient air t_S in the dark for the p-type substrates. (c) τ_{eff} measurement in relation to t_{ann} on symmetric n-type lifetime samples. (d) Stability of τ_{eff} in relation to ambient air t_S in the dark for the n-type substrates. All Fz-Si samples are coated by Al_2O_3 layers at $T_{dep} = 60°C$. The deposited Al_2O_3 layer thickness is 14 nm $\leq d_2 \leq$ 16 nm. τ_{eff} is extracted at $\Delta n = 1 \times 10^{15}$ cm^{-3}. The dashed lines are a guide to the eye. Data from Ref. [234].

Lifetime samples deposited at T_{dep} = 95°C

For the p-type samples featuring d_2, the as-deposited τ_{eff} values range between 150 µs $\leq \tau_{eff} \leq$ 165 µs, as shown in Fig. 6.8(a). After 5 min of annealing τ_{eff} values of samples annealed at $T_{ann} = 200°C$ show the highest increase. A $\tau_{eff} = 698$ µs for the sample annealed at $T_{ann} = 200°C$ is attained. A lower increase is measured on samples annealed at $T_{ann} = 150°C$. The samples annealed at the highest temperature $T_{ann} = 300°C$ show a drop in τ_{eff} after the second annealing step $t_{ann} = 15$ min.

The highest $\tau_{eff} = 1546$ µs is achieved after an hour of annealing at $T_{ann} = 200°C$. After that, the additional annealing leads to a decrease reaching values above $\tau_{eff} > 1$ ms. Stability measurement results are shown in Fig. 6.8(b), where no drastic τ_{eff} value drops are seen.

For the n-type samples featuring d_2, the as-deposited τ_{eff} values vary in the range between 78 µs $\leq \tau_{eff} \leq$ 137 µs, as shown in Fig. 6.8(c). The τ_{eff} values in relation to the annealing show similar trends to the p-type case. Measurements even after 120 days still show high τ_{eff} values, see Fig. 6.8(d).

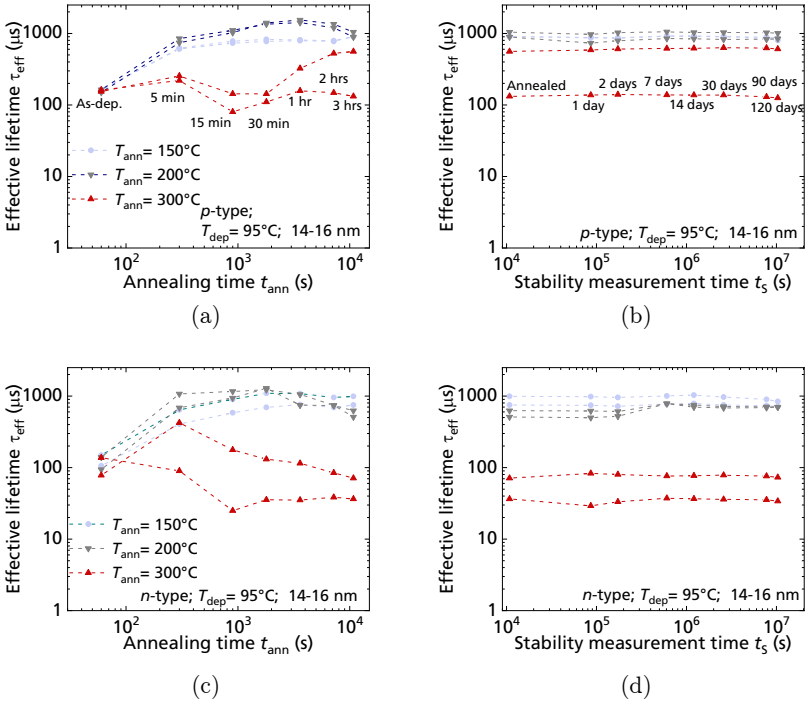


Fig. 6.8. (a) Effective minority carrier lifetime τ_{eff} measurement in relation to annealing time t_{ann} on symmetric p-type lifetime samples. (b) Stability of τ_{eff} in relation to ambient air t_S in the dark for the p-type substrates. (c) τ_{eff} measurement in relation to t_{ann} on symmetric n-type lifetime samples. (d) Stability of τ_{eff} in relation to ambient air t_S in the dark for the n-type substrates. All Fz-Si samples are coated by Al_2O_3 layers at $T_{dep} = 95°C$. The deposited Al_2O_3 layer thickness is 14 nm $\leq d_2 \leq$ 16 nm. τ_{eff} is extracted at $\Delta n = 1 \times 10^{15}$ cm^{-3}. The dashed lines are a guide to the eye. Data from Ref. [234].

As a general outcome, lifetime samples deposited at $T_{dep} = 95°C$ and annealed at $T_{ann} = 200°C$ lead to highest τ_{eff}. Annealing at the highest temperature $T_{ann} = 300°C$ leads to drops of τ_{eff} values. The results are independent from the doping type. Very high τ_{eff} values are measured even after $t_S = 120$ days.

Lifetime samples deposited at $T_{dep} = 130°C$

For the p-type samples featuring d_1, the as-deposited τ_{eff} values range between $6\ \mu s \leq \tau_{eff} \leq 16\ \mu s$, as shown in Fig. 6.9(a). Annealing at all the chosen temperatures shows an increase in τ_{eff} with the successive annealing steps. The highest $\tau_{eff} = 627\ \mu s$ is measured for the sample annealed at $T_{ann} = 200°C$ after the 1 hr annealing step. Additional annealing at this temperature leads to drops in τ_{eff} values. Even after $t_S = 120$ days, high τ_{eff} values are still measured, see Fig. 6.9(b).

For the n-type samples featuring d_1, the as-deposited τ_{eff} values range between $4\ \mu s \leq \tau_{eff} \leq 13\ \mu s$, as shown in Fig. 6.9(c). After the 15 min annealing step, the maximum $\tau_{eff} = 309\ \mu s$ is achieved for the sample annealed at $T_{ann} = 300°C$. After that, the additional annealing steps reduce the τ_{eff} values, except for the samples annealed at $T_{ann} = 150°C$. They encounter a gradual increase reaching a maximum $\tau_{eff} = 93\ \mu s$. As a result of the stability investigation, even after $t_S = 120$ days τ_{eff} values are measured to be stable; see Fig. 6.9(d).

For the p-type samples featuring d_2, the as-deposited τ_{eff} values range between $4\ \mu s \leq \tau_{eff} \leq 85\ \mu s$, as shown in Fig. 6.10(a). After the 5 min annealing the maximum $\tau_{eff} = 1099\ \mu s$ is achieved for the sample annealed at $T_{ann} = 300°C$. This shows a $94\%_{rel}$ increase from the as-deposited state. After that, the additional annealing steps reduce the τ_{eff} values for the samples annealed at $T_{ann} = 300°C$. A further step after 2 hrs annealing leads to a $\tau_{eff} = 1630\ \mu s$ in the case of the sample annealed at $T_{ann} = 200°C$. However, an additional annealing of 3 hrs leads to a decrease in τ_{eff}. Very high τ_{eff} values are still measured after 120 days, see Fig. 6.10(b).

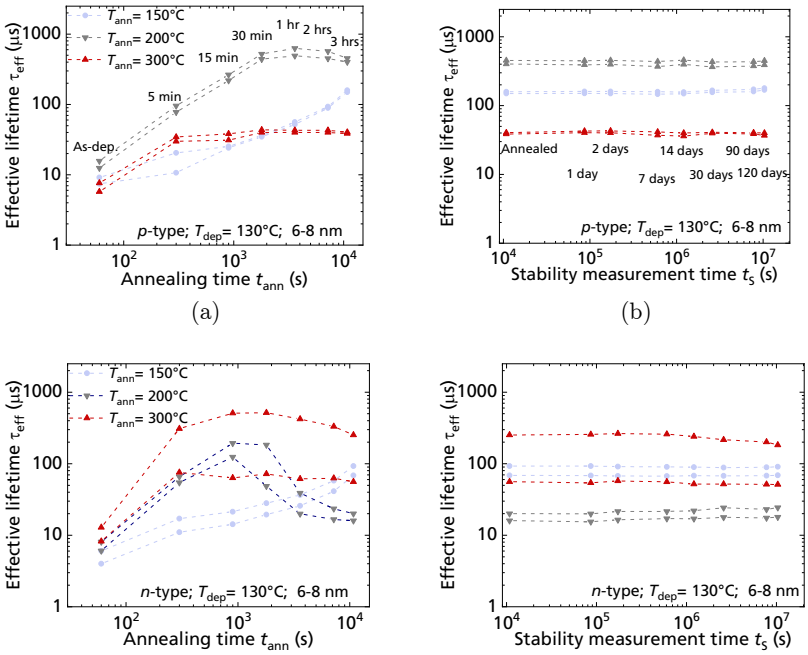


Fig. 6.9. Effective minority carrier lifetime τ_{eff} measurement in relation to annealing time t_{ann} on symmetric p-type lifetime samples. (b) Stability of τ_{eff} in relation to ambient air t_S in the dark for the p-type substrates. (c) τ_{eff} measurement in relation to t_{ann} on symmetric n-type lifetime samples. (d) Stability of τ_{eff} in relation to ambient air t_S in the dark for the n-type substrates. All Fz-Si samples are coated by Al_2O_3 layers at $T_{dep} = 130°C$. The deposited Al_2O_3 layer thickness is 6 nm $\leq d_1 \leq$ 8 nm. τ_{eff} is extracted at $\Delta n = 1$ x 10^{15} cm^{-3}. The dashed lines are a guide to the eye. Data from Ref. [234].

For the n-type samples featuring d_2, the as-deposited τ_{eff} values range between 3 µs $\leq \tau_{eff} \leq$ 11 µs, as shown in Fig. 6.10(c). After the 5 min annealing a $\tau_{eff} = 1176$ µs is achieved for the sample annealed at $T_{ann} = 300°C$. This shows a 99%$_{rel}$ increase from the as-deposited state, that is the highest relative rise. Annealing at lower temperatures also leads to an increase in τ_{eff}. After that, the additional annealing steps reduce the τ_{eff} values for the samples annealed at $T_{ann} = 300°C$. A further annealing step of 2 hrs leads to $\tau_{eff} = 1417$ µs for a sample annealed at $T_{ann} = 200°C$. The last annealing step decreases τ_{eff} values. As shown in Fig. 6.10(d), the measurements even after 120 days show high τ_{eff} values.

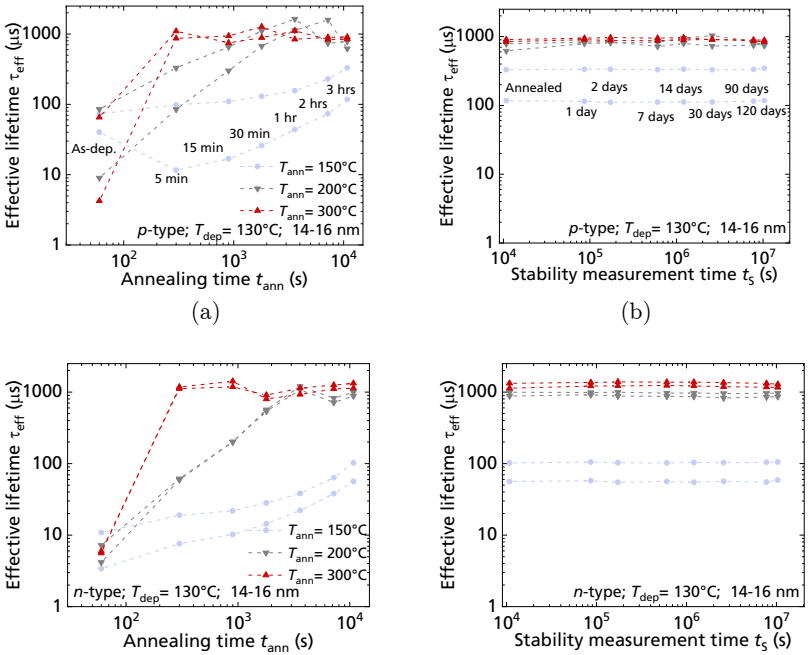


Fig. 6.10. Effective minority carrier lifetime τ_{eff} measurement in relation to annealing time t_{ann} on symmetric p-type lifetime samples. (b) Stability of τ_{eff} in relation to ambient air t_S in the dark for the p-type substrates. (c) τ_{eff} measurement in relation to t_{ann} on symmetric n-type lifetime samples. (d) Stability of τ_{eff} in relation to ambient air t_S in the dark for the n-type substrates. All Fz-Si samples are coated by Al_2O_3 layers at $T_{dep} = 130°C$. The deposited Al_2O_3 layer thickness is 14 nm $\leq d_2 \leq$ 16 nm. τ_{eff} is extracted at $\Delta n = 1 \times 10^{15}$ cm^{-3}. The dashed lines are a guide to the eye. Data from Ref. [234].

As a general outcome of the lifetime samples deposited at $T_{dep} = 130°C$ and featuring the d_2 Al_2O_3 layers, the highest annealing temperature $T_{ann} = 300°C$ is required to obtain the highest increase in τ_{eff}. The results are mainly independent from the base doping type and are stable as a function of t_S.

6.4.4 Discussion

A summary of the highest τ_{eff} value results for each sample type at each deposition temperature is listed in Table 6.1. The results can be discussed by focusing on the passivation quality: (i) thickness dependency,

(ii) interdependency of T_{dep} and T_{ann}, (iii) annealing duration t_{ann}, and (iv) stability of the surface passivation in relation to t_S.

i. Thickness dependency

In general, it is observed that groups deposited with 14 nm $\leq d_2 \leq$ 16 nm show higher τ_{eff} than groups of samples with 6 nm $\leq d_1 \leq$ 8 nm. These results are independent from the chosen deposition process T_{dep}. It is well-known that surface passivation quality of Al_2O_3 is dependent on the thickness of the passivation layer [213]. This is mainly explained by the

Table 6.1. Summary of results attaining highest τ_{eff} for each of the deposition temperature groups with T_{dep} = {60°C, 95°C, 130°C} on 1 Ωcm p-type and n-type Fz-Si substrates. The deposited layer thicknesses investigated are 6 nm $\leq d_1 \leq$ 8 nm and 14 nm $\leq d_2 \leq$ 16 nm. The t_{ann} shows the last annealing step duration in the successive annealing stages. S_{eff} is calculated by using equation (2.23). By referring to Ref. [59], bulk lifetime τ_{bulk} values on p-type and n-type are considered to be τ_{bulk} = 3870 µs and τ_{bulk} = 7480 µs, respectively. τ_{eff} at excess carrier concentration Δn = 1 x 10^{15} cm^{-3} is analyzed.

Sample type	T_{ann} (°C)	t_{ann}	Highest τ_{eff} (µs)	S_{eff} (cm/s)	Highest stable τ_{eff} at t_S = 120 days (µs)	Highest stable S_{eff} at t_S = 120 days (cm/s)
For samples processed at T_{dep} = 60°C						
p-type – d_1	-	-	270	43.1	155 (T_{ann} = 150°C)	77.4
n-type – d_1	-	-	567	16.3	321 (T_{ann} = 150°C)	29.8
p-type – d_2	150	3 hr	995	9.3	349	32.6
n-type – d_2	150	3 hr	842	10.5	321	29.8
For samples processed at T_{dep} = 95°C						
p-type – d_2	200	1 hr	1546	4.9	1010	9.1
n-type – d_2	200	30 min	1289	6.4	841	10.6
For samples processed at T_{dep} = 130°C						
p-type – d_1	200	1 hr	627	16.7	448	24.7
n-type – d_1	300	30 min	517	18.0	183	53.3
p-type – d_2	200	1 hr	1631	4.4	889	10.8
n-type – d_2	300	15 min	1417	5.7	1289	6.4

decrease in the chemical passivation by possibly the higher number of interface defect density with thinner layers used.

ii. Interdependency of T_{dep} and T_{ann}

The interdependency of the T_{dep} and T_{ann} is observed in most of the cases agreeing with results showing that for low T_{dep} a low T_{ann} is required. This confirms the similarity of the interdependency for processes at $T_{dep} \geq 130°C$ reported in Ref. [31]. For instance, for $T_{dep} = 60°C$, the lowest chosen annealing temperature $T_{ann} = 150°C$ is seen to establish an enhanced passivation quality in comparison to the other annealing temperatures. For the highest deposition temperature $T_{dep} = 130°C$ the highest $T_{ann} = 300°C$ is seen to be the most effective PDA temperature. It is also observed that in the case of the low temperature processes especially $T_{dep} = 60°C$ and d_1, as-deposited values are higher than the annealed ones, with the lowest as-deposited S_{eff} values shown in this case. This proposes a possibility of an invitro activation of the surface passivation that already starts occurring during the deposition within the reactor.

iii. Annealing duration t_{ann}

Generally, the results show the increase of surface passivation quality with the increase of t_{ann} until in some cases a saturation is reached. Too long annealing durations also show a degradation in the surface passivation quality observed in cases where the T_{dep} is low and T_{ann} is high. Possible explanation could be the effusion of hydrogen, which might influence the chemical surface passivation negatively.

iv. Stability of the surface passivation

After 120 days of storage in ambient air, in most cases a reduction in τ_{eff} is recorded. However, the severity of the drop is different in the different studied groups. The largest degradation is observed on substrates deposited at $T_{dep} = 60°C$. However, $\tau_{eff} > 1$ ms at $t_S = 120$ days are still observed on both p-type and n-type substrates that are deposited at higher temperatures, i.e., $T_{dep} = 95°C$ and $T_{dep} = 130°C$.

Implications of results on fabricated silicon solar cells

To the best of the author's knowledge, the attained S_{eff} values $S_{\text{eff}} = 4.4$ cm/s and $S_{\text{eff}} = 5.7$ cm/s on p-type and n-type substrates are the lowest in comparison to the literature reported values for Al_2O_3 surface passivation by thermal ALD at these temperature levels. Even at $t_S = 120$ days, the surface passivation quality quantified by $S_{\text{eff}} < 10$ cm/s, is considered suitable for the excellent surface passivation of passivated emitter and rear cell (PERC) devices [235].

In the case of use for post-metallization surface passivation, the chosen T_{dep}, T_{ann}, and $t_{\text{ann}} < 30$ min are low enough to avoid possible damage to already existing structures of metallized cells; please refer to section 7.3. The results also show that an effective surface passivation is attained in air ambient, and no additional gases are required during the annealing processes. In some cases, the results also imply the possible PDA that could already take place in module integration process steps. Investigated T_{ann} levels are also observed for instance in the lamination process at set temperatures of around 150°C [236]. In other words, no additional PDA would be required since a process with a thermal treatment already exists in the process sequence. Nevertheless, additional experiments must be performed to understand the impact of the surface passivation on a module level and under accelerated stability tests.

Advanced characterization of layers

To further study the structural composition of the deposited Al_2O_3 layers, Fourier transformed-infrared spectroscopy (FT-IR) measurements [237] are conducted by using the spectrometer *Vertex 80v* tool from *Bruker* [238]. FT-IR measurements indicate the spectral absorbance of the Al_2O_3 layers in the mid-infrared range. The p-type samples used for the investigation feature 40 nm-thick Al_2O_3 layers deposited at $T_{\text{dep}} = \{60°C, 95°C, 130°C\}$. Measurements in both the as-deposited and the annealed state are conducted. The annealing is performed at $T_{\text{ann}} = 200°C$ for $t_{\text{ann}} = 25$ min on a hotplate. According to the literature, the infrared absorption in the wave number range $2600 \leq \nu \leq 3800$ cm^{-1} are interpreted as OH (stretch) mode bonds [31, 101, 239–241]. As the chemical passivation is driven by hydrogen bonds, this specific range is of interest.

As shown in Fig. 6.11, the results indicate that for the lowest deposition temperature T_{dep} investigated, the amount of hydrogen is higher. After annealing, the absorbance data shows lower levels. The reduction of the peak intensities after annealing is a strong sign of the mobility of hydrogen within the Al_2O_3 layers. The mobility of the hydrogen indicates a higher possibility of the dangling bond saturation, contributing to the chemical passivation.

Capacitance-voltage (CV) measurements [242], using the semiconductor analyzer *Agilent Technologies B1500A* [243], are performed to measure the amount of fixed charge density Q_f of the deposited Al_2O_3 layers on n-type silicon substrates. The layers are deposited at the investigated $T_{dep} = \{60°C, 95°C, 130°C\}$ with $d_{Al2O3} = 19$ nm. The results in Fig. 6.12 show the deduced Q_f at different T_{dep} and T_{ann}.

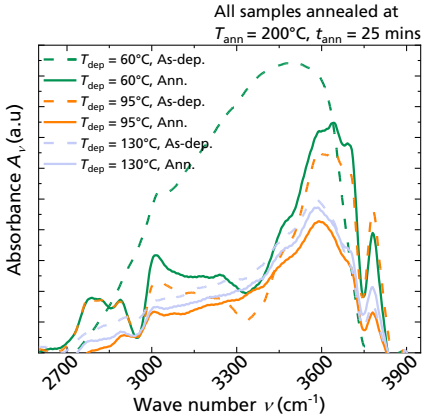


Fig. 6.11. FT-IR spectral absorbance of Al_2O_3 layers deposited at $T_{dep} = \{60°C, 95°C, 130°C\}$. Measurements are performed in the as-deposited (as-dep.) and annealed (ann.) states. The spectra $2600 \leq \nu \leq 3800$ cm^{-1} range are considered as they indicate the OH (stretch) composition. The samples feature a 40 nm-thick Al_2O_3 layer deposited by thermal ALD. For clarification, the spectral lines are shown after data smoothing by averaging over 10 adjacent measurement points.

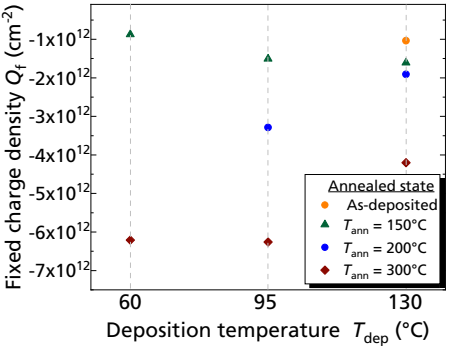


Fig. 6.12. CV measurement results showing the fixed charge density Q_f of Al_2O_3 layers deposited at T_{dep} and annealed at T_{ann}.

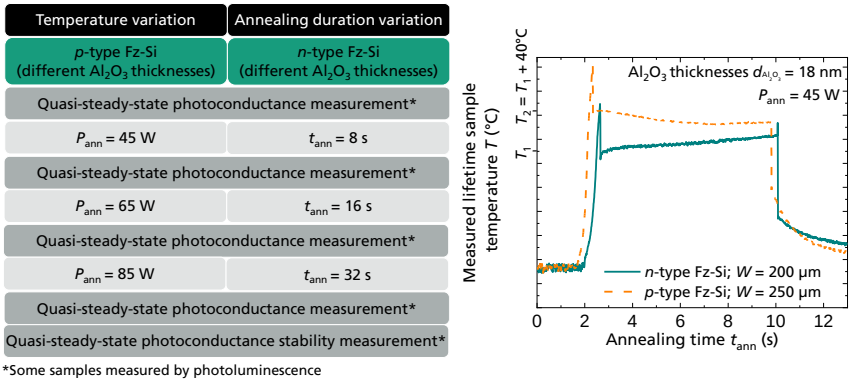
The high negative Q_f ranging between -8.7×10^{-11} cm^{-2} and -6.3×10^{-12} cm^{-2} is demonstrated. Even in the as-deposited case, a strongly negative $Q_f = -1 \times 10^{-12}$ cm^{-2} is shown. The reduction in Q_f in the annealed states is in agreement with results reported in Ref. [216]. The highly-charged layer implies a possible high field effect that contributes to the physical surface passivation.

6.5 Alternative fast post-deposition annealing

An alternative fast post-deposition annealing process is desired for a more rapid process step in comparison to hotplate annealing. In turn, a faster process (i.e., in seconds instead of minutes) is of interest. In this section, the investigation aims to determine the impact of an infrared laser-based heating using a vertical cavity surface-emitting laser (VCSEL) process [244] on deposited lifetime samples. The setup uses laser modules featuring a wavelength of $\lambda = 808$ nm [244]. For the temperature monitoring of the heated silicon substrates an infrared camera is integrated [245]. For more details about the system and the functionality of the setup, please refer to *Ourinson*' s dissertation [246].

Experiment description

For the experiment, both lowly-doped p-type and n-type Fz-Si lifetime samples are considered. The substrates feature Al_2O_3 layers deposited via thermal ALD. Fig. 6.13(a) shows the experimental process flow.



(a) (b)

Fig. 6.13. (a) Experimental process flow for the investigation of surface passivation on p-type and n-type Fz-Si by low temperature ALD Al_2O_3 and alternative fast laser annealing. (b) Temperature profile measurement results on p-type and n-type Fz-Si lifetime samples featuring $d_{Al2O3} = 18$ nm Al_2O_3 layers. The samples are annealed at a constant $P_{ann} = 45$ W and an annealing duration of $t_{ann} = 8$ s. The p-type and n-type Fz-Si wafers have the thicknesses $W = 250$ µm and $W = 200$ µm, respectively. T_1 is the approximate plateau temperature attained by the n-type sample, while T_2 is the approximate plateau temperature attained by the p-type sample. Temperatures below 300°C are recorded.

Lifetime samples with three different Al_2O_3 average layer thicknesses (i.e., $d_1 = 5$ nm, $d_2 = 7$ nm, $d_3 = 12$ nm) for each of the doping types are used. The deposition process at $T_{dep} = 95$°C is chosen. The main variation groups are in (i) the annealing temperature attained by the annealing laser power P_{ann} variation and (ii) the annealing duration t_{ann}. As examples, shown in Fig. 6.13(b), temperature profiles are measured on p-type and n-type Fz-Si lifetime samples featuring $d_{Al2O3} = 18$ nm.

Results and discussion

For most of the groups, a clear τ_{eff} increase in relation to P_{ann} or t_{ann} is measured as shown in Fig. 6.14. τ_{eff} values of above 1 ms are attained for both p-type and n-type substrates. Only in the case of the p-type sample deposited by an average thickness $d_1 = 5$ nm, final measurement values below $\tau_{eff} < 500$ µs are achieved. Fig. 6.15 shows an example of the photoluminescence (PL) measurement results on a p-type sample deposited by an average thickness $d_1 = 5$ nm in the (a) as-deposited state as well as (b) after the first annealing step at constant P_{ann}.

As a comparison, PL images on a p-type sample deposited by an average thickness $d_3 = 12$ nm in the as-deposited and annealed states are also shown in Fig. 6.15(c) and (d), respectively. The activation of the surface passivation by the alternative annealing method in the case of the lifetime sample deposited by d_3 is evident.

The highest τ_{eff} obtained on a p-type lifetime sample is $\tau_{\text{eff}} = 1100$ µs (corresponding to $S_{\text{eff}} = 8.1$ cm/s). They feature a thickness of $d_{\text{Al2O3}} = 12$ nm and $d_{\text{Al2O3}} = 7$ nm and are annealed for 8 s at $P_{\text{ann}} = 65$ W. On an n-type lifetime sample with a $d_{\text{Al2O3}} = 5$ nm, the highest $\tau_{\text{eff}} = 1258$ µs (corresponding to $S_{\text{eff}} = 6.6$ cm/s) is attained after processing. τ_{eff} values that are comparable to results after hotplate-based PDA are obtained reaching $\tau_{\text{eff}} > 1$ ms.

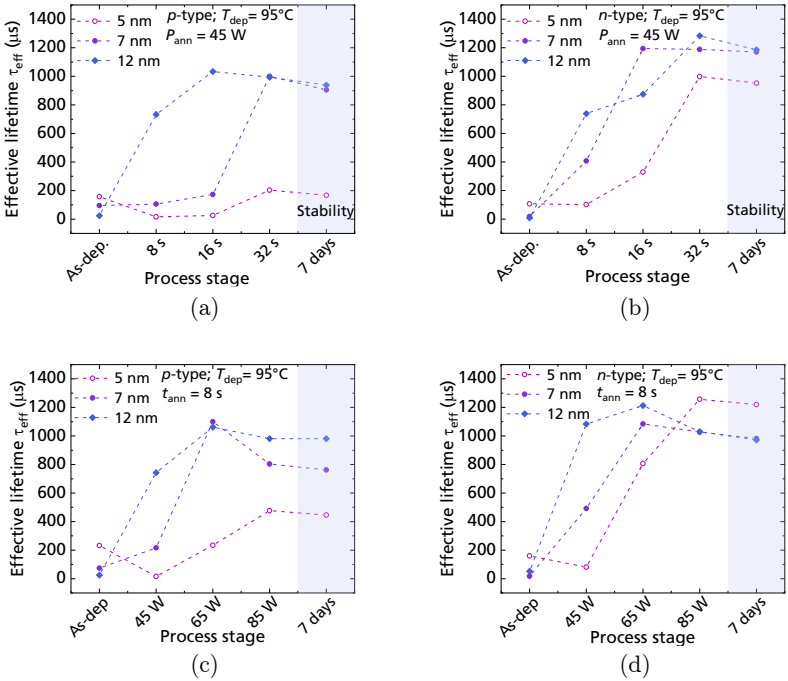


Fig. 6.14. τ_{eff} in relation to annealing duration t_{ann} at constant laser power $P_{\text{ann}} = 45$ W for (a) p-type and (b) n-type lifetime samples. τ_{eff} in relation to P_{ann} at constant $t_{\text{ann}} = 8$ s for (c) p-type and (d) n-type lifetime samples. All used Fz-Si substrates are deposited at $T_{\text{dep}} = 95$°C. Three deposited Al_2O_3 thicknesses: $d_1 = 5$ nm, $d_2 = 7$ nm, and $d_3 = 12$ nm are considered. Stability measurement after 7 days are also shown. The dashed lines are a guide to the eye.

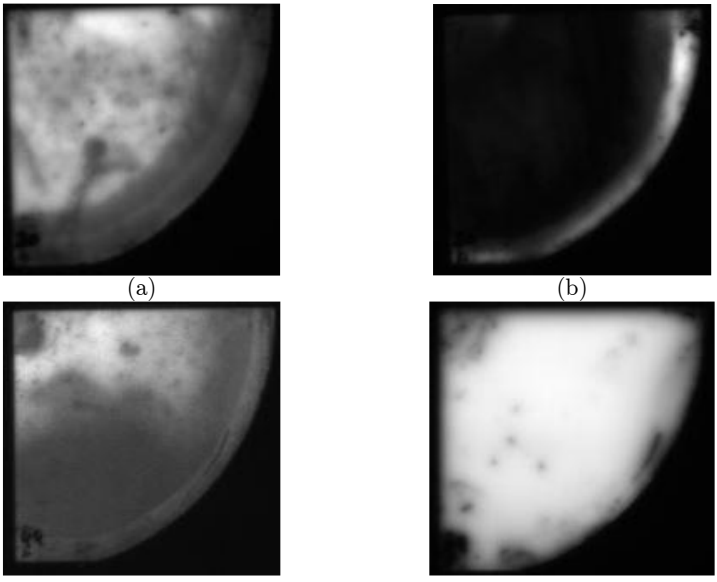


Fig. 6.15. PL image of a *p*-type Fz-Si lifetime sample featuring d_1 thickness in (a) the as-deposited state and (b) first annealed state. PL image of a *p*-type Fz-Si lifetime sample featuring d_3 thickness in (c) as-deposited and (d) first annealed state. Brighter signals indicate higher local τ_{eff} values. The annealing is performed at constant $P_{\text{ann}} = 45$ W for a duration of $t_{\text{ann}} = 8$ s. The measurements are conducted at an irradiance of 1 suns equivalent to 651 W/m^2. The used suns equivalent is defined by a photon flux $\Phi = 2.5 \times 10^{17}$ photons(808 nm)/cm^{2}s^{-1}.

6.6 Chapter summary

This chapter investigates the surface passivation quality attained by thermal ALD of Al_2O_3 layers on lowly-doped Fz-Si samples. Of special interest are the deposition and post-deposition annealing (PDA) processes at low temperatures. That is with the aim of examining possible dependencies of substrate temperature during deposition T_{dep} and annealing temperatures T_{ann} at temperatures lower or equal to 130°C and 300°C, respectively. Temperature levels lower than the latter one are interesting for the post-metallization application in order to avoid possible detrimental effects on already existing cell structures in the metallized state.

The experimental investigation shows the strong dependency of T_{dep} on T_{ann}. The activation of the passivation layer at low T_{dep} requires low T_{ann}.

Excellent surface passivation quality is attained with effective surface recombination velocities $S_{\text{eff}} = 4.4$ cm/s and $S_{\text{eff}} = 5.7$ cm/s on p-type and n-type substrates, respectively. These values are to the best knowledge of the author the lowest reported S_{eff} values to date for such low temperature thermal ALD-based surface passivation. This considers the PDA occurring in ambient air.

The stability measurements of samples in air ambient after $t_{\text{S}} = 120$ days of storage in the dark still show high surface passivation quality. As a result, $S_{\text{eff}} < 10$ cm/s is still attained after the 120^{th} day of storage for lifetime samples featuring average thicknesses between 14 – 16 nm, except for samples deposited at $T_{\text{dep}} = 60$°C. FT-IR measurements hint towards the highly mobile hydrogen, while the C-V measurements confirm the highly negative nature of the fixed charges. These results indicate that the Al_2O_3 deposited layers serve both chemical and field effect surface passivation mechanisms.

To shorten the PDA processing duration (i.e., in comparison to hotplate annealing), a laser-based alternative annealing process is tested. The annealing leads to the increase of τ_{eff} to values above 1 ms in the best case at shortest tested duration of $t_{\text{ann}} = 8$ s and lowest used laser power $P_{\text{ann}} = 45$ W. By that the functionality of the rapid activation of the ALD-deposited Al_2O_3 on lowly-doped lifetime samples is proven.

7 Passivated Edge Technology for Separated Silicon Solar Cells

7.1 Introduction

The concept and the approach of the passivated edge technology (PET) is introduced in 4.3. The approach includes post-separation passivation layer deposition and annealing steps. In this chapter, a review of edge passivation methods, existing before the start of the dissertation, is provided. Knowing that PET involves post-metallization thermal processes, the impact of post-metallization annealing (PMA) on p-type shingled passivated edge, emitter, and rear (pSPEER) solar cells is studied. Determining the PMA influence allows the use of PET thermal processes within the accepted temperature ranges and durations. An experiment presents the influence of different PET processes on pSPEER solar cells. As a result, pSPEER cells with PET are fabricated which are then called $p\text{SPEER}^{\text{PET}}$ solar cells. The chapter is concluded by an overview of the historical development during the time frame of this work from the initial bifacial shingle solar cells from the first published results in 2018 to the most efficient $p\text{SPEER}^{\text{PET}}$ solar cells.

7.2 Review of edge passivation methods

Aiming towards the reduction of recombination at the silicon solar cell edge, several passivation methods are discussed in literature and will be reviewed in this section. As a specific type of surface passivation, edge passivation can be mainly achieved by (i) decreasing the density of traps (i.e., defects) at the edges and/or (ii) the reduction of charge carriers of one type from the edge. An emitter window approach that keeps the intended separation path (or edge) far from the emitter region leads to the reduction of edge recombination [15, 16, 20, 21]. That results mainly from the reduction of minority charge carrier flow through the emitter towards the

intended edge. Practically, an emitter window can be, e.g., obtained by using diffusion barriers created before the emitter formation diffusion process [22]. Moreover, the manufacturing of isolation trenches in the emitter also aims to cut the flow of charge carriers of a kind to the intended separation path [18]. The development of the isolation trenches is technically done by laser-ablated grooves that feature thermally-grown silicon dioxide (SiO_2) or polysilicon passivation layers. Additionally, allowing the growth of SiO_2 on wet-chemically treated edges has also shown successful edge passivation results specifically at low illumination conditions [165]. To repel charge carriers by a surface field from the edge, the creation of highly-doped edge regions is proposed as an alternative approach [19].

All these discussed approaches are effective methods for the possible reduction of charge carrier recombination at the edge. However, these approaches require either additional frontend process steps, e.g., for the emitter window fabrication case, or propose post-metallization wet-chemical processes.

7.3 Post-metallization annealing

As discussed in section 4.3.2, the PET is the combination of post-metallization deposition and annealing processes that is performed after the host cells are separated into shingle solar cells. It is known that post-metallization annealing (PMA) after firing (i.e., contact formation), can lead to the increase of series resistance r_S and drops in fill factor FF [228, 229]. This implies that the thermal treatment during the PET process steps should be below critical annealing temperatures $T_{ann,crit}$ and annealing durations $t_{ann,crit}$ that might harm the metallization and/or the already existing surface passivation.

7.3.1 Experimental details

An experiment is conducted to understand the impact of PMA on *p*SPEER solar cells and to identify critical temperature levels suitable for the PET. Separated shingle solar cells with *Gen4* metallization layout are used for the investigation; see Appendix A3 for an overview about the metallization layout generations. The solar cells feature a *p*-type gallium-doped Cz-Si (Cz-Si:Ga) base material, which means boron-oxygen-related light-induced

degradation [146] does not play a role. The experimental process flow is shown in Fig. 7.1. At first, an initial current-voltage (IV) measurement is performed, followed by the first PMA on a hotplate at $T_{\mathrm{ann}} = 200°\mathrm{C}$ and $t_{\mathrm{ann}} = 25$ min. After that, the cells are characterized by IV measurements to observe the impact of the first annealing step. This sequence of successive annealing and IV measurements is repeated. In total, four annealing and characterization steps are considered, with the last one completed at $T_{\mathrm{ann}} = 300°\mathrm{C}$ and $t_{\mathrm{ann}} = 120$ min. Combining the duration of all the annealing steps, a total $t_{\mathrm{ann}} = 230$ min of annealing is performed with interruptions for the characterization between each annealing step.

A similar experiment is performed on metallized test structures to investigate the consequence of PMA even further on the line resistances of the rear side and front side fingers (i.e., Group 2), in addition to the front side contact resistivity $\rho_{\mathrm{C,FS}}$ and rear side contact resistivity $\rho_{\mathrm{C,RS}}$ (i.e., Group 3). Front and rear lateral finger resistances are characterized by four-point-probe (4pp) measurements [75] before and after successive annealing steps. The total annealing duration is also $t_{\mathrm{ann}} = 230$ min.

The front and rear side contact resistivity values are also determined before and after cumulative annealing steps by the transfer length method

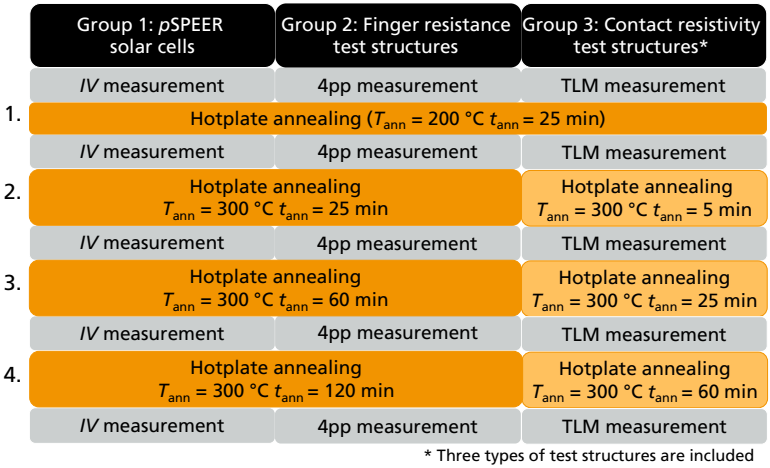


Fig. 7.1. Description of the process flow for the investigation of successive PMA on *p*SPEER solar cells and test structures. The solar cells are only measured from the front side by IV measurement. The test structures are measured from the front and the rear side to determine the front and rear finger and contact resistances, by means of 4pp and TLM measurements. For the TLM measurements, three types of test structures are considered in this experiment.

(TLM) [247–250]. The initial annealing step is performed at $T_{ann} = 200°C$ and $t_{ann} = 25$ min, like groups 1, 2, and 3, while the total annealing duration is $t_{ann} = 115$ min. The TLM structures in group 3, which were annealed on another day, are heated with different successive annealing parameters T_{ann} and t_{ann}, due to a fallacy. Despite these differences in the annealing parameters the aim of the experiment does not change.

7.3.2 Results and discussion

*p*SPEER solar cells

In the initial state, the *p*SPEER solar cells feature a mean open-circuit voltage $V_{OC} = (668 \pm 4)$ mV, a short-circuit current density $j_{SC} = (38.8 \pm 4)$ mA/cm², and a fill factor $FF = (80.7 \pm 0.6)\%$; see Fig. 7.2. The mean energy conversion efficiency is $\eta = (20.9 \pm 0.4)\%$. After the first PMA step, no reduction in η is recorded. The second PMA step leads to a decrease in η (i.e., $\Delta\eta = -0.2\%_{abs}$), mainly due to reduction in FF (i.e., $\Delta FF = -0.4\%_{abs}$) and short-circuit current density j_{SC} (i.e., $\Delta j_{SC} = -0.1$ mA/cm²), despite the minor increase in V_{OC} (i.e., $\Delta V_{OC} = 1$ mV). At this stage, the drop in FF is attributed to the reduction in pseudo fill factor pFF, while the series resistance r_S is measured to be constant.

The additional PMA steps lead to further decrease in η. It is observable that the third annealing step causes an r_S increase, by $\Delta r_S = +0.07$ Ωcm², compared to the initial value. After the final annealing step, a total η loss of $\Delta\eta = -0.7\%_{abs}$ is observed. The loss is mainly attributed to the reduction $\Delta V_{OC} = -5$ mV, $\Delta FF = -1.9\%_{abs}$, and $\Delta j_{SC} = -0.2$ mA/cm² compared to initial values. The FF loss is attributed to the rise of $\Delta r_S = +0.26$ Ωcm² and a decrease in $\Delta pFF = -0.6\%_{abs}$.

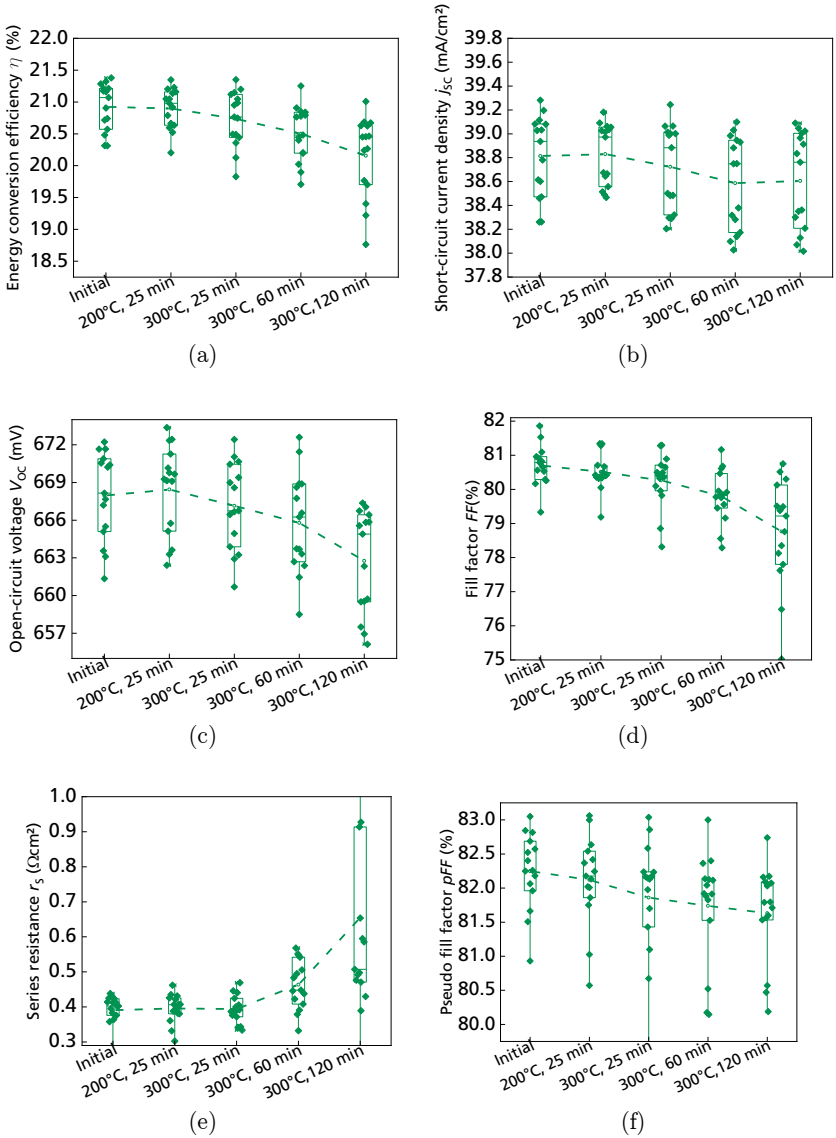


Fig. 7.2. IV measurement results at each PMA state showing (a) energy conversion efficiency η, (b) short-circuit current density j_{SC}, (c) open-circuit voltage V_{OC}, (d) fill factor *FF*, (e) series resistance r_S, and (f) pseudo fill factor *pFF*. The η and j_{SC} results are total area values. The dashed line is the interconnection of the mean values in the box plots, showing the trend.

The constant η after the first annealing step indicates that the used $T_{ann} = 200°C$ and $t_{ann} = 25$ min do no have a detrimental impact on the solar cells (i.e., $T_{ann} < T_{ann,crit}$ and $t_{ann} < t_{ann,crit}$). The additional cumulative annealing of the solar cells possibly reduces the surface passivation quality, quantified by V_{OC} and pFF losses, already after the second annealing step. Futher annealing steps then lead to a deterioration of the metal-semiconductor contact quantified by the rise in r_S. This is in addition to the further reduction in the surface passivation quality and possible rise in metal-induced surface recombination. Since no reduction in η is recorded after the first annealing step, annealing with $T_{ann} = 200°C$ and $t_{ann} = 25$ min can be considered for the thermal activation process used in the PET.

Finger resistance test structures

As a result of the successive annealing steps, the finger line resistance is unchanged even after the last annealing step at $T_{ann} = 300°C$ and $t_{ann} = 120$ min (not shown). The main reason for this outcome is the already sintered metal particles within the formed finger after firing. The thermal impact in the PMA is not high enough for the restructuring of the finger metal bulk, which usually require higher temperatures (around 500°C) to undergo microstructural changes [251].

TLM test structures

Results of the annealing investigation on the TLM structures' $\rho_{C,FS}$ and $\rho_{C,RS}$ are shown in Fig. 7.3(a) and (b), respectively. The first annealing step (i.e., $T_{ann} = 200°C$ and $t_{ann} = 25$ min) does not lead to any increase in $\rho_{C,FS}$ for samples from type 1, 2 and 3. After the completion of all the annealing steps (i.e., after the total $t_{ann} = 115$ min), the mean $\rho_{C,FS}$ increases slightly for the type 1 sample group showing a $\Delta\rho_{C,FS} = + 0.6$ mΩcm^2. The impact on the type 2 and 3 samples is higher with $\Delta\rho_{C,FS} = + 1.2$ mΩcm^2 and $\Delta\rho_{C,FS} = + 2.1$ mΩcm^2, respectively. The highest increase in the $\rho_{C,FS}$ values of the three groups takes place in the last annealing stage. The rear side measurements show no changes in $\rho_{C,RS}$ at all.

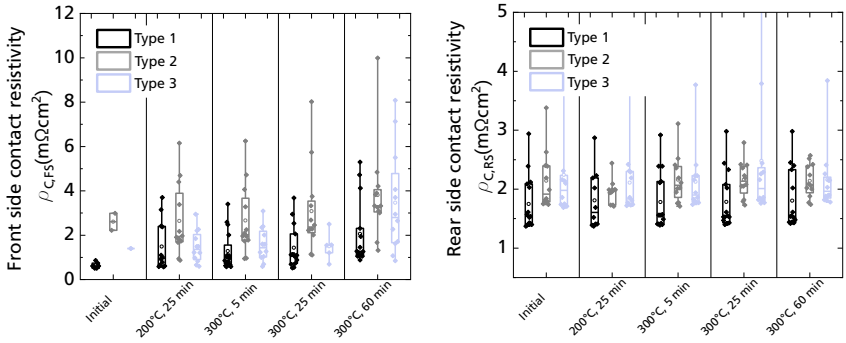


Fig. 7.3. TLM measurement results showing the (a) front side contact resistivity $\rho_{C,FS}$ and (b) rear side contact resistivity $\rho_{C,RS}$ at each PMA state. Three types of TLM structures are considered with three different precursor materials but with an identical metallization. Type 2 and 3 feature identical front side emitter and surface passivation layers. They differ in the rear side silicon nitride (SiN_X) capping layer thickness.

Hence, the TLM results prove that $\rho_{C,FS}$ is mainly affected by the post-firing thermal annealing after several annealing steps, whereas the first annealing step has no detrimental impact. In the case of the $\rho_{C,RS}$, annealing at studied T_{ann} and t_{ann} does not harm the contact.

A probable explanation for the increase of $\rho_{C,FS}$ is the restructuring of the silver contact formation interface with the silicon as reported in Ref. [230]. The interface in the front side formed contact includes a glass layer, which increases its thickness and restructures with additional post-firing steps [230]. The restructuring of the interface glass depends on the softening glass frit transition temperatures as a material property [252, 253]. Post-firing annealing reduces the current flow from the silicon to the silver bulk by created gaps between the silver bulk and the crystals [254].

Knowing that $T_{ann} = 200°C$ and $t_{ann} = 25$ min are suitable parameters for the activation of Al_2O_3, shown in section 6.4, the first annealing step with those parameters is convenient for the PET application.

7.4 Edge passivation by PET

7.4.1 Proof-of-concept

The proof-of-concept of the PET approach was first published in Ref. [175][9]. The study investigates the impact of the different separation processes: laser scribing and mechanical cleaving (LSMC) as well as thermal laser separation (TLS) on the outcome of the PET results on solar cells. Industrial p-type Cz-Si:Ga passivated emitter and rear cell (PERC) precursors with an edge length of 156.75 mm are used for the fabrication of host cells featuring the *Gen4* metallization layout. Both separation processes cause similar pFF losses $\Delta pFF = -1.2\%_{abs}$, showing the similar edge recombination impact on cell level after separation. However, after PET by the deposition and annealing of Al_2O_3 layers with $d_1 = 7$ nm and $d_2 = 14$ nm thicknesses, the highest regain in pFF is measured on TLS-separated cells showing $\Delta pFF = +0.7\%_{abs}$.

The LSMC-separated cells show a $\Delta pFF = +0.3\%_{abs}$ after edge passivation. The stability of the results after ambient air storage in the dark depends on the deposited Al_2O_3 layer thicknesses $d_1 = 7$ nm and $d_2 = 14$ nm. Cells deposited by $d_1 = 7$ nm show a reduction in pFF even after the first stability measurement after 73 hours of storage. The thicker layer $d_2 = 14$ nm demonstrates stable results with pFF values staying constant (i.e., deviations of less than $\Delta pFF \leq 0.1\%_{abs}$) even after around a week of storage.

As summarized in Table 7.1, IV measurement results showed a pSPEER^{PET} solar cell peak designated area output power density $p_{out} = 23.5$ mW/cm^2 for the TLS-separated cell with PET. The result was + 0.4 mW/cm^2 higher than that of an LSMC-separated cell without PET. Although LSMC-separated cells are also positively influenced by PET, the results in the investigation demonstrate the advantage of TLS-separated smoother edges with lower surface defects for an enhanced edge passivation quality. These results are specific for the chosen cell architecture, initial host cell performance level, and its metallization layout design.

[9] The author of the dissertation is also the first author of the paper in Ref. [175].

Table 7.1. IV data for *p*SPEER solar cells with the highest p_{out} results from each of the cells: (i) LSMC-separated cells and (ii) TLS-separated edge-passivated cells. Designated area measurement results (i.e., excluding the busbar area) are provided since the cell busbars are intended to be covered by shingling. The measured total cell area is $A_{tot} = 3263$ mm². The cell tester is calibrated using reference shingle cells measured at *Fraunhofer ISE CalLab PV cells*. Adapted from Ref. [175].

Measured side	η_{des} (%)	V_{OC} (mV)	$j_{SC,des}$ (mA/cm²)	*FF* (%)	*pFF* (%)	r_S (Ωcm²)	β (%)	p_{out} (mW/cm²)
LSMC-separated cell without PET								
Front side	21.7	667	40.3	80.9	82.4	0.35	66	23.1
Rear side	14.4	657	27.0	81.0	82.0	0.35		
TLS-separated cell with PET								
Front side	22.1	669	40.5	81.4	83.2	0.38	67	23.5
Rear side	14.7	660	27.2	81.8	82.8	0.35		

With the progress in the dissertation, advancements in the TLS, as well as an increased understanding of the low temperature Al_2O_3-based silicon surface passivation processes are achieved; discussed in the chapters 5 and 6. Considering the findings in the separate fields, another experiment is performed that aims to fabricate *p*SPEER^{PET} solar cells by incorporating the optimized TLS process, suitable surface passivation processes, and the *Gen6* metallization layout design.

7.4.2 Experimental details for *p*SPEER^{PET} solar cell fabrication

Host cell fabrication

For the fabrication of the host cells, the basic frontend and backend process sequence of PERC, explained in section 3.2, is performed. Two groups of materials are used to fabricate full wafer-sized host cells that are (i) *ISE* frontend and backend processed, and (ii) *ISE* backend processed. This indicates that group 1 undergoes both the frontend and the backend processes at *Fraunhofer ISE*. For the fabrication of host cells in group 2, the frontend processes are performed externally, while the backend processes are completed internally.

The starting material for the group 1 samples undergoing the frontend processes internally are as-cut *p*-type boron-doped Czochralski-grown (Cz-Si:B) wafers with an edge length of 156.75 mm. The base

resistivity ρ_B of the samples is on average $\rho_B = (0.73 \pm 0.01)$ Ωcm. After the alkaline texturing, the wafers undergo the phosphorous oxychloride ($POCl_3$) emitter diffusion process where the emitter is formed leading to an average emitter sheet resistance $R_{sh} = (95 \pm 3)$ Ω/sq. The following wet chemical process removes the rear side emitter and etches the phosphosilicate glass (PSG)/SiO_2 layer stack on the front side. The rear side is then surface passivated by a post-cleaning 6 nm-thin Al_2O_3 layer, afterwhich an outgassing step in a tube furnace is performed. Next, the Al_2O_3 layer is capped by a 75 nm-thick silicon nitride (SiN_X) layer. The layer combination leads to a rear side that is optically optimized for bifacial applications. Group 2 samples are industrial *p*-type Cz-Si:Ga passivated precursors with an edge length of 156.75 mm. The precursors feature ρ_B values ranging between 0.3 Ωcm ≤ ρ_B ≤ 0.9 Ωcm. The rear side of the precursors is passivated by Al_2O_3 capped by a thick SiN_X layer, which correspond to precursors optimized for the fabrication of monofacial cells.

Both groups 1 and 2 undergo an identical backend process sequence. The backend process steps start with the rear local laser contact opening process, followed by the rear side silver non-firethrough busbar printing step. The screen printing of the rear side aluminum contact grid covering the laser-ablated openings is performed. Next, the front side silver busbars and fingers are screen printed in a dual print process, such that the busbars are printed first, followed by the fingers. The *Gen6* layout is designed to obtain five shingle cells per host cell, where each cell has the designed total area A_{tot} = 22 mm x 156.75 mm. After that the metal-semiconductor contact is formed in the firing process. In the case of group 1, the rear side aluminum finger is measured to have an average finger width $w_{f,RS} = (204 \pm 2)$ µm, while the front side silver finger width features $w_{f,FS} = (34 \pm 1)$ µm. The rear side and front side busbar pads show average thicknesses of $w_{BB,RS} = (534 \pm 2)$ µm, and $w_{BB,FS} = (734 \pm 3)$ µm, respectively. In the case of group 2 cells, $w_{f,RS} = (217 \pm 4)$ µm, $w_{f,FS} = (33 \pm 1)$ µm, $w_{BB,RS} = (526 \pm 7)$ µm, and $w_{BB,FS} = (729 \pm 3)$ µm are obtained.

PET for cells

The experimental process flow after the fabrication of the host cells is shown in Fig. 7.4. The host cells from group 1, that feature a Cz-Si:B base material undergo boron-oxygen regeneration by means of an ultrafast regeneration (UFR) process [142, 143]. Host cells from group 2 do not

require a UFR, since Cz-Si:Ga material is not prone to boron-oxygen-related light-induced degradation. The host cells of both groups are measured by the SunsV_{OC} technique as discussed in section 4.4.2. Three positions on each busbar are contacted by the measurement probe.

The host cells of both groups are separated from the rear side by TLS considering the process parameters chosen for the separation of PERC cells. Next, the separated cells are measured by the SunsV_{OC} technique to characterize the impact of the separation. After that, the separated cells from both host cell groups are divided among five subgroups undergoing: (i) no deposition (i.e., without), (ii) deposition at temperature $T_{dep} = 130°C$ and Al_2O_3 layer thickness $d_1 = 7$ nm, (iii) $T_{dep} = 130°C$ and $d_2 = 14$ nm, (iv) $T_{dep} = 95°C$ and $d_2 = 14$ nm, and (v) $T_{dep} = 130°C$ and $d_3 = 28$ nm. The separation and deposition steps are completed on the same processing day. The thermal atomic layer deposition (ALD) takes place in the *FlexAL* reactor; explained in section 6.4. The cells are stacked in the reactor such that 48 shingle cells are processed in one run. The stacking of cells on top of each other does not allow a conformal deposition on the areas between the cells. Fig. 7.5 shows images of (a) the front side and (b) the rear side of shingle cells from group 1 that feature the different post-metallization Al_2O_3 thicknesses. The wrap around effect of the deposition leads to the coating of the edges and also the front and rear side busbars. With the increase of the deposited Al_2O_3 layer thickness, the color of the cells also changes particularly at the exposed regions near the edge.

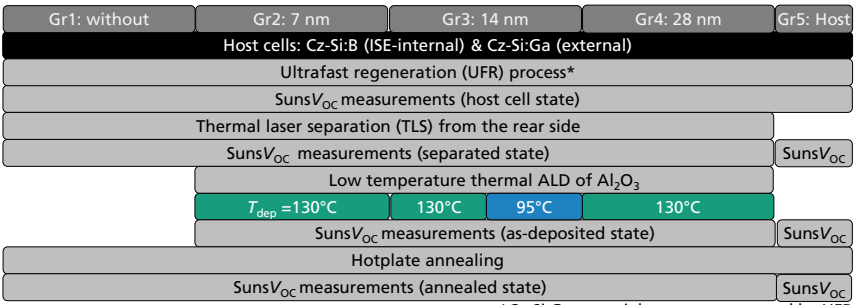


Fig. 7.4. Process flow for the experimental investigation of PET impact. The process steps and characterization steps are shown.

Once deposited, the cells are measured again by SunsV_{OC} technique in the as-deposited state. Finally, the cells are measured after hotplate annealing at temperature $T_{ann} = 200°C$ and for the duration $t_{ann} = 25$ min. Other host cells undergo only an annealing process and are measured as a reference for the quantification of the annealing impact. A reference cell, not shown in the process flow, is measured to monitor the reproducibility of the SunsV_{OC} measurements.

7.4.3 *p*SPEER^{PET} solar cell results and discussion

The SunsV_{OC} measurement results at all the stages are plotted in Fig. 7.6 and Fig. 7.7 for group 1 and group 2, respectively. The host cells from group 1 achieve an average $V_{OC} = (669 \pm 3)$ mV and an average $pFF = (83.3 \pm 0.2)\%$, while host cells of group 2 achieve $V_{OC} = (674 \pm 3)$ mV and $pFF = (83.8 \pm 0.2)\%$. Throughout the measurement states, the mean V_{OC} values do not change significantly showing a

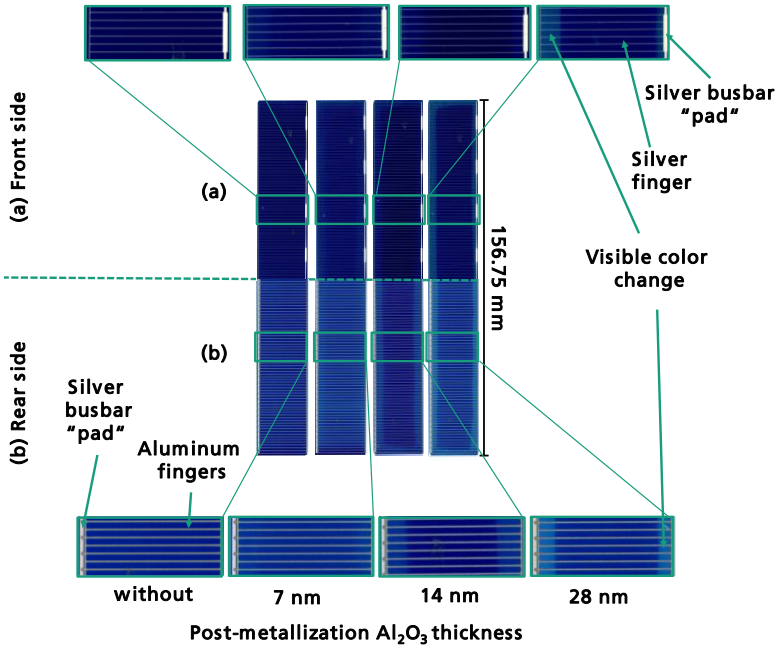


Fig. 7.5. Photographs of *p*SPEER solar cells from group 1. Different post-metallization Al_2O_3 thicknesses from (a) the front side and (b) the rear side. With the increase of the deposited Al_2O_3 thicknesses, the stronger change in color is visible.

highest variation reaching $\Delta V_{OC} = \pm$ 2 mV. These results agree with the simulation results shown in Refs. [170, 171], which show such deviations in V_{OC} values for cells in this performance range (i.e., initial V_{OC} level). The discussion of each process's impact is based on the *pFF* results which influences η. The results of each of the groups 1 and 2 is discussed separately, followed by a general discussion.

Group 1: Frontend and backend ISE (Cz-Si:B)

As shown in Fig. 7.6(b), the separation process leads to an average reduction in *pFF* of $\Delta pFF = -0.7\%_{abs}$ from the host cell to shingle cell stage. This drop in *pFF* is caused by an increase in edge recombination. After PET, the highest average *pFF* increase of $\Delta pFF = +0.5\%_{abs}$ from the separated to the edge passivated state is observed on the cells processed with $T_{dep} = 95°C$ and $d_2 = 14$ nm. The average *pFF* values stay constant for the group of cells deposited with $T_{dep} = 130°C$ featuring the thinnest layer $d_1 = 7$ nm.

The other cell groups that undergo PET show an average increase $\Delta pFF = +0.4\%_{abs}$ from the separated to the annealed state. The cells that undergo just the annealing step, show a decrease of $\Delta pFF = -0.1\%_{abs}$ from the separated to the annealed state.

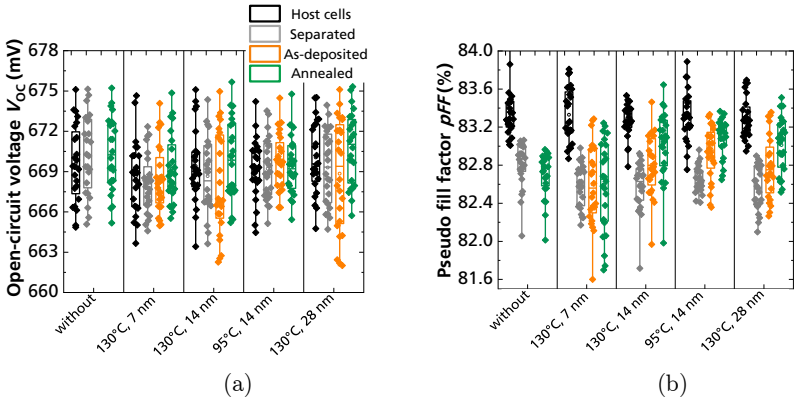


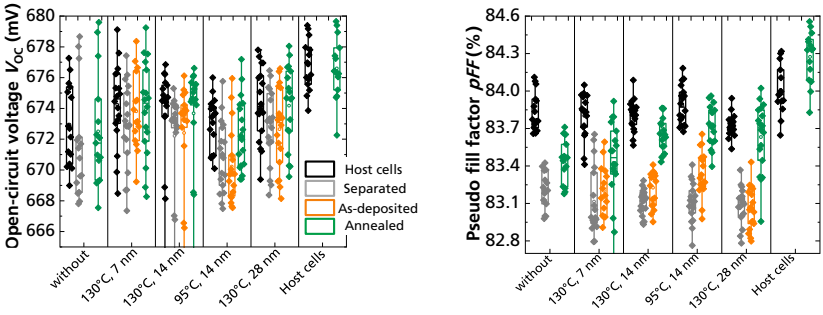
Fig. 7.6. SunsV_{OC} measurement results for the investigation of PET showing (a) V_{OC} and (b) *pFF* on cells fabricated in *ISE* frontend and backend (group 1). Measurement results at the different stages: (i) host cell, (ii) separated, (iii) as-deposited, and (iv) annealed are shown (i.e., boxplots from left being the host cells to right being the annealed cell). Data from Ref. [234].

Group 2: Backend ISE (Cz-Si:Ga)

As a result of edge recombination, the separation process leads to the reduction in *pFF* values that are quantified by an average drop of $\Delta pFF = -0.7\%_{abs}$ from the host cell to shingle cell stage; see Fig. 7.7(b). Applying the PET leads to the highest average *pFF* increase of $\Delta pFF = +0.6\%_{abs}$ from the separated to the edge-passivated state. This is observed on the cells processed with $T_{dep} = 95°C$ that feature $d_2 = 14$ nm. The increase corresponds to about $80\%_{rel}$ regain of *pFF* because of the PET. The lowest *pFF* increase of $\Delta pFF = +0.3\%_{abs}$ is shown on the cells processed with $T_{dep} = 130°C$ featuring the thinnest layer $d_1 = 7$ nm.

The other cell groups that undergo PET show a high *pFF* increase of $\Delta pFF = +0.5\%_{abs}$ from the separated to the annealed state. The annealing activation process is necessary for the boost in the *pFF* values. The cells that do not undergo PET show an increase by $\Delta pFF = +0.2\%_{abs}$ from the separated to the annealed state. The annealed host cells show an increase $\Delta pFF = +0.3\%_{abs}$. Considering these results the edge passivation by PET itself contributes to an increase of $\Delta pFF = +0.4\%_{abs}$.

It is evident that the PET process performed at $T_{dep} = 95°C$ featuring $d_2 = 14$ nm shows the highest gains in *pFF* for both cell groups 1 and 2. IV data for *p*SPEER solar cells with the highest p_{out} results from each of the groups are shown in Table 7.2. In the case of group 1 cells, the solar cell with the highest p_{out} attains $p_{out} = 23.6$ mW/cm² (considering an



(a) (b)

Fig. 7.7. SunsV_{OC} measurement results for the investigation of PET showing (a) V_{OC} and (b) *pFF* on cells fabricated in *ISE* backend (group 2). Measurement results at the different stages: (i) host cell, (ii) separated, (iii) as-deposited, and (iv) annealed (i.e., boxplots from left being the host cells to right being the annealed cell). Data from Ref. [234].

additional rear side irradiance of $G_{rear} = 100$ W/m²). On the front side $\eta_{des} = 21.9\%$, $V_{OC} = 668$ mV, $j_{SC,des} = 40.8$ mA/cm², $FF = 80.3\%$, and $r_S = 0.46$ Ωcm² are determined. The cell attains the highest recorded bifaciality $\beta = 76\%$ shown in this dissertation, because of the optimized rear side surface passivation layers and metallization layout. In the case of group 2 cells, the highest $p_{out} = 23.7$ mW/cm² is attained featuring front side $\eta_{des} = 22.2\%$, $V_{OC} = 675$ mV, $j_{SC,des} = 40.7$ mA/cm², $FF = 80.7\%$, and $r_S = 0.45$ Ωcm². A $\beta = 66\%$ is achieved, knowing that the rear side surface passivation is not optimized for bifacial use.

The results show that despite the post-metallization annealing step, very low r_S values are preserved while leading to an enhanced cell performance by the PET. The presence of Al_2O_3 dielectric layers on the busbars raises concerns about the electrical resistances on the interconnection level, which are being further investigated. Nevertheless, the PET applied on TLS-separated silicon heterojunction (SHJ) half solar cells also show an improved cell performance even after module integration by conventional interconnection [255].

Table 7.2. IV data for *p*SPEER^{PET} solar cells with the highest p_{out} results from each of the cells from group 1 completely internally-fabricated (i.e., frontend and backend process steps) and cells from group 2 fabricated in the backend starting from industrial precursors. Designated area measurement results (i.e., excluding the busbar area) are provided since the cell busbars are intended to be covered by shingling. The measured total cell area is $A_{tot} = 3449$ mm². The cell tester is calibrated using reference shingle cells measured at *Fraunhofer ISE CalLab PV cells*.

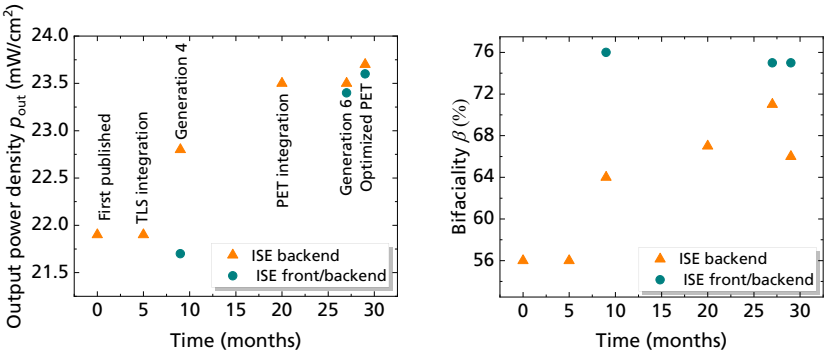
Measured side	η_{des} (%)	V_{OC} (mV)	$j_{SC,des}$ (mA/cm²)	*FF* (%)	*pFF* (%)	r_S (Ωcm²)	β (%)	p_{out} (mW/cm²)
Group 1: Internal frontend and backend (Cz-Si:B)								
Front side	21.9	668	40.8	80.3	82.3	0.46	75	23.6
Rear side	16.5	660	30.9	81.1	82.1	0.34		
Group 2: Internal backend (Cz-Si:Ga)								
Front side	22.2	675	40.7	80.7	82.7	0.45	66	23.7
Rear side	14.7	662	27.3	81.4	82.3	0.34		

7.5 Performance development of bifacial shingle solar cells

Throughout the dissertation work that started in 2017, the bifacial shingle cells have been improved, leading to enhanced p_{out} values with the progress of the work. The development is achieved by improvements in the PERC precursors used, the updates in metallization configurations, separation processes, and the integration of PET in the process flow. The most important milestones in the solar cell p_{out} and β are shown in Fig. 7.8(a) and (b), respectively.

The first published *p*SPEER solar cell attained a $p_{out} = 21.9$ mW/cm² (converted from the total area $p_{out} = 21.5$ mW/cm² to a designated area result by using equation (4.1)) [173]. The backend processes were performed inhouse. Moreover, these cells were separated by means of laser scribing and mechanical cleaving. Using similar host cells with the identical *Gen1* metallization layout, the first *p*SPEER cells with thermal laser separation (TLS) were fabricated [256]. A similar $p_{out} = 21.9$ mW/cm² has been attained.

The adaptation to the *Gen4* metallization with thinner finger widths on the rear side as well as further optimized rear side optics lead to $\beta = 76\%$ and $p_{out} = 21.7$ mW/cm². These were the first completely internally-fabricated *p*SPEER solar cells and both frontend and backend processes were conducted internally. These cells were fabricated in parallel to the



(a) (b)

Fig. 7.8. Progress of the *p*SPEER solar cell results throughout this dissertation time frame showing p_{out} and β starting from the first published paper. Designated area values excluding the busbar area are shown in the plots.

production of the first bifacial PERC solar cells in the *PV–TEC*-Frontend and Backend laboratories. Meanwhile, *p*SPEER solar cells with external precursors featuring the *Gen4* layout, described in detail in Ref. [257], were also fabricated attaining $p_{out} = 22.8$ mW/cm² [258].

As a derivative of *p*SPEER solar cells, the application of PET lead to the adapted *p*SPEER^{PET} solar cell architecture. The first published results presented a cell with an achieved $p_{out} = 23.5$ mW/cm² [175].

As a result of the TLS combined with the developed PET and the optimizations in the metallization layout of *Gen6*, the completely internally-fabricated cells attain a $p_{out} = 23.6$ mW/cm² featuring $\beta = 75\%$. Meanwhile, cells fabricated from external precursors attain $p_{out} = 23.7$ mW/cm² with a $\beta = 66\%$.

Apart from the obtained results on PERC cell structures, the PET approach is also attractive for the post-metallization/separation treatment of other silicon solar cell concepts. PET has been also tested on silicon SHJ half cells in combination with industrial annealing [255]. First results are also shown on shingle solar cells with TOPCon cell architecture.

7.6 Current industry status of separated solar cells

During the progress of this dissertation, harvesting the advantages of separated solar cell concepts, the photovoltaics market witnessed a gradual shift towards separated silicon solar cell concepts (i.e., mainly half solar cells) [259]. This was clearly shown by the introduction of commercial photovoltaic modules with conventionally-interconnected half cells [13]. Additionally, an increasing interest in the topics of shingling was evidently seen by the increasing number of publications [260–264]. Recently, several companies have adopted the approach showing the increase of interest by an increasing number of patents [265, 266], and commercially available monofacial modules with cells interconnected by shingling [267–269].

Due to the advantages provided by separated cells, their market share is expected to rise in the upcoming years [5]. Wafer sizes with increased edge lengths 182 mm up to 210 mm are already available in the market [32]. Cells fabricated with larger wafer sizes require the separation of cells prior to interconnection. In 2020, with the use of such cell formats, record modules with rated powers of above 500 W have been achieved by cells

featuring at least one separated edge [270–273]. Particular advantages of the shingling technique are shown in cell-interconnection configurations such as the "Matrix" which is interesting for the growing field of vehicle integrated photovoltaics applications [174].

7.7 Chapter summary

This chapter first reviews the existing approaches previously used for edge passivation. Some of the approaches available in the literature demand numerous frontend passivation processes for, e.g., the emitter window approach formed by diffusion barriers. Other approaches involve post-metallization wet-chemical edge treatment. The post-metallization passivated edge technology (PET), introduced in chapter 4, is then experimentally investigated on the solar cell level.

Knowing that the PET involves a deposition and an annealing step, the impact of the successive post-metallization annealing (PMA) on *p*SPEER solar cells is characterized by current-voltage (IV) measurements. Additionally, the PMA influence on the front side contact resistivity $\rho_{C,FS}$, rear side contact resistivity $\rho_{C,RS}$, and finger resistances is studied. In total four annealing steps are considered with different set annealing temperatures T_{ann} and durations t_{ann}. Cumulative annealing is performed such that cells and test structures are measured in between successive annealing steps. It is shown that the first annealing step at $T_{ann} = 200°C$ and $t_{ann} = 25$ min, has no detrimental impact on cells or cell structures. Additional annealing steps lead to the reduction of open-circuit voltage ΔV_{OC} and rise in fill factor ΔFF. After the fourth (last) annealing step that takes place at $T_{ann} = 300°C$ and $t_{ann} = 120$ min, a total energy conversion efficiency η loss of $\Delta\eta = -0.7\%_{abs}$ is observed in comparison to the initial cell values. This is caused by an average reduction $\Delta V_{OC} = -5$ mV, $\Delta FF = -1.9\%_{abs}$, and average losses in short-circuit current density $\Delta j_{SC} = -0.2$ mA/cm². Moreover, the losses in *FF* are explained by the rise in series resistance $\Delta r_S = +0.26\ \Omega cm^2$ and the drop in pseudo fill factor of $\Delta pFF = -0.6\%_{abs}$. On cell level, it is evident that excessive PMA leads to the degradation of both the surface passivation and the metal-semiconductor contact. The results on the test structures show the rise of $\rho_{C,FS}$ reaching $\Delta\rho_{C,FS} = +2.1\ m\Omega cm^2$ in one of the tested groups after the final annealing stage. The $\rho_{C,RS}$ and finger resistance value stay constant even after the last annealing step. The results can be explained by referring to previous

studies expecting a restructuring of the front side contact interface between the emitter and silver bulk after extensive PMA. The rear side contact is shown to be robust at such thermal budget levels. Nevertheless, a single selected PMA step at $T_{ann} = 200°C$ and $t_{ann} = 25$ min does not damage already existing cell structures. This means a single PMA step can be used in PET for the activation of the passivation layer.

The influence of the PET approach on TLS-separated and laser-scribed and mechanically cleaved (LSMC) solar cells is explained. PET process steps have a positive impact on cells separated by both separation methods mainly quantified by a rise in *pFF*. Yet, the highest gains are seen on TLS-separated cells where $\Delta pFF = +0.7\%_{abs}$ from the as-separated state is achieved (i.e., regaining around $50\%_{rel}$). A thicker Al_2O_3-deposited layer $d_2 = 14$ nm shows stable results after storage in ambient air environment. Such stability in *pFF* results is not confirmed for cells deposited with a thinner layer of $d_1 = 7$ nm. TLS-separated edge passivated cells attain an output power density $p_{out} = 23.5$ mW/cm² that is + 0.4 mW/cm² higher than a reference group separated by LSMC and does not undergo PET. For an enhanced edge passivation, a separation process that leads to lower surface defects is required.

With the progress of the dissertation in the separation and surface passivation processes, an experiment joining the relevant findings from each of the fields is performed for the fabrication of *p*SPEER^{PET} solar cells. Two main groups of cells are fabricated, where group 1 undergoes the frontend and backend processes starting from *p*-type Cz-Si:B wafers and group 2 undergoes the backend processes starting from *p*-type Cz-Si:Ga PERC precursors. The separation in both groups leads to average drops in *pFF* being $\Delta pFF = -0.7\%_{abs}$ because of edge recombination. The PET process performed at $T_{dep} = 95°C$ featuring $d_2 = 14$ nm shows the highest gains in *pFF* for both cell groups 1 and 2. Group 1 cells show a gain of $\Delta pFF = +0.5\%_{abs}$ and group 2 records $\Delta pFF = +0.6\%_{abs}$. A regain of about $80\%_{rel}$ from the initial ΔpFF separation-related loss is demonstrated by the application of the PET. The most efficient cell from group 1 attains a designated area output power density $p_{out} = 23.6$ mW/cm² featuring a bifaciality $\beta = 76\%$. The most efficient *p*SPEER^{PET} solar cell result from group 2 attains $p_{out} = 23.7$ mW/cm² and $\beta = 66\%$.

Finally, the historical performance development of the bifacial shingle solar cell within this work is discussed. The development has a come a long way

from the first published *p*SPEER solar cell featuring a peak designated area $p_{\mathrm{out}} = 21.9\ \mathrm{mW/cm^2}$, to the most efficient *p*SPEER$^{\mathrm{PET}}$ solar cell result $p_{\mathrm{out}} = 23.7\ \mathrm{mW/cm^2}$.

8 Summary and Outlook

In this dissertation, the bifacial p-type silicon shingled passivated edge, emitter, and rear (pSPEER) solar cell is developed. The solar cell concept connects the ideas of shingling, bifaciality, and the p-type silicon passivated emitter and rear cell (PERC) technology. Shingling (i.e., overlapping) of separated solar cells increases the active cell area within the photovoltaic module, reduces shading losses by the visually busbarless appearance, and decreases the electrical resistance losses on the interconnection level. Having both, bifacial solar cells, and solar modules, improves the output power density p_{out} by making use of the rear side irradiance. As a derivative of the PERC solar cell, the pSPEER solar cell benefits directly from the advancements made in the PERC fabrication. The pSPEER solar cell features a p-type silicon base – in this dissertation it is Czochralski-grown silicon (Cz-Si). The front side phosphorous-doped emitter is coated and passivated by a silicon dioxide (SiO_2)/silicon nitride (SiN_X) passivation layer stack. The rear side passivation consists of dielectric layers comprising SiO_2, aluminum oxide (Al_2O_3), and SiN_X. The emitter is contacted by a silver finger grid, while the rear side contacts are formed by an aluminum finger grid. The laser-assisted separation conducted after contact firing is an additional process step to the PERC sequence. In this step, the full wafer-sized host cell, e.g., with 156.75 mm edge length, is separated into for example six shingle cells with widths of 26.125 mm each.

This post-metallization separation process results in solar cells with newly formed cell edges on which native growth of SiO_2 occurs. Nevertheless, the absence of a high quality surface passivation on these new edge surfaces eventually leads to high edge recombination and thus to energy conversion efficiency losses. To reduce the recombination at the obtained edges, the passivated edge technology (PET) is developed within this work as a post-metallization/separation edge passivation approach. The PET itself comprises an Al_2O_3 layer formation at low deposition temperatures of a maximum of 130°C by means of thermal atomic layer deposition (ALD) and

a post-deposition annealing (PDA) step at temperatures of 200°C or below. The low temperature processing prevents possible damage to the solar cell's metal contacts and/or surface passivation. As a result of the conformal ALD coating, the Al_2O_3 passivation layer is deposited all over the complete cell including the busbars and the edges. Applying PET on *p*SPEER solar cells leads to a new solar cell architecture, introduced as "*p*SPEER^{PET}".

The shingle solar cells feature smaller cell sizes in comparison to conventional full cell or half cell formats. For the accurate characterization of shingle solar cells, an adapted current-voltage (IV) measurement contacting scheme is presented. This allows the IV measurement of shingle solar cells by contacting the front side and rear side busbars using IV-pin arrays. Besides, a contacting approach to use the SunsV_{OC} measurement technique is introduced that allows the very accurate measurements of solar cells in different post-metallization states such as the full wafer-sized host cells, the separated shingle cells, and the edge-passivated shingle cells. The measurements are conducted by considering identical contacting positions on the separated shingle cell's busbars to that of their original positions within the host cells before separation. As the position-dependent open-circuit voltages V_{OC} and pseudo fill factors *pFF* are determined, the deduction of process-related changes, such as separation or edge passivation, are possible.

The separation process after contact firing is an essential step in the fabrication sequence of separated solar cells. For that reason, emphasis is placed on the thermal laser separation (TLS) which is also applied to produce, e.g., half solar cells in industry. The TLS technology comprises two laser-based steps: (i) A scribe process that forms a short initial crack at a wafer edge, and (ii) a non-ablative cleave process that propagates the crack in a desired direction by induced thermal stress. The cleave process itself consists of the application of a laser beam that locally heats the substrate and an immediately following cooling by a water/air aerosol jet. The TLS process leads to smooth cell edges with low surface defect density. Although the cleave process takes place at temperatures well-below the melting point of silicon, the thermal budget can still have an impact on the surface passivation layers present on solar cells. In this work, a method using photoluminescence (PL) imaging is introduced to optimize the TLS cleave process by observing the impact of different process parameters on solar cell precursors. By conducting the laser cleave process without applying the initial laser scribe, the wafers are kept in their full wafer-sized formats. This allows the individual investigation of the cleave process with

its elliptical beam spot and water/air cooling. Several cleave lines can be applied on a sample, for e.g., four lines, each with varying process parameters. For the parameter range investigated, the increase of cleave laser power P_C causes proportional PL signal drops $\varphi(x)$ on boron-doped Cz-Si PERC precursors. The reduction in $\varphi(x)$ can be attributed to the reduction of the surface passivation quality near the separation path and/or to boron-oxygen-related light-induced degradation (LiD). However, the surface passivation reduction and/or the induced LiD after the cleave process is not a permanent issue. This is proven by a regain of the lost $\varphi(x)$, e.g., after an additional ultrafast regeneration (UFR) process. In the case of silicon heterojunction (SHJ) cell precursors, an increase of P_C leads to accordingly proportional $\varphi(x)$ drops. The reduction in $\varphi(x)$ is attributed to degradation of the surface passivation quality. Applying the same UFR process as above does not yet lead to any regain in $\varphi(x)$.

For each of the two cell precursor types, optimized cleave parameters are determined. The optimized process is defined as the one that leads to the least $\varphi(x)$ drop but still to a successful mechanical separation in case the scribe process is performed. As an example, four cleave lines, corresponding to a $1/5^{th}$ shingle cell format, are applied. The solar cells that undergo only the cleave process (no initial scribe) show a loss in pFF of $\Delta pFF = -0.1\%_{abs}$ in case of PERC and of $\Delta pFF = -0.4\%_{abs}$ in case of SHJ. For completely TLS-separated cells, i.e., the scribe and cleave processes are both conducted, a mean pFF drop of, e.g., $\Delta pFF = -0.3\%_{abs}$ is recorded in the case of PERC shingle cells. For SHJ shingle cells, $\Delta pFF = -2.1\%_{abs}$ is found after complete separation. The results show that the newly formed edge surfaces cause the main portion of the pFF loss. This also indicates that the optimized cleave process has a secondary impact on the separation loss.

In another investigation, the electrical performance of solar cells with different sizes separated by TLS are compared to cells separated by laser scribing and mechanical cleaving (LSMC). The LSMC technique, also used in industry, consists also of two process steps: (i) A laser scribe process that is performed along the entire separation path, and (ii) a mechanical breaking process that then physically separates the substrates. For cells processed from the emitter-free rear side, the advantage of TLS-separated cells is clearly seen with the decrease of PERC cell sizes. The smallest investigated cell has a total cell area $A_{tot} = 1.15$ cm x 1.15 cm ≈ 1.32 cm² (i.e., around 0.5% of the host cell area). The V_{OC} and pFF differences from the host cell to the separated cells becomes larger with the decrease of the

cell size. Taking the example of the smallest cell with $A_{tot} \approx 1.32$ cm² under low illumination conditions, for which the impact of edge recombination is the strongest, the LSMC-separated cell shows a drop in V_{OC} of around $5\%_{rel}$ (i.e., $\Delta V_{OC,low} = -29$ mV) from the host cell to the separated state, while the TLS-separated one shows only a drop of $4\%_{rel}$ (i.e., $\Delta V_{OC,low} = -23$ mV). Additionally, a *pFF* drop of around $6\%_{rel}$ (i.e., $\Delta pFF = -5.3\%_{abs}$) is found in the case of the LSMC-separated cell while the TLS-separated one shows only a drop of $4\%_{rel}$ (i.e., $\Delta pFF = -3.2\%_{abs}$). A plausible explanation of the reason behind the advantage of TLS is the defect poorer edges in comparison to that of the LSMC-separated cells.

For the PET, Al_2O_3 layers are used because they offer a high quality surface passivation by combining good chemical with a strong field effect passivation. In the case of thermal ALD of Al_2O_3 layers, a PDA step is required for the activation of the passivation layer properties leading to high quality surface passivation. In this work, excellent surface passivation is demonstrated by effective surface recombination velocities $S_{eff} = 4.4$ cm/s for *p*-type silicon and $S_{eff} = 5.7$ cm/s for *n*-type silicon. These results show a record for low S_{eff} values achieved by thermal ALD Al_2O_3 surface passivation layers at the investigated deposition temperatures T_{dep} equal to or below 130°C. Moreover, an interdependency of T_{dep} and the annealing temperatures T_{ann} is observed. As an example, the lowest investigated $T_{dep} = 60$°C requires the lowest $T_{ann} = 150$°C for an effective activation of the surface passivation properties. To investigate the stability of the surface passivation over time, the samples are stored in the dark and are remeasured after different time intervals up to 120 days. In most cases, a very stable behavior in the passivation quality is found for the samples deposited at $T_{dep} = 95$°C and $T_{dep} = 130$°C with 14 nm to 16 nm thick Al_2O_3 layers. Samples deposited at $T_{dep} = 60$°C show drops in their effective lifetimes already after the first stability measurement (after one day) independent from the Al_2O_3 layer thickness. Even after 120 days, for some cases, $S_{eff} < 10$ cm/s is obtained which still corresponds to an excellent surface passivation for solar cell fabrication. The results show the potential of the developed surface passivation for the use as PET as well as other technologies where temperature-sensitive substrates are processed.

Combining the advancements in the TLS process and the low temperature surface passivation, the impact of PET on metallized solar cells is investigated. The cells are characterized in the following states: (i) host cell, (ii) separated cell, (iii) as-deposited, and (iv) annealed. The work demon-

strates that the TLS process leads to an average drop of $\Delta pFF = -0.7\%_{abs}$ because of the high edge recombination directly after separation. With the application PET, a regain of about $80\%_{rel}$ from the initial ΔpFF loss by the separation could be demonstrated. This implies that the total loss after TLS and PET can be reduced to only $\Delta pFF = -0.1\%_{abs}$. The results show the effective functionality of the PET approach and the successful integration within the process sequence for the fabrication of edge-passivated pSPEER^{PET} solar cell.

During this dissertation, bifacial shingle PERC solar cells are developed through targeted process optimization runs, both in the frontend and in the backend. The use of industrial p-type Cz-Si PERC precursors with passivation layers on both sides supported various optimization batches in the backend processes. Completely internally-fabricated cells starting from as-cut p-type Cz-Si wafers undergo both the frontend and the backend processes. This offers the flexibility in developing tailor-made processes for the required application such as the development of the rear side passivation to boost the bifaciality β of the cells. The most efficient pSPEER^{PET} solar cell fabricated from the industrial PERC precursors yields $p_{out} = 23.7$ mW/cm^2 and $\beta = 66\%$ (considering an additional 10 mW/cm^2 rear side irradiance). These precursors feature a rear side SiN_X layer that is optimized for monofacial use. In the case of the internally-fabricated pSPEER^{PET} cells, the rear side optical properties are optimized by a thinner rear side SiN_X capping layer for enhanced rear side light coupling. The most efficient completely internally-fabricated pSPEER^{PET} cell achieves a $p_{out} = 23.6$ mW/cm^2 and the highest $\beta = 76\%$. With the developments during the progress of the dissertation, highly-efficient bifacial shingle solar cells are fabricated.

As an outlook on the solar cell level, the integration of selective emitter structures can further boost their performance. This can be either a selective laser doped emitter on the front side for improved contact properties of the metallization and/or the creation of emitter windows at the edges of the shingle solar cells to further reduce edge recombination. Apart from the current PET approach, for which the Al_2O_3 layer deposition occurs all over the cell surfaces including the metallization, also the investigation of local layer deposition techniques that ideally only coat the surfaces of the edges offer further optimization potential. This comes hand-in-hand with the necessity of upscaling the corresponding PET process into pilot-line production, also for larger wafer formats with wafer edge lengths of

currently up to 210 mm. On the module interconnection level, the integration of edge-passivated solar cells in different stringing schemes, such as conventional or matrix interconnection, needs to be examined.

The work demonstrates the successful development of bifacial *p*-type silicon shingle solar cells by integrating TLS and PET to obtain edge-passivated *p*SPEER$^{\mathrm{PET}}$ solar cells. For these cells, around 80%$_{\mathrm{rel}}$ of the separation-related *pFF* losses could be regained by applying the developed PET process sequence. This significant reduction of the edge recombination losses has been first demonstrated within this work and is fundamental for the further research, development, and application of the singulation concept in highest efficiency photovoltaic devices.

9 Deutsche Zusammenfassung

Die vorliegende Dissertation beschreibt die Entwicklung bifazialer „*p*-Type Shingled Passivated Edge, Emitter, and Rear" (*p*SPEER) Solarzellen. Das neuartige Solarzellenkonzept verbindet die grundlegenden Ideen der Schindeltechnologie, der Bifazialität und der „Passivated Emitter and Rear Cell" (PERC) Solarzellentechnologie miteinander. Die Schindelanordnung (d.h. überlappende Verschaltung) von vereinzelten Solarzellen vergrößert die aktive Zellfläche innerhalb des photovoltaischen Moduls, verringert die Abschattungsverluste durch das visuell busbarlose Erscheinungsbild und verringert die elektrischen Widerstandsverluste auf der Verbindungsebene. Mit beidem, sowohl den bifazialen Solarzellen als auch den Solarmodulen, ergibt sich eine Verbesserung der Ausgangsleistungsdichte p_{out} unter Ausnutzung der rückseitigen Bestrahlungsstärke. Als Derivat der PERC-Solarzelle profitiert die *p*SPEER-Solarzelle direkt von den Fortschritten in der PERC-Herstellung. Die *p*SPEER-Solarzelle verfügt über eine *p*-dotierte Siliciumbasis – in dieser Dissertation handelt es sich um Czochralski-gewachsenes Silicium (Cz-Si). Der mit Phosphor dotierte Emitter auf der Vorderseite ist mit einem Passivierungsschichtstapel aus Siliciumdioxid (SiO_2)/Siliciumnitrid (SiN_X) beschichtet und passiviert. Die rückseitige Passivierung besteht aus einem Stapel dielektrischer Schichten aus SiO_2, Al_2O_3 und SiN_X. Der Emitter wird durch ein Silber-Fingergrid kontaktiert, während die rückseitigen Kontakte aus einem Aluminium-Fingergrid bestehen. Die nach dem Kontakttempern durchgeführte laserbasierte Vereinzelung ist ein zusätzlicher Prozessschritt zur PERC-Sequenz. In diesem Schritt wird die Zelle mit voller Wafergröße, z.B. mit 156,75 mm Kantenlänge in beispielsweise sechs Schindelzellen mit jeweils 26,125 mm Zellbreite aufgetrennt.

Dieser Vereinzelungsprozess nach der Metallisierung führt zu Solarzellen mit neu gebildeten Zellkanten, an denen natives Wachstum von SiO_2 auftritt. Das Fehlen einer hochwertigen Oberflächenpassivierung auf diesen neuen Kantenoberflächen führt aber zu einer hohen Kantenrekombination und damit zu Zelleffizienzverlusten. Um die Rekombination an den erhaltenen Kanten zu reduzieren, wurde im Rahmen dieser Dissertation die „Passivated Edge

Technology“ (PET) als Ansatz zur Passivierung nach der Metallisierung/Vereinzelung entwickelt. Die PET selbst umfasst eine Al_2O_3-Schichtausbildung bei niedrigen Abscheidungstemperaturen von maximal 130°C mittels thermischer Atomlagenabscheidung (ALD) und einem thermischen Temperschritt („Post-Deposition Anneal“, PDA) bei Temperaturen von 200°C oder darunter. Die Niedertemperaturprozessierung verhindert eine mögliche Beschädigung der Metallkontakte der Solarzelle und/oder der Oberflächenpassivierung. Infolge der konformen ALD-Beschichtung wird die Al_2O_3-Passivierungsschicht über die gesamte Zelle einschließlich der Busbars und der Kanten abgeschieden. Die Anwendung von PET auf *p*SPEER-Solarzellen führt zu einer neuen Zellarchitektur die hier als „*p*SPEER$^{\text{PET}}$“ eingeführt wird.

Die Schindelsolarzellen weisen im Vergleich zu herkömmlichen Vollzellen- oder Halbzellenformaten kleinere Zellgrößen auf. Zur genauen Charakterisierung von Schindelsolarzellen wird ein angepasstes Kontaktschema für die Messung der Strom-Spannungs-(IV)-Charakteristik vorgestellt. Dies ermöglicht die IV-Messung von Schindelsolarzellen durch Kontaktieren der vorderen und hinteren Busbars mit IV-Pin-Kontaktleisten. Außerdem wird ein Kontaktierungsansatz zur Verwendung der SunsV_{OC}-Messtechnik eingeführt, der sehr genaue Messungen von Solarzellen in verschiedenen Zuständen nach der Metallisierung ermöglicht, wie z.B. den Zellen mit voller Wafergröße, den vereinzelten Schindelzellen und den kantenpassivierten Schindelzellen. Die Messungen werden durchgeführt, indem die identischen Kontaktpositionen auf den Busbars für die vereinzelten Schindelzellen hinsichtlich ihrer ursprünglichen Positionen innerhalb der Zellen vor der Vereinzelung verwendet werden. Basierend auf den positionsabhängigen Werten für Leerlaufspannung V_{OC} und Pseudo-Füllfaktor *pFF*, lassen sich Rückschlüsse auf prozessbedingte Veränderungen ziehen, z.B. nach der Vereinzelung.

Der Vereinzelungsprozess nach dem Kontakttempern ist ein wesentlicher Schritt in der Herstellungssequenz von vereinzelten Solarzellen. Aus diesem Grund wird ein Schwerpunkt auf das thermische Laserstrahl-Separieren (TLS) gelegt, das auch zur Herstellung von beispielsweise Halbsolarzellen in der Industrie angewendet wird. Die TLS-Technologie umfasst zwei laserbasierte Schritte: (i) einen Scribe-Prozess, der an einer Waferkante einen kurzen initialen Riss ausbildet, und (ii) einen nicht ablativen Cleave-Prozess, der den Riss durch induzierte thermische Spannung in eine gewünschte Richtung vorantreibt. Der Cleave-Prozess selbst besteht aus der Anwendung eines Laserstrahls, der das Substrat lokal erwärmt, und einer unmittelbar folgenden Abkühlung durch einen Wasser-/Luft-Aerosolstrahl. Der

TLS-Prozess führt zu glatten Zellkanten mit geringer Oberflächendefektdichte. Obwohl der Cleave-Prozess bei Temperaturen weit unter dem Schmelzpunkt von Silicium stattfindet, kann das Wärmebudget dennoch einen Einfluss auf die Oberflächenpassivierungsschichten der Solarzellen haben. In dieser Dissertation wird eine Methode unter Verwendung der Photolumineszenz-(PL)-Bildgebung eingeführt, um den TLS-Cleave-Prozess zu optimieren, indem die Auswirkungen verschiedener Prozessparameter auf Solarzellen-Precursoren untersucht werden. Durch Durchführen des Cleave-Laserprozesses ohne Anwendung des initialen Laser-Scribes werden die Wafer in ihren vollen Wafergrößen belassen. Dies ermöglicht die individuelle Untersuchung des Cleaveprozesses mit seinem elliptischen Strahlfleck und der Wasser-/Luft-Kühlung. Auf einer Probe können mehrere Cleave-Linien aufgebracht werden, z.B. vier Linien mit jeweils unterschiedlichen Prozessparametern. Für den untersuchten Parameterbereich verursacht die Erhöhung der Cleave-Laserleistung P_{C} proportionale PL-Signalabfälle $\varphi(\mathrm{x})$ auf mit Bor-dotierten Cz-Si PERC-Precursoren. Die Verringerung von $\varphi(\mathrm{x})$ kann auf die Verringerung der Oberflächenpassivierungsqualität in der Nähe des Trennpfades und/oder durch Bor-Sauerstoff verursachte lichtinduzierte Degradation (LiD) zurückgeführt werden. Die nach dem Cleave-Prozess induzierte Verringerung der Oberflächenpassivierung und/oder der LiD ist jedoch kein dauerhaftes Phänomen. Dies wird durch die Wiedererlangung des verlorenen $\varphi(\mathrm{x})$, z.B. nach einem ultraschnellen Regenerationsprozess (UFR), gezeigt. Im Fall von Silicium-Heterojunction-(SHJ)-Zellprecursoren führt eine Zunahme von P_{C} zu entsprechend proportionalen $\varphi(\mathrm{x})$-Verlusten. Die Verringerung von $\varphi(\mathrm{x})$ wird auf eine Degradation der Oberflächen-Passivierungsqualität zurückgeführt. Die Anwendung des gleichen UFR-Prozesses führt bisher zu keiner Wiedererlangung von $\varphi(\mathrm{x})$.

Für jeden der beiden Zellprecursorentypen wurden optimierte Cleave-Parameter bestimmt. Der optimierte Prozess ist definiert als derjenige, der zur geringsten $\varphi(\mathrm{x})$-Reduktion führt, aber dennoch zu einer erfolgreichen mechanischen Trennung, falls der Scribe-Prozess durchgeführt wird. Als Beispiel werden vier Cleave-Linien angewandt, die einem 1/5-Schindelzellenformat entsprechen. Die Solarzellen, die nur einen Cleave-Prozess durchlaufen (kein initialer Scribe), zeigen bei PERC einen Verlust im pFF von $\Delta pFF = -0{,}1\%_{\mathrm{abs}}$ und bei SHJ von $\Delta pFF = -0{,}4\%_{\mathrm{abs}}$. Für vollständig TLS-vereinzelte Zellen, d.h. die Scribe- und Cleave-Prozesse werden beide durchgeführt, wird im Fall von PERC-Schindelzellen ein durchnittlicher Verlust von z.B. $\Delta pFF = -0{,}3\%_{\mathrm{abs}}$ festgestellt. Für SHJ-Schindelzellen

ergibt sich nach kompletter Trennung ein $\Delta pFF = -2{,}1\%_{abs}$. Die Ergebnisse zeigen, dass die neu gebildeten Kanten den Hauptteil der *pFF*-Reduktion verursachen. Dies zeigt ebenfalls an, dass der optimierte Cleave-Prozess einen sekundären Einfluss auf den Vereinzelungs-induzierten Verlust hat.

In einer weiteren Untersuchung wurde die elektrische Leistung von Solarzellen unterschiedlicher Größen, die durch TLS aufgetrennt werden, mit Zellen verglichen, die durch „Laserstrahl-Anritzen und mechanisches Brechen" (LSMC) getrennt wurden. Die LSMC-Technik wird auch in der Industrie verwendet und besteht ebenfalls aus zwei Prozessschritten: (i) Ein Scribe-Prozess wird entlang des gesamten Trennpfades durchgeführt, und (ii) ein mechanischer Brechprozess führt dann zur physikalischen Auftrennung der Substrate. Bei Zellen, die von der emitterfreien Rückseite prozessiert werden, ist der Vorteil von TLS-vereinzelten Zellen deutlich mit der Abnahme der PERC-Zellgrößen zu sehen. Die kleinste untersuchte Zelle hat eine Gesamtzellfläche $A_{tot} = 1{,}15$ cm x 1,15 cm $\approx 1{,}32$ cm² (d.h. etwa 0,5% der vollformatigen Waferfläche). Der Unterschied zwischen den V_{OC}- und *pFF*-Werten der Zelle zu den vereinzelten Zellen wird mit abnehmender Zellgröße größer. Am Beispiel der kleinsten Zelle mit $A_{tot} \approx 1{,}32$ cm² unter niedrigen Beleuchtungsbedingungen, bei denen der Einfluss der Kantenrekombination am stärksten ist, zeigt die durch LSMC aufgetrennte Zelle eine Reduktion im $V_{OC,low}$ von etwa $5\%_{rel}$ (d.h. $\Delta V_{OC,low} = -29$ mV) von der Zelle hin zum aufgetrennten Zustand, während die TLS-getrennte Zelle einen Abfall von $4\%_{rel}$ zeigt (d.h. $\Delta V_{OC,low} = -23$ mV). Zusätzlich wird ein *pFF*-Abfall von ungefähr $6\%_{rel}$ (d.h. $\Delta pFF = -5{,}3\%_{abs}$) im Fall der LSMC-getrennten Zelle bestimmt, während die TLS-getrennte Zelle nur einen Verlust $4\%_{rel}$ zeigt (d.h. $\Delta pFF = -3{,}2\%_{abs}$). Eine plausible Erklärung für den Vorteil von TLS sind die defektärmeren Kanten im Vergleich zu denen von LSMC-getrennten Zellen.

Für die PET werden Al_2O_3-Schichten eingesetzt, da sie eine qualitativ hochwertige Oberflächenpassivierung bieten indem sie eine gute chemische mit einer stark ausgeprägten Feldeffektpassivierung verbinden. Im Fall der thermischen ALD von Al_2O_3-Schichten ist ein PDA-Schritt zur Aktivierung der Passivierungsschicht-Eigenschaften erforderlich, was zu einer Oberflächenpassivierung von hoher Qualität führt. In dieser Arbeit wird eine ausgezeichnete Oberflächen-Passivierungsqualität durch effektive Oberflächenrekombinationsgeschwindigkeiten von $S_{eff} = 4{,}4$ cm/s auf *p*-dotiertem Silicium und $S_{eff} = 5{,}7$ cm/s auf *n*-dotiertem Silicium demonstriert. Diese Ergebnisse zeigen einen Rekord für niedrige S_{eff}-Werte, die durch thermische ALD-Al_2O_3-Oberflächenpassivierung bei den untersuchten Abschei-

dungstemperaturen T_{dep} gleich oder unter 130°C erreicht wurden. Darüber hinaus wird ein Zusammenhang zwischen T_{dep} und den Annealing-Temperaturen T_{ann} beobachtet. Beispielsweise erfordert die niedrigste untersuchte $T_{dep} = 60°C$ die geringste $T_{ann} = 150°C$ für eine wirksame Aktivierung der Oberflächenpassivierungseigenschaften. Um die Stabilität der Oberflächenpassivierung über die Zeit zu untersuchen, werden die Proben im Dunkeln gelagert und nach unterschiedlichen Zeitintervallen von bis zu 120 Tagen erneut gemessen. In den meisten Fällen wird ein sehr stabiles Verhalten in der Passivierungsqualität für die bei $T_{dep} = 95°C$ und $T_{dep} = 130°C$ mit 14 nm bis 16 nm dicken abgeschiedenen Al_2O_3-Schichten ermittelt. Proben die bei $T_{dep} = 60°C$ beschichtet wurden zeigen bereits nach der ersten Stabilitätsmessung (nach einem Tag) eine starke Reduktion der effektiven Lebensdauern, unabhängig von der Al_2O_3-Schichtdicke. In einigen Fällen wird auch nach 120 Tagen ein Wert von $S_{eff} < 10$ cm/s ermittelt, was nach wie vor einer hervorragenden Oberflächenpassivierung für die Herstellung von Solarzellen entspricht. Die Ergebnisse zeigen das Potenzial der entwickelten Oberflächenpassivierung für die Verwendung als PET sowie für andere Technologien, bei denen temperaturempfindliche Substrate prozessiert werden.

Durch Zusammenbringen der Fortschritte im TLS-Prozess und der Oberflächenpassivierung bei niedrigen Temperaturen wurde der Einfluss von PET auf metallisierte Solarzellen untersucht. Die Zellen werden in den folgenden Zuständen charakterisiert: (i) Zellen vor Vereinzelung, (ii) vereinzelte Zellen, (iii) nach Abscheidung und (iv) getempert. Die Arbeit zeigt, dass der TLS-Prozess aufgrund der hohen Kantenrekombination direkt nach Vereinzelung zu einem durchschnittlichen Abfall von $\Delta pFF = -0{,}7\%_{abs}$ führt. Mit Anwendung der PET konnte eine Wiedererlangung von etwa $80\%_{rel}$ vom anfänglichen ΔpFF-Verlust durch die Vereinzelung demonstriert werden. Dies impliziert, dass der Gesamtverlust nach TLS und PET auf nur $\Delta pFF = -0{,}1\%_{abs}$ reduziert werden kann. Die Ergebnisse zeigen die effektive Funktionalität des PET-Ansatzes und die erfolgreiche Integration in die Prozesssequenz zur Herstellung einer kantenpassivierten pSPEER^{PET}-Solarzelle.

In dieser Dissertation wurden bifaziale PERC-basierte Schindelsolarzellen mit Optimierungen der Frontend- und Backend-Prozesse entwickelt. Die Verwendung von industriellen p-dotierten Cz-Si PERC-Precursoren mit beidseitigen Passivierungsschichten unterstützte verschiedene Optimierungsrunden in den Backend-Prozessen. Vollständig intern hergestellte Zellen, beginnend mit p-dotierten „as-cut“ Cz-Si-Wafern, durchlaufen sowohl die Frontend- als auch Backend-Prozesse. Dies bietet die Flexibilität zur Entwicklung angepasster

Prozesse für die erforderliche Anwendung, wie beispielsweise die Entwicklung der Passivierschicht auf der Rückseite, um die Bifazialität β von Zellen weiter zu steigern. Die effizienteste pSPEER$^{\mathrm{PET}}$-Solarzelle, hergestellt aus den industriellen PERC-Precursoren, erreicht $p_{\mathrm{out}} = 23{,}7\ \mathrm{mW/cm^2}$ und $\beta = 66\%$ (unter Berücksichtigung einer zusätzlichen rückseitigen Bestrahlungsstärke von 10 $\mathrm{mW/cm^2}$). Diese Zellen verfügen über eine rückseitige SiN_X-Schicht, die für die monofaziale Anwendung optimiert ist. Bei den intern hergestellten pSPEER$^{\mathrm{PET}}$-Zellen sind die optischen Eigenschaften der Rückseite durch eine dünnere SiN_X-Passivierschicht für die verbesserte rückseitige Lichteinkopplung optimiert. Die effizienteste vollständig intern hergestellte pSPEER$^{\mathrm{PET}}$-Solarzelle erreicht $p_{\mathrm{out}} = 23{,}6\ \mathrm{mW/cm^2}$ und das höchste $\beta = 76\%$. Mit den Entwicklungen im Verlauf der Dissertation konnten somit hocheffiziente bifaziale Schindelsolarzellen hergestellt werden.

Als Ausblick auf Solarzellenlevel kann die Integration selektiver Emitterstrukturen die Leistung der Solarzellen weiter steigern. Dies kann entweder ein selektiv laserdotierter Emitter auf der Vorderseite für verbesserte Kontakteigenschaften der Metallisierung und/oder die Ausbildung von Emitter-Fenstern an den Kanten der Schindelsolarzellen sein, um die Kantenrekombination weiter zu verringern. Neben dem aktuellen PET-Ansatz, in dem die Al_2O_3-Schichtabscheidung überall auf den Zelloberflächen einschließlich der Metallisierung erfolgt, bietet ebenfalls die Untersuchung lokaler Schichtabscheidungs-Technologien, die idealerweise nur die Oberflächen der Kanten beschichten, weiteres Optimierungspotenzial. Dies geht einher mit der Notwendigkeit, den entsprechenden PET-Prozess in die Pilotlinienproduktion zu skalieren, auch für größere Waferformate mit Waferkantenlängen von derzeit bis zu 210 mm. Auf der Ebene der Modulverbindung steht an, die Integration von kantenpassivierten Solarzellen in verschiedenen Verstringungs-Schemata, wie die konventionelle oder Matrix-Verbindung, zu untersuchen.

Die Arbeit demonstriert die erfolgreiche Entwicklung von bifazialen p-dotierten Silicium-Schindelsolarzellen durch die Integration von TLS und PET für die Herstellung von kantenpassivierten pSPEER$^{\mathrm{PET}}$-Solarzellen. Für diese Zellen konnten durch Anwendung der entwickelten PET-Prozesssequenz etwa $80\%_{\mathrm{rel}}$ der trennungsbedingten pFF-Verluste wiedererlangt werden. Diese signifikante Reduzierung der Kantenrekombinationsverluste wurde erstmals in dieser Arbeit gezeigt und ist von grundlegender Bedeutung für die weitere Forschung, Entwicklung und Anwendung des Vereinzelungskonzepts in Photovoltaik-Bauteilen mit höchsten Wirkungsgraden.

10 Appendix

A.1 Current-voltage measurement techniques for shingle solar cells at Fraunhofer ISE CalLab PV Cells[10]

The *Fraunhofer ISE CalLab PV cells* provides current-voltage (IV) measurements for shingle (or strip) solar cells. During this dissertation, a special measurement chuck was constructed for the purpose of *p*SPEER solar cell measurements; see Fig. 10.1. The measurement chuck includes vacuum holes for the suction of the solar cell on the chuck surface. This improves the thermal contact between the cell and the chuck. Moreover, the non-illuminated side (i.e., rear side during the measurement) is electrically contacted by both voltage and current contact strips that are integrated within the chuck. The chuck is non-reflective and enables one-sided measurements without the contribution of the light transmitted through the solar cell and reflected into the cell in the relevant wavelength range. During the measurement, at first the illuminated side is contacted by a Kelvin probe to obtain the shading-free short-circuit current I_{SC}. After obtaining the accurate I_{SC}, a second measurement is conducted by an IV-pin array that creates a uniform potential over the entire busbar. During the second measurement the irradiance is increased to reach the I_{SC} values attained from the first illuminated side measurement. This is done to compensate for the shading losses caused by the IV-pin array. As a result, the measurement results show the IV curves from which the solar cell output parameters can be extracted. The IV measurement follows the international electrotechnical commission (IEC) bifacial photovoltaic device measurement standards IEC TS 60904-1-2 [274]. Reference cells measured at the *CalLab PV cells* are used to calibrate the cell tester IV measurements performed during the time frame of this dissertation.

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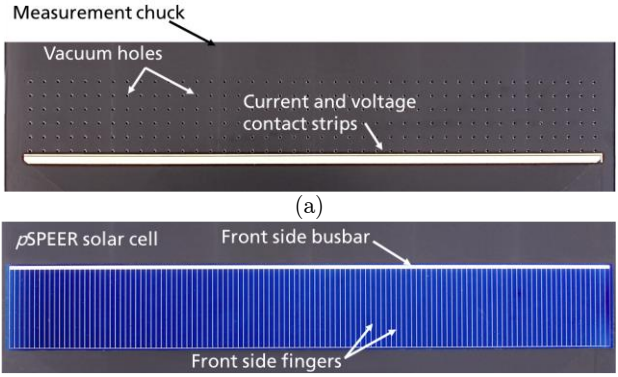

Fig. 10.1 (a) IV measurement chuck used at *Fraunhofer ISE CalLab PV cells* for the measurement of *p*SPEER solar cells. (b) A sample *p*SPEER solar cell placed on the measurement chuck. Chosen *p*SPEER solar cells that are measured on this chuck are then used to calibrate the measurements performed in the industrial cell tester.

A.2 Ellipsometry

In this dissertation, spectroscopic ellipsometry measurements are performed to characterize deposited Al_2O_3 thicknesses d_{Al2O3} as well as refractive indices n_{Al2O3} on floatzone silicon samples. They are determined by polarization phase change of the reflected light in comparison to that of the incident light [275]. The ellipsometer *M-2000F* from the company *J. A. Woollam Co. Inc.* is used for the measurements [276]. The tool records measurements in the wavelength range $250\ \text{nm} \leq \lambda \leq 1000\ \text{nm}$. The Cauchy model [277], used for the interpretation of the Al_2O_3 layer properties, disregards any absorption of these layers in the investigated wavelength ranges by relying on results from Ref. [278].

A.3 Generations of *p*SPEER metallization layouts

The metallization layouts for the bifacial shingle cells, or *p*SPEER solar cells as they are called in the present work, were continuously developed within the progress of the work. Table 10.1. summarizes the main features of the in total seven metallization layout generations from the first generation *Gen1* up to the last generation *Gen7*.

Table 10.1. Summary of the seven *p*SPEER solar cell metallization layout generations *Gen1* to *Gen7*.

		Metallization layout generation						
	Name	*Gen1*	*Gen2*	*Gen3*	*Gen4*	*Gen5*	*Gen6*	*Gen7*
Size	Area A_{tot} (mm x mm)	23 x 148	23 x 148	23 x 148	22 x 148	22 x 156.75	22 x 156.75	26.125 x 156.75
Front side	Busbar width (mm)	1.3* /0.2**	1.3*	0.2**	0.8*	0.8*	0.7***	0.6*
	Interconnection overlap (mm)	1.05	1.05	0.95	0.8	0.8	0.6	0.9
	Finger pitch (mm)	1.48	1.3	1.3	1.3	1.3	1.2	1.3
	Finger width (µm)	35	33	33	35	35	27/33	33
Rear side	Busbar width (mm)	0.6	0.6	0.5	0.5	0.5	0.5	0.7
	Interconnection overlap (mm)	1.05	1.05	0.75	0.75	0.75	0.5	0.55
	Finger pitch (mm)	1.0	1.0	1.0	1.3	1.3	1.2	1.0
	Finger width (µm)	250	250	150	150	175	150	200

*Continuous busbar, **Double busbar, ***Patterned busbar with 8 pads with the corresponding busbar thickness.
Gen6 and *Gen7* are designed for the possibility of a dual printing step on the front side.

Both the front and the rear side are subjected to adaptations with the advancement of layout generations. The advancements in the shingle cells' metallization layouts include the changes in: (i) the shingle cell perimeter size, (ii) busbar width and geometry, (iii) intended minimum interconnection overlap, (iv) finger pitch (i.e., distance between the fingers), (v) nominal finger width, (vi) finger to busbar overlap length and geometry of the overlap, and (vii) the possibility of dual print processes also on the front side.

Concerning the cell size, from *Gen1* up to the *Gen4*, the metallization layout is designed to obtain six equal shingle cells from one host cell (i.e., one wafer). The designs are compatible with wafer sizes with an edge length of 156 mm and larger. *Gen5* and *Gen6* are designed to obtain five shingle cells from each host cell. The designed cell length (i.e., 156.75 mm) allows the fabrication of the shingle cells from wafers with an edge length of 156.75 mm. In *Gen7*, six shingle cells from each host cell are obtained, without having additional wafer material losses. The four shingle cells gotten from the middle of the wafer are rectangular, while the two cells on the very outside have curved "pseudo" edges.

In all the generations, the rear side printing steps of the busbar and fingers take place in a dual print process, such that the busbar is printed first followed by the printing of the fingers. For the metallization of the front side, *Gen1* up to *Gen5* enable a single print process for the printing of the fingers and the busbars in one step. To gain flexibility in the choice of the printing metal pastes for the busbars and fingers (i.e., the use of different pastes for each), dual printing for the front side is introduced in the last two generations *Gen6* and *Gen7*.

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List of Symbols

Symbol	Definition	Usual unit (dimension)
A_{ν}	Absorbance at wave number	1
$A_{\mathrm{BB,front}}$	Area covered by the front side busbar	mm^2
$A_{\mathrm{BB,rear}}$	Area covered by the rear side busbar	mm^2
A_{C}	Covered area	mm^2
A_{des}	Designated area excluding the busbar	mm^2
$A_{\mathrm{des,front}}$	Front side designated area	mm^2
$A_{\mathrm{des,rear}}$	Rear side designated area	mm^2
$A_{\mathrm{f,front}}$	Area covered by the front side fingers	mm^2
$A_{\mathrm{f,rear}}$	Area covered by the rear side fingers	mm^2
$A_{\mathrm{met,front}}$	Total front side metal coverage area of the cell	mm^2
$A_{\mathrm{met,rear}}$	Total rear side metal coverage area of the cell	mm^2
A_{opt}	Optical factor	1
A_{tot}	Total cell area	mm^2
a	Lattice constant	nm
a_{C}	Cleave process air flow	l/min
B_{rad}	Radiative recombination coefficient	$\mathrm{cm}^{-3}\mathrm{s}^{-1}$
C_{n}	Electron Auger coefficient	cm^6/s
C_{p}	Hole Auger coefficient	cm^6/s
D	Minority carrier diffusivity	cm^2/s
D_{it}	Interface defect density states	$\mathrm{eV}^{-1}\mathrm{cm}^{-2}$
d_1	Average sample thickness of group 1	nm
d_2	Average sample thickness of group 2	nm
d_{Al2O3}	Average thickness of Al_2O_3 layer	nm

Symbol	Definition	Usual unit (dimension)
d_{SiO2}	Silicon oxide thickness	nm
$\mathrm{d}T/\mathrm{dx}$	Position-dependent temperature gradient	°C/px
E_C	Conduction band	eV
E_F	Fermi level	eV
E_{ph}	Photon energy	eV
E_G	Band gap	eV
E_{mech}	Young's modulus	GPa
E_t	Energy level of trap states	eV
E_V	Valence band	eV
e_l	Cleave ellipse length	mm
e_w	Cleave ellipse width	mm
FF	Fill factor	%
FF_0	Ideal fill factor	%
f_S	Frequency of scribe process laser	kHz
G	Irradiance	W/m^2
G_{front}	Front side irradiance	W/m^2
G_{rear}	Rear side irradiance	W/m^2
G_{th}	Rate of charge carrier generation at thermal equilibrium	$cm^{-3}s^{-1}$
I_0	Initial incident light intensity	W/m^2
I_L	Incident light intensity	W/m^2
I_{SC}	Short-circuit current	mA
I_{str}	String current	mA
iV_{OC}	Implied open-circuit voltage	mV
j	Current density	mA/cm^2
j_0	Dark saturation current density	fA/cm^2
j_{01}	D1 dark saturation current density	mA/cm^2
j_{02}	D2 dark saturation current density	nA/cm^2
$j_{0,edge}$	Edge-related recombination current per length	nA/cm
$j_{02,edge}$	Edge-related saturation current density	nA/cm
$j_{02,tot,edge}$	Total edge-related saturation current density	nA/cm^2

Symbol	Definition	Usual unit (dimension)
j_{mpp}	Current density at maximum power point	mA/cm^2
j_{ph}	Photogenerated current density	mA/cm^2
j_{SC}	Short-circuit current density	mA/cm^2
$j_{SC,1Sun}$	Short-circuit current density at an irradiance of $G = 1000\ W/m^2$	mA/cm^2
$j_{SC,des}$	Designated area short-circuit current density	mA/cm^2
L_{eff}	Effective diffusion length	nm
l_{Sm}	Measured scribe length values as a result of the TLS scribe process	µm
mpp	Maximum power point	mW
N	Dopant concentration	cm^{-3}
$N°$	Number of atomic layer deposition cycles	1
N_A	Doping concentration in the p-type substrate	cm^{-3}
N_C	Density of states for the conduction band	cm^{-3}
N_t	Trap density	cm^{-3}
N_V	Density of states for the valence band	cm^{-3}
n_0	Thermal equilibrium electron concentration	cm^{-3}
n_1	Electron concentration	cm^{-3}
n_{Al2O3}	Index of refraction for the Al_2O_3 layer	1
n_{edge}	Ideality factor of the second diode in the solar cell equivalent circuit for modeling the edge	1
$n_{i,eff}$	Intrinsic carrier concentration	cm^{-3}
n_{i1}	Ideality factor of the first diode in the solar cell equivalent circuit	1
n_{i2}	Ideality factor of the second diode in the solar cell equivalent circuit	1
n_s	Surface electron concentration	cm^{-3}
P_{ann}	Annealing laser power	W
P_C	Output power of cleave process laser	W
P_{loss}	Resistive power loss	W
P_r	Rated power	W
P_S	Output power of scribe process laser	W

Symbol	Definition	Usual unit (dimension)
P_{sep}	Perimeter of separated edge	mm
p_0	Thermal equilibrium hole concentration	cm^{-3}
p_1	Hole concentration	cm^{-3}
p_s	Surface hole concentration	cm^{-3}
pFF	Pseudo fill factor	%
pFF_a	Pseudo fill factor before processing	%
pFF_b	Pseudo fill factor after processing	%
p_{out}	Output power density	mW/cm^2
Q_f	Fixed charge density	cm^{-2}
R_L	Reflection coefficient	1 or %
R_{rec}	Net recombination rate	$cm^{-3}s^{-1}$
R_{sh}	Emitter sheet resistance	Ω/sq
R_{sur}	Surface recombination rate	$cm^{-3}s^{-1}$
R_T	Total resistance resistance on a string level	Ω
R_{tot}	Total recombination rate	$cm^{-3}s^{-1}$
r_p	Shunt resistance (parallel resistance)	Ωcm^2
r_S	Series resistance	Ωcm^2
S_{eff}	Effective surface recombination velocity	cm/s
$S_{eff,edge}$	Effective surface recombination velocity at the separated edge	cm/s
S_r	Surface recombination velocity	cm/s
T	Temperature	K or °C
T_1	Measured temperature 1	°C
T_2	Measured temperature 2	°C
T_{ann}	Annealing temperature	°C
$T_{ann,crit}$	Critical annealing temperatures	°C
T_{dep}	Deposition temperature	°C
T_{STC}	Temperature at standard test conditions	°C
t_{ann}	Annealing duration (or time)	min
$t_{ann,crit}$	Critical annealing duration	min
t_S	Storage time after surface passivation	days

Symbol	Definition	Usual unit (dimension)
V	Voltage	mV
V_{mpp}	Voltage at maximum power point	mV
V_{OC}	Open-circuit voltage	mV
$V_{\mathrm{OC,low}}$	Open-circuit voltage at low illumination	mV
V_{OCa}	Open-circuit voltage after processing	mV
V_{OCb}	Open-circuit voltage before processing	mV
V_{Th}	Thermal voltage	mV
v_{C}	Cleave process velocity	mm/s
v_{OC}	Normalized voltage	1
v_{S}	Scribe process velocity	mm/s
v_{th}	Average thermal velocity of carriers	cm/s
W	Wafer thickness	µm
$w_{\mathrm{BB,FS}}$	Front side busbars width	µm
$w_{\mathrm{BB,RS}}$	Rear side busbars width	µm
$w_{\mathrm{f,FS}}$	Front side silver finger width	µm
$w_{\mathrm{f,RS}}$	Rear side aluminium finger width	µm
z	Material length	µm
α	Absorption coefficient	cm^{-1}
β	Bifaciality factor	1 or %
δ_{p}	Penetration depth	µm
$\varepsilon_{\mathrm{mech}}$	Strain (relative deformation)	1
η	Energy conversion efficiency	%
η_{des}	Designated area energy conversion efficiency	%
η_{FS}	Front side energy conversion efficiency	%
η_{RS}	Rear side energy conversion efficiency	%
λ	Wavelength	nm
μ_{n}	Electron mobility	$\mathrm{cm}^2/(\mathrm{V.s})$
μ_{p}	Hole mobility	$\mathrm{cm}^2/(\mathrm{V.s})$
ρ_{B}	Base resistivity	Ωcm
$\rho_{\mathrm{C,FS}}$	Front contact resistivity	$\mathrm{m\Omega cm}^2$
$\rho_{\mathrm{C,RS}}$	Rear contact resistivity	$\mathrm{m\Omega cm}^2$

Symbol	Definition	Usual unit (dimension)
$\rho_{L,FS}$	Front lateral resistivity	$m\Omega cm^2$
$\rho_{L,RS}$	Rear lateral resistivity	$m\Omega cm^2$
σ_{mech}	Stress (force per unit area)	MPa
τ	Recombination lifetime	µs
$\tau_{Au,h}$	Auger lifetime under high injection conditions	µs
$\tau_{Au,l}$	Auger lifetime under low injection conditions	µs
τ_{bulk}	Bulk recombination lifetime	µs
τ_{eff}	Effective lifetime	µs
τ_{n0}	Time constant for electron's capture	µs
τ_{p0}	Time constant for hole's capture	µs
τ_{rad}	Radiative recombination lifetime	µs
τ_{SRH}	Shockley-Read-Hall recombination lifetime	µs
$\tau_{Surface}$	Surface recombination lifetime	µs
Φ	Photon flux	$cm^{-2}s^{-1}$
$\varphi(x)$	Photoluminescence signal counts	1
$\varphi_a(x)$	Photoluminescence signal counts after the cleave process	1
$\varphi_b(x)$	Photoluminescence signal counts before the cleave process	1
$\varphi_n(x)$	Normalized PL signal counts after UFR	1
φ_{PL}	Photoluminescence intensity	1
$\Delta\sigma$	Excess photoconductance	S/m
Δn	Excess carrier concentration of electrons	cm^{-3}
Δp	Excess carrier concentration of holes	cm^{-3}
σ_n	Electron capture cross-section	cm^2
σ_p	Hole capture cross-section	cm^2
ν	Wave number	cm^{-1}

List of Abbreviations

Abbreviation	Meaning
||	Surface species during the deposition reactions
4pp	Four-point-probe
Ag	Silver
Al	Aluminium
Al_2O_3	Aluminum oxide
Al-BSF	Aluminum back surface field
ALD	Atomic layer deposition
AM1.5G	Air mass 1.5 global spectrum
ARC	Antireflection coatings
a-Si:H	Hydrogenated amorphous silicon
biPERC	Bifacial passivated emitter and rear cell
B-O	Boron-oxygen
CCD	Charged coupled device
CV	Capacitance-voltage
Cz-Si	Czochralski-grown silicon
Cz-Si:B	Boron-doped Czochralski-grown silicon
Cz-Si:Ga	Gallium-doped Czochralski-grown silicon
D1	First diode
D2	Second diode
$\mathrm{d}T/\mathrm{dx}$	Position-dependent temperature gradient
ECA	Electrically conductive adhesives
EL	Electroluminescence
E_C	Conduction band
E_V	Valence band

Abbreviation	Meaning
eeh	Electron-electron-hole interaction in Auger recombination
ehh	Electron-hole-hole interaction in Auger recombination
FS	Front side
FT-IR	Fourier transformed-infrared spectroscopy
Fz-Si	Floatzone-grown silicon
Ga_2O_3	Gallium oxide
Gen1 - *7*	Metallization layout generations
GPC	Growth per cycle
H_2/N_2	Forming gas
$H_2O_{(g)}$	Water vapor
HF	Hydrofluoric acid
HfO_2	Hafnium dioxide
HNO_3	Nitric acid
IBC	Interdigitated back contact
IEC	International electrotechnical commission
ISE	Institute for Solar Energy Systems
ITRPV	International Technology Roadmap for Photovoltaics
IV	Current-voltage
k	Separated perimeter-to-area ratio
L-BSF	Local back surface field
LCO	Laser contact opening
LDC	Laser direct cleaving
LIC	Laser-induced cutting
LiD	Light induced degradation
LSMC	Laser scribing and mechanical cleaving
N_2	Nitrogen gas
Nb_2O_5	Niobium pentoxide
P/A	Perimeter-to-area ratio
PDA	Post-deposition annealing
PECVD	Plasma enhanced chemical vapor deposition

Abbreviation	Meaning
PERC	Passivated emitter and rear cell
PERL	Passivated emitter and rear locally diffused
PERT	Passivated emitter and rear totally diffused
PET	Passivated edge technology
PL	Photoluminescence
PMA	Post-metallization annealing
$POCl_3$	Phosphorous oxychloride
PSG	Phosphosilicate glass
PV	Photovoltaic
PV–TEC	Photovoltaic Technology Evaluation Center
*p*SPEER	*p*-type silicon shingled passivated edge, emitter, and rear
$p\text{SPEER}^{\text{PET}}$	*p*-type shingled passivated edge, emitter, and rear with passivated edge technology
QSSPC	Quasi-steady state photoconductance
ROIs	Regions of interest
RS	Rear side
SCR	Space charge region
SEM	Scanning electron microscope
SHJ	Silicon heterojunction
SiN_X	Silicon nitride
SiO_2	Silicon dioxide
SRH	Shockley-Read-Hall
STC	Standard test conditions
Ta_2O_5	Tantalum pentoxide
TCO	Transparent conductive oxide
TLM	Transfer length method
TLS	Thermal laser separation
TMA	Trimethylaluminum $Al(CH_3)_2$
TOPCon	Tunnel oxide passivated contact
UFR	Ultra fast regeneration
VCSEL	Vertical cavity surface-emitting laser

Physical Constants

Values extracted from Ref. [279] and rounded.

Symbol	Description	Value
c	Speed of light in vacuum	299 792 458 m/s
h	Planck constant	6.626×10^{-34} J.s
k_B	Boltzmann constant	1.381×10^{-23} J/K
q	Elementary charge	1.602×10^{-19} C

List of Publications

Journal publications

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This dissertation presents the development and characterization of the bifacial *p*-type silicon shingle solar cells with edge passivation. As a derivative of the bifacial passivated emitter and rear cell (biPERC), the developed device adopts the biPERC fabrication process flow with an additional laser-assisted separation.

The work introduces the passivated edge technology (PET) to regain losses caused by charge carrier recombination at the newly-formed edges after separation. PET encompasses a low temperature ($T \leq 130°C$) aluminum oxide (Al_2O_3) deposition by atomic layer deposition and an additional annealing step. The impact of the thermal laser separation on the solar cell's electrical performance is studied. Moreover, very low effective surface recombination velocity values S_{eff} of around 5 cm/s are attained with Al_2O_3 layers on floatzone silicon substrates at studied low process temperatures. PET leads to around $80\%_{rel}$ pseudo-fill factor regain of losses from the as-separated shingle cell state. The new device is called the *p*-type shingled, passivated, edge, emitter, and rear (*p*SPEER^{PET}) solar cell and attains a peak output power density of $p_{out} = 23.7$ mW/cm^2.

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