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A Review of Platinum Diffusion in Silicon and Its Application for Lifetime Engineering in Power Devices

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In silicon power semiconductors, platinum is used to improve the switching characteristics of the devices by adjusting the lifetime of the minority charge carriers. Platinum diffusion in silicon has been a research topic for many scientists over the past decades. Herein, the current state of knowledge is presented together with the concepts developed for its use in silicon power devices. The relevant processes include diffusion from a platinum silicide, postimplantation annealing, and phosphorus-diffusion gettering. The evaluation of corresponding experiments and the calibration of the models have not only resulted in more narrow limits for the equilibrium concentrations of vacancies and self-interstitials in silicon and the transport capacity of interstitial platinum, but also in improved devices.

1. Introduction

In applications dealing with high power and high-frequency switching, silicon power devices with certain switching characteristics are needed to minimize losses and to meet high-efficiency requirements. One way of influencing the switching characteristics is to add atoms with energy levels in the forbidden bandgap of silicon. These atoms provide pathways so that the electrons and holes can recombine faster, thus reducing their lifetime. One element with such properties in silicon is platinum.

The platinum atoms can be introduced by two different methods: diffusion from a Pt-silicide layer and platinum implantation followed by annealing. The latter has the implantation dose as an additional design parameter. First, there is a lot to learn from experiments in which the platinum was introduced from a Pt-silicide layer. Such knowledge is very useful when it comes to the calibration of the model parameters for the basic mechanisms because it is less complex compared to postimplantation annealing, which inevitably is associated with implantation damage as well as with the formation of platinum agglomerates at high implantation doses.

Another process of interest is phosphorous-diffusion gettering (PDG) of platinum in silicon. It can be used to further tailor the platinum profiles and the charge-carrier lifetime adjustment, and thereby to further optimize the performance of silicon power devices in terms of soft switching.[1,2]

In this article, we review how the platinum is introduced into silicon power devices, how the relevant processes are modeled, and how the calibration of these models has made contributions to basic research, including an establishment of more narrow limits for the equilibrium concentrations of vacancies and self-interstitials in silicon, as well as an improved parameterization of the transport capacity of interstitial platinum.

Finally, we elaborate on the usage of the Pt models in a technology computer-aided design (TCAD) simulation chain to tailor, e.g., the performance of a power diode to the application's requirements. In a first step, the fabrication process is simulated by applying the Pt diffusion model, resulting in the spatial distribution of charge-carrier traps. In a second step, the trap contribution to the on-state charge-carrier distribution as well as the device behavior during transient switching events can be evaluated.

2. The Role of Platinum in Power Devices

For the control of inductive loads such as electric motors, so-called voltage-link converters are commonly used in modern drives. By means of suitable modulation methods, these have the task of supplying a sinusoidal load current with variable frequency and level at the output, which is required for direct operation of a motor in a variable-speed drive. The concept is characterized by high efficiency and has a wide range of applications today, from the consumer sector (washing machines, air conditioners) to drive technology for automobiles, high-speed trains, and industrial applications to power generation (wind turbines, solar plants) and power distribution (high voltage direct current [HVDC] transmission). The key components here are

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fast-switching metal oxide semiconductor (MOS)-controlled bipolar power transistors, referred to in technical terminology as insulated gate bipolar transistors (IGBTs). These components are designed for a blocking capability of at least 400 V up to over 6500 V, depending on the application. By alternately switching on and off in a bridge circuit, the desired frequency is generated at the output, e.g., by means of pulse-width modulation. An example of such a power module is shown in **Figure 1**a.

To keep the switching losses as low as possible, a high switching speed is aimed for. However, due to the inductive load, a high induction voltage is generated during sudden switching-off, which could even destroy the active switch. Therefore, a free-wheeling diode must be provided in the parallel branch to take over the current flow driven by the inductance in the off state. When the transistor is switched on again, any residual current still flowing through the diode, the so-called reverse-recovery current, is commutated to the IGBT and contributes significantly to its switch-on losses. To evaluate and optimize the diode switching behavior, one single branch of the module is used as a test circuit as shown in Figure 1b. The reverse-recovery current is determined from a double-pulse measurement, involving the top-most diode (D_1) and the bottom-most IGBT (T_2) only. First, T_2 is turned on, and a current flows through the inductive load and T_2. Next, T_2 is turned off, and the current driven by the load now flows through D_1. Finally, T_2 is turned on again, the load current flows through the IGBT, and the reverse-recovery current transient from the diode (small blue arrow), marked with I_{rr} in the figure, goes on top of the load current.

The switching-on speed of the transistor has an influence on the switching dynamics of the diode because it determines the steepness of the current decrease in the diode, the dI/dt (I = current, t = time). In addition to the switching speed and the on-current level of the diode, the storage charge is an influencing variable for the switching losses as well. Its magnitude is determined by the recombination speed of the electron–hole plasma, which carries the current in the forward direction, during the reverse-recovery process in the diode. The characteristic time constant for this is the minority carrier lifetime. Therefore, to reduce switching losses, it is necessary to reduce the minority carrier lifetime. For more details, the interested reader is referred to relevant textbooks on power electronics, for example, the book by Lutz et al.[3]

2.1. Reduced Carrier Lifetime by the Introduction of Traps

The classical technique for reducing the minority carrier lifetime is the diffusion of noble metals such as gold or platinum into the drift zone of the semiconductor device. These impurities result in the introduction of energy levels in the forbidden bandgap, around midgap, which act as traps for charge carriers. The traps effectively reduce the lifetime for electrons and holes through trap-assisted recombination (known as Shockley–Read–Hall recombination). Alternatively, irradiation with high-energy particles such as electrons, hydrogen, or helium nuclei can be used for this purpose.[4–8] However, these can lead to undesirable side effects such as damage of the gate oxide, especially in MOS devices with an integrated reverse diode like a reverse conducting IGBT (RC-IGBT).[9]

Besides the desired reduction in switching losses, the incorporation of recombination centers leads to an increase in the voltage drop under forward load (forward power loss) and to an increase in the leakage current in the reverse state of the diode (reverse power loss). For the latter, the exact location of the recombination center in the bandgap is crucial. Baliga[10] showed that, in comparison with electron irradiation or gold diffusion, platinum recombination centers combine the most favorable properties. First of all, both gold and electron irradiation defects result in higher leakage currents compared to platinum. In n-type silicon, the acceptor level of gold is located in the middle of the bandgap, whereas the acceptor level of platinum is more shallow.[10] Second, the switching characteristics are better for gold- and platinum-diffused devices compared with the case of

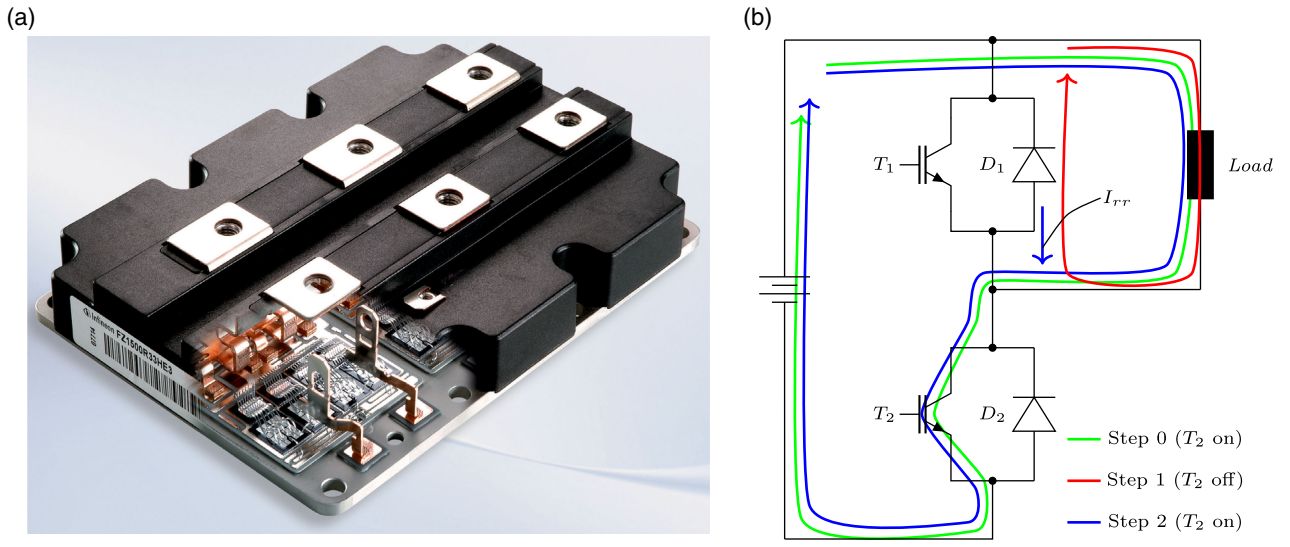

Figure 1. a) An image of a partially opened 3.3 kV 1500 A single switch power module, providing a view on the IGBTs and power diodes inside. b) Test circuit (single branch) used to measure the reverse-recovery current and a principle sketch of a double-pulse measurement in three steps. The currents of the three steps are indicated by the arrows. The small blue arrow indicates the reverse-recovery current (I_{rr}) in the last step.

electron irradiation. Platinum is therefore often preferred, especially when higher operating temperatures (such as 150–175 °C) are demanded. The requirements set on the packaging technology to prevent thermal drift of the overall system such as an IGBT module, namely, low thermal resistance and effective cooling, are thus significantly relieved.

Nevertheless, the platinum recombination centers are not unquestionably superior. The temperature dependence of the forward voltage drop, which is important to connect several chips in parallel, e.g., in an IGBT module,[11] can, however, become problematic when the Pt doping level becomes too high.[5] The reason for this lies in the different cold and hot characteristic curves. Without lifetime adjustment, the voltage drop at high temperature (150 °C) is lower than at room temperature. Thus, the *I*–*V* curves may intersect at a certain current level which should be below the nominal current.[11,12] This has the consequence that the forward voltage drop increases under surge load (typically at 2–3 times the nominal current) and the associated heating, which counteracts a further increase and leads to a distribution of the load current to the (colder) parallel-connected components.[12] In this case, a positive temperature coefficient (TC) prevails. If, on the other hand, the point of intersection is very high or, in extreme cases, both curves do not intersect at all, the situation is characterized by a negative TC and the attenuation acts very late or not at all.[11,12]

With increasing Pt concentration, an increasingly negative TC is observed.[5] So, the amount of lifetime adjustment with Pt is limited by this effect. In very fast switching devices, a combination of different methods of lifetime control may thus be applied, i.e., irradiation techniques in addition to Pt diffusion.[4,13]

As an illustrative example of the effect of lifetime adjustment with platinum, **Figure 2** shows measurements of the reverse-recovery transient current of a platinum-diffused diode and a diode without platinum.[14] The peak current is considerably smaller for the platinum-diffused diode. The lifetime-adjusted diode in the example had a symmetric U-shaped platinum distribution. Practically symmetrical "bathtub-shaped" or "U-shaped" distributions of the recombination centers are typical for noble metal diffusion with gold or platinum for minority carrier lifetime reduction according to the state-of-the-art. This is a consequence of the diffusion behavior of such elements, as described for platinum in Section 3.2.

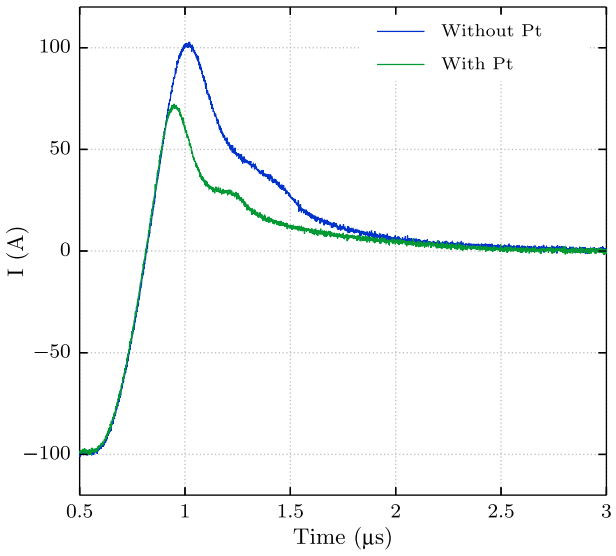

Figure 2. Measurements of the reverse-recovery transient current (current scale inverted) of a diode (with and without platinum), during IGBT turn-on in a half-bridge configuration for a DC-link voltage of 600 V at a temperature of 175 °C. Adapted with permission.[14] Copyright 2018, IEEE.

When the diode is flooded in forward direction, the concentrations of electrons and holes are far above the level of the base doping and the characteristic quantity for the calculation of the forward voltage drop V_f is the high-injection lifetime τ_{HL}, also called ambipolar lifetime, which depends via

$$\tau_{HL} = \frac{\sigma_n \nu_p + \sigma_p \nu_p}{\sigma_n \sigma_p \nu_n \nu_p} \frac{1}{N_{Pt}} \tag{1}$$

inversely on the concentration of electrically active platinum N_{Pt}. σ_n and σ_p denote the capture cross sections for electrons and holes, and ν_n and ν_p the respective thermal velocities. According to Coffa et al.,[2] the first fraction takes a value of $1.33 \times 10^7\ \mathrm{s\,cm^{-3}}$. How V_f is calculated is described by, for example, Lutz et al.[3]

Lifetimes of 100 ns to a few 100 ns are expected for components with platinum (symmetrical U-shaped profiles), whereas components without platinum have lifetimes up to some 100 μs, depending of course on the wafers used.

2.2. Current Snap-Off and Soft Switching

Another desired diode property, relevant particularly in the last phase of the fast switching-off process, is that the reverse-recovery current does not suddenly snap off under fast switching conditions. This would result in extremely high dI/dt values, which lead to oscillations and voltage overshoots due to the inductances in the circuit, which, in turn, could destroy the diode.

Current snap-off is a particular problem for diodes with so-called punch-through dimensioning. The punch-through concept aims to reduce switching losses by reducing the width of the drift zone. Thus, the electric field reaches the cathode side and is then rapidly dissipated by the backside n^+-emitter and mostly by a weaker n-doped field stop zone adjacent to it.[15] In contrast, in non-punch-through devices, the electric field is dissipated exclusively by the base doping. This results here in a neutral zone in front of the cathode, where charge carriers are stored and can thus supply the reverse-recovery current required for soft switching.

Besides the switching speed, the magnitude of the on-state current also plays a decisive role in the reverse-recovery process of the diode. The lower the on-state current, the lower the electron–hole plasma concentration and the less storage charge is then available for the reverse-recovery current.

The lack of stored charge can also be an issue after the lifetime adjustment. Although a symmetrical distribution of the platinum atoms leads to a reduction of the switching losses, it can also contribute to a hard switching behavior characterized by an early snap-off of the reverse-recovery current, especially for punch-through devices.

In order to avoid reverse-current snap-off, even with punch-through dimensioning, additional measures must be taken to ensure a sufficiently high storage charge reservoir on the cathode side, which can feed the reverse-recovery current until the required DC-link voltage is reached. To achieve this goal, the charge-carrier distribution must already be set asymmetrically in the steady-state forward operation mode. This means that the plasma concentration on the cathode side must be greater than that on the opposite anode side.

2.3. PDG for Axial Inhomogeneous Lifetime Profiling

An asymmetrical plasma distribution can be realized either by an introduction of a local lifetime sink in axial direction in the vicinity of the anode or by a zone with increased lifetime adjacent to the cathode. This is often combined with a homogeneous lifetime adjustment in the bulk. The homogeneous part can be produced, e.g., by Pt diffusion or electron irradiation, while a local sink is realized exclusively by irradiation techniques. Here, recombination-effective impurities are created at a certain depth by bombarding the Si crystal with, for example, hydrogen or helium nuclei.[4–6,8]

An alternative approach is to form a zone with increased lifetime at the cathode side by PDG. PDG is a well-established technique used to remove metal impurities from silicon in device manufacturing processes. It is a topic to which many scientists have contributed over the last half century. For a summary of the mechanisms involved, the interested reader is referred, e.g., to the review article of Schröter et al.[16].

For silicon power diodes, platinum is first introduced by diffusion from a Pt silicide or by implantation and drive-in annealing. As explained below, such processes lead to symmetrical, U-shaped distributions of the Pt atoms in the silicon. For the PDG step, phosphorus is introduced at high concentrations on one side either by depositing a phosphorus glass or by ion implantation. During a subsequent anneal, the electrically active platinum atoms are partly removed.[12,17] This results in an asymmetric platinum distribution and thus in an asymmetric lifetime profile.[12,17]

Two examples of how the platinum profiles can look after PDG compared to a symmetrical U-shaped profile are shown in **Figure 3**a together with one set of measurements of the electrically active platinum concentration by deep-level transient spectroscopy (DLTS) from Schmidt and Bauer[17] obtained after platinum diffusion from a Pt-silicide layer (775 °C for 2 h) followed by PDG: P-implantation (1×10^{15} cm^{-2}, 45 keV) followed by annealing (700 °C for 1 h). The green dashed curve is the result of "less" PDG in comparison to the red dotted curve, i.e., the green curve corresponds to a PDG anneal carried out for a shorter time or at a lower temperature. The process of PDG will be described further in Section 3.4.

An example of the influence the asymmetrical Pt profiles have on the reverse-recovery current compared to a symmetrical profile is shown in Figure 3b. The platinum was first introduced by diffusion from a Pt-silicide layer. The asymmetrical platinum profiles were obtained after a complete removal of the Pt-silicide layer and an additional phosphorus implantation from the backside (5×10^{15} cm^{-2}, 45 keV), followed by annealing at 600 °C or 700 °C for 1 h. After PDG at 600 °C, the diodes are already significantly softer than the symmetrical reference (U-shape). After PDG at 700 °C, the tail phase is extremely long (i.e., extremely soft) which, in turn, corresponds to a massive turn-off power loss. For the application, a trade-off is required between minimizing switching losses and maintaining the desired softness.

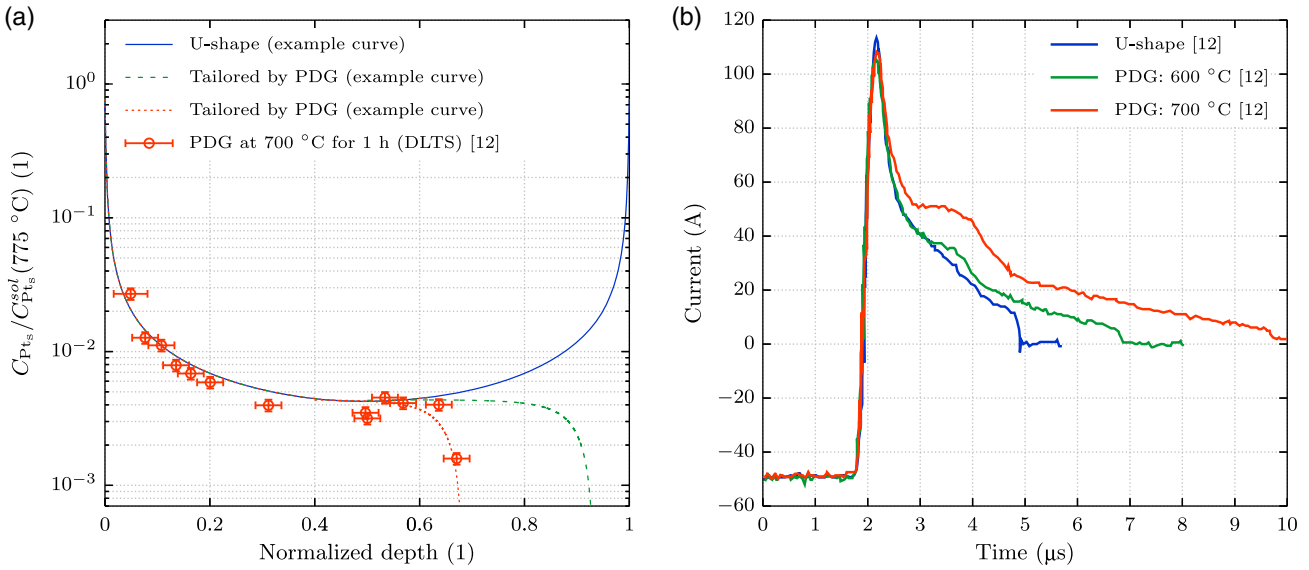

Figure 3. a) Illustrative example curves of one symmetrical and two asymmetrical profiles of electrically active platinum together with one measured profile after PDG (platinum diffusion from a Pt-silicide layer (775 °C for 2 h) followed by PDG (700 °C for 1 h), 670 µm wafer thickness).[17] The Pt_s concentration is normalized by $C^{sol}_{Pt_s}$ at 775 °C from Johnsson.[18] The asymmetrical profiles correspond to profiles obtained after PDG. b) Measurements of the reverse-recovery current (current scale inverted) of diodes with symmetrical versus asymmetrical Pt profiles (tailored by PDG) for a DC-link voltage of 3600 V at a temperature of 125 °C.[17]

3. Processes and Process Modeling

A good understanding of the processes used to introduce and tailor platinum profiles in silicon is essential for device development. The models are a fundamental part of the TCAD simulation chain, used to predict the electrical behavior of the final devices. The existing models of platinum diffusion in silicon have been developed over the past decades. Over one hundred experiments have been reported in the literature with variations in annealing time, annealing temperature, wafer thickness, preprocessing, and substrate material.[18–34] All studies have, to some extent, contributed to a better understanding of the processes and the underlying mechanisms have, generally speaking, been identified. In the last of these studies, all these experiments were taken into consideration by Johnsson.[18] The resulting models for the three most important processes are presented in this section: platinum diffusion from a Pt-silicide layer, post-implantation annealing of platinum, and PDG of platinum.

3.1. Platinum Diffusion from a Pt-Silicide Layer

Most of the models describing platinum diffusion from a Pt-silicide layer found in the literature involve four species:[21,25,30] platinum on substitutional sites (Pt_s), platinum on interstitial sites (Pt_i), silicon self-interstitials (I), and vacancies (V). The substitutional platinum is assumed to be electrically active, and it is the concentration of electrically active platinum that has been measured in most studies, mainly by DLTS.

The substitutional platinum is assumed to be immobile. Its concentration changes as interstitial platinum atoms go in and out of substitutional lattice sites by reacting with self-interstitials and vacancies. The Frank–Turnbull mechanism postulates that interstitial platinum atoms become substitutional by occupying vacant lattice sites.[35] It can be described by the quasichemical reaction

$$\mathrm{Pt_i} + \mathrm{V} \underset{k_{\mathrm{FT}\leftarrow}}{\overset{k_{\mathrm{FT}\rightarrow}}{\rightleftharpoons}} \mathrm{Pt_s} \tag{2}$$

Complementary to this, the kick-out mechanism postulates that interstitial platinum atoms go into substitutional sites by displacing silicon lattice atoms to interstitial positions.[36] It can be described by the quasichemical reaction

$$\mathrm{Pt_i} \underset{k_{\mathrm{KO}\leftarrow}}{\overset{k_{\mathrm{KO}\rightarrow}}{\rightleftharpoons}} \mathrm{Pt_s} + \mathrm{I} \tag{3}$$

In addition to these reactions, bulk generation and recombination of vacancies and self-interstitials need to be included. It can be described by the quasichemical reaction

$$\mathrm{I} + \mathrm{V} \underset{k_{\mathrm{IV}\leftarrow}}{\overset{k_{\mathrm{IV}\rightarrow}}{\rightleftharpoons}} \varnothing \tag{4}$$

where the "∅" stands for an undisturbed lattice site. The reaction rate constants in the forward direction, denoted by $k_{\mathrm{FT}\rightarrow}$, $k_{\mathrm{KO}\rightarrow}$, and $k_{\mathrm{IV}\rightarrow}$, can be derived from Waite's theory,[37] assuming diffusion-limited reactions. For the Frank–Turnbull mechanism, as an example, it can be expressed as

$$k_{\mathrm{FT}\rightarrow} = 4\pi a_{\mathrm{FT}} (D_{\mathrm{Pt_i}} + D_{\mathrm{V}}) \tag{5}$$

where a_{FT} is the reaction radius. $D_{\mathrm{Pt_i}}$ and D_{V} denote the diffusion coefficients of Pt_i and V, respectively. The reaction is assumed to take place immediately when the two defects approach each other to a distance of a_{FT}. The reaction radii are expected to be approximately equal to the distance between two silicon atoms and at least in our work we saw no necessity to consider significant additional reaction barriers. The reaction rate constant in the opposite direction, $k_{\mathrm{FT}\leftarrow}$, can be expressed via the concentrations in steady state

$$k_{\mathrm{FT}\leftarrow} = k_{\mathrm{FT}\rightarrow} \frac{C^{\mathrm{sol}}_{\mathrm{Pt_i}} C^{\mathrm{eq}}_{\mathrm{V}}}{C^{\mathrm{sol}}_{\mathrm{Pt_s}}} \tag{6}$$

where $C^{\mathrm{sol}}_{\mathrm{Pt_i}}$ and $C^{\mathrm{sol}}_{\mathrm{Pt_s}}$ are the respective solubility concentrations of Pt_i and Pt_s, and $C^{\mathrm{eq}}_{\mathrm{V}}$ is the equilibrium concentration of vacancies. The reaction rates are expressed analogously for the other reactions.

Quast[28] found it necessary to extend the model defined by Equation (2), (3), and (4) by also considering the interaction between platinum and immobile vacancy–impurity complexes present from crystal growth or prior processing steps. He introduced VO_2 complexes to model diffusion in CZ-grown silicon.[28] To model diffusion in FZ-grown silicon he suggested two types of vacancy–nitrogen complexes, of which only one interacts with platinum.[28] Johnsson[18] also found it necessary to include the interaction with such defects in order to explain differences due to substrate material and preprocessing.

To describe the interaction between interstitial platinum and the immobile vacancy–impurity complexes mentioned above in a generic way, Johnsson[18] introduced for the latter the species VX. The respective quasichemical reaction is given by

$$\mathrm{Pt_i} + \mathrm{VX} \overset{k_{\mathrm{VX}}}{\rightarrow} \mathrm{Pt_s} + \mathrm{X} \tag{7}$$

where k_{VX} denotes the reaction rate for Pt_i to become substitutional by reacting with a vacancy–impurity complex. It is expressed according to Waite's theory,[37] assuming diffusion-limited reactions, in analogy to Equation (5). However, it might be necessary to include a reaction barrier, depending on the type of vacancy–impurity complex.[18,28] The reaction in the backward direction is assumed to be unlikely, and it is assumed that the impurity product X does not react with any other species.

Using the methodology of binary reactions, described, for example, by Pichler,[38] the reactions in Equation (2), (3), (4), and (7) result in a system of coupled continuity equations for the species involved which contain diffusion terms for the mobile species.

The boundary conditions complete the model. Badr[32] suggested to model the concentration of vacancies and self-interstitials at the surfaces with first-order boundary conditions for annealing in inert ambient following, e.g., the work of Hu.[39] For annealing, e.g., in oxidizing ambients and to account for the effects of high phosphorus concentrations during PDG, the boundary conditions for self-interstitials and vacancies are adjusted accordingly. The Pt-silicide layer is modeled by a Dirichlet boundary condition for interstitial platinum with the

solubility concentration, assuming an infinite source of platinum. A Neumann boundary condition is used for interstitial platinum at the surface not covered by a Pt-silicide layer, assuming that the platinum cannot leave the wafer (because of the low vapor pressure of platinum). Immobile species are assumed to not interact with the surface.

3.2. The U-Shaped Profile

In contrast to typical impurity diffusion profiles, measured profiles of electrically active platinum are usually U-shaped (also in the case of one-sided diffusion) and this deserves an explanation. An example of the evolution of the substitutional platinum concentration across the wafer depth during annealing from simulations is shown in **Figure 4**. The example is taken from Johnsson[18] and shows diffusion from a Pt-silicide layer (at depth 0) into a 725 μm-thick wafer during annealing at 800 °C. A homogeneous concentration of vacancies of 1×10^{12} cm^{-3} was used as initial conditions in the simulations, significantly higher than the initial concentration of self-interstitials.[18]

In the initial phase of the annealing process, interstitial platinum atoms diffuse very rapidly from the silicide into the wafer and decorate predominantly the preexisting vacancies in the bulk. As time progresses, the concentration profile of substitutional platinum extends deeper into the wafer; see the respective profiles after times t_1 through t_3 in Figure 4. At time t_3, the interstitial platinum atoms have reached the other surface and almost all of the initially present vacancies are occupied by platinum. However, the concentration of substitutional platinum is increasing more rapidly at the surfaces than in the bulk. This is because the surface acts as a source of new vacancies for the Frank–Turnbull mechanism and as a sink for the self-interstitials

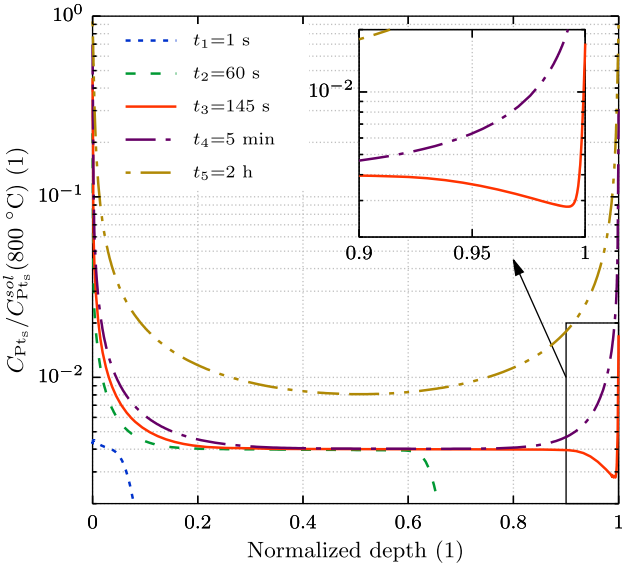

Figure 4. An example of how the typical U-shaped profile of the substitutional platinum concentration is obtained from one-sided diffusion during annealing at 800 °C (simulations). The Pt_s concentration is normalized by $C^{sol}_{Pt_s}$ at 800 °C from Johnsson. Adapted with permission.[18] Copyright 2019, A. Johnsson.

generated by the kick-out mechanism, so that neither mechanism is limited by reactant depletion. The rapid increase of the substitutional platinum concentration is first seen in the profile at time t_2 at the surface with the Pt-silicide layer, i.e., at the origin of the depth scale. As soon as the interstitial platinum atoms reach the other surface at time t_3, one can observe that the same effect sets in there. From then on, the U-shaped profile begins to form. How fast the U-shape is established depends on the wafer thickness, the annealing temperature, and also on the initial concentrations of intrinsic point defects. The U-shaped profile would, of course, be established faster with platinum sources on both surfaces, and the profile would then be completely symmetric. The bulk concentration will eventually increase with the annealing time; compare the profiles after times t_4 and t_5 in Figure 4. It requires out-diffusion of self-interstitials from the bulk to the surfaces which allows the kick-out mechanism to proceed, or in-diffusion of vacancies from the surfaces to the bulk, which allows the Frank–Turnbull mechanism to proceed.

To summarize, the U-shape is a result of the fast-diffusing interstitial platinum, the Frank–Turnbull mechanism and the kick-out mechanism, and the transport of intrinsic point defects. The same typical U-shaped profiles are also found when the platinum is introduced via ion implantation followed by annealing, based on the same principles.

3.3. Platinum Implantation Followed by Annealing

To model postimplantation annealing of platinum in silicon, the model for platinum diffusion from a Pt-silicide layer is extended. The source of platinum is in this case the implanted profile: A finite source, contained in a region close to the implanted surface. The implanted profiles can be obtained from Monte Carlo simulations. Giles' +1 model[40] was used successfully to describe implantation damage. In the +1 model, it is assumed that the point defects generated during ion implantation recombine quickly, and that one self-interstitial (+1) per implanted ion on a substitutional site remain. However, considering the high mass of platinum atoms, even more than one self-interstitial can be expected to form for each substitutional platinum atom.[41] For all implantation conditions investigated, the damage can be assumed to remain below the amorphization threshold.[18] Clustering and precipitation of self-interstitials in the implanted region can be accounted for by, e.g., the moment-based model of Zechner et al.[42]

In addition to the implantation damage and self-interstitial clustering, another phenomenon needs to be considered: incomplete activation of platinum. This means that for certain annealing times and temperatures, only a fraction of the implanted platinum atoms are found to be electrically active after annealing. The phenomenon was first found experimentally by Badr,[31] and confirmed by Hauf et al.[34] and Johnsson.[18] The "missing" platinum is likely to be contained in complexes like clusters or precipitates. Badr et al.[31] suggested an empirical dynamic cluster model. Badr's model includes one cluster type, formed from two substitutional platinum atoms and three self-interstitials. Hauf et al.[34] and Johnsson[18] carried out further experiments of postimplantation annealing of platinum in silicon to get a

better idea of the conditions associated with incomplete activation. It was found that the model of Badr et al.[31] could not describe some of the later experimental results and that the model had to be modified.[18,34]

To learn more about the nature of the clusters or precipitates, a few selected wafers were investigated by high-resolution energy-filtered transmission electron microscopy (HR-EFTEM).[34] For an implanted dose of $1 \times 10^{13}\,\mathrm{cm}^{-2}$ and an annealing temperature of 778 °C, large precipitates were found which were identified as platinum silicide by energy dispersive X-ray spectroscopy (EDX).[34] The corresponding HR-EFTEM image is shown in **Figure 5**a. For an annealing temperature of 900 °C, no large precipitates were found, only cluster-like structures. These may be platinum-related, but this could not be verified by EDX.

Based on these findings and complementary secondary-ion mass spectrometry (SIMS) measurements,[18] the missing platinum is assumed to be contained in complexes in a region close to the implanted surface. The formation of such complexes also explains the trend observed in the work of Johnsson:[18] The amount of electrically active platinum saturates for higher implanted doses. The conditions for saturation naturally depend on the implanted dose, the annealing time, and temperature.

Four selected experimental results, for two doses (2×10^{12} cm^{-2} and $1 \times 10^{13}\,\mathrm{cm}^{-2}$) and two annealing temperatures (778 °C and 850 °C), are shown in Figure 5b to highlight what a model finally has to capture to describe postimplantation annealing. The corresponding simulation results, using the model from Johnsson,[18] are included to guide the eyes.

Let us first look at the influence of the annealing temperature: As anticipated, the higher temperature results in higher concentrations of Pt_s compared to the lower temperature. Looking closer at the 850 °C profiles, the higher dose results in a higher concentration of Pt_s both in the bulk and at the surface, but the difference is not as large as it would be if all of the implanted platinum would be active. Approximately 72% is found to be active for the lower dose, whereas only approximately 22% of the implanted dose is found to be active for the higher dose. This means that there is a large amount of platinum contained in precipitates or clusters, and even less platinum is found to be active after annealing at 778 °C.

The 778 °C profiles are almost identical within the experimental limits, i.e., there is a saturation in the active dose. However, one can also see that the lower implanted dose results in slightly higher measured concentrations of Pt_s. This might seem a little surprising, but it can be explained because the smaller supersaturation associated with the lower dose is related to slower precipitation kinetics, visible for this particular combination of dose, annealing time, and temperature. This trend is consistent with the model for dopant precipitation from Dunham.[43]

It is quite a challenge to find a clustering or precipitation model that can reproduce the experimental data, especially one which results in the formation of Pt agglomerates only near the implanted surface. According to Ostwald ripening theory, the Pt complexes forming around the implantation peak maintain in their vicinity an interstitial platinum concentration which exceeds the equilibrium concentration at least slightly. Due to the high diffusivity of interstitial platinum, this concentration is established basically everywhere in the wafer, which could result in the formation of platinum complexes over the entire wafer depth. So far, however, there is no experimental evidence of such platinum complexes off the implanted surface. To prevent the formation of platinum complexes also in the model, their formation needs to set in sharply at somewhat higher Pt_i

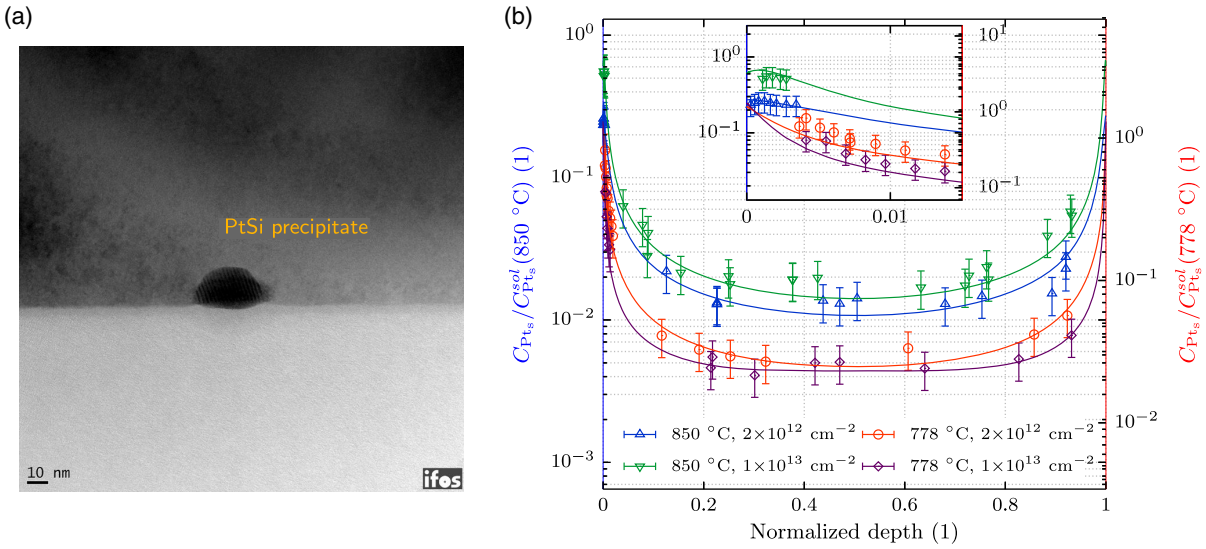

Figure 5. a) HR-EFTEM image after postimplantation annealing of platinum in silicon. 1×10^{13} cm^{-2}, 778 °C for 2 h (+ standard ramping). The dark spot in the middle was identified as a PtSi precipitate by EDX. Adapted with permission.[34] Copyright 2018, IEEE. b) DLTS measurements (symbols) and corresponding simulation results (lines, using the model from Johnsson[18]) of the substitutional platinum concentration after implantation (150 keV) and annealing at 850 °C (substrate material: CZ-grown dislocation-free silicon, n-type, P-doped, 1–3 Ω cm, (100), 725 µm). The inset shows the concentration close to the implanted surface. The left and right *y*-axes are normalized by $C^{sol}_{Pt_s}$ at 850°C and 778 °C from Johnsson,[18] respectively.

concentrations. This is something none of the simple cluster model used to describe the formation of inactive dopant complexes can achieve and even simple precipitation models are close to their limits.

To reproduce the experimental data, Johnsson[18] presented a heuristic model for platinum precipitation inspired by Pichler,[44] Dunham,[43] and Zechner et al.,[42] using a moment-based approach to describe larger clusters and precipitates of platinum. An earlier version of this model was presented by Hauf et al.,[34] which considered large precipitates of a fixed size. In the later model, it was no longer necessary to assume a fixed size, and the large clusters are represented by a moment-based approach instead.[18] The zeroth moment is the concentration of platinum atoms in precipitates n_{ppt} and the first moment is the concentration of precipitates $C_{\mathrm{Pt_{ppt}}}$. Johnsson's model can be expressed by the following quasichemical reactions

$$\mathrm{Pt_s} + \mathrm{Pt_i} \xrightarrow{g_1} \mathrm{Pt_2} + \mathrm{V} \tag{8}$$

$$\mathrm{Pt_2} \xrightarrow{d_1} 2\mathrm{Pt_i} \tag{9}$$

$$\mathrm{Pt_2} + \mathrm{Pt_i} \xrightarrow{g_2} \mathrm{Pt_{ppt}} \tag{10}$$

$$\mathrm{Pt_{ppt}} + \mathrm{Pt_i} \xrightarrow{g_{\mathrm{ppt}}} \mathrm{Pt_{ppt}} \tag{11}$$

$$\mathrm{Pt_{ppt}} \xrightarrow{d_{\mathrm{ppt}}} \mathrm{Pt_i} + \mathrm{Pt_{ppt}} \tag{12}$$

where $\mathrm{Pt_{ppt}}$ is used to denote a platinum precipitate without considering its size. The d's denote the dissolution rates, and the g's the generation rates. The model only includes one intermediate cluster $\mathrm{Pt_2}$. By assuming that the $\mathrm{Pt_2}$ clusters only from one $\mathrm{Pt_s}$ atom and one $\mathrm{Pt_i}$ atom makes their formation more likely in the implanted region than in the bulk. It is a basis for having the precipitates form and grow in implanted region in the simulations, as suggested by the experimental data. The $\mathrm{Pt_2}$ clusters are assumed to dissolve into two platinum interstitials. How the formation, growth, and dissolution of Pt precipitates are modeled are described by Equation (10), (11), and (12), respectively. In addition, it is necessary to consider the size evolution of the precipitates through the following differential equations

$$\frac{\partial n_{\mathrm{ppt}}}{\partial t} = 3g_2 C_{\mathrm{Pt_i}} C_{\mathrm{Pt_2}} + g_{\mathrm{ppt}} C_{\mathrm{Pt_i}} C_{\mathrm{Pt_{ppt}}} - d_{\mathrm{ppt}} C_{\mathrm{Pt_{ppt}}} \tag{13}$$

$$\frac{\partial C_{\mathrm{Pt_{ppt}}}}{\partial t} = g_2 C_{\mathrm{Pt_i}} C_{\mathrm{Pt_2}} - d_{\mathrm{ppt}} \frac{C_{\mathrm{Pt_{ppt}}}}{n_{\mathrm{ppt}}} C_{\mathrm{Pt_{ppt}}} \tag{14}$$

The full system of equations used by Johnsson[18] to model postimplantation annealing of platinum in silicon includes self-interstitial agglomeration, platinum precipitation, the Frank–Turnbull mechanism, the kick-out mechanism, bulk recombination, and reaction with immobile VX complexes. The complexes and precipitates of self-interstitials, and of platinum, are all assumed to be immobile. Neumann boundary conditions are used for interstitial platinum at both surfaces. The boundary conditions for intrinsic point defects and immobile species are the same as for diffusion from a Pt-silicide layer.

An important note is that Badr et al.[31] concluded from own experiments that the substrate material had no noticeable influence on the results. However, by considering further experiments, Johnsson[18] could show that the substrate material and the prior processing steps may actually have a significant influence on the results under certain conditions. This effect was considered in the initial conditions for the VX complexes.

Johnsson[18] calibrated the reaction rate constants of the Pt-precipitation model against own data and the data from Badr,[32] with annealing temperatures ranging from 770 °C to 900 °C (the annealing time was always 2 h followed by cooling), and implanted doses ranging from 5×10^{11} cm^{-2} to 5×10^{13} cm^{-2}. With the model, the available experiments could be reproduced. Nevertheless, there is surely room for improvement. The precipitation model is clearly a simplification of the actual precipitation process, and it would be more accurate to consider further cluster sizes as well as the interaction with intrinsic point defects. However, the system rapidly becomes very complex, and difficult to calibrate based on the available experiments. For example, the experimental data available, although covering a reasonable range of temperatures and implanted doses, do not provide temporal resolution of the evolution of incomplete activation of platinum.

3.4. PDG of Platinum in Silicon

For PDG of platinum in silicon, a high concentration of phosphorus is introduced at the surface from which the platinum is to be removed. The phosphorus can be introduced by deposition of a phosphorus glass or via ion implantation, and the gettering proceeds during subsequent annealing. The phosphorus diffuses mainly via vacancies at high concentrations and mainly via self-interstitials at lower concentrations. The latter leads to a supersaturation of self-interstitials when interstitial phosphorus atoms kick out lattices atoms to become substitutional. In the case of implanted phosphorus, the self-interstitial concentration in areas far beyond the phosphorus profile is additionally increased by the annealing of the implantation damage.

The generated silicon self-interstitials diffuse toward the bulk and displace substitutional platinum to interstitial sites via the kick-out mechanism in the backward direction. The interstitial platinum atoms, in turn, diffuse toward the P-rich region where they may form complexes with the phosphorus atoms[45,46] or even platinum silicide precipitates.[47] Macroscopically, such complex formation acts as a sink for $\mathrm{Pt_i}$ and getters them from the bulk. In the end, the combination of mobilization by the self-interstitial oversaturation and gettering by the phosphorus atoms results in the asymmetric concentration profiles of substitutional platinum as shown in Figure 3a.

PDG was investigated by Zimmermann[21] for the gettering of gold and platinum, where the phosphorus was introduced via a deposition process. Zimmermann fitted a value for the supersaturation of self-interstitials at the surface and added additional equations to the model to describe the capture of gold or platinum in the P-rich region. PDG of platinum was also investigated by Badr,[32] where the phosphorus was introduced via ion implantation, and the PDG annealing was carried out in a temperature range from 827 °C to 852 °C. The platinum was introduced

before by diffusion from a Pt-silicide layer. Alternatively, the platinum can be introduced via implantation followed by annealing.[12]

Badr simulated the PDG process in two steps. First, the phosphorus diffusion was simulated using the model by Wolf[48] implemented in Sentaurus Process of Synopsys. The resulting supersaturation of self-interstitials at the surface due to the phosphorus diffusion versus time was saved and used as a boundary condition in a second simulation using the general purpose solver PROMIS.[49] The concentration profiles resulting from the platinum diffusion from a Pt-silicide layer were used as initial conditions. Dirichlet boundary conditions were used for both self-interstitials and vacancies, where α_{SS}^{I} represent the time-dependent supersaturation of self-interstitials

$$C_I^{surface} = \alpha_{ss}^{I} \times C_I^{eq} \tag{15}$$

$$C_V^{surface} = \frac{1}{\alpha_{ss}^{I}} \times C_V^{eq} \tag{16}$$

The gettering of the platinum by the phosphorus was, for simplicity, modeled by a diffusion-limited sink for interstitial platinum at the P-implanted surface.

While the model of Badr[32] was already able to reproduce the main features of the PDG of platinum in silicon, it required somewhat different parameters for C_I^{eq} than used in the same work for platinum diffusion from silicides and during postimplantation annealing. In the continuation of the work by Johnsson,[18] it was found that these parameters were incompatible with other platinum diffusion experiments, especially at lower temperatures. Johnsson could finally avoid the inconsistencies by showing that with only a few minor changes to the default parameters of Sentaurus Process Advanced Calibration (O.2018.11), it is possible to fit the data from the SIMS measurements and SRP measurements as well as the platinum profiles after PDG, using a consistent parameter set, and without exceeding the reported upper limits for C_I^{eq}. The upper limits for C_I^{eq} will be discussed further in Section 4.3.2. As a final note, the model for PDG was calibrated only for a small temperature range. More experimental data are needed in order to extend the process window and to further improve the predictability of the model.

4. Contributions to Basic Research from Model Calibration

To successfully model postimplantation annealing and PDG of platinum in silicon with a consistent parameter set, a good model describing platinum diffusion from a Pt-silicide layer is required first. It establishes the basis for the more complex processes. However, it is not trivial to find one set of model parameters that can describe all of the experiments of platinum diffusion from a Pt-silicide layer reported in the literature. In some way, this can also be seen as an advantage: Because of the constraints posed by different experiments, it is possible to draw some conclusions about the properties of platinum in silicon as well as the properties of intrinsic point defects.

A general issue with the models found in the literature is that the parameter values are widely different. For some parameters, they even differ by several orders of magnitude at certain temperatures. This is the case because not all experiments are sensitive to all parameters, and some parameters can seemingly be chosen freely while still reproducing the experimental results. Although considering all of the reported works, it is rather challenging to find a parameter set which satisfies all constraints simultaneously. First, the parameters that can be identified independently have to be determined. Then, the rest can be evaluated. In the case of platinum diffusion in silicon, we start to evaluate the solubility concentration of substitutional platinum. We move on to the transport capacity of interstitial platinum, to finally evaluate the equilibrium concentrations and diffusivities of vacancies and silicon self-interstitials.

4.1. Solubility Concentration of Substitutional Platinum in Silicon

Measurements of the solubility concentration of platinum have been reported in a wide temperature range from experiments of diffusion from a Pt-silicide layer. One method is to measure the concentration after long-time annealing. The concentration of electrically active platinum is then assumed to correspond to the solubility concentration. This method was applied in several studies,[19,20,23] in which the platinum concentration was measured by neutron activation analysis (NAA) or DLTS. Another method to estimate $C_{Pt_s}^{sol}$, presented by Gösele et al.,[36] is based on the domination of the kick-out mechanism. By comparing measurements of the bulk concentration obtained after annealing for different times at the same temperature T, $C_{Pt_s}^{sol}(T)$ can be estimated, provided that the transport capacity of silicon self-interstitials is known and that the initial conditions are the same. Jacob et al.[26] used this approach in their work. The data were reevaluated by Johnsson,[18] using the transport capacity for silicon self-interstitials reported by Südkamp and Bracht.[50]

Reported experimental data are shown together with reported parameter values for $C_{Pt_s}^{sol}$ in **Figure 6**. Most of the reported expressions follow an Arrhenius law, valid only for a certain temperature range. It is not possible to fit a single Arrhenius expression to all of the data. An expression valid in the whole temperature range, such as that of Johnsson[18] used to calculate the corresponding curve in Figure 6, requires the consideration of the liquid impurity phase above the eutectic temperature (at 979 °C) in analogy to the work of Weber[51] on transition metals in silicon.

4.2. Transport Capacity of Interstitial Platinum

The transport capacity of interstitial platinum governs how quickly the platinum propagates in the wafers during annealing. It is the product of the solubility concentration and the diffusion coefficient, $C_{Pt_i}^{sol} D_{Pt_i}$. This parameter does not always have a significant influence on the simulation results, and that is why there are large differences in the expressions used for this parameter in the literature. A few examples are shown in **Figure 7**a. Nevertheless, two types of experiments have proved useful in

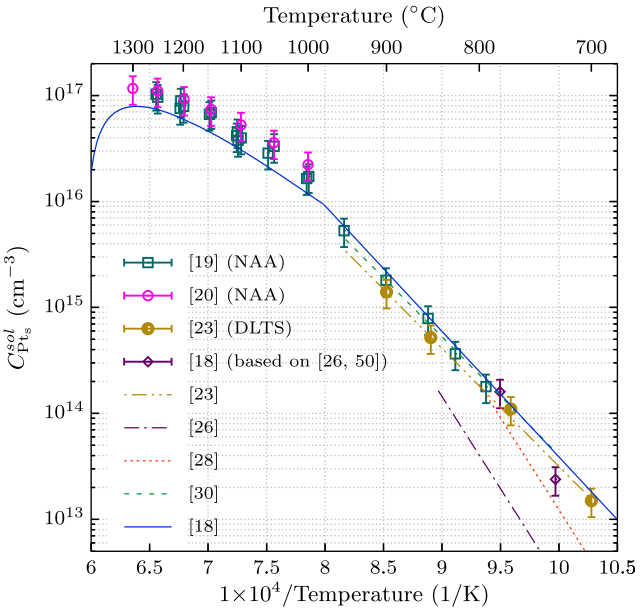

Figure 6. Reported parameter values and measurements of the solubility concentration of substitutional platinum. Adapted with permission.[18] Copyright 2019, A. Johnsson.

narrowing down the range: diffusion in highly dislocated silicon from Lerch et al.[24] and diffusion at low temperatures in dislocation-free silicon with rather high initial concentrations of grown-in vacancies.[18]

Lerch et al.[24] estimated values of the so-called effective diffusivity, $D^{\text{eff}}_{\text{Pt}}$, from the diffusion of platinum into highly dislocated silicon in a temperature range of 950 to 1120 °C, assuming that the dislocations act as sinks for self-interstitials and that the kick-out mechanism is dominating. $D^{\text{eff}}_{\text{Pt}}$ can be simplified further since $C^{\text{sol}}_{\text{Pt}_s} \gg C^{\text{sol}}_{\text{Pt}_i}$ at high temperatures,[19,20] and is then given by

$$D^{\text{eff}}_{\text{Pt}} = \frac{C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}}{C^{\text{sol}}_{\text{Pt}_s} - C^{\text{sol}}_{\text{Pt}_i}} \approx \frac{C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}}{C^{\text{sol}}_{\text{Pt}_s}} \tag{17}$$

[24]. From the effective diffusivity, Lerch et al.[24] extracted $C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}$ based on the data for $C^{\text{sol}}_{\text{Pt}_s}$ reported by Hauber et al.[20] The values from Lerch et al.[24] are shown in Figure 7a together with values obtained by Johnsson[18] from a reevaluation of the same data using her new parameter values for $C^{\text{sol}}_{\text{Pt}_s}$, as shown in Figure 6.

Lower limits of $C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}$ deduced by Johnsson[18] are also shown in Figure 7a. They were derived from simulations of Zimmermann's experiments[21] of one- and two-sided diffusion in a temperature range from 700 to 950 °C. An example is shown in Figure 7b. The data were reported by Zimmermann[21] (measured by DLTS) and correspond to one-sided diffusion from a Pt-silicide layer at 770 °C for 30 min. The simulations were carried out for increasing values of $C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}$ at 770 °C. The blue solid line in Figure 7b represents the lower limit.

Based on the data from Lerch et al.[24] and the lower limits, Johnsson[18] suggested a new expression for $C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}$ which was used to calculate the corresponding curve in Figure 7a.

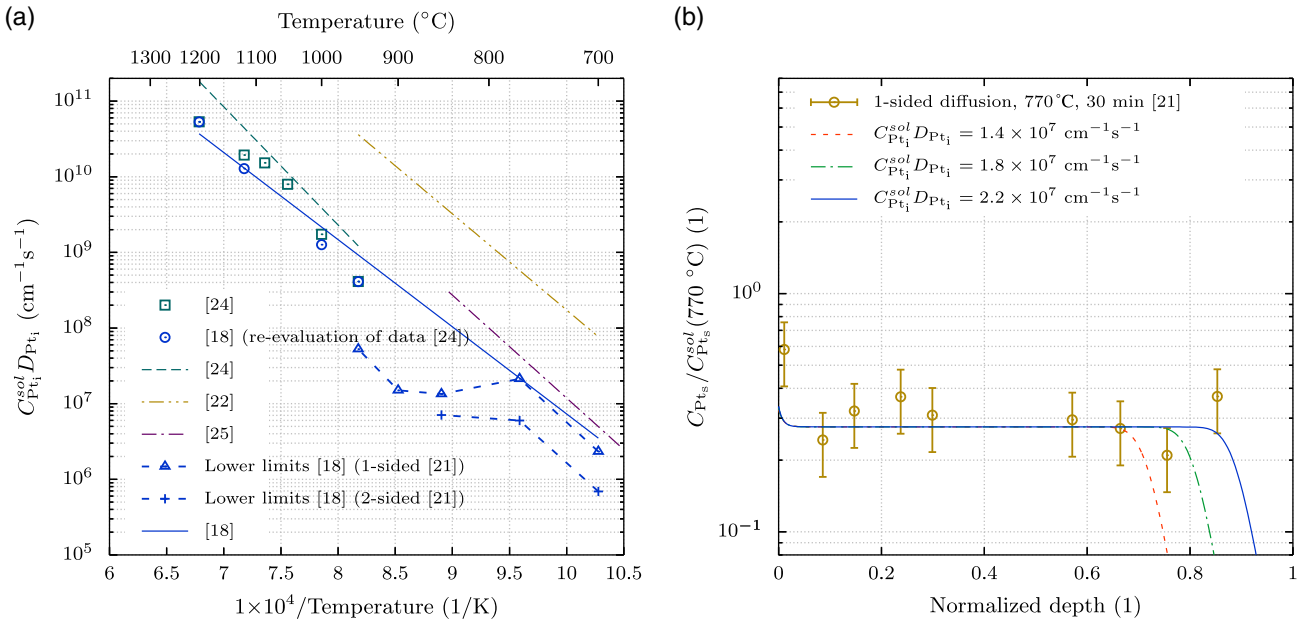

Figure 7. a) Some reported values of the transport capacity of interstitial platinum together with the lower limits from Johnsson.[18] Adapted with permission.[18] Copyright 2019, A. Johnsson. b) Measured concentrations of substitutional platinum from Zimmermann[21] after one-sided diffusion at 770 °C for 30 min together with corresponding simulation results using the model from Johnsson[18] for increasing values of $C^{\text{sol}}_{\text{Pt}_i} D_{\text{Pt}_i}$. The Pt_s concentration is normalized by $C^{\text{sol}}_{\text{Pt}_s}$ at 770 °C from Johnsson.[18]

4.3. Properties of Intrinsic Point Defects

Although the transport capacities of vacancies and self-interstitials have been determined with a fairly high degree of certainty,[50] there exist many suggestions for the individual properties (C_V^{eq}, D_V, C_I^{eq}, and D_I) in the literature. As these properties cannot be measured directly, there are large variations in the reported values and it is not trivial, or rather impossible, to find one expression that fits all studies. A more comprehensive review can, e.g., be found in the book by Pichler.[38] The expressions used in the studies of platinum diffusion differ largely as well. The individual values of these parameters have, thus far, only been found to have a significant influence in experiments where the anneal ended with a cooling phase.[30,33] A controlled cooling phase, where the temperature is ramped down, is typically used in industry processes.

4.3.1. The Equilibrium Concentration of Vacancies

Badr et al.[29,30] investigated the effect of the ramping rate in the cooling-down phase of the furnace after an annealing process and found that it does have an influence on the concentration of substitutional platinum in the near-surface region. In Badr's experiments, the platinum was introduced from a Pt-silicide layer during annealing at 830 °C followed by cooling at different rates (0.6, 1.2, 2.3, and 4.6 K min^{-1}).[29] The concentration at the surface was measured to be lower for the slower cooling rates.[29] The rate dependence could be traced back to the Frank–Turnbull mechanism in the backward direction.[30] In other words, the reaction rate constant $k_{FT_\leftarrow}$ in the model has to be large enough in order to account for the measurements.

The effect of varying $k_{FT_\leftarrow}$ in the simulations is shown for one example in **Figure 8**a in comparison to measurement data. The measurements (DLTS) correspond to the experiment with a cooling rate of 0.6 K min^{-1} and the simulation results correspond to increasing values of $k_{FT_\leftarrow}$, as indicated in the graph.

Under the assumption of $D_{Pt_i} \gg D_V$, the expression for $k_{FT_\leftarrow}$ can be simplified

$$k_{FT_\leftarrow} = 4\pi a_{FT}(D_{Pt_i} + D_V)\frac{C_{Pt_i}^{sol} C_V^{eq}}{C_{Pt_s}^{sol}} \approx 4\pi a_{FT}\frac{C_{Pt_i}^{sol} D_{Pt_i}}{C_{Pt_s}^{sol}} C_V^{eq} \quad (18)$$

From Equation (18), Badr et al.[30] deduced a lower limit for C_V^{eq} based on their parameter set, with $C_{Pt_i}^{sol} D_{Pt_i}$, a_{FT}, and $C_{Pt_s}^{sol}$ fixed. This limit at 830 °C was reevaluated by Johnsson[18] for her parameter set, using the corresponding parameters for $C_{Pt_i}^{sol} D_{Pt_i}$ shown in Figure 7a.

On the other hand, if C_V^{eq} at 830 °C is chosen large, for example, like in the work of Jacob et al.,[26] it would result in a too large reduction of C_{Pt_s} in the near-surface region during cooling. A supporting example can be found in the work of Badr et al.,[29] showing the simulation results of the same cooling experiments using the complete parameter set from Jacob et al.[26]. However, such large values for C_V^{eq} are less relevant for the calibration. This becomes clear while considering information from Voronkov and Falster[52] at the melting temperature for silicon, and experiments of RTA followed by platinum diffusion from Quast.[28]

At the melting-point temperature of silicon, Voronkov and Falster[52] suggested that the difference $C_V^{eq} - C_I^{eq}$ should be approximately 1.6×10^{14} cm^{-3}. This is based on data obtained

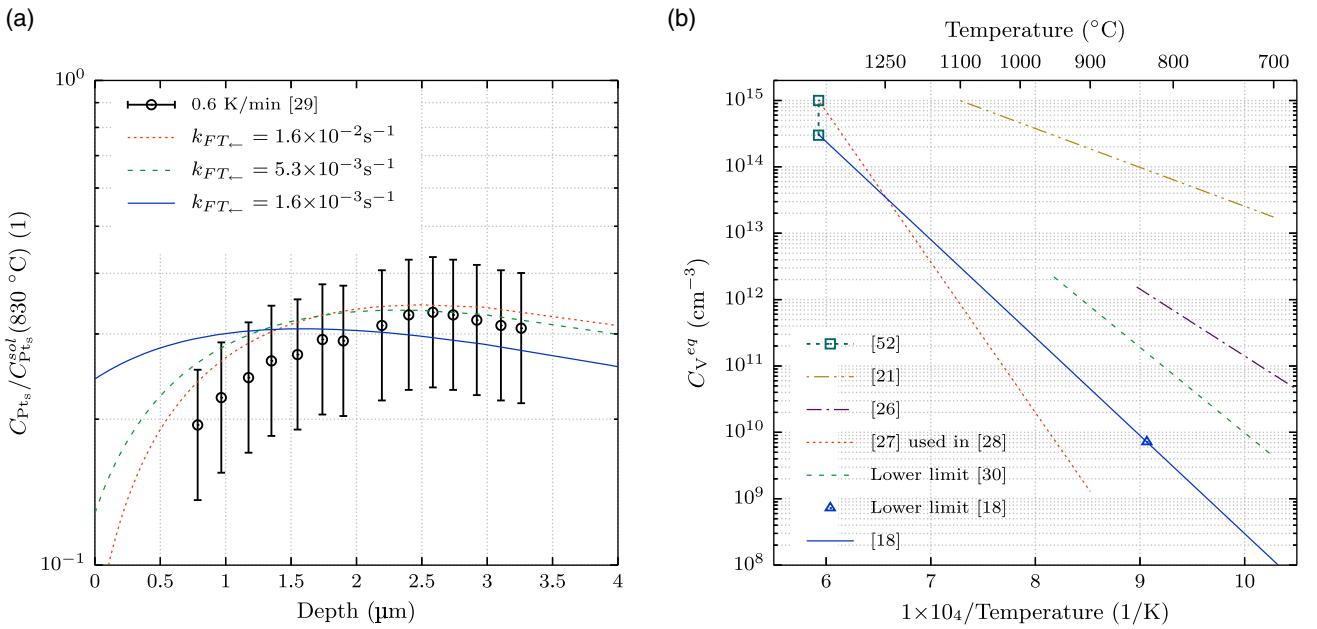

Figure 8. a) Simulations with increasing values of $k_{FT_\leftarrow}$ at 830 °C of one-sided diffusion at 830 °C for 2 h followed by controlled cooling with a rate of 0.6 K min^{-1} compared to corresponding data measured by Badr et al.[29] and Johnsson.[18] The Pt_s concentration is normalized by $C_{Pt_s}^{sol}$ at 830 °C from Johnsson.[18] b) Some reported values of the equilibrium concentration of vacancies together with the lower limit from Johnsson[18] at 830 °C. a,b) Adapted with permission.[18] Copyright 2019, A. Johnsson.

from crystal growth and from rapid thermal annealing (RTA) effects on voids. They also estimated that C_V^{eq} at the melting temperature should lie between 3×10^{14} cm^{-3} and 1×10^{15} cm^{-3},[52] as shown in Figure 8b.

What does not appear in the graph for the sake of conciseness, but is considered in the evaluation of Johnsson,[18] are constraints on C_V^{eq} derived from Quast's experiments.[28] Quast used RTA to establish vacancy–oxygen complexes in the wafers before introducing the platinum. According to the evaluation of those experiments, the difference $C_V^{eq} - C_I^{eq}$ at 1250 °C should approximately be between 7.7×10^{12} cm^{-3} and 1.4×10^{13} cm^{-3}. At such a high temperature, this is a rather small difference. If C_I^{eq} could be chosen freely, this constraint would not be a large issue. That is, however, not the case: There is an upper limit for C_I^{eq} at lower temperatures. It was deduced by Johnsson et al.[33] as they completed the cooling-rate study by Badr et al.[30] with DLTS measurements of the bulk concentrations of substitutional platinum.

4.3.2. The Equilibrium Concentration of Silicon Self-Interstitials

The measured platinum concentration in the bulk of the wafers, mentioned already in the previous section, shows no significant influence of the cooling rate.[33] However, if the parameter for C_I^{eq} at 830 °C was chosen large enough in the simulations, it resulted in a lower, rate-dependent Pt_s concentration in the bulk after cooling.[33] An example is shown in **Figure 9**a for two cooling rates, 4.6 and 0.6 K min^{-1}, for two values of C_I^{eq} at 830 °C. The observed effect could be traced back to the kick-out mechanism in the backward direction and the transport of self-interstitials during the cooling phase.[33] From this observation, Johnsson et al.[33] deduced an upper limit for C_I^{eq} at 830 °C. Similarly, an upper limit could be deduced after annealing at 800 °C in the continuation work by Johnsson,[18] who also reevaluated the upper limit at 830 °C from Johnsson et al.[33] with an updated parameter set.

The upper limits from Johnsson[18] are shown in Figure 9b, together with the data from Voronkov and Falster[52] mentioned earlier and parameter values used in other studies of platinum diffusion.[18,21,25,28,30,32] Also shown in Figure 9b is the data calculated from the expression for C_I^{eq} proposed by Badr[32] for PDG, mentioned already in Section 3.4. The expression for C_I^{eq} suggested by Johnsson,[18] which is presented graphically also in the figure, satisfies the constraints from Voronkov and Falster,[52] Quast,[28] as well as the upper limits discussed above.

5. Device Simulations

TCAD simulations can provide an extremely valuable insight into device physics which govern the behavior of IGBTs, diodes, and of course other semiconductor components. A proper understanding allows to tailor the performance of power devices to the needs of various applications. Nowadays, cutting-edge performance can only be achieved by a detailed understanding of the application and by being able to model the device behavior under the respective conditions.

The models described in the previous sections can be included in TCAD process simulations, in order to estimate the spatial distribution of substitutional platinum in a silicon power diode. This way, the thermal budgets which occur during the fabrication

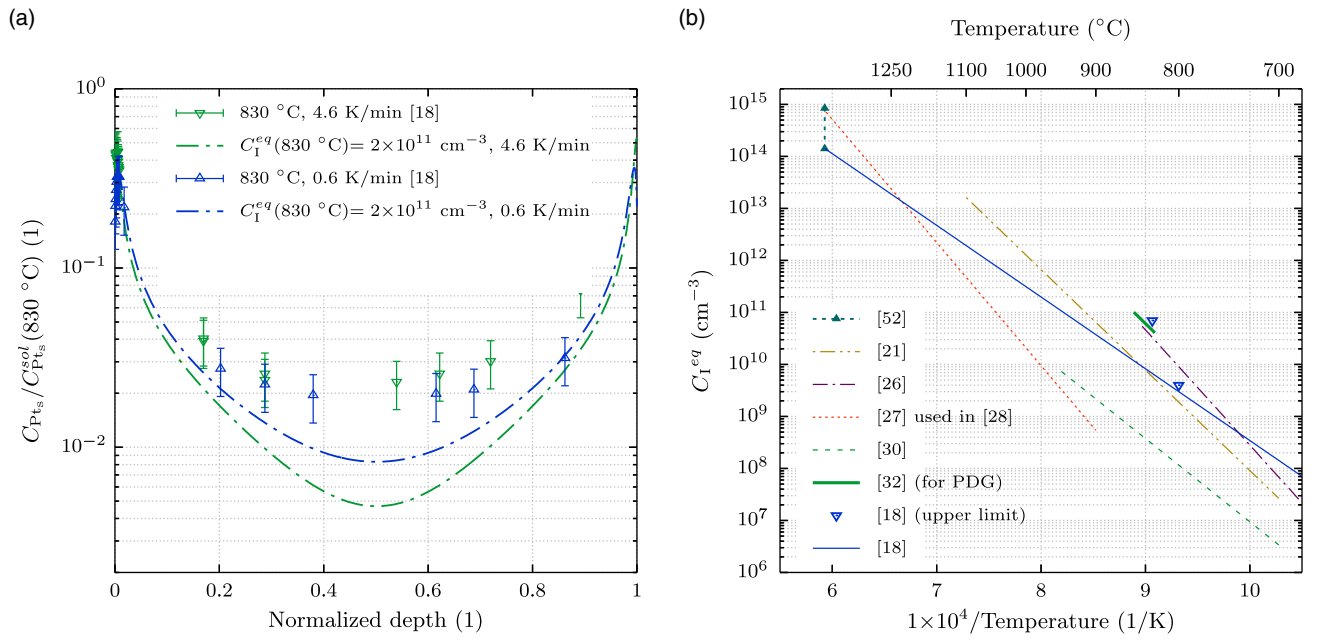

Figure 9. a) Simulations with increasing values of C_I^{eq} at 830 °C of one-sided diffusion at 830 °C for 2 h followed by controlled cooling with a rate of 4.6 and 0.6 K min^{-1} compared to corresponding data measured by Johnsson.[18] The Pt_s concentration is normalized by $C_{Pt_s}^{sol}$ at 830 °C from Johnsson.[18] b) Some reported values of the equilibrium concentration of silicon self-interstitials together with the upper limit at 830 °C. a,b) Adapted with permission.[18] Copyright 2019, A. Johnsson.

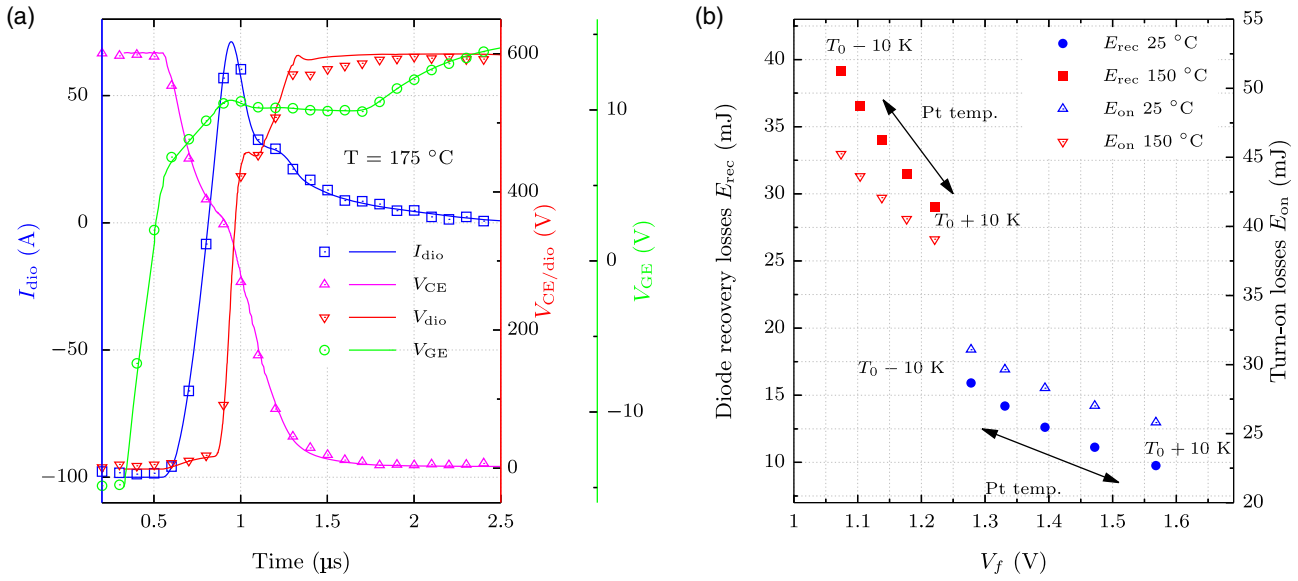

Figure 10. a) Time transients of the diode current (I_{dio}, current scale inverted), diode voltage (V_{dio}), the IGBT collector–emitter voltage (V_{CE}), and the IGBT gate voltage (V_{GE}) for simulation (solid lines) and experiment (open symbols), showing an excellent agreement. 1200 V 100 A free-wheeling diode in a half-bridge configuration with a 1200 V 140 A IGBT. DC-link voltage: 600 V, switching current: 100 A, gate resistor: 23 Ω, temperature: 175 °C. b) Simulated trade-off diagram comparing the dynamic (E_{rec}, E_{on}) and static (V_f) losses at room temperature and 150 °C. a,b) Reproduced with permission.[14] Copyright 2018, IEEE.

process and which influence the platinum distribution can be accounted for. Also, this allows to investigate the effect of process variations on the trap distribution.

In a second step, the spatial trap distribution serves as an input for estimating the electrical device performance in a TCAD device simulation. To simulate the electrical behavior, the energy levels and capture cross sections for electrons and holes are needed. Values for these properties can, for example, be found in the work of Deng and Kuwano[53] and Siemieniec et al.[5]. Of course, the simulations require a proper calibration of the effect of platinum-related traps on the charge carrier lifetime. Only when taking into account the energy level and the capture cross sections in dependency of the temperature, a proper calibration can be obtained.[14] **Figure 10**a shows an exemplary comparison of simulation and experiment for an IGBT turn-on event and the concurrent reverse recovery of the power diode. The platinum distribution in the example diode is asymmetric: After the platinum-diffusion step, the diode was thinned from the backside, creating an asymmetric platinum profile in the remaining substrate.[14] The same applies to the diodes in Figure 10b.

Figure 10b shows how device simulation can easily predict the change of static and dynamic losses (e.g., the forward voltage drop V_f and the switching losses E_{on} and E_{rec}, which occur in the IGBT and diode during IGBT turn-on) for a variation of the Pt diffusion temperature of a few Kelvin around a target temperature T_0. Finally, the balancing of static and dynamic losses is key when it comes to maximizing the switching power of devices in the application. An application, which uses a low switching frequency of the pulse width modulation (PWM), benefits from low on-state losses. Here, the switching losses do not contribute as much the total loss performance. On the other hand, a high-frequency application is much more sensitive to the dynamic losses. Being able to simulate the device performance in a predictive manner therefore allows for an efficient development process, saving costs in terms of material and time-to-market. Last but not least, other important key parameters such as, e.g., the diode softness, voltage or current slopes, diode ruggedness and critical overvoltages can be investigated by this full chain of process and device simulation in TCAD.

6. Conclusion and Outlook

Platinum is and will continue to be an important part of silicon power devices. In today's customer-oriented market, it is paramount to understand customer and user needs and to be able to exactly tailor the device characteristics accordingly. In order to meet such requirements as well as keeping the time-to-market short, a predictive TCAD chain is absolutely necessary. In extension, this means that we need predictive process and device simulation models.

In this article, we have presented three important processes and corresponding process models: platinum diffusion from a Pt-silicide layer, postimplantation annealing, and PDG. We have also shown how experiments of platinum diffusion in silicon have made contributions to basic research for the transport capacity of interstitial platinum, lower limits for the equilibrium concentration of vacancies, and an upper limit for the equilibrium concentration of silicon self-interstitials.

The use of an implantation process ensures good reproducibility and it is well suited for integration in a semiconductor production line. Even though the existing process model is sufficient for an industry-relevant process window, the understanding of the damage evolution during annealing associated with platinum implantation is still in an early phase. To further improve the

model for postimplantation annealing, additional dedicated experiments are needed.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

lifetime engineering, phosphorus-diffusion gettering, platinum diffusion, platinum implantation, platinum silicide, silicon power devices

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