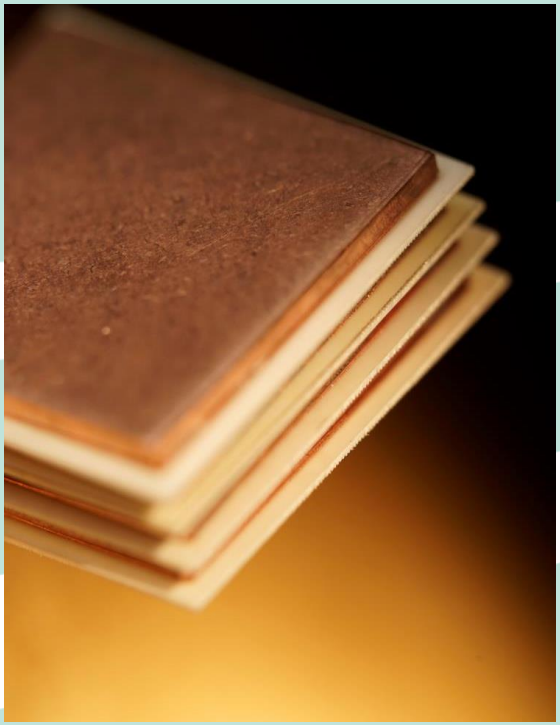
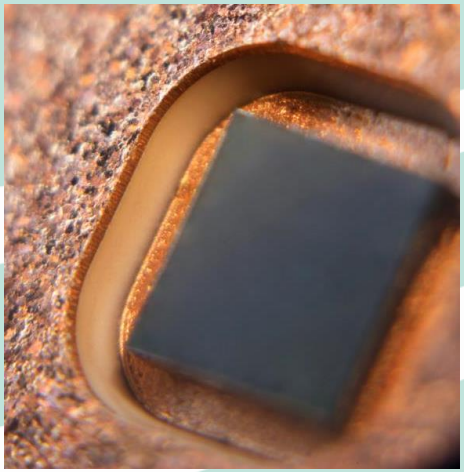
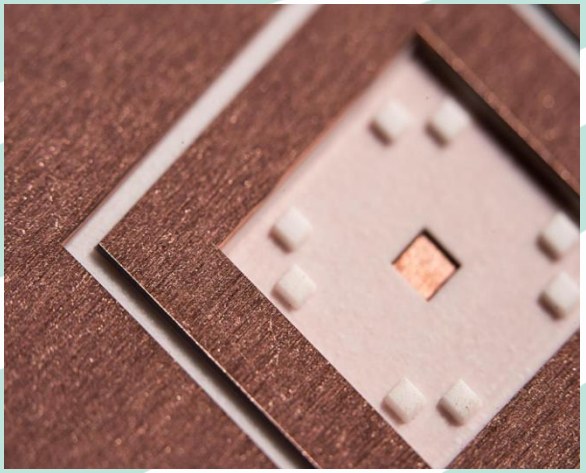
FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY

DEVICE AND RELIABILITY







Ceramic Embedding Technologies for High Temperature Power Electronics

Linh Bach, Zechun Yu

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Content

- Motivation for Ceramic Embedding
- Concept of DBC Embedding
- Evaluation of Embedding Process
  - Laserstructuring Process of DBC Substrate
  - Die Attach Process of Power Semiconductor
- Test and Result
- Summary and Conclusion

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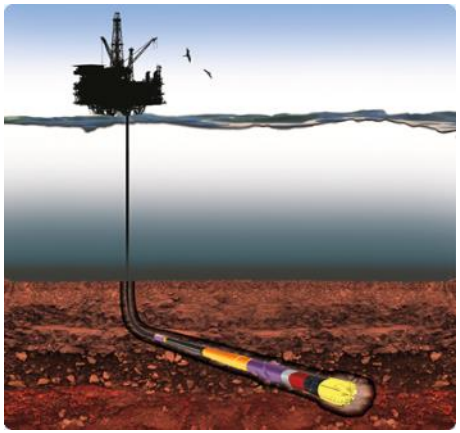
Motivation for Ceramic Embedding

High

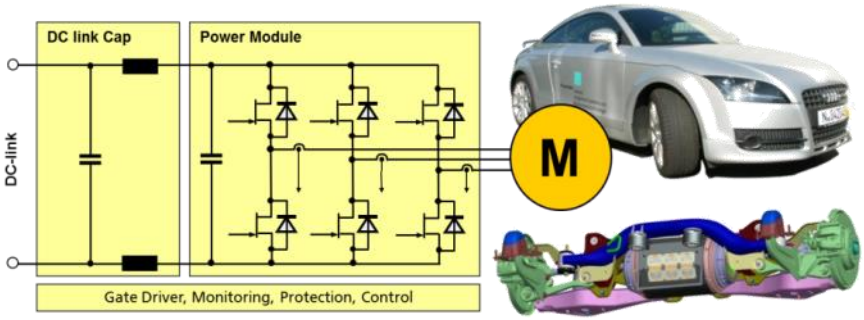
- Power
- Temperature
- Switching speed
- Reliability



*Down-hole oil & gas well drilling

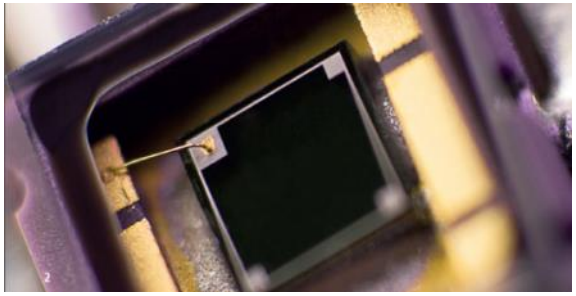
Aviation

Aerospace



Electric Vehicles Technology IISB

...and more



HT Sensor Technology IISB

** http://www.analog.com/en/analog-dialogue/articles/high-temperature-electronic-pose-design-challenges.html*

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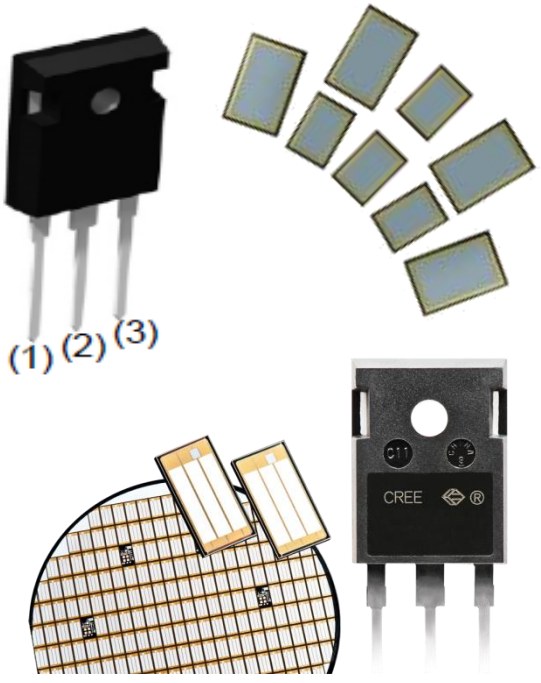
Motivation for Ceramic Embedding

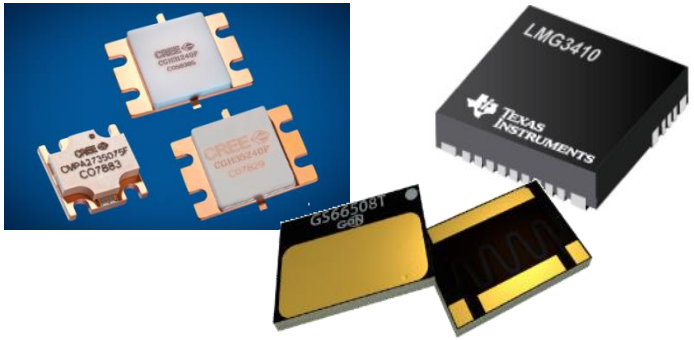
- WBG Device technologies

SiC devices

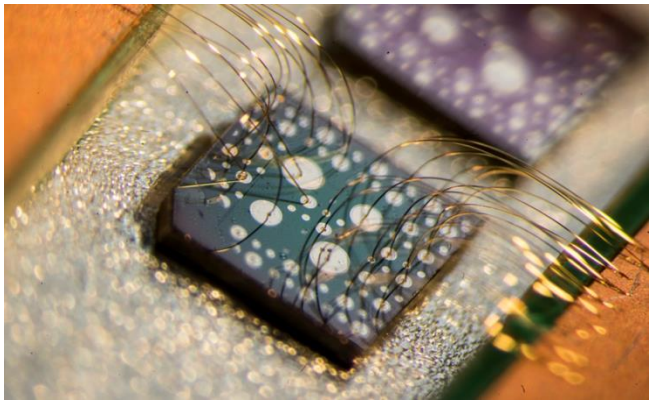


@Cree

GaN devices



and other (Ultra) WBG…
e. g. Diamond



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Motivation for Ceramic Embedding

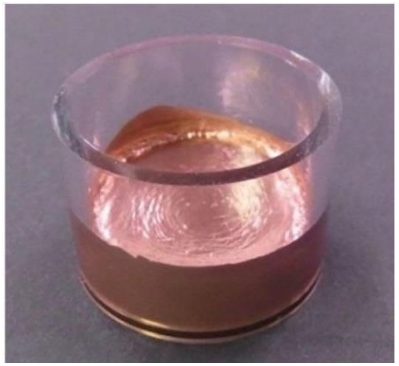
- Die attach material

HT solder alloys
AuGe, AuSn, diffusion solder, etc.

https://www.indium.com/nanofoil/

and more….

Cu sinter paste



Ag sinter paste

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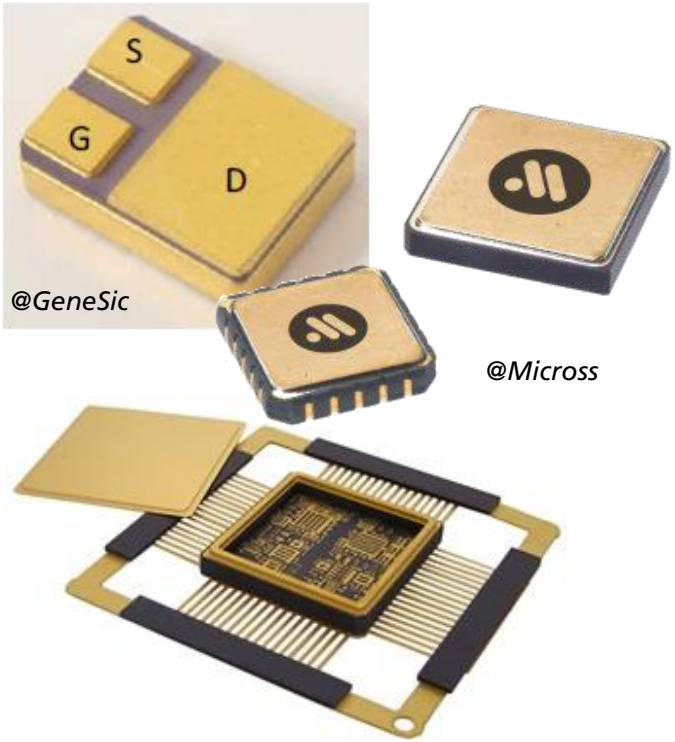
Motivation for Ceramic Embedding

- Power module concept

Hermetic packages

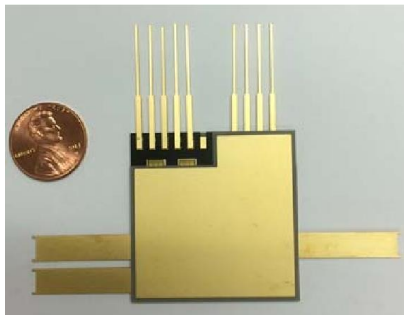


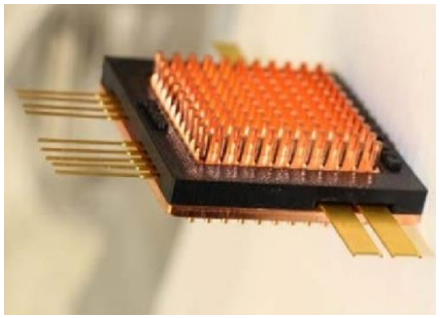
@GeneSic

@Micross

http://www.hybridassembly.net/HermeticSeamSealing/

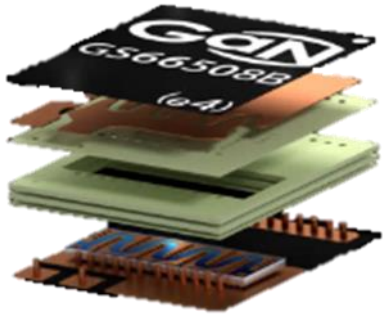
Double sided cooled packages



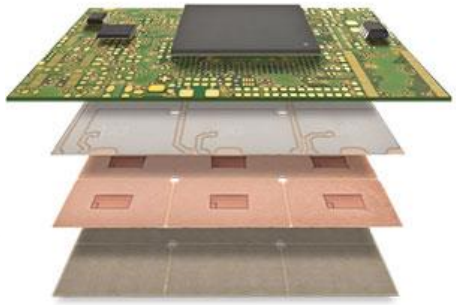


Z. Liang et al.: Integrated double sided cooling packaging of planar SiC power modules

PCB Embedding



GaNPX® package



p² Pack®.

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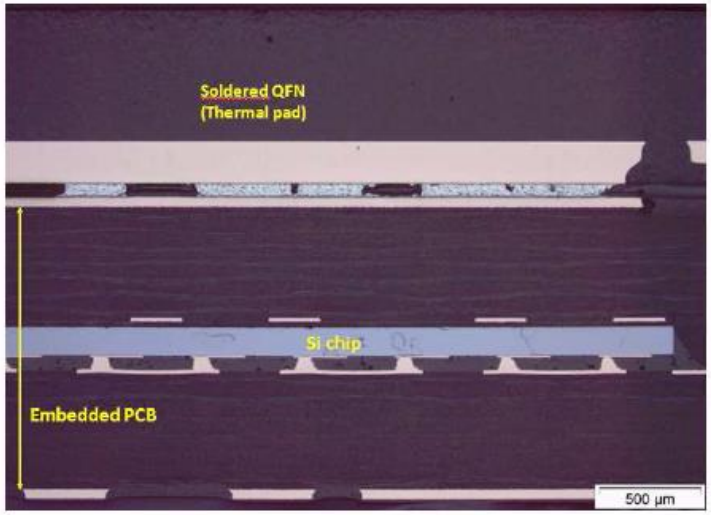
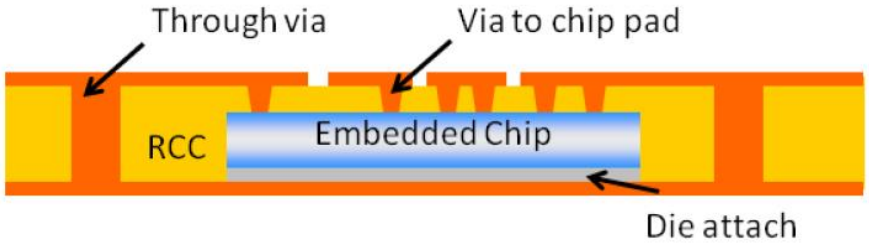
Motivation for Ceramic Embedding

- Features of State-of-the-Art PCB embedding (organic insulation)
  - Miniaturization → no housing, 3D-integration, reduction of connection points
  - High switching → short current paths, vias instead of bond wires, low parasitic inductance
  - More efficient cooling → double-sided cooling, thermal vias



Stahr et al.: Simulation of Embedded Components in PCB Environment and Verification of Board Reliability



Boettcher et al.: Embedding of Chips for System in Package realization - Technology and Applications

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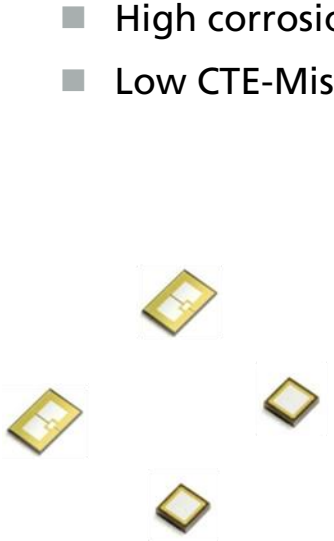
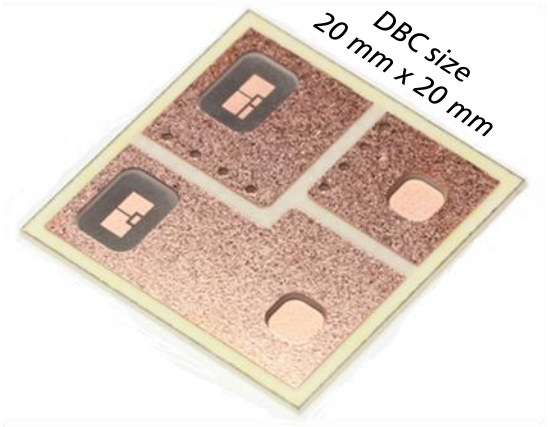
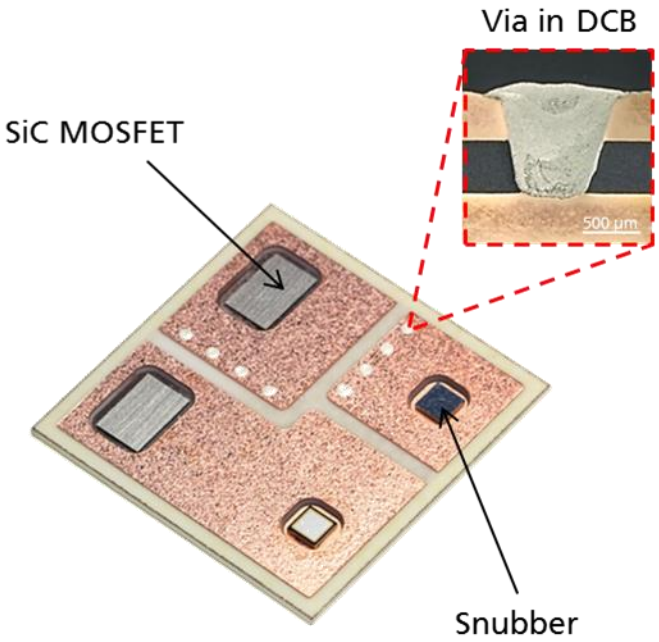
Motivation for Ceramic Embedding

- Additional features with **Ceramic embedding**
  - High temperature capability (> 200 °C)
  - High thermal conductivity (Al_2O_3, AlN, Si_3N_4)
  - High current carrying capability (Cu layer > 300 µm)
  - High corrosion resistance (ceramic)
  - Low CTE-Mismatch







Packaging solution for taking out full potential of WBG

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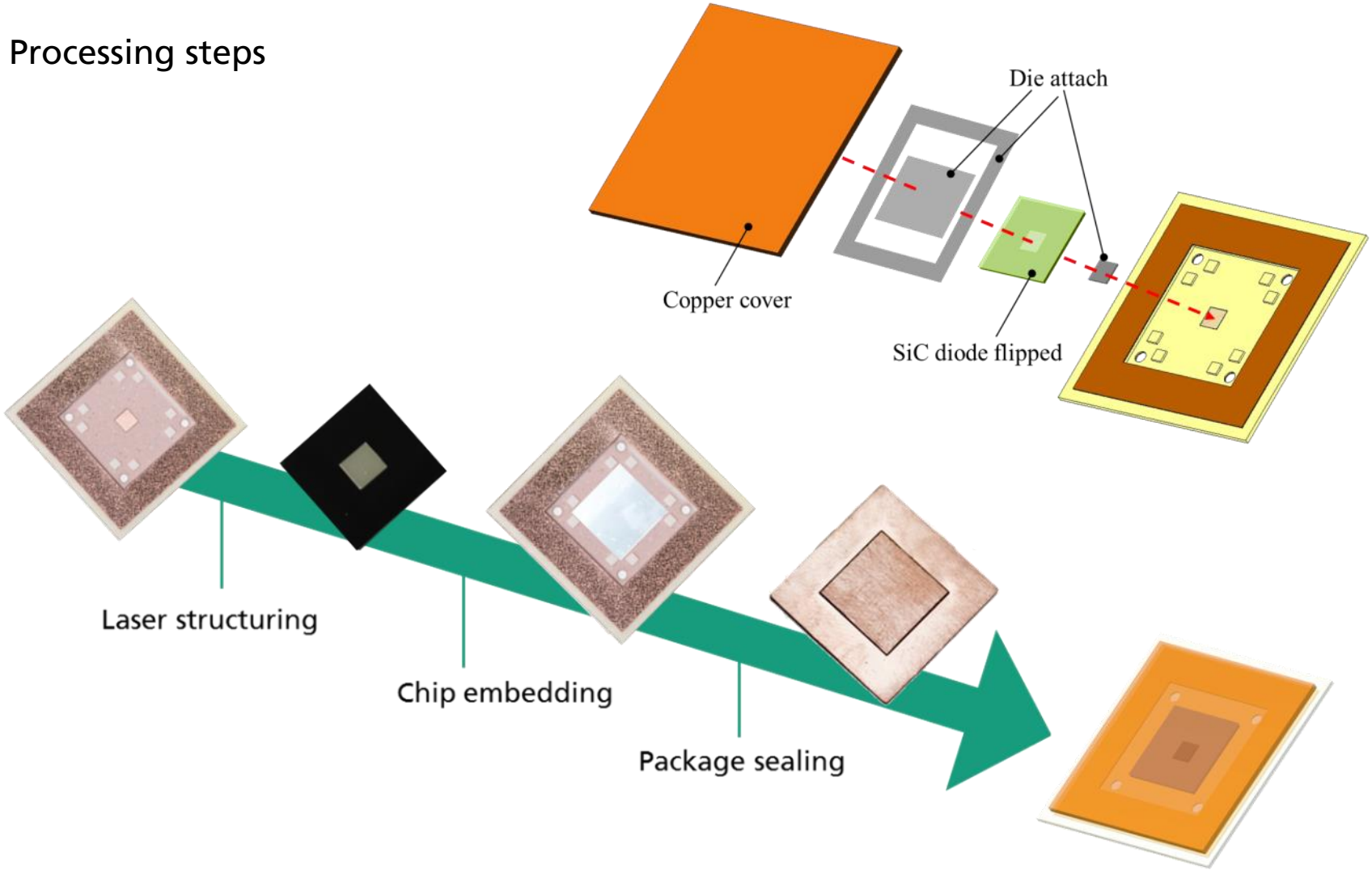
Concept of DBC Embedding

- Processing steps



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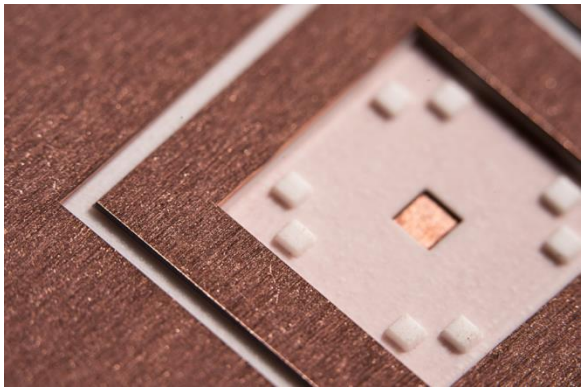
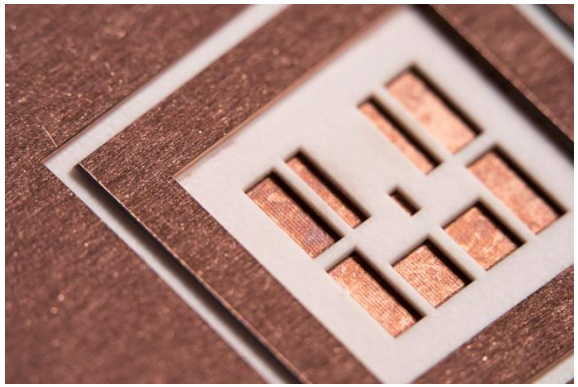
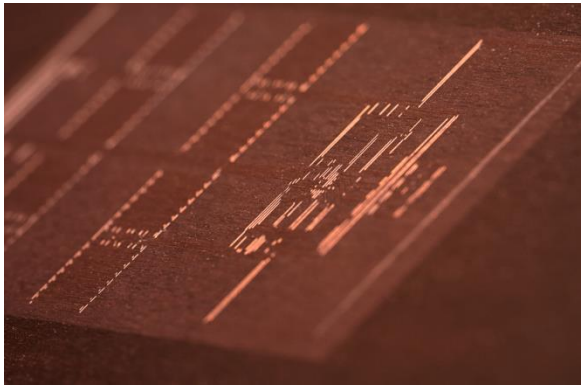
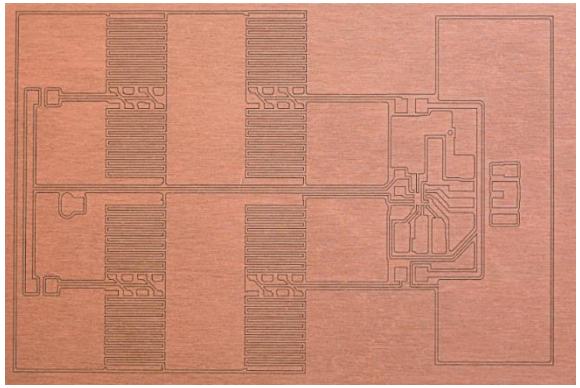
Evaluation of Embedding Process - Laser processing

- Ultra short pulse laser processing of DBC substrate
  - Rapid prototyping and design flexibility
  - Sufficient surface quality for packaging process









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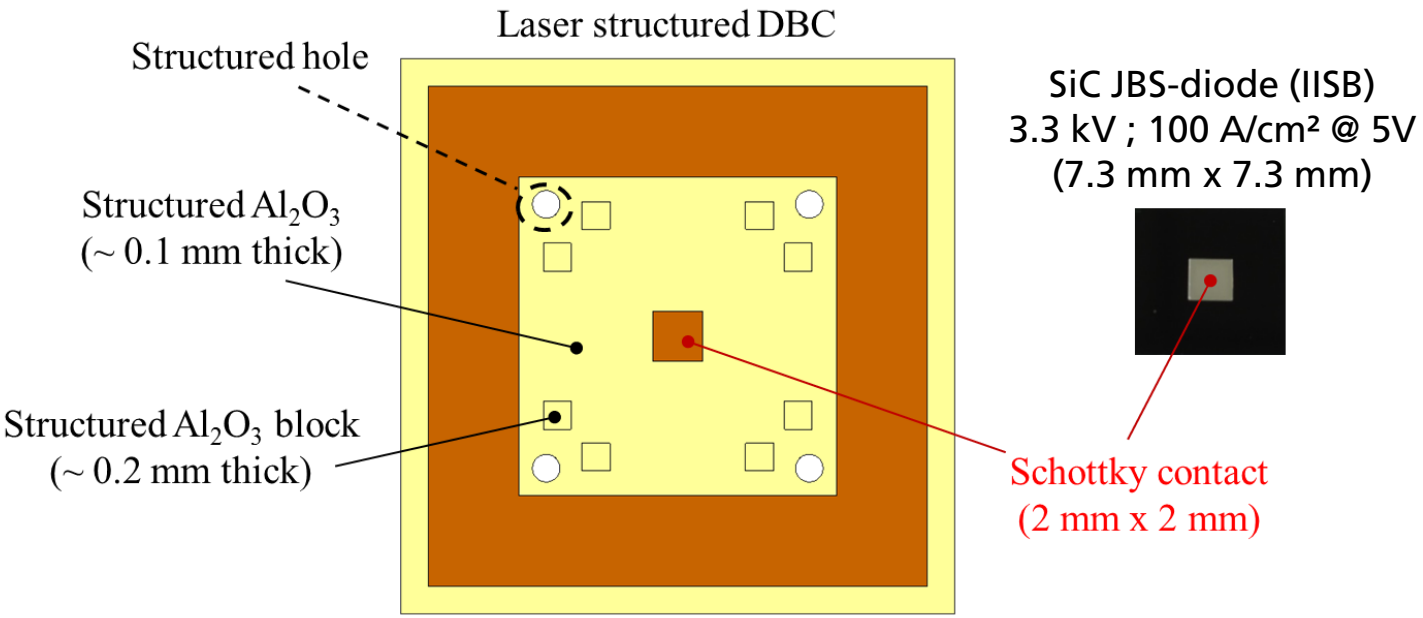
Evaluation of Embedding Process - Laserstructuring of DBC Substrate

- Laser system used
  - Femtosecond laser, 1030 nm (infrared), 800 fs
- Specimen tested
  - DBC substrate, Cu/ Al_2O_3/ Cu (100/ 380/ 100 µm), 20 mm x 20 mm



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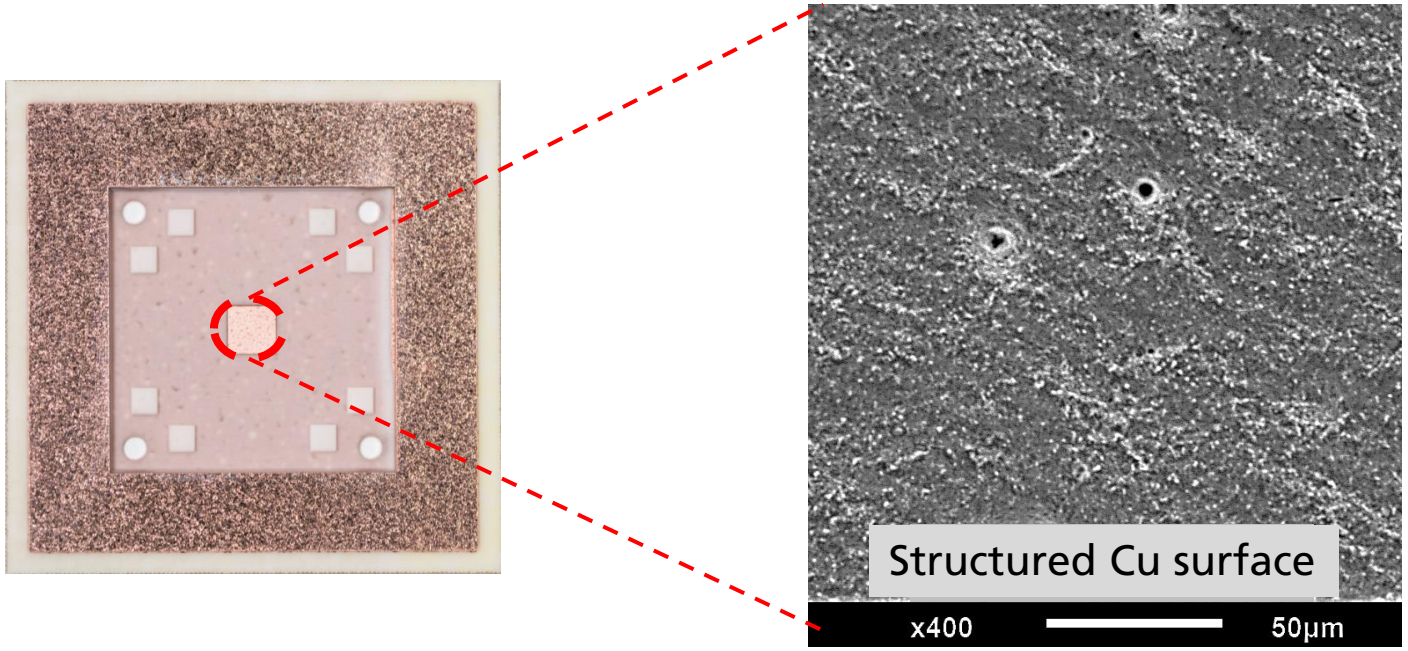
Evaluation of Embedding Process - Laserstructuring of DBC Substrate

- **Femtosecond laser**
- High precision structuring
- No crack occurrences in Al_2O_3 and Cu
- No remained Cu_2O on the surface



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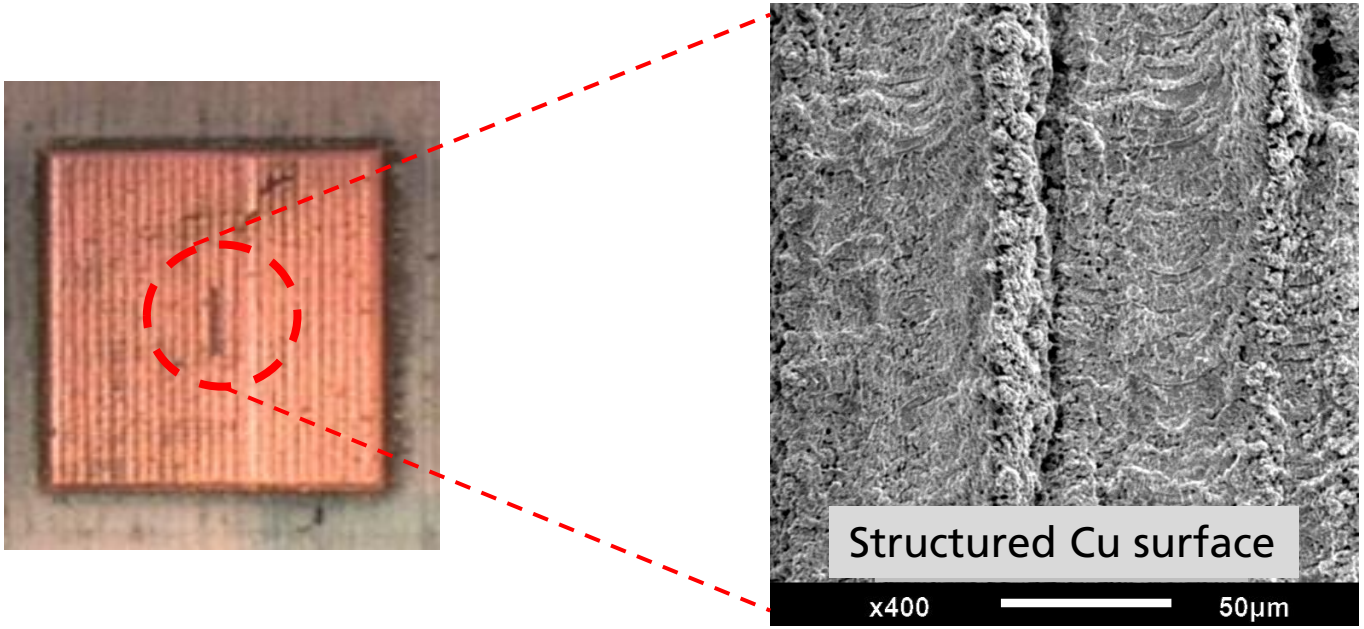
Evaluation of Embedding Process - Laserstructuring of DBC Substrate

- **Nanosecond laser**, 355 nm (UV)
- Effective structuring of Al_2O_3 and Cu
- Crack occurrences in Cu
- Remained Cu_2O on the surface



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Evaluation of Embedding Process - Laserstructuring of DBC Substrate

- Comparison of solder quality on laser structured DBC substrate
- **Solder preform** in structured Cu layer, soldered at 240 °C, nitrogen atmosphere
- Nanosecond laser → bad wetting behavior, insufficient surface quality of Cu
- Femtosecond laser → good wetting behavior, smooth surface of Cu

Structured DBC, nanosecond laser

Solder preform

Structured DBC, femtosecond laser

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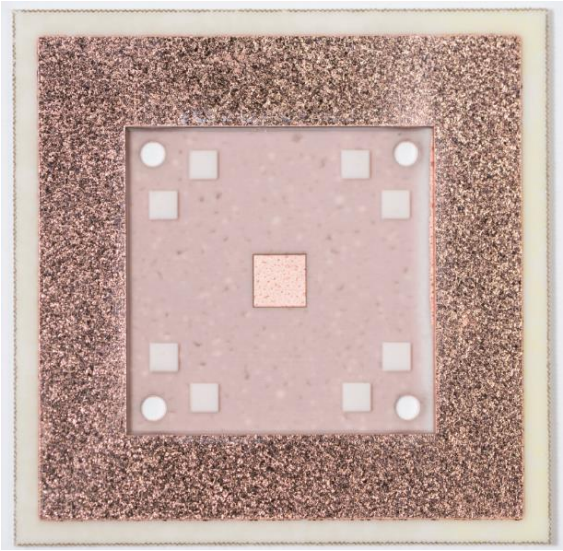
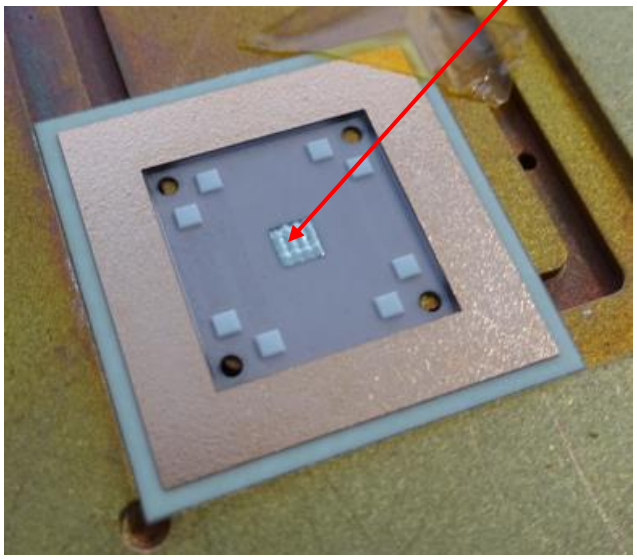
Evaluation of Embedding Process - Die Attach Process of Power Semiconductor

- Jet printing of Ag paste in laser structured DBC
  - Dot line thickness ~ 80 µm per layer
  - Drying process at 80°C for 60 min
  - Sinter layer thickness reduced by 50% after drying





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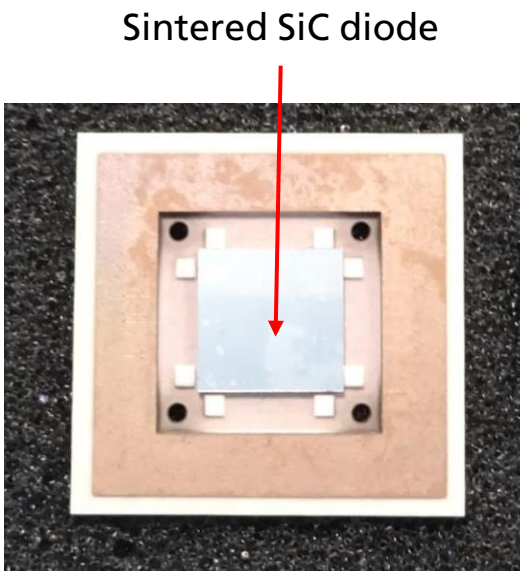
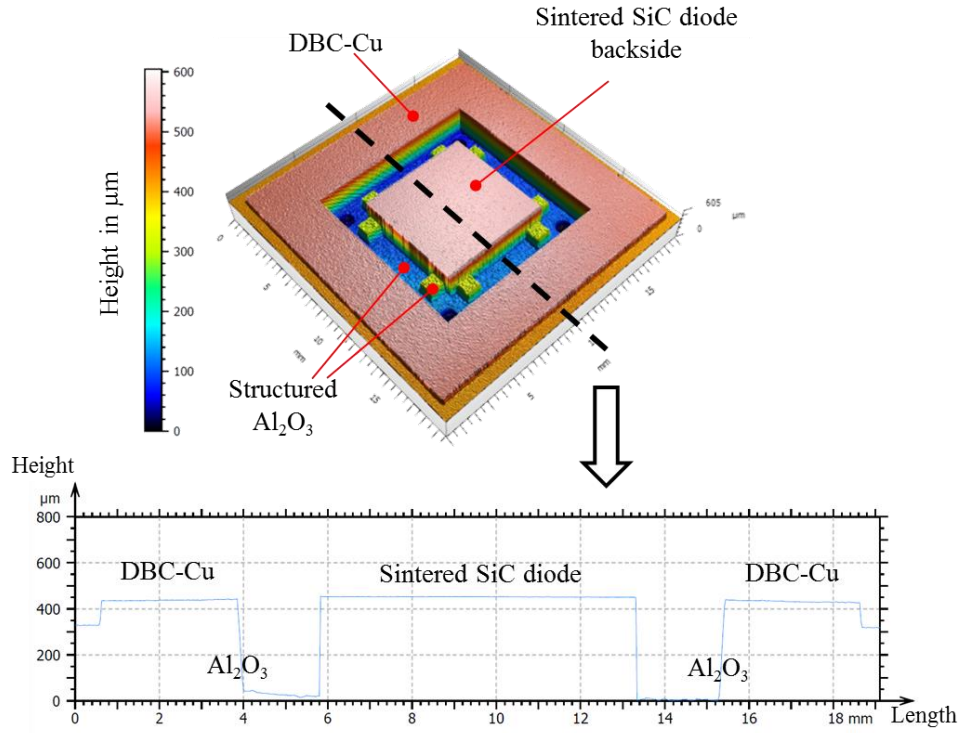
Evaluation of Embedding Process - Die Attach Process of Power Semiconductor

- SiC JBS-diode **sintered** onto structured DBC substrate
- Pressure-assisted sintering
  - 250°C sinter temperature, 5 min sinter time, 4 MPa sinter pressure





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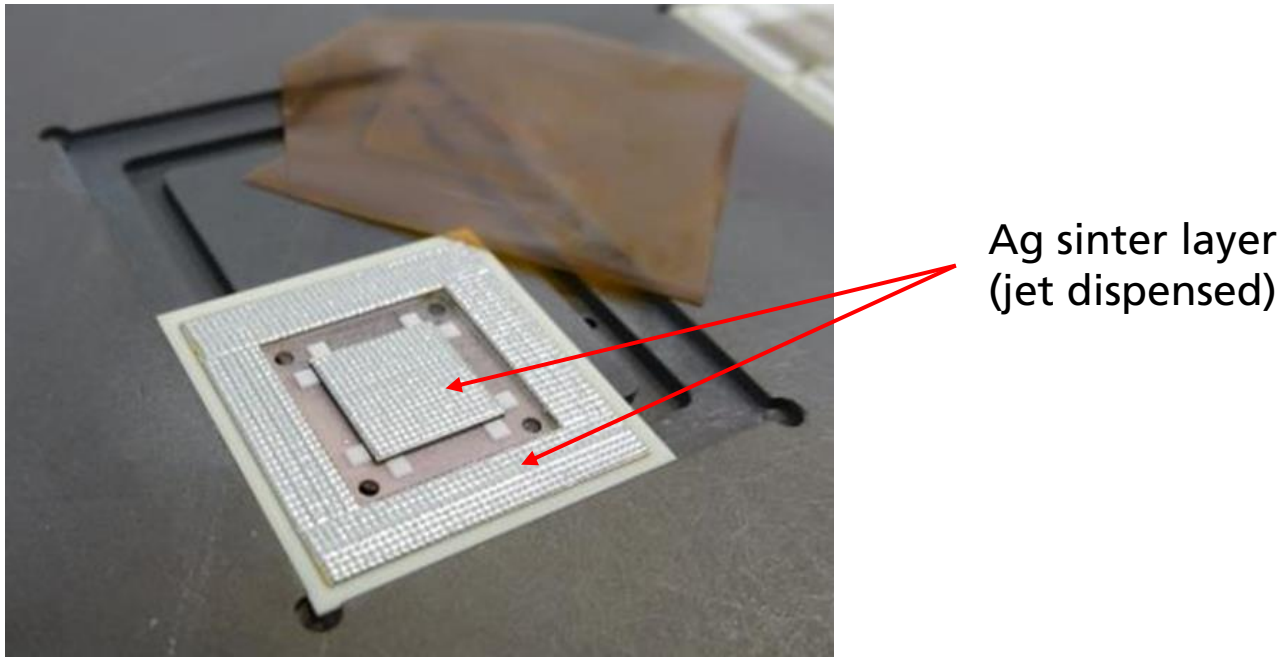
Evaluation of Embedding Process - Die Attach Process of Power Semiconductor

- Sealing of the package with a Cu cover
- Pressure-assisted sintering
  - 250°C sinter temperature, 5 min sinter time, 4 MPa sinter pressure



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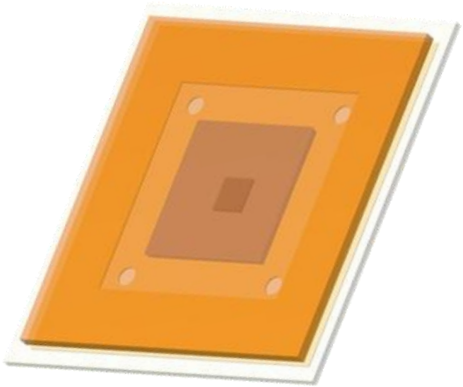
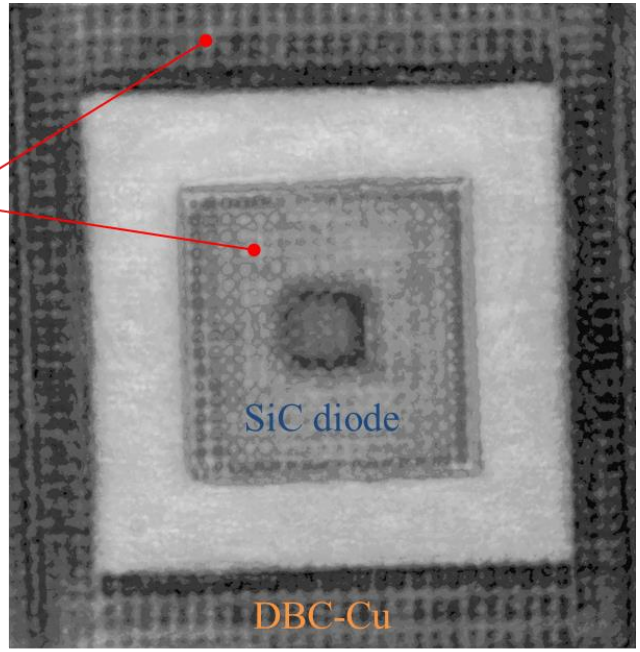
Evaluation of Embedding Process - Die Attach Process of Power Semiconductor

- SiC JBS-diode **sintered** onto structured DBC substrate
- Even distribution of sinter layer after sintering
- No chip crack detected





Scanning acoustic microscopy analysis

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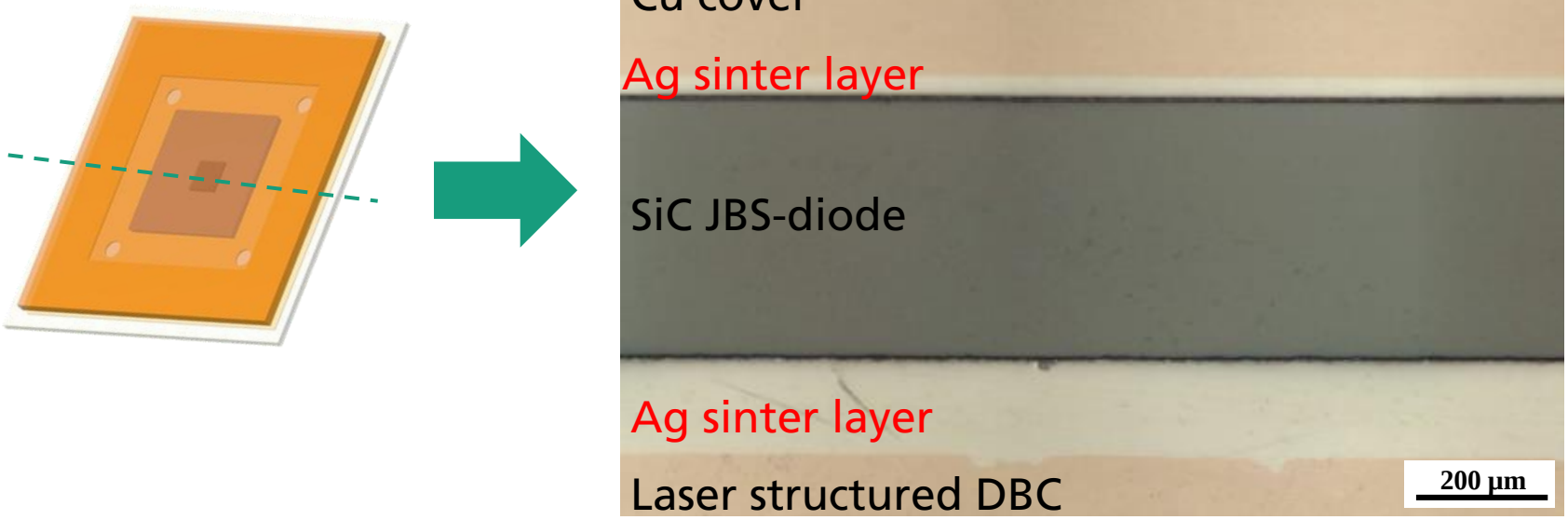
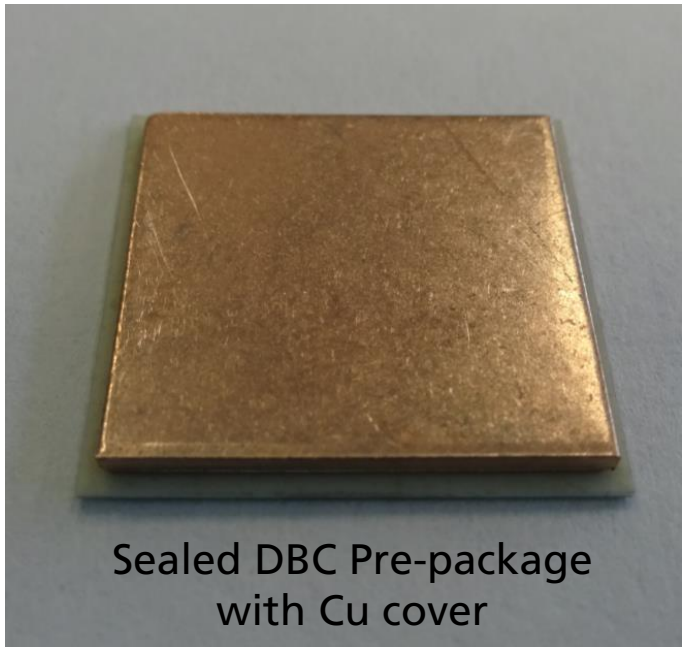
Evaluation of Embedding Process - Die Attach Process of Power Semiconductor

- Cross section of SiC JBS-diode embedded DBC substrate by **Ag sintering**
- No critical voids and cracks in the sinter bond line
- Good joining quality of Cu, Ag paste and chip metallization

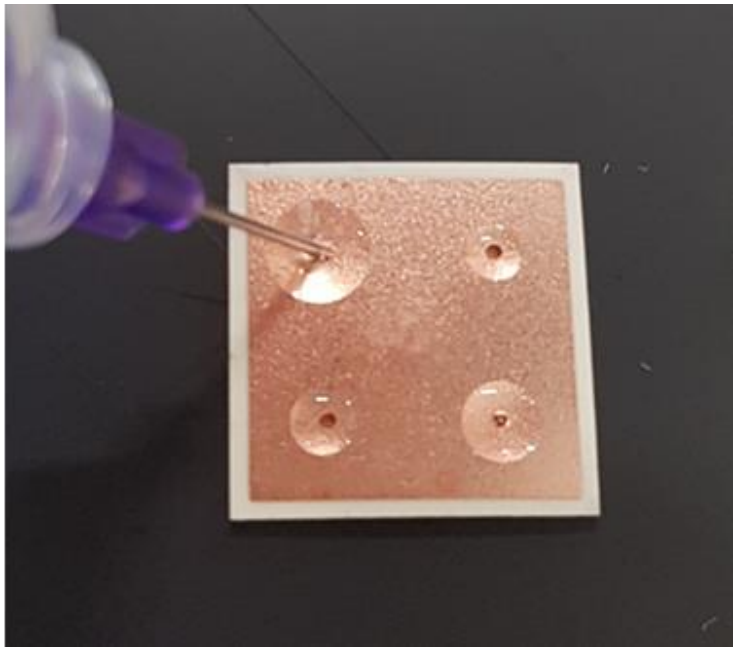


Evaluation of Embedding Process - Potting Process of Embedded DBC Package

- Dispensing of potting system inside DBC package
  - High temperature capability up to 250 °C (silicon gel)
- Filling DBC package through lasered holes



Sealed DBC Pre-package with Cu cover



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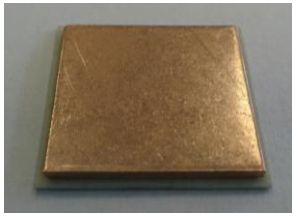
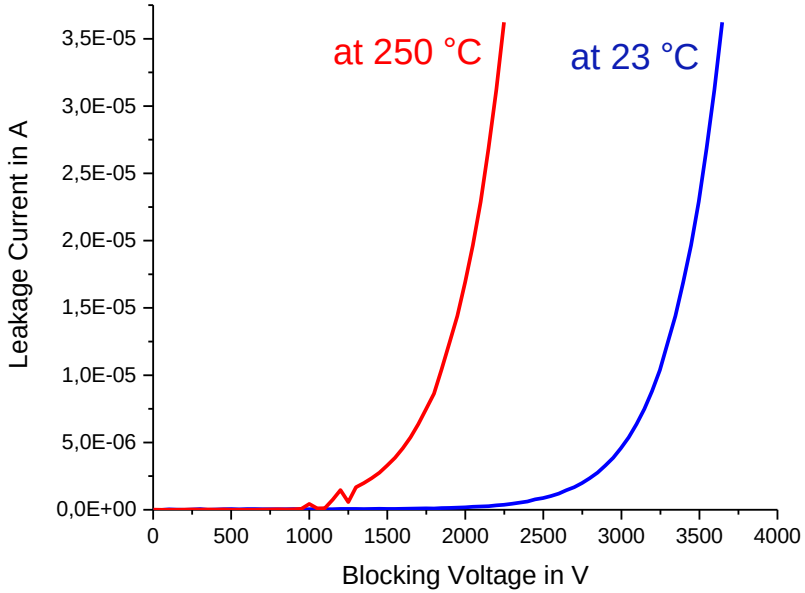
Test and Result

- Sealing and measuring of embedded package with Cu cover
- Current and blocking characteristics correspond to values from data sheet
  - Diode turn on @ ~1.2 V, blocking voltage up to 3.3 kV
- Pre-package showed no failure up to 250°C during measurement





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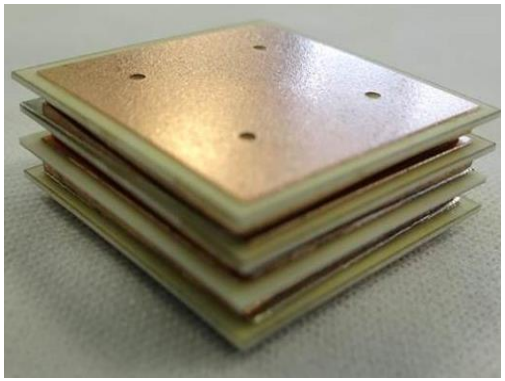
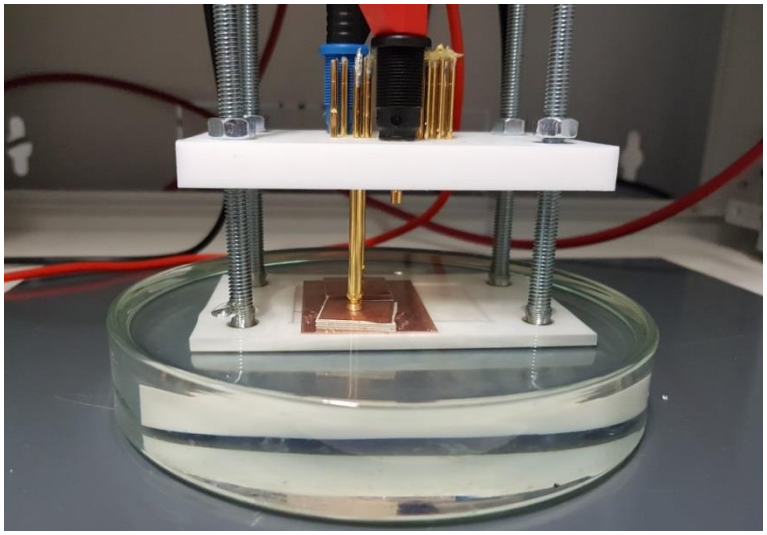
Test and Result

- **Stacking** of single embedded SiC diode pre-packages
- Pre-packages connected in series
- Total package thickness of 5.4 mm
- Blocking voltage measured up to 12.5 kV





Technological feasibility confirmed

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Summary and Conclusion

- **Ceramic embedding** seems promising for **WBG** and high temperature applications above **300 °C**
- **Laser process** can be rated as potential application for ceramic embedding
  - **Femtosecond laser** for high-precision material ablation → high embedding quality (chip soldering and sintering)
- **Soldering** and **silver sintering** suitable for chip embedding process
- **Electrical functionality** of DBC embedded package (**up to 250°C**; **12.5 kV**) tested and validated
- DBC embedded package compact, robust and easy to use for system users
- Long-term tests, lifetime and reliability still under investigation

THANK YOU FOR YOUR ATTENTION!

Fraunhofer IISB

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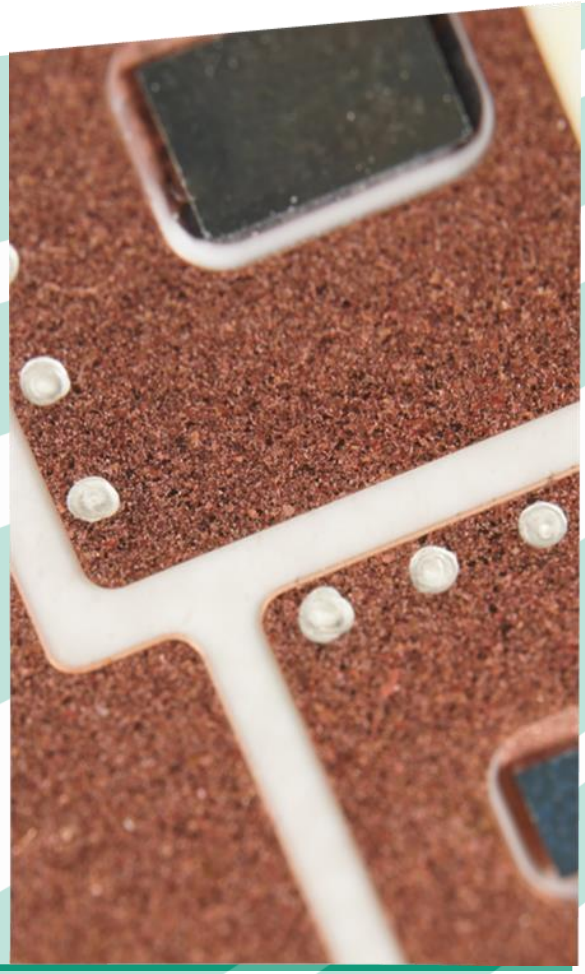
Contact



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