Automated Virtual Prototyping for Fastest Time-to-Market of New System in Package Solutions

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Abstract—A modular system of parametric FE models is created using ANSYS parametric design language (APDL) for automated virtual prototyping of current and future System-in-Package (SiP) solutions based on fan-out-wafer-level-packaging (FOWLP) technologies. The principles of the hierarchical architecture are described and instructive examples are given for all levels, i.e., from the part models to the four demonstrator packages. Further, the results of first simulations addressing the typical load case of temperature cycling between -40°C and 125°C clearly demonstrate the validity of the approach as they agree to the experimental finding. The system of models is now applicable to a large variety of future SiP products based on FOWLP. It will allow virtual prototyping, i.e., replace time consuming experimental tests during the product definition phase.

Keywords—System-in-Package (SiP), fan-out wafer level packaging (FOWLP), Parametric FE modelling, thermal cycling (TC), Package on Package (PoP)

I. INTRODUCTION

The internet of things (IoT) and many applications in the fields of automotive, industrial and personal electronics will require innovative electronic systems offering a variety of new functionalities within shortest time-to-market yet with high reliability, functional safety and at costs low enough to be acceptable for the mass market. System-in-package (SiP) solutions based on fan-out-wafer-level-packaging (FOWLP) technologies are able to meet these technical requirements and performance expectations [1]. The new miniaturized systems will integrate different active and passive components made of semiconductor and ceramic materials by metal interconnects within a set of various organic materials in the most compact way. All the materials involved have their specific and very diverse properties regarding thermal expansion and stiffness. Hence, reactions like warpage and thermo-mechanical stresses will occur any time the temperature changes in fabrication, test and operation, which affects the yield in production and reliability in the field use. Therefore, these risks must already be assessed during the development of the new SiP products so that design, material selection and process conditions can be optimized aiming at high yield and all reliability requirements met. Unfortunately, the physical assessments are very costly with the necessary reliability tests being particularly time consuming. Virtual prototyping based on numerical models offer an attractive alternative [2,3]. Finite element simulation allows the analysis of the thermo-mechanical situation during fabrication and service within a few hours while physical tests would rather take several months. However, the lead processes, setting up the required geometric models and obtaining all the essential material data, may easily eat up most of the time advantage or even make the development longer because of the additional need for a validation of the virtual results before practical decisions can be casted based on them.

For virtual prototyping, many attempts have been made to create fully parametric FE model for one component but much less work has been reported for a system with different types of component variations [3-5]. The paper introduces a modular approach to a system of models that is capable of covering a full portfolio of current and future SiP products based on FOWLP. All level of packaging components: die, mold, redistribution layers (RDL), solder balls, vias, passives and board are integrated in a combined set of models. It is based upon a clear hierarchical architecture defining families of similar SiP structures (Fig.1) divided into several levels of building blocks, for which a library of parametric models is established using ANSYS™ [6] and comprehensively pre-calibrated. Those part models can be assembled very flexibly to represent not only the full spectrum of the current but also many of the future SiP products. The assemblage of the part models is controlled by another parametric script and so is the execution of the simulation runs and a first level of result evaluation. This way, the complete virtual assessment, i.e., the full DoE (Design-of-Experiments) assessment can be performed automatically.

Fig. 1. Families of similarly complex SiP modules [7].

The paper describes the principles of the hierarchical architecture stepwise using flowchart, presents instructive examples
of the basic building blocks. The approach is demonstrated on four real application packages and it shows first results of thermo-mechanical simulation. Also, the agreement between experimental test and simulation result for one package clearly demonstrate the validity of the approach, which is also applicable to many other multi-scale packaging and integration technologies in electronic components and systems.

II. PARAMETRIC FE MODELLING

A. The strategy for parametric FE modelling

In order to have a system of parametric FE models of various FOWLP based SiP products, the packages with similar structures from Amkor’s FOWLP integration roadmap have been selected and divided into 3 families depending on the package complexities as shown in the Fig.1 [7]. Family 1 includes the simplest structure with one die, RDL below chip, mold compound and solder balls. In addition to the basic component of family 1, family 2 has more complex structure like two or three dies, RDL on top of chip and TPV (Thru-Package-Vias). Family 3 has most complex structures like passive components, package on package (PoP)/3D stacks and solder balls between two packages in addition to the components from previous two families.

Initial strategic considerations:

• Separate macros for different package families with the possibilities of combination of macros from different package families.

• Separate part models library for substrate, solder ball, vias and passive components.

• Use of line elements for vias.

• Separate material library and smeared material properties for RDL and substrate.

• Contact elements in case of dissimilar mesh.

B. The flowchart for parametric FE modelling

ANSYS APDL macros for creating the FE models have been represented as main macros, submacros and sub-submacros in the flowchart in Fig.2. The sub-submacros are the macros files called by the submacros. Similarly, the submacros are the macro files called by the main macros. The set of macros start with defining the geometry parameters, material definitions, element definitions and real constants for contact elements. For each package, unique geometry parameter file is necessary which is called by the main macros. Then the program called submacros which is the main modeling macros with 5 steps.

• Step 1. This step creates parametric areas, subtract areas from each other retaining the given area numbers, creates areas mesh, extrudes areas to create volumetric mesh and assigns material properties to volume elements (Fig.3). Four parameters per area are necessary, i.e., area dimensions and distances from reference position. By subtraction of areas, it can create complex area shape (top middle in Fig.3) and areas inside area. In case of defining wrong dimensions in geometry parameter file, it can show warning message, e.g., if any areas are overlapping with each other or if any areas are crossing package outer boundaries. Local co-ordinate system at the center of each area is created in order to have easy selection of particular area and volume to assign material properties. Also, an element size parameter is defined to have control over mesh density. Currently, the routine is created for square and rectangular area but it can be extended to circle and some other shapes also. This step gives flexibility to create geometry and FE model for any combination of components like multiple dies, vias and integrated passives for various SiP products.
- Step 2. This step creates FE part models of different types of solder balls, vias and passives by calling different sub-submacros files. Example of FE part models for upper and lower half of the solder ball with PCB are shown in Fig. 4 (a) which can be used for board level reliability simulation. Part models for substrate without solder ball are also created (Fig. 4b) which can be used to fill nonpopulated solder ball region in the solder ball matrix. Solder balls without PCB are required for PoP and first level reliability simulation (Fig. 4c). The parameter is also defined either to include underfill or not. The purpose of dividing the solder ball in upper and lower parts is to have flexibility to choose different types of solder ball configurations, such as solder mask defined or non-solder mask defined pads, at both sides independently and for different level of solder balls in case of PoP. The detailed cross sectional views in Fig. 4 (d) and (e), show mesh of upper and lower parts of solder balls (Fig. 4a, 4c) maintaining the exact node location at the middle of the ball irrespective of ball, pad or UBM (under bump metallization) diameter at both sides. Number of elements and the spacing ratio between elements in solder ball are also parametric in thickness direction to allow fine mesh at the regions of high interest and coarser mesh elsewhere. Furthermore, the routine can be adapted easily to copper pillar bump or some other shapes, too.

![Fig. 4. Example of FE part models for upper and lower half of the solder balls (a) with substrate (b) for nonpopulated solder ball region, (c) without substrate but with underfill, (d) and (e) cross sectional views](a) (b) (c) (d) (e)

- Step 3. Solder ball matrix is created in this step by copying part models from step 2 based on the matrix parameters defined in the geometry parameter file. The routine is such that any combinations of solder ball matrix is possible for given ball pitch. It also fills the nonpopulated solder ball region at any particular location in the matrix. Similar approach of copying the respective preprepared part models can be used for creating vias and passives at desired location.

- Step 4. The remaining package region outside the solder ball matrix region is modeled with or without underfill. With underfill, fully parametric meniscus can also be added in spite of complex parametric element spacing ratio of underfill meshes. Considering that the PCB in the solder ball matrix is already created in previous step, this step creates remaining PCB region in the surrounding of the solder ball matrix region.

- Step 5. Multi Point Constraint (MPC) based contact elements are used between the FE models created in step 2-4 and in step 1 which have mesh dissimilarity. In addition, the standard contact elements are created between solder and solder mask or underfill.

After completing 5 steps using submacros, the main macros will check for the PoP parameter. If the next level package is present, i.e., PoP=1, than the routine will repeat all the 5 steps again with the dimensions of next level: package, die, solder ball matrix and RDL layers defined in the geometry parameter file. If PoP=0, than the boundary conditions are applied based on the defined symmetry condition parameters. Finally, the FE analysis is performed according to the load steps defined in the respective sub-submacro (being fully parametric as well) and the results are extracted up to the level needed as for lifetime prediction. For example, the creep strain energy density accumulated in a steady state thermal cycle averaged across the identified critical plane of that joint, which is seen (by this simulation) to fail first.

### III. APPLICATION OF THE MODULAR SYSTEM OF MODELS

The modular system of parametric FE models has been used to create four demonstrator packages with very different configurations (Fig. 5a). Each of them has specific solder ball size and matrix structure. Package P1 is for a 60 GHz radar sensor. It has the simplest geometry of the four packages: a 12 by 12 solder ball matrix with some nonpopulated solder ball regions. Package P2 is for a silicon photomultiplier with the special feature of TPV at two corners of the package and 12 solder balls. Package P3 is for an automotive inertial sensor with one ASIC and two MEMS devices having various small components and a complex solder ball matrix. Package P4 finally is for a camera module. Its complex PoP configuration comprises a chip scale package on top of the FOWLP. It has 11*11 solder balls at PCB side, 8*10 solder balls between two packages covered with underfill, and 4*20 TPV at the periphery of the FOWLP.

The results of the parametric area definition in step 1 are shown in Fig. 5 (b) for all packages. P3 and P4 can use half symmetric FE models while even a quarter FE model is sufficient for P1. Only P2 requires a full FE model because the TPV are at diagonal corners. The final FE models created fully automatically based on the input parameters by all the steps of
Fig. 5. Demonstrator packages (a) schematic, (b) package areas created using parametric area modeling step, (c) FE models without substrate, (d) FE models with substrate mentioning nodes and (e) warpage at -40°C after 2.5 thermal cycles.

submacros are depicted in Fig. 5 (c) without PCB with the view of solder balls and in Fig. 5 (d) with PCB for all packages. Out of the four packages, only P4 required two loops through the 5 steps because of its PoP configuration.

Besides the large variety of FOWLP packages demonstrated here, the proposed system of models is easily adaptable to create similar sets for many of the fan-out technologies mentioned in [8] such as, eWL-B-PoP (Embedded Wafer Level Ball Grid Array PoP), RCP (Redistributed Chip Package), InFO (Wafer Level Integrated Fan-out), FOPLP (Fan-out Panel Level Packaging), PFO (Panel Fan-Out) package, and also SWIFT-PoP (Silicon Wafer Integrated Fan-out Technology) [9].

IV. SIMULATION

Finite element analyses have been performed in order to investigate the validity of the approach and the system of models. The materials and their constitutive laws used for thermomechanical analysis are listed in Tab. 1. Linear element SOLID185 has been used with full integration element formulation. One parameter has also been defined to add mid-side nodes if quadratic element shall be used. Further, the symmetry boundary conditions and constraints are applied according to quarter, half, or full model, respectively.
TABLE I. COMPONENT MATERIAL AND CONSTITUTIVE LAWS

<table>
<thead>
<tr>
<th>Component material</th>
<th>Constitutive law</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>Linear elastic</td>
</tr>
<tr>
<td>Mold compound</td>
<td>Visco-elastic</td>
</tr>
<tr>
<td>Copper RDL</td>
<td>Elastic-plastic</td>
</tr>
<tr>
<td>FR4</td>
<td>Linear elastic, Orthotropic</td>
</tr>
<tr>
<td>Solder ball</td>
<td>Visco-elastic</td>
</tr>
<tr>
<td>Solder mask</td>
<td>Visco-elastic</td>
</tr>
<tr>
<td>Underfill</td>
<td>Visco-elastic</td>
</tr>
<tr>
<td>Polyimide</td>
<td>Linear elastic</td>
</tr>
<tr>
<td>Glass</td>
<td>Linear elastic</td>
</tr>
</tbody>
</table>

The structure is assumed stress-free at the beginning of mold cure. The time-temperature loading profile is shown in Fig. 6 after cooling from molding temperature to 25°C in 5 min and storage at room temperature for one week. Then, 2.5 temperature cycles (TCs) are simulated from -40°C to 125°C with 20 min per half cycle. The last cycle has been found to represent the steady-state case, i.e., the result parameters have reached the cyclic magnitudes that do not change further in the subsequent TCs.

![Fig. 6. Time-temperature profile for thermomechanical analysis](image)

V. RESULT AND DISCUSSION

The simulated warpage results for the different packages at -40°C after 2.5 thermal cycles can be seen in Fig. 5 (e), where-by the PCB is not shown for clarity reasons. Using two cores of a regular office workstation, the automatic creation of the model and the execution of the full simulation required less than one hour for packages P1 and P2, and 2-4 hours for P3 and P4, respectively. That means, entire case studies for some 12 to 20 DoE legs may well be completed within one day when using powerful multicore workstations. Considering the complexity of the packages and the loading situations, this demonstrates the great potential the virtual prototyping approach offers for a massive reduction in time-to-market for future SiP products.

In small modules, which just accommodate one SiP, the PCBs are showing some convex or smiling warpage during the thermal cycle that is induced by the expansion mismatch between component and PCB. In case of package P1, a concave shape warpage of 25 μm was found caused by the higher shrinkage of passivation layers compared to the mold compound. P2 exhibits 4 μm crying warpage because of the higher shrinkage of PCB compared to the component, which forces the solder ball to contract inward at PCB side. P3 shows a similar behavior with a small warpage of 4 μm. The component is trying to deform in smiling shape due to shrinkage of mold. However, the PCB shrinkage is large compared to that of the component and outbalances the package warpage so that the result is a slightly concave shape of package. P4 has more complex combinations of CTE mismatch between components but overall, it shows crying warpage of 15 μm.

In large modules with many SiP components, the PCB warpage induced by the individual component is widely suppressed due to the stiffness of the surrounding board and the counteracting effects of the neighboring components. Exemplarily, this configuration has also been simulated between -50°C and +150°C for P3. Applying symmetric boundary conditions at the PCB edges, the situation of an array of SiPs on a large module board is modeled restricting PCB warpage. The results of the equivalent creep strain that are accumulated in the solder balls over 2.5 TCs are illustrated in Fig. 7 (a). It shows a maximum strain of 6% which occurs in one of the inner solder balls. This differs from the result obtained for the same SiP when modeled on a small module without symmetric boundary conditions. Then, the maximum strain occurs at the outermost corner balls as usually expected.

![Fig. 7. (a) Accumulated equivalent creep strain in the solder balls and (b) Averaged accumulated creep strain energy density (mJ/mm²) in the result extraction layer (half layer shown left) of the solder balls close at the interface to the chip pad](image)

Continuing the result evaluation, the creep strain energy density, Wcr, which is accumulated within a steady state thermal cycle, is averaged across a 5 μm thick layer of free solder just below UBM (Fig. 7b left). This is the critical plane within the solder joint, along which the fatigue cracks propagate. The averaged Wcr is an established criterion for lifetime prediction according to the Coffin Manson approach [10]:

\[
N_f = C_1 / Wcr^{C_2}
\]

with \(N_f\) denoting the characteristic number of cycle to failure, Wcr being the accumulated creep strain energy density averaged as described before, while \(C_1\) and \(C_2\) are constants.
Fig. 8 shows these results for the component P3 mounted on the large module. In addition to the position of the maximum already seen before, it can now be noticed first that the magnitude of the accumulated energy density per cycle is relatively small, which indicates a high lifetime expectancy for the solder joints of this module. Second, all joints of the inner two lines show magnitudes in a narrow range between 0.19 mJ/mm² and 0.21 mJ/mm² which predicts a very similar lifetime expectancy for the full set of these joints. Third, the outer line shows yet 3x smaller magnitudes (i.e., below 0.08 mJ/mm²). In real tests, these joints should show the least fatigue failures.

Fig. 8. PCB used for practical reliability testing [11] with the simulated sample indicated.

In parallel to the simulations, experimental board level reliability tests have been performed for package P3 mounted on large boards as shown in Fig. 8. It was found that no SiP failed the functional test even after 2000 TCs between -50°C and +150°C [11], which truly corresponds to a high lifetime. Still, the physical failure analysis revealed some fatigue damages at the joints. In particular, (i) cracks in the copper pad metallization and (ii) cracks in the solder were found at the component side of the joints besides some black pad failures, i.e., complete fractures at the solder-pad interface at the PCB side. The latter defect can be avoided by the new PCBs whose pads omit nickel. Typical examples of the fatigue failure modes are seen in Fig. 9 (a). The extension of the solder crack is too small to cause a functional failure. Likewise, the copper pad is cracked at the points of maximum load but well intact along the rest of the perimeter. Otherwise, pad lifts would have been found while Fig. 9 (a) actually shows the copper film being tilted, i.e., the crack is accompanied by a small local delamination, limited to the site of highest loading. In future, this delamination could be avoided by measures like strengthening the interface (e.g., by plasma cleaning before Cu deposition) or decreasing the interface load (e.g., by increasing the Cu film thickness). Then, the solder fatigue cracks would be the only remaining failure mode. Most likely, it will also occur near to those places in the joints, which have now shown the copper cracks. The solder fatigue is unavoidable. However, the current test results indicate that functional solder failures, which require a complete fatigue fracture, will only happen after much more TCs. That means, the modules under investigation really have a high lifetime expectancy already. This is in good alignment to the simulations results.

In Fig. 9 (b), those joints are highlighted, in which onsets of fatigue damages were found by the physical failure analysis after 2000 TCs. The analysis investigated the top half of the component by successive cross sectioning. The pattern of the highlighted joints shows that fatigue effects are not only focusing on joints in the inner lines but also occur in the outer line. However, the outer line of this particular sample was affected by black pad defects at three positions, which may have led to higher stresses in the neighboring joints. Since this defect is no longer relevant, the conclusion on the fatigue life in the outer line will be subject to further tests.

Fig. 9. (a) Fatigue failure modes (i) copper fracture, (ii) solder fatigue and (b) Location of the solder fatigue ‘F’ and copper failure denoted by half circle with red and yellow color respectively in the half symmetric solder ball matrix. The location of the copper fracture is denoted by the direction of the arrow [11].

In summary, the experimental observations are in good agreement to the simulation findings: (i) The magnitude of fatigue stress is low so that the lifetime expectancy is high for the solder joints. (ii) There is little difference in the stress level among the inner joints.

VI. CONCLUSIONS

The paper focuses on the creation of modular system of parametric FE models, which is very essential for automated virtual prototyping of current and future SiP solutions. The contributions are summarize as follows:

1) Fast generation of parametric FE model for FOWLP based SiP products using library of part models for sol-
ter ball, vias and passives. The flexibility of approach is demonstrated by creating the FE models for four very different FOWLP devices.

(2) The thermomechanical analysis results have proven the feasibility of the approach: Simulating a typical complex load scenario, realistic results have been obtained within the reasonably low computation time of a few hours, which are in good agreement to experimental findings.

(3) From this study, it has become clear that even complex FOWLP packaging structures can be assessed fully automatically using this method. Modifying the parameters between the simulation runs, complete DoE based design studies can be executed as batch job that directly yields the optimum package without further manual involvement. This will be a powerful tool for minimizing the time to market of new IoT products.

ACKNOWLEDGMENT

Authors would like to thank Heikki Kuisma for providing test results. This work was performed within the project EuroPAT-MASiP which has received funding from the Electronic Component Systems for European Leadership Joint Undertaking under grant agreement No 737497. This Joint Undertaking receives support from the European Union’s Horizon 2020 research and innovation programme and Portugal, Austria, Netherlands, Finland, Germany, Hungary, Ireland, France, and Sweden. Also, part of this work was performed under the Federal Cluster of Excellence EXC 1075 “MERGE Technologies for Multifunctional Lightweight Structures” supported by German Research Foundation (DFG).

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