Introduction to Design, Test and Thermal Management of 3D Integrated Circuits

When we started to work on the first volume of Wiley's *Handbook of 3D Integration* in 2007, we intended these volumes to be an encompassing treatise on 3D integration – a new technical field of semiconductor technology and electronic systems packaging. This ambitious goal of Wiley-VCH and the editors was achieved with the help of Christopher Bower who served as co-editor of the first two volumes. We chose to initially focus on 3D-IC process technology, such as fabrication of through-silicon vias (TSVs) and wafer thinning and temporary and permanent bonding technologies.

Volume 3, released in 2014, continued coverage of new developments in process technology as future production was still on the horizon. We felt that volume 4 should be strongly dedicated to design, test, and thermal management of 3D-IC.

Since the mid-2010s, 3D integration and silicon interposer technologies have become well-accepted approaches for fabrication of high-performance memory-enhanced products, explicitly stacked DRAMs, which are currently in high-volume production at both Samsung and Hynix. Samsung started the production of “3D Stacked DDR4 DRAM” with via-middle technology in August 2015. So finally, after more than three decades of R&D, 3D-IC integration has arrived in the electronic industry!

Another application that has gone into volume production is CMOS image sensors (CIS). In 2017 Sony announced the industry's first three-layer stacked CIS: a 90 nm generation back-illuminated CIS top chip, 30 nm generation DRAM middle chip, and 40 nm generation image signal processor (ISP) bottom chip for smartphone cameras. All of the other major CIS manufacturers are following suite.

On the other hand, there have also been drawbacks. Most significantly, 3D memory-on-logic applications, widely predicted by many sources, have been postponed several times and will be still not introduced in 2019. While the major issue, of course, is the high cost of 3D-IC manufacturing, another reason for postponing the introduction has been the success of TSV interposer technology. These, also called “2.5D” concepts, enable a high interconnection density between side-by-side devices, through TSV and redistribution layers, without introducing “true 3D integration” (i.e., TSV interconnects through stacked active devices). Considering TSV interposer technologies as well, the market has exceeded US$ 4 billion in 2016, and the forecast for TSV-based products for the different applications appears to be very promising (Figure 1).

1 Revenue forecast TSV-based products by application.

Source: 3D TSV and 2.5D Business Update – Market and Technology Trends Report, Yole Développement, 2017.

One of the most promising silicon interposer approaches has been TSMC's CoWoS (Chip-on-Wafer-on-Substrate). The CoWoS technology has been in production since 2013 with one of the first applications being Xilinx's FPGAs. The CoWoS concept opened a new track in the roadmap toward 3D-IC production, such as the Xilinx Virtex-7 product H580T, labeled the “first heterogeneous 3D FPGA”.

In addition to the above developments, industrial consortia have been targeting 3D integration as a key technology for heterogeneous IC/MEMS products, demanding smart system integration rather than extreme high interconnect densities (as early as already established in 2013, the European e-BRAINS platform). Heterogeneous integration technologies are being developed for functional diversification systems, for example, integration of CMOS with other devices, such as analog/RF, solid-state lighting, HV power, passives, sensors/actuators, chemical and biological sensors, and biomedical devices. This heterogeneous integration started with system-in-packaging technology and is expected to evolve into 3D heterogeneous integration. Many R&D activities worldwide are focusing on heterogeneous integration for novel functionalities. Corresponding 3D integration technologies are in evaluation at several companies, research institutions, and industrial-driven research consortia.

Recently, three new relevant international roadmap initiatives have started, highlighting heterogeneous 3D integration as a key element: the International Roadmap for Devices and Systems (IRDS), as follow-up of ITRS, directed by Paolo Gargini (IEEE SSCS, a.o.); the Heterogeneous Integration Roadmap (HIR), initiatively directed by William Chen (Semi, IEEE EPS a.o.); and furthermore NanoElectronics Roadmap for Europe: Identification and Dissemination (NEREID) (funded by the European Commission). Including as well Sensor and MEMS/IC applications, a main subject of HIS and NEREID is clearly on heterogeneous systems. While targeting more on computing applications, the IRDS predicts an area of so-called 3D power scaling with transition to vertical device structures and heterogeneous integration to become the key technology driver in the years 2025–2040.

To summarize, dedicated 3D integration technologies are today in a ramp-up phase toward high volume production. Nevertheless, there is still a huge amount of related problems, e.g. thermal issues, design and test issues, materials optimization, robustness of the processes, thermomechanical reliability of the systems, and last but not the least high production costs, which can only be solved by significant development efforts.

For this volume, we invited Paul D. Franzon (NCSU) for “Design,” Erik Jan Marinissen (IMEC) for “Test,” and Muhannad S. Bakir (Georgia Institute of Technology) for “Thermal Management” to serve as co-editors. They succeeded in assembling excellent contributions from both academic and industrial practitioners in these three key areas of interest. The book is organized into three corresponding parts:

- **Part I: Design**

  Paul D. Franzon (editor)

  Contributions from Fraunhofer, Georgia Institute of Technology, IMEC, Kaiserslautern University, Kobe University, NCSU, and TSMC

- **Part II: Test**

  Erik Jan Marinissen (editor)

  Contributions from ARM, Cadence Design Systems, Duke University, FormFactor, Google, IMEC, NTHU, Synopsys, TSMC, and TU Delft

- **Part III: Thermal Management**

Muhannad S. Bakir (editor)

Contributions from Georgia Institute of Technology, IBM, IMEC

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