Abstract—Continuous downscaling of integrated circuits has reached a bottleneck. Technologies such as system in a package, multi-chip module and integration of chips on an active or passive interposer can further improve the system performance. Bunch of wires interface standard was recently introduced for chip to chip short interfaces within a package. This standard required both terminated and unterminated driver topologies for different data rates and interconnect lengths. This paper presents a first ever reported transmitter implementation of this interface.

Unterminated and terminated impedance controlled drivers with feedback calibration enable transmitter power optimization for a given interconnect based on the respective signal integrity at the receiver side. Results show that this transmitter can support both low and high speed low power communication between chips for interconnects up to 11 mm length with energy consumption of 0.34 pJ/bit at maximum data rate of 13 Gb/s. The transmitter is designed and taped out in 22 nm FDSOI technology node.

Index Terms—Bunch of wires, co-design, interconnect, multi-chip communication, transmitter.

I. INTRODUCTION

For high speed signalling on printed circuit boards (PCB) and backplane cards, techniques such as pulse amplitude modulation (PAM4) are getting popular. Chang and coworkers presented an 80 Gb/s PAM4 transmitter which is impractical for short interfaces [1]. Poulton et al. introduced a ground referenced signalling technique for 25 Gb/s signalling in packages [2]. This supported communication on an interconnect only up to 10 mm. Carusone et al. demonstrated a parallel interface design for chip to chip communication on interposer but only for length up to 4 mm with maximum 20 Gb/s per wire [3]. Active interposer based 2.5D implementation of multi-chip system was shown by Vivet et al. [4]. Extremely short chip-to-chip interconnects were kept purely passive while longer interconnects were enabled by usage of CMOS repeater buffers in the active interposer.

Specifications given in the bunch of wires (BOW) interface proposal require transmitter physical interface (PHY) support for both unterminated and terminated signalling [5]. Lengths up to 10 mm and 2-8 Gb/s data rate should be supported by unterminated signalling. Terminated signalling should support the similar length range for data rates in the range of 4-16 Gb/s. A critical requirement is the availability of control in the interface for impedance calibration in terminated driver. Similarly, the drive strength control in unterminated signalling could help save power for short interconnects. This is required to optimize to PHY energy consumption while enabling flexibility in the interconnect routing on interposer or package.

This work presents a generic interface which can be easily transferred from one technology node to another. It presents the library for critical blocks needed in short interfaces. Unterminated and terminated driver (source series terminated SST) along with pre-driver for drive strength control and impedance matching are designed. The complete transmitter is designed from schematic to layout level in 22 nm FDSOI technology and taped out.

Section II describes the complete transmitter architecture and describes the individual blocks in detail. Section III shows the simulation results of the transmitter at different speeds on different interconnects. Finally, Conclusion section IV summarizes the work and concludes the paper.

II. TRANSMITTER

The transmitter and test system architecture are shown in Figure 1. It consists of a central clock management unit (CMU) with a clock generator and distribution network for complete PHY and test system. Dual phase clock is generated to drive the blocks using high speed C^2MOS logic architecture [6]. The clock is distributed on chip through 3-stage fanout of 4 (FO4) buffers for driving the load consisting of data generator flip-flops and multiplexers. Pseudorandom PRBS-7 data is generated at the system clock rate for testing the transmitter outputs. For terminated drivers, data is multiplexed using 2:1 multiplexers. Half rate and double data rate signals are then sent to the respective unterminated and terminated pre-drivers and drivers for transmitting the signal out of the chip. Each block is described in detail below.
A. Predriver and Driver

For chip-to-chip interfaces, the energy consumption of the transmitter can be reduced by decreasing the capacitive load at the pad. For 60 µm medium diagonal octagonal pad with top three metal layers, the extracted capacitance is 40 fF. Furthermore, the driver can be placed right beneath the output signal high frequency pad to reduce the wiring capacitance and also increase the bandwidth density of the transmitter. For 13 Gb/s transmitter with 0.1 mm signal pad pitch, bandwidth density of 1.3 Tbps/mm² can be achieved. For unterminated driver, the pre-driver consists of 3 stage fanout of 3 (FO3) inverting buffers while the driver consists of a single large inverting buffer to drive the pad capacitance. The size of the driver inverter stages could be changed in order to tackle with different interconnect losses and different pad capacitances in older technology nodes. For the terminated driver, pre-driver produces pull up and pull down Enable signals for the driver pull up and pull down slices. Due to impedance matching requirements of the driver, size of pull up and pull down transistors must be changed.

The schematic for terminated driver topology in this work is shown in Figure 2, where pull up and pull down pre-driver signals enable or disable the 1-2-4-8× sized transistors based on the calibration control signals. The f×2 transistors are always on depicting the minimum possible drive strength setting. All enabled transistors in the driver operate in the linear or triode region so that their drain-source impedance is defined by the current and voltage relationship across the drain and source terminals. If transistors of the driver enter into saturation region even for a short duration of the data bit-stream then followed by a selector run at half rate (clkₚₙ). Chang et al. showed that even latch-less topology can be used to multiplex the two data streams [7]. But that is only possible with 4-phase clocks and is shown to work up to only 5 Gbps full rate (Dₚₙ). This work does not

![Fig. 2. Terminated driver schematic](image)

B. Driver Calibration

In order to calibrate the drive strength of unterminated drivers for different interconnect lengths and widths with different losses, a feedback topology with pattern checker could be used as shown in Figure 3. The periodic steady-state (PSS) data is sent on the forwarded clock channels with driver similar to data driver and similar drive strength setting. The periodic steady state reference voltage $V_{ref}$ extracted at the receiver end is used to slice the incoming test pattern 1110101000 which includes long and short 1 and 0 bits. Until a certain given number of patterns are detected at the pattern checker in receiver, the size of the drivers is incremented by a calibcounter block in the transmitter. Due to this feedback topology, the interconnect variations are automatically taken into account along with any process and temperature variations at the receiver or transmitter end.

For terminated drivers, the impedance calibration is also adjusted in a similar manner using a pattern checker at receiver end but $V_{ref}$ is not extracted from clock inputs. Instead, a constant reference voltage $vdda/4$ is used. The calibration bits are incremented until the pattern matches are found. This tuning mechanism has the advantage that it shall start the link with always minimum drive strength and only increment it until the link achieves minimum possible signal quality. Thus, feedback tuning circuitry is necessary for interconnect and driver co-design optimization.

C. 2:1 Mux

Traditional multiplexers have 5 latch architecture where one bit-stream is latched through three latches and other bit-stream through two latches then followed by a selector run at half clock rate (clkₚₙ). Chang et al. showed that even latch-less topology can be used to multiplex the two data streams [7]. But that is only possible with 4-phase clocks and is shown to work up to only 5 Gbps full rate (Dₚₙ).
use 5 latches as in traditional architectures and also avoids complete latch-less topology due to speed requirements. The 2:1 Mux shown in Figure 4 uses a single latch topology which works up to 13 Gb/s $D_{fr}$. The single latch 2:1 Mux in this transmitter is shown in Figure 5, which is based on C$^2$MOS topology and requires complementary clocks.

D. Clock Management Unit (CMU) and Test Data

A two-phase complementary clock for the system is generated by a 3-stage CMOS inverter based ring oscillator. Instead of placing metal-on-metal or MOS capacitors at the nodes of the ring oscillator, longer channel length transistors instead of 20 nm are used. Since CMOS ring oscillators are very sensitive to power supply noise, an on-chip voltage regulator could be used. In this test system, oscillator power supply is separate from the rest of system to avoid the supply noise. By changing the supply voltage, clock rate can be changed to meet the required bunch of wire interface clock rate. In order to reduce the phase and duty cycle variation between the two clock phases, complementary small inverters are placed at the three nodes of the ring oscillator. The simulated phase noise for RCC extracted ring oscillator is shown in Figure 6.

For chip to chip communication in packages and on interposer, chips can be working at a high rate internal clock. In order to fulfill this requirement, this work designs a PRBS-7 parallel data generator instead of a slow shift register based architecture. In order to run the PRBS-7 at high clock rates, the flip-flops and XOR cells must be fast enough. C$^2$MOS architecture uses two clock phases and is very suitable for high speed digital structures [6]. The width of transistors is chosen to be 0.75 μm with minimum possible 20 nm length.

III. Simulation Results

Total area consumed by the transmitter including an oscillator, data generator, multiplexer, and driver is 115×40 μm which is ideal for placing these transmitter blocks in 100 μm pitch pads. The top view of transmitter layout is shown in Figure 7.

In order to simulate the transmitter and evaluate its performance, s-parameters are measured and simulated for an organic substrate package channel. The length of the measured package interconnect is 3.8 mm. For longer interconnects, the s-parameters can be cascaded together. The measured to simulated s-parameter comparison is shown in Figure 8. Measured line is 10 μm wide with spacing of 10 μm from the ground lines on both sides.

The extracted capacitance of the pad along with wiring capacitance of the terminated driver is around 70 fF. Similarly expected receiver chip pad capacitance is assumed to be about 70 fF. The receiver is assumed to be 50 Ω terminated to ground for terminated signalling. It is important to evaluate the transmitter termination performance for 15-20% far end receiver termination mismatch. This relaxes the receiver termination.
Fig. 8. Measured and simulated s-parameters of 3.8 mm organic interconnect circuitry and improves the signal integrity. For 1 ns delay transmission line with 50 Ω impedance, received signal with 20% mismatch (i.e. 40 Ω) receiver termination is shown in Figure 9a. The reflections in eye diagram and small voltage swing depict the high output impedance of the driver. With full drive strength of SST using the calibration bits in pre-driver, output is shown in Figure 9b. It can be seen that with more drive strength causing the driver output impedance to decrease, reflections have been removed from output and the output swing is increased. By extracting the layout of the transmitter, maximum clock generation is up to 6.66 GHz at 1 V supply, thus limiting the transmitter to 13 Gb/s data rate. For SST terminated driver, maximum possible 13.3 Gb/s and 9.16 Gb/s data rate outputs are shown for 11.4 mm long interconnect in Figure 9c and 9d. For 13.3 Gb/s simulation, some lines show charge sharing problems in previous multiplexer stage. This problem limits the maximum data rate achievable with this architecture to 13 Gb/s.

For unterminated signalling mode, this work achieves 5 Gb/s up to 4 mm long organic interconnects and higher data rate for shorter interconnects. The eye diagrams for 70 Ω load with and without interconnect are shown in Figure 10.

Oscillator consumes 200 µA current at 6.66 GHz with 1 V supply. The drivers are designed with the same thin oxide transistors as in the digital blocks. They can sustain 0.8-1 V power supply. With 1 V oscillator supply and 0.8 V rest of transmitter supply, total energy consumption is 0.34 pJ/bit at 13.3 Gb/s. This energy performance is very close to recent published works [2][3].

Fig. 9. (a)(b) 9.16 Gb/s terminated output (SST) at 40 Ω termination after 1 ns delay 50 Ω impedance transmission line with minimum and maximum driver strength, respectively (c)(d) 13.3 Gb/s and 9.16 Gb/s SST driver output with maximum drive strength at far end 50 Ω termination after 11.4 mm organic interconnect, respectively

IV. CONCLUSION

This paper presents a transmitter for bunch of wires chip-to-chip communication interface standard in multi-chip systems. It offers interconnect based co-design of terminated and unterminated drivers along with the digital C4MOS library. The design can be conveniently transferred to other technology nodes. It offers energy efficiency of 0.34 pJ/bit at 13.3 Gb/s on 11 mm long organic substrate channel.

REFERENCES