DEVELOPMENT OF NANOIMPRINT LITHOGRAPHY FOR SOLAR CELL TEXTURISATION

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ABSTRACT: A novel processing scheme for the defined texturisation of silicon solar cells is presented. This process chain is based on nanoimprint lithography (NIL) to structure etching masks in combination with plasma etching processes for the pattern transfer into the silicon substrate. This process chain is intended for the honeycomb texturing of multicrystalline silicon solar cells. In this study we use high efficiency monocrystalline silicon to investigate the effect of the processes used without being limited by material related issues. Very high short circuit current densities exceeding 40 mA/cm² are demonstrated. Besides this proof of concept related studies, we report on our progress in developing a roller-NIL tool to allow a continuous process flow for structuring high-resolution etching masks.
Keywords: Texturisation, Multicrystalline Silicon, Light Trapping

1 INTRODUCTION

The texturisation of a solar cell is a widely known measure to increase its efficiency. This gain in efficiency is based on two optical effects resulting of a texture: (i) the overall reflectivity across the relevant part of the solar spectrum can be lowered and (ii) a deflection of incoming light can be achieved leading to light trapping or confinement [1].

High efficiency silicon solar cells fabricated in laboratory scale make use of defined texturing schemes. Namely the most prominent are the inverted pyramids on monocrystalline silicon (c-Si) and the honeycomb texture on multicrystalline silicon (mc-Si), which were applied reaching the highest efficiencies on these materials up to now [2, 3]. Looking at the potential gain resulting from a defined texture, the additional efforts are especially benefitting for mc-Si.

Up to now, no defined textures are applied in an industrial scale fabrication of silicon solar cells. Photolithography and related processes are too consumptive for an industrial realization. However, the need for an improvement in the efficiency of silicon solar cells pushes the industry towards more sophisticated cell structures using for example dielectric passivation layers on the rear side [4] or innovative texturing schemes. Especially, for the honeycomb texturing of mc-Si, there is ongoing research to develop new processes for the patterning of etching masks and the subsequent etching processes. Routes investigated in other groups include laser ablation of a dielectric etching mask [5] or inkjet patterning of a polymeric etching mask [6]. Both are combined with wet chemical etching for the pattern transfer into the silicon substrate.

The process chain we are working on is based on nanoimprint lithography (NIL), where a structured stamp is used to pattern a polymer layer, which then can be used as etching mask. Of course, in a first step master structures have to be originated, which later on are replicated to fabricate the stamps for the NIL process. We are using interference lithography for the master origination of the hexagonal pattern and cast molding processes using elastomeric polymers for the stamp fabrication. In the type of NIL, a UV-curable resist is structured [7] and plasma etching processes are used to transfer the honeycomb pattern into the substrate.

In a first step we conducted reflection measurements to assess the quality of the texture generated using this innovative process chain. Another issue are the electrical properties of substrates, which ran through this process chain. This is of special interest for plasma etching processes, because of potentially plasma induced damages. Textured samples out of float zone c-Si material were prepared, to measure emitter saturation current densities j_{0E} and thus get information about limitations of implied open circuit voltages V_{oc}. First cells were processed using the presented process chain and the internal quantum efficiency (IQE) was measured to additionally get information about potential surface damages. Further on, I-V characteristics of honeycomb textured cells are measured to finally confirm the potential of this novel texturing scheme.

Additionally to the basic characterisation of this process chain, results of our newly developed roller-NIL tool are presented. This technology aims for an industrially feasible patterning of etching masks in a continuous process flow.

2 EXPERIMENTAL

2.1 Nanoimprint lithography (NIL)

In the NIL process sequence a substrate we want to texture is coated with a negative tone photoresist, then the stamp is pressed into this resist, while maintaining the pressure a UV-light source is switched on to cure the resist by flashing through the stamp and finally the stamp can be demolded. Beneath the polymer layer we applied an adhesion promoter layer, which is also beneficial for a later lift off of the resist after the etching process.The patterned resist layer which remains on top of the substrate can later on be used as etching mask. This process sequence is schematically visualized in figure 1.

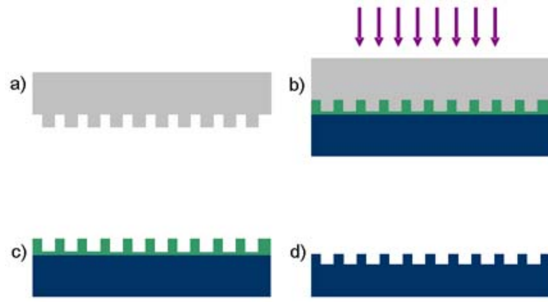

Figure 1: Schematic overview of the texturing process by UV-Nanoimprint Lithography. The PDMS stamp (a) is pressed gently into a UV-curable resist with low viscosity, previously deposited on top of the silicon substrate, and the resist is hardened with a UV light flashing through the stamp (b). After demolding the resist layer is used as etching mask in the following reactive ion etching (RIE) process. Finally, the remaining resist has to be removed to obtain the textured silicon substrate as shown in d).

The hexagonal pattern of the master structures was originated using three beam interference lithography [8]. These structures were replicated into nickel shims by electroplating. The stamps for the NIL were fabricated via cast molding of a two component addition curing silicone. Already within the curing process the silicone is bonded onto a quartz substrate which acts as carrier substrate for the NIL process. We use flexible materials for the stamps to allow a conformal contact on full substrate size. At the moment the stamp size is limited to 100x100 mm², however there is no problem in principle concerning the upscaling of the stamp size.

Besides a complete pattern transfer into the curable polymer layer, a crucial parameter is the residual layer thickness beneath the depressed areas. This residual layer thickness has to be as homogeneous and as small as possible to ensure an immediate and simultaneous start of the etching of the silicon substrate in the following process step. Figure 2 shows an imprinted polymer layer on top of a mc-Si substrate.

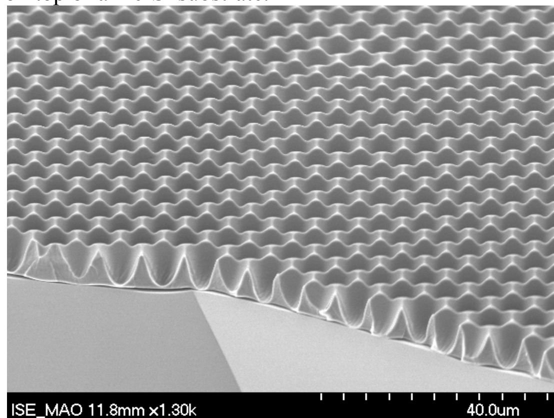

Figure 2: Via NIL structured etching mask on top of a mc-Si substrate. The substrate size is 100x100 mm² and the pattern has a period of 8 µm.

2.2 Etching processes

For the etching of the silicon we chose fluoride based plasma processes. An optically good texture shows a high aspect ratio and should not exhibit flat surface areas normal to the incident light. To realize an optimum texture, we combined a reactive ion etching (RIE) process with a microwave (MW) plasma etching process [9].

The RIE process is conducted in the beginning using a parallel plate reactor setup with the power being coupled in capacitively. Too high bias voltages should be avoided to minimize plasma induced damages of the surface and regions close to the surface. Defects might occur due to damages of the lattice structure or insertion of impurity atoms [10]. Gases used for this process are sulfur hexafluoride (SF_6) and oxygen (O_2). The RIE process is used to generate deep etching pits with steep sidewalls. After this process the remaining resist is removed in a lift off process using an organic solvent.

After this lift off process, the etching pits, which still have flat areas in between, are widened in an isotropic MW plasma etching process. This MW plasma etching process is conducted without any applied bias voltages and thus a purely chemical etching using the fluoride radicals occurs. This allows the removal of potentially damaged areas. The etching process should be finished just when all flat areas between the etching pits vanish.

3 CHARACTERISATION

3.1 Reflection measurements

Reflection measurements were conducted using a Fourier spectrometer. To allow a comparison of different measurements *R(λ)*, these were weighted with the AM1.5g solar spectrum and a factor *λ/(hc)* to take the quantity of photons into account by

$$R_W = \frac{\int_{\lambda_1}^{\lambda_2} S(\lambda) R(\lambda) \frac{\lambda}{hc} d\lambda}{\int_{\lambda_1}^{\lambda_2} S(\lambda) \frac{\lambda}{hc} d\lambda}, \qquad (1)$$

with *S(λ)* being the solar spectrum, *h* Planck´s constant, *c* the speed of light and λ_1 and λ_2 the integration boundaries relevant for silicon solar cells (300 – 1200 nm).

The values for the weighted reflection R_w for the honeycomb texture via NIL and plasma etching were varying for different kinds of surface roughnesses. While on bright etched c-Si substrates values of 12.5 % were reached, rough mc-Si substrates were processed leading to values of around 18 % (without antireflection coating). In comparison to these values, the industrial standard acidic texture on mc-Si allows values of around 22 % for R_w. Furthermore, the excellent values using this novel process chain demonstrated on c-Si are even in the range of the inverted pyramids. This demonstrates the potential of this process chain.

The discrepancy of R_w for the honeycomb texture on different substrates can be explained by less homogeneous etching masks on rougher surfaces in terms of their residual layer thickness. This automatically leads to an asynchronous starting of the etching process and thus to an inhomogeneous texture. However, the plasma etching processes were optimised for bright etched c-Si surfaces and there is room for optimisation of the etching processes to rougher surfaces on mc-Si substrates.

3.2 Emitter saturation current densities

Lifetime samples of different texturing schemes were prepared to evaluate surface recombination effects of the honeycomb texture. The different types of surfaces which were investigated are a random pyramids texture (alkaline wet chemical etching), an isotexture (acidic wet chemical etching) and the honeycomb texture fabricated by the here presented process chain. The samples for the random pyramids and the honeycomb texture were processed on FZ p-type 8 Ωcm substrates. For a reasonable acidic wet chemical texturing (comparable to the standard isotexture on mc-Si), it is necessary to use substrates still comprising saw damaged areas [12]. Because of a lack of FZ substrates of the same resistivity and not yet having the saw damage removed, for the isotextured substrates FZ p-type 0.9 Ωcm material was used.

After the texturing of the substrates, a shallow 120 Ω/square emitter was realized by a $POCl_3$ diffusion, on the front side a combination of a thin thermal oxide and an antireflection silicon nitride was applied and the backside was passivated using silicon nitride. The lifetime samples were then measured with the quasi-steady-state photo conductance (QssPC) method. The isotextured substrate was evaluated at low level injection and the random pyramid and honeycomb textured substrate was evaluated at high level injection using the slope method [13, 14].

After determining the surface recombination velocity S_{eff}, the emitter saturation current density j_{0E} was calculated via

$$j_{0e} = S_{eff} \frac{qn_i^2}{(\Delta n + N_A)}, \quad (2)$$

where n_i is the intrinsic charge carrier density, N_A the base doping and Δn the injection level. The j_{0E} values then can be used to calculate the limits of the implied open circuit voltages V_{OC} by

$$V_{OC,\max} = \frac{kT}{q} \ln\left(\frac{j_{sc}}{j_0} + 1\right), \quad (3)$$

with kT/q being 25.9 mV, the short circuit current density j_{SC} assumed to be 38 mA/cm² and the base saturation current j_{0B} being neglected ($j_0 = j_{0E} + j_{0B}$). Figure 3 shows a graph with the calculated j_{0E} and thus implied V_{OC} values.

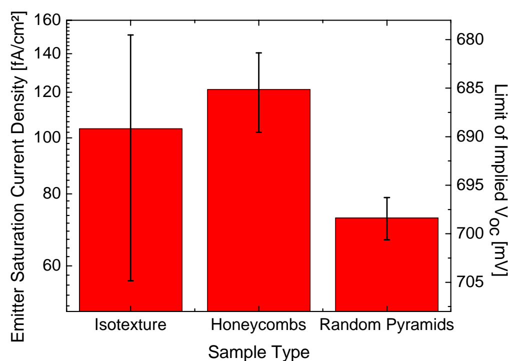

Figure 3: Values of the emitter saturation current density and the limit of the thereby implied V_{OC} for substrates with different textures extracted out of lifetime measurements using the QssPC method.

The values for j_{0E} are slightly higher for the honeycomb texture compared to the isotexture (121 fA/cm² and 103 fA/cm² respectively). The random pyramids show values of around 73 fA/cm². Due to the rather distinct surface enlargement for the random pyramids and the honeycomb texture to a planar surface, one can put the two values of j_{0E} of these textures into relation. The random pyramids should have a surface enlargement of around 1.7 and the honeycombs of around 2.5 compared to a flat surface. This difference already could be used to explain the difference in j_{0E}. These measurements indicate that there is no major problem concerning contaminations or surface damages due to this new process chain.

3.3 Solar cell results

For the solar cell processing of the honeycomb textured substrates again FZ p-type 8 Ωcm material and a 120 Ω/square emitter was used. Again the front surface was passivated by a 10 nm thick thermal silicon oxide with an antireflection silicon nitride on top of it. The rear side also was passivated by a thermal oxide and was contacted through laser fired contacts (LFC) [15]. The front contacts were realized using photolithographic processes, evaporation of TiPdAg and subsequent electroplating. The honeycomb texture was applied on the full 4´´ wafer area, however to generate more data seven cells were processed on one substrate with 2x2 cm² cell size. In table 1 the corresponding solar cell results are listed. The values of V_{OC} are limited by the low base doping plus the therefore necessarily small pitch used in the LFC process [12]. A fill factor of around 70 % indicates that the thin TiPdAg front side metallization was not able to contact the emitter properly. Additional experiments showed, that there is no such problem with aerosol printed and fired contacts. Here very low normalised contact resistances of 0.41+-0.16 Ωcm were measured on honeycomb textured wafers with 30 µm wide contacts. Thus, there is no basic problem concerning the contacting of this type of texture. Remarkably, the values for the short circuit current density are exceeding 40 mA/cm² showing the potential of this texturing scheme and confirming the high quality of this novel technological approach.

Table I: Solar cell results of 2x2 cm² honeycomb textured FZ p-type cells.

	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
Best cell	629,7	40,1	73,9	18,7
Average of 20 cells	622,4	39,3	70,0	16,5

Additionally to the I-V-curves also spectral response measurements were conducted (figure 4). These measurements confirm the indications given by the j_{0E} characterizations. Especially the high internal quantum efficiency in the short wavelength regime confirms very low plasma induced damages.

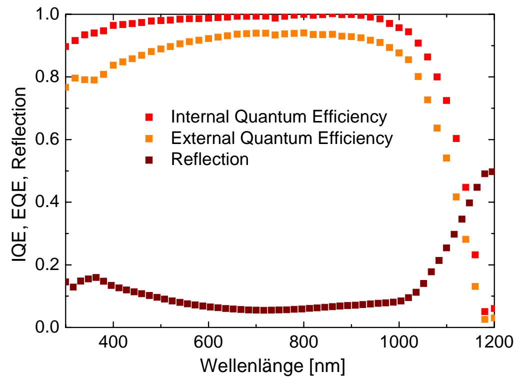

Figure 4: Spectral response measurements on honeycomb textured FZ solar cells.

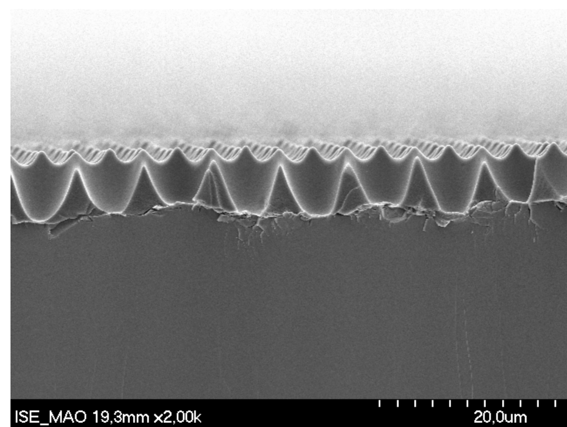

Figure 5: Via roller-NIL structured polymer layer on top of a rough mc-Si substrate. The hexagonal patterned polymer layer has a very low residual layer thickness (polymer thickness beneath the depressed areas), which is essential for following etching processes. The patterned substrate size was 100x100 mm².

4 DEVELOPMENT OF A ROLLER-NIL TOOL

Besides of working on the proof of concept, we are currently developing a tool to allow a continuous process flow in the NIL process. In this so called roller-NIL process, the applied etching mask still is made of an UV-curable photoresist, which is structured by embossing by a stamp situated on a roll.

Working with silicon as substrate material sets some restrictions for the construction of this roller-NIL tool. First, since we want to allow a UV-curing of the resist while being in contact with the stamp, and silicon is not transparent in this spectral range, we have to enable UV flashing through the stamp. Secondly, since we are developing this tool for mc-Si substrates, we have to deal with rough, wavy and brittle substrates. These two demands can be met using transparent silicone materials for the stamp and a quartz cylinder as roll. The wafer transport is realised using a conveyor band with a vacuum chuck. Force monitoring is implemented into the bearing of the roll to adjust the pressure of the roll onto the substrate. At the moment spin coating is still used to apply the resist, however an in-line coating process via an applicator roll or inkjet systems is intended to be implemented.

First very promising tests already were conducted on our prototype showing an excellent replication of the master structures as can be seen in figure 5. Also the homogeneity even seems to be superior to the planar stamp setup for NIL. The origin of this increased homogeneity could be related to a homogenisation due to the rolling of the resist or a smaller contact area compared to a planar setup, but this has to be investigated further on. The very low residual layer thickness even for rough surfaces shows the high adaptability of the flexible stamp. Besides the potentially increased throughput of a roller-NIL tool, another advantage lies in the controlled demolding of the stamp. The resist properties had to be changed for this novel tool, but first etching tests revealed, that also the new formulation shows a high resistivity in plasma etching processes.

5 SUMMARY

We presented an innovative process chain for the defined texturing of silicon independent of crystal orientations. As application we chose the honeycomb texturisation of mc-Si. First results show, that the optical properties are already superior to the maskless acidic wet chemically fabricated textures and there is room for optimization. Electrical characterization of the textured substrates shows, that contamination due to these new processes and plasma induced surface damages are a minor problem. Solar cells were processed with short circuit current densities exceeding 40 mA/cm². Contacting schemes typically applied for high efficiency cells using photolithography and evaporation led to low fill factors, but first tests using aerosol printing with subsequent electroplating showed that there is no basic problem in the contacting of these textures. Further on, first very promising results of our newly developed roller-NIL tool were demonstrated on rough mc-Si substrates.

6 ACKNOWLEDGEMENT

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