Vertical Interconnections using Through Encapsulant Via (TEV) and Through Silicon Via (TSV) for High-Frequency System-in-Package Integration

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Abstract

In this paper we investigate two vertical interconnect options for high-frequency system-in-package (SiP) integration: through encapsulant via (TEV) applied to the embedded wafer level ball grid array (eWLB) technology and through silicon via (TSV). We compare both solutions in terms of size and electrical performance. We use analytic expressions and electromagnetic simulations for our analysis and present measurement results of selected structures for verification. The results show that the choice of TEV and TSV depends on application and cost window.

Introduction

For on-going downscaling and need for integration of ever more functionality system-in-package (SiP) technologies allow significant advantages. Among them are time to market, cost, and performance. During recent years the embedded wafer level ball grid array (eWLB) package has been introduced [1, 2]. The eWLB has demonstrated to be an excellent platform for system integration with excellent high-frequency performance. On the one hand side-by-side multi-chip integration in an eWLB package, possibly with high-quality (high-Q) embedded passives in the fan out region of the redistribution layer (RDL), is an attractive SiP solution [3, 4, 5, 6]. On the other hand the use of vertical interconnections in the package and double-sided RDL extend the integration capabilities to the third dimension (3D). Using vertical interconnections increases design capabilities allowing package-on-package modules, integration of surface-mount components (SMD) onto top RDL, and integration of passives in the volume of mold compound [7, 8]. In the eWLB technology vertical interconnection can be realized either in the mold compound as through encapsulant via (TEV) or in the silicon chip as through silicon via (TSV).

In this paper, we compare TEV and TSV interconnect options in terms of size and electrical performance. Due to different manufacturing processes TEV and TSV differ in size, diameter, and filling. On the one hand, TSVs allow the most compact design and the highest degree of miniaturization. On the other hand, TEVs offer lower resistance and reduced inductance compared to TSVs but at the cost of increased size. An optimal system design requires a trade-off between size, performance, and cost. We use analytic expressions and electromagnetic simulations to compare both interconnect solutions and derive their performance limits. We underline the importance of technology optimization for optimal system design. Finally, we show measurement results of vertical interconnections manufactured using TEVs and TSVs.

Vertical Interconnection in eWLB

The key component for 3D integrations is vertical interconnection. In the eWLB technology we can realize this interconnection either in the mold compound as TEV or in the silicon chip as TSV. Fig. 1 illustrates these two options. Nowadays TSVs are widely used in Si interposer solutions, memory stacks, sensors, FPGAs etc. TEVs are used to fabricate passives like 3D solenoid inductors etc. in the fan-out area of the eWLB package. Both interconnections prove themselves in practice. But to decide the right one for a given application we need to compare both. We start the comparison by their fabrication.

Through Encapsulant Via (TEV)

We form TEVs by laser drilling and subsequent filling with Cu by sputtering and electroplating. The resulting TEVs have cylindrical shape and voids inside. Fig. 2 shows a cross-sectional photograph and an X-ray tomography image of TEVs manufactured in eWLB. The diameter of TEVs is about 100–150 µm and the thickness of the Cu coating is about 10 µm. The thickness of the mold substrate is 450 µm resulting in an aspect ratio of about 3–4.5. The minimal pitch of TEVs is 300 µm.

Through Silicon Via (TSV)

TSVs are commonly used for vertical interconnections between the top and the bottom side of a Si wafer. There are different types of TSVs. In this approach, we use full-filled Cu-TSVs in a so-called via-first approach. We manufacture

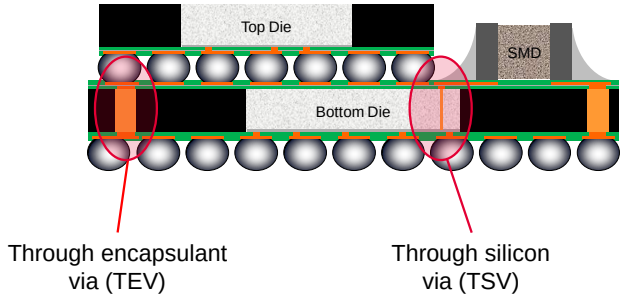
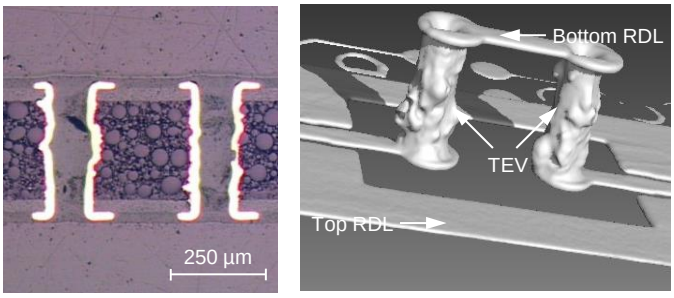
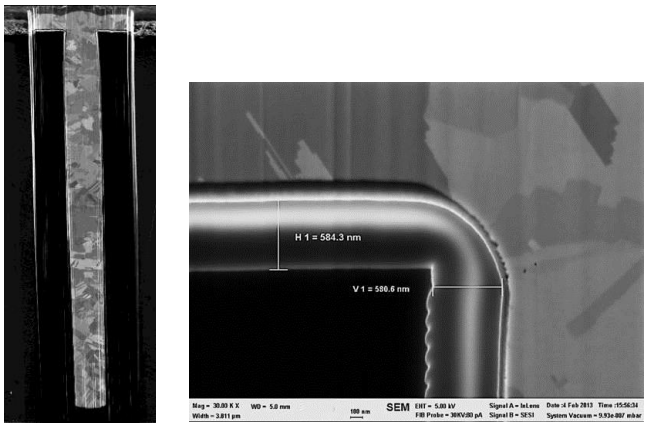


Fig. 1. Two vertical interconnect options in the eWLB.



(a) (b)

Fig. 2. (a) Cross-sectional photograph and (b) X-ray tomography image of TEVs fabricated in eWLB.



(a) (b)

Fig. 3. (a) Focused ion beam (FIB) cross-section of Cu-TSV of 10 µm diameter and 110 µm depth and (b) detailed view of TSV interface Si/SiO_2/Cu.

TSVs using deep reactive ion etching (DRIE), followed by isolation with oxide (SiO_2) using chemical vapor deposition (CVD), and Cu filling using electro-chemical deposition.

The TSV characteristics depend on the TSV approach in terms of size and technological features. In this investigation, we use TSVs with a diameter of 10 µm and a depth of 110 µm having an oxide liner isolation and a sputtered Ti/Cu barrier/seed layer and full-filled metallization by Cu electroplating. This TSV configuration is typically used for Si interposer, where in active devices the TSV dimension is in a range of typ. 5 µm diameter with a depth of less than 50 µm. Fig. 3 shows a cross-sectional photograph of TSVs manufactured in silicon chip.

Electrical Characteristics of Vertical Interconnections

If the physical length of a via is much smaller than a wavelength at maximal considered frequency, we can describe the vertical interconnection using simple lumped resistance (R), inductance (L), capacitance (C), and conductance (G). Typically, a one hundredth of a wavelength is recommended as an upper limit on spatial dimensions to ensure that the phase variation across the component is negligible. For Si ($\varepsilon_r = 11.9$) and typical via depth of 100 µm we get 8.7 GHz as an upper limit for a lumped-element approximation.

Fig. 4(a) illustrates a simplified geometry of a hollow round vertical interconnection. A metallic cylinder of inner diameter d_1, outer diameter d_2, and length l is surrounded by a thin passivation layer of thickness t_{ox} and a substrate material of horizontal dimensions much larger than l and d. Fig. 4(b) shows an equivalent circuit model corresponding to this geometry. This representation is generic and applies for both TEVs and TSVs. For TEVs, the substrate is mold compound (insulator) and there is no passivation layer ($t_{ox} = 0$). For TSV, the substrate is Si (semiconductor) and there is a thin SiO_2 layer to isolate the via metallization from the conducting substrate.

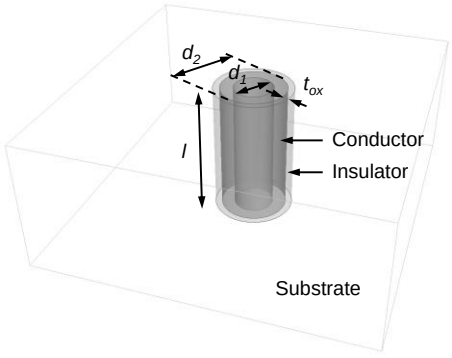
In the following, we calculate and compare the RLCG parameters of the equivalent circuit for TEVs and TSVs of typical dimensions. We use simple analytic expressions for demonstrative purposes to indicate dependence on physical parameters. More accurate formulas for design purposes can be found in e.g. in [9, 10].

Resistance R_{via}

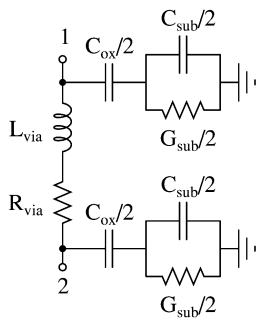
The resistance of a hollow round via of depth l and inner and outer diameters d_1 and d_2, respectively, can be calculated using the known formulas for DC and AC:

$$R_{\text{via}}(f) = \begin{cases} \dfrac{4l}{\pi\sigma(d_2^2 - d_1^2)} & \text{for } \delta \geq \dfrac{d_2 - d_1}{2} \\ \dfrac{l}{\pi\sigma(d_2\delta - \delta^2)} & \text{for } \delta \leq \dfrac{d_2 - d_1}{2} \end{cases} \quad (1)$$

where σ is the conductivity of the filling metal and δ is the skin depth. The expression for AC assumes that the skin effect



(a)



(b)

Fig. 4. (a) Simplified geometry of a vertical interconnection and (b) its corresponding equivalent circuit model.

is fully developed and the current flows through a thin layer on the outer surface of the metallic cylinder. Table 1 lists the resistance values calculated using (1) for Cu vias of depth $l = 100$ µm and different diameters d_1 and d_2. The upper two rows with $d_2 = 10$–20 µm are representative for TSVs whereas the lower two rows with $d_2 = 100$–200 µm are representative for TEVs.

Inductance L_{via}

The inductance contribution of a single via in a specified package interconnection depends on the other components creating the current loop (RDL traces, solder balls, etc.) and their geometrical configuration. Moreover, the existence of neighboring metals and return current can lower the effective loop inductance. Therefore, the partial self-inductance with return current at infinity is used to evaluate the inductance of a single via.

For an isolated straight wire of length l diameter d_2 the inductance can be calculated using the formula [11]:

$$L_{\text{via}}(f) = \frac{\mu_0 l}{2\pi}\left\{\ln\left[\left(\frac{2l}{d_2}\right)+\sqrt{1+\left(\frac{2l}{d_2}\right)^2}\right]+\left(\frac{d_2}{2l}\right) - \sqrt{1+\left(\frac{d_2}{2l}\right)^2}+\frac{1}{4}\tanh\left(\frac{4\delta}{d_2}\right)\right\} \quad (2)$$

where δ is the skin depth. The last term in (2) is responsible for the frequency dependence of the inductance. Table 2 shows the inductance values calculated using (2) for Cu vias of depth $l = 100$ µm and for different diameters d_2. Unlike (1), (2) assumes $d_1 = 0$ and thus does not account for a void inside a TEV. As a result, the values calculated for TEVs at DC are slightly overestimated.

In the above calculation we assumed that the substrate for TSVs is made of high-resistivity Si and there are no eddy currents. In case of low-resistivity Si, the current flow in a TSV can cause eddy currents which in turn can cause energy losses and lower the effective self-inductance of an interconnection.

Table 1. Resistance R_{via} calculated using (1) for round Cu vias of depth $l = 100$ µm and different diameters d_1 and d_2.

Via type	d_1 (µm)	d_2 (µm)	R_{via} (mΩ)			
			DC	1 GHz	5 GHz	10 GHz
TSV	0	10	22	33	65	89
	0	20	5.5	15	31	43
TEV	80	100	0.61	2.7	5.9	8.4
	180	200	0.29	1.3	3.0	4.2

Table 2. Self-inductance L_{via} calculated using (2) for round Cu vias of depth $l = 100$ µm and different diameters d_2.

Via type	d_2 (µm)	L_{via} (pH)			
		DC	1 GHz	5 GHz	10 GHz
TSV	10	60	58	57	57
	20	47	44	43	43
TEV	100	22	17	17	17
	200	14	9.6	9.4	9.4

Capacitance and Conductance C_{ox}, C_{sub}, G_{sub}

Unlike for resistance and inductance, the phenomena governing the capacitive behavior of TSV and TEV are different due to semiconductor nature of Si.

For high-resistivity Si there is no substantial difference in behavior between TEVs and TSVs. The capacitance C_{sub} of a via depends on the distance to the neighboring metals and can be calculated only for a particular package layout. Therefore, similarly to inductance, the capacitance can be evaluated assuming the reference conductor at infinity, i.e. as self-capacitance. For an isolated straight wire of length l and diameter d the self-capacitance C_{sub} can be calculated using quasi-static simulator or roughly estimated for $l \gg d_2$ using the following formula [12]:

$$C_{\text{sub}} \approx \frac{2\pi\varepsilon_0\varepsilon_{\text{r sub}} l}{\ln\left(\frac{2l}{d_2}\right)}\left[1+\frac{1-\ln 2}{\ln\left(\frac{2l}{d_2}\right)}\right] \quad (3)$$

where $\varepsilon_{\text{r sub}}$ is the relative permittivity of the substrate material. Once the capacitance is known, the conductance can be calculated as:

$$G_{\text{sub}}(f) = \left(\tan\delta_{\text{sub}} + \frac{\sigma_{\text{sub}}}{\omega\varepsilon_0\varepsilon_{\text{r sub}}}\right)\omega C_{\text{sub}} \quad (4)$$

where $\tan\delta_{\text{sub}}$ and σ_{sub} is the loss tangent and the conductance of the substrate, respectively. The capacitance C_{ox} of a thin passivation layer can be calculated using:

$$C_{\text{ox}} = \frac{2\pi\varepsilon_0\varepsilon_{\text{r ox}} l}{\ln\left(\frac{d_2+2t_{\text{ox}}}{d_2}\right)} \quad (5)$$

Table 3 lists the capacitances C_{sub} and C_{ox} calculated using quasi-static simulator for Cu vias of depth $l = 100$ µm for two different materials: mold compound ($\varepsilon_{\text{r sub}} = 3.0$) and Si ($\varepsilon_{\text{r sub}} = 11.9$). The thickness of SiO_2 ($\varepsilon_{\text{r ox}} = 4.0$) passivation for TSV is $t_{\text{ox}} = 0.5$ µm. The values in brackets are calculated using (3) and (5) and are given for comparison. The last column shows the effective capacitance of a via calculated as a series connection of capacitances C_{sub} and C_{ox}, i.e. $C_{\text{via}} = C_{\text{sub}}C_{\text{ox}}/(C_{\text{sub}}+C_{\text{ox}})$.

Table 3. Capacitances C_{sub} and C_{ox} calculated using quasi-static simulator for round Cu vias of depth $l = 100$ µm and different diameters d_2. The thickness of passivation for TSV is $t_{\text{ox}} = 0.5$ µm. The values in brackets are calculated using (3) and (5).

Via type	d_2 (µm)	C_{sub}(fF)	C_{ox} (fF)	C_{via} (fF)
TSV $\varepsilon_r = 11.9$	10	24.3 (25.5)	233 (233)	22.0
	20	29.6 (34.5)	456 (456)	27.8
TEV $\varepsilon_r = 3.0$	100	11.4	∞	11.4
	200	16.5	∞	16.4

For medium and low-resistivity Si the behavior of a TSV becomes more complicated due to existence of slow-wave and dielectric quasi-TEM modes [13]. Fig. 5 shows the resistivity-frequency plot which defines the propagation mode depending on resistivity of Si. The solid blue curve denotes the dielectric relaxation frequency f_{sub}:

$$f_{\text{sub}} = \frac{\sigma_{\text{sub}}}{2\pi\varepsilon_0\varepsilon_{\text{r sub}}} \qquad (6)$$

At frequencies below f_{sub} the resistive losses of Si dominate over capacitive component leading to increased effective capacitance seen by a travelling signal ($C_{\text{via}} \to C_{\text{ox}}$). At frequencies above f_{sub} the electric filed can penetrate the Si substrate which decreases the effective capacitance ($C_{\text{via}} \to C_{\text{sub}}C_{\text{ox}}/(C_{\text{sub}} + C_{\text{ox}})$) of Si. Fig. 6 illustrates the capacitance of a TSV of dimensions corresponding to the top row of Table 3 simulated for four typical substrate resistivities: 1, 10, 100, and 1000 Ω·cm. The corresponding relaxation frequencies are 150, 15.0, 1.50 GHz, and 150 MHz. As expected, the capacitance reaches the maximum value of about 240 fF at lower frequencies and drops down to about 20 fF at higher frequencies. The observed increase of capacitance due to slow-wave effects corresponds to an effective relative permittivity of $\varepsilon_{\text{r eff}} \approx 160$, thus much higher than this of Si.

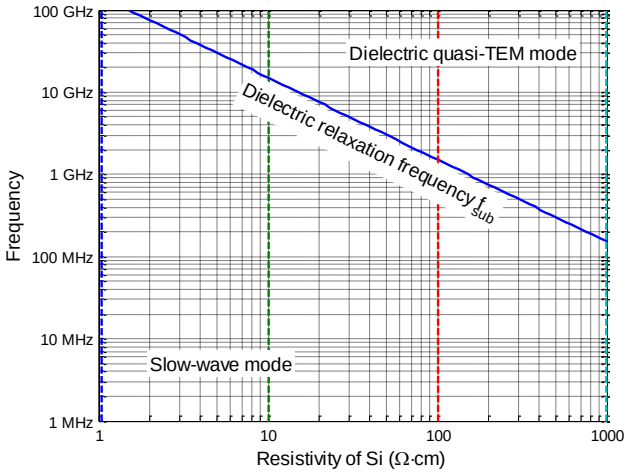


Fig. 5. Resistivity-frequency plot defining the propagation mode depending on resistivity of Si.

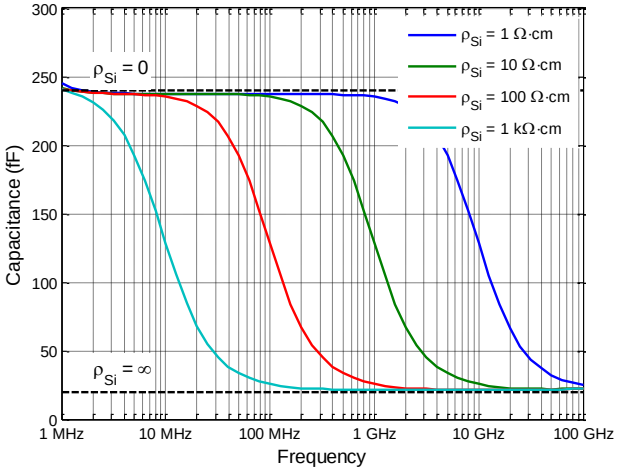


Fig. 6. Effective capacitance seen by a signal traveling through a 100-µm deep TSV depending on resistivity of Si.

Discussion

Table 1 confirms natural expectation than the TEVs offer significantly lower resistances due to larger size. The biggest difference is at DC by factor of almost 50 because of the resistances dependence on via cross section. At frequencies at which the skin effect is developed, the resistance is inversely proportional to via diameter and the factor drops down to 10. The presented comparison does not include the contact resistances at the via-RDL interface. This contact resistance may be of importance for TSVs due to their small contact area. Table 2 shows that the use of TEVs instead of TSVs allows one to reduce by three to four times the inductive contribution of a vertical interconnection. Thus, for applications where low resistances and inductances are required, e.g. for low frequency power applications with high currents, TEVs are better choice.

Using a vertical connection using TEVs may require RDL routing in the fan-out area of eWLB which means additions resistance and inductance in series. Moreover, (1) does not account for surface roughness which can considerably increase the resistance at higher frequencies. The latter effect can be of significance for TEVs due to relative rough mold surface after laser drilling. Thus, for high-frequency applications, TSV with their smooth conductors and lower diameters and pitches seems to be better choice.

Despite higher permittivity of Si, the self-capacitances of TEVs and TSVs are comparable due to larger size of TEVs, as can be seen from Table 3. A particular attention must be paid when medium or low-resistivity Si is used. As a result of slow-wave mode in TSVs, the signals propagating at lower frequencies experience larger delay than the signals at higher frequencies. This effect can cause serious distortions of broadband signals. The slow-wave effect can be reduced by increasing the thickness of the passivation layer in TSVs.

Summarizing the pros and cons of TSV and TEV we propose a 3D system where the power/ground 3D transitions using the TEVs while the high speed RF signals can use TEVs. The extra effort to combine both 3D integration techniques will not necessarily produce extra costs. When the 3D system benefits from TEV and TSV this may lead to changes in system design and may reduce overall costs (for example when saving a heat sink because of power reduction). In the end it is up to the system designer to evaluate this trade-off.

Measurement Results

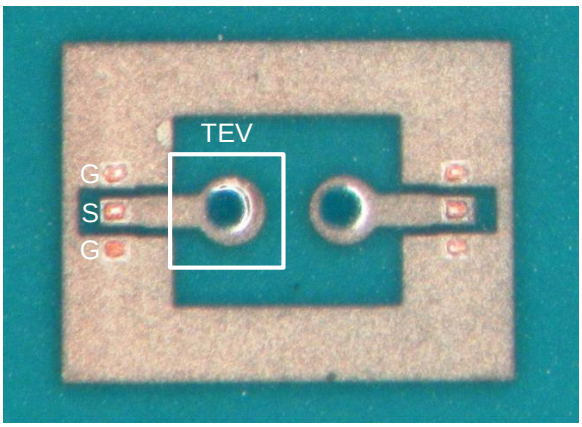
We manufacture test structures with TEVs and TSVs to verify theoretical considerations presented in the previous sections. Fig. 7 shows the photographs of a series (back-to-back) connection of two TEVs and TSVs. Both photographs are to scale and the size difference of almost an order of magnitude between TEVs and TSVs is clearly visible.

We perform the scattering parameter (S-parameter) measurements using an Anritsu 37397 vector network analyzer (VNA) in the frequency range 0.1–10 GHz. We calibrate the

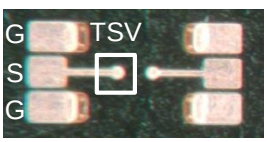
VNA with the short-open-load-thru (SOLT) performed by means of a standard calibration substrate. This calibration establishes the reference impedance $Z_{\text{ref}} = 50\ \Omega$ and the reference plane near the tips of the probes. We use the second-tier multiline thru-reflect-line (TRL) calibration using custom on-wafer transmission line standards to remove the effects of the on-wafer launch structures.

We assume the symmetry of a via ($S_{11} = S_{22}$) to determine the S-parameters of a single via from the measurement of a back-to-back connection. From the measured S-parameters we calculate the RLC parameters assuming the π-circuit topology from Fig. 4(b). Due to different depths of TEVs and TSVs (450 µm for TEV versus 110 µm for TSV) we rescale the obtained circuit parameters to 100 µm depth for easier comparison. Fig. 8 shows the measured and rescaled resistance and inductance of a 100-µm deep TEV and TSV. We measure a test structure without RDL connection on the bottom side of the wafer to determine the self-capacitance of a single via. Fig. 9 compares the measured and rescaled self-capacitances of a 100-µm deep TEV and TSV.

Table 4 shows the RLC values for TSV and TEV measured at 1 and 5 GHz. Due to smaller diameter, the TSV shows much higher resistance and also increased inductance, as expected. The inductances measured for both TSV and TEV agree well with the values from Table 2. The inductance measured for TEV is 15–16 pH and lies between the values estimated for 100-µm and 200-µm cylindrical vias. This is expected due to non-uniform shape of TEV, as shown in Fig 2. On contrary, the resistances measured for TSV and TEV differ considerably from those in Table 1. The higher value of the measured resistances could be partially explained by contact resistance at the via-RDL interface (for TSV) and surface roughness (for TEV). However, the main reason for

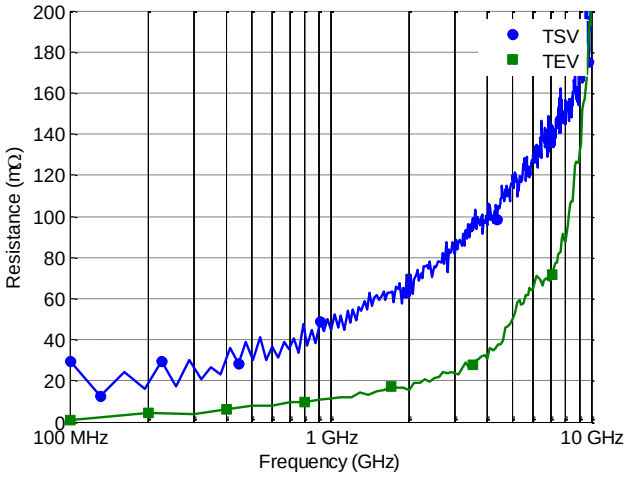


(a)



(b)

Fig. 7. Photographs of a series (back-to-back) connection of two (a) TEVs and (b) TSVs. Both photographs are to scale.



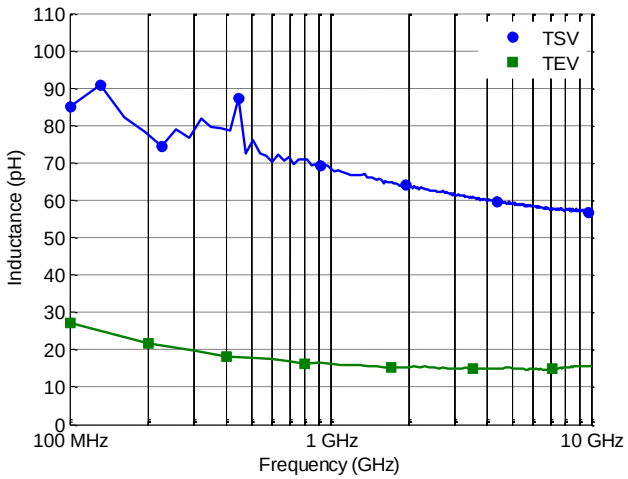


Fig. 8.Measured resistance and inductance of a 100-µm deep TEV and TSV.

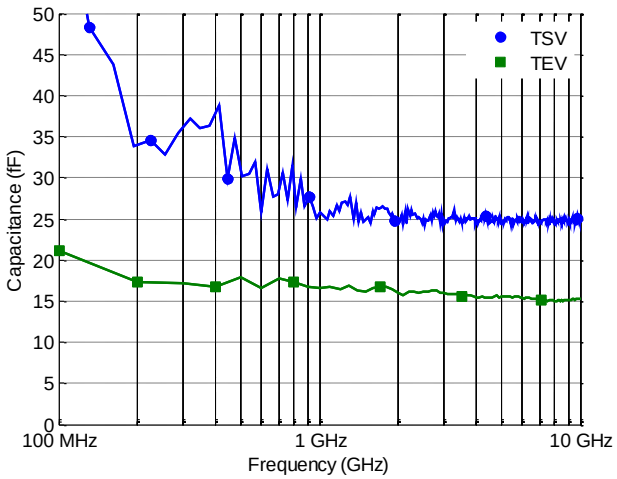


Fig. 9. Measured capacitance of a 100-µm deep TEV and TSV.

Table 4. RLC values for TSV and TEV measured at 1 and 5 GHz.

Via type	Frequency	R_{via} (mΩ)	L_{via} (pH)	C_{via} (fF)
TSV	1 GHz	45	68	22
	5 GHz	110	59	20
TEV	1 GHz	11	16	17
	5 GHz	50	15	16

observed discrepancies is generally known reduced sensitivity for the resistance measurement compared to inductance measurement [14]. At measured frequencies, the impedance of our vias is dominated by its reactive part and the resistive part is much smaller than system impedance of 50 Ω. Moreover, limited contact repeatability in on-wafer measurements and manufacturing tolerances reduce the accuracy of de-embedding and make it more difficult to characterize low-impedance components.

The capacitances measured for TSV agree quite well with those in Table 3. Moreover, we observe a clear increase of capacitance at frequencies below 1 GHz due to slow-wave mode. The measured relaxation frequency of about 1 GHz indicates the resistivity of Si in the range of 100 Ω·cm.

Conclusions

We investigated two vertical interconnect options for eWLB integration platform: TEV and TSV. We compared electrical characteristics of both solutions and derived their performance limits. We presented measurement results of selected TEV and TSV structures to verify presented theoretical considerations. TEVs offer lower resistance and reduced inductance and capacitance compared to TSVs but at the cost of increased size. When combining TSV and TEV in a SiP, the system designer can choose between different vertical transitions with different size and electrical behavior depending on the purpose of application. This will improve the electrical behavior of the system and will lead to a better trade-off between size, performance, and cost.

Acknowledgments

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