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Influence of triangular defects on the electrical characteristics of 4H-SiC devices

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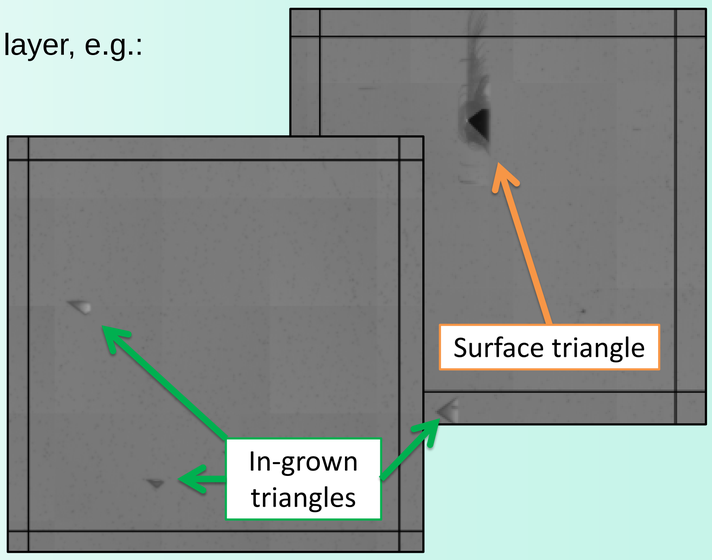
Epitaxial defects in SiC

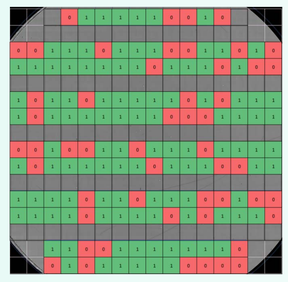
- Multitude of defects in epitaxial layer, e.g.:
  - Dislocations
  - Scratches
  - Downfalls
  - Step-bunches
  - Triangular defects
- Focus on triangular defects
  - Critical influence on device characteristics [3]
  - Length of several 100 µm
  - In-grown triangles
  - Surface triangles



DLS images of in-grown and surface triangles.

Our approach

- UVPL imaging of wafers before device processing by defect luminescence scanner (DLS) [1] and repeated during processing
  → Defect map of each wafer after critical process steps
- Fabricate 4H-SiC JBS diodes [2] and VDMOS transistors on scanned wafers
  - Devices designed for 3.3 kV and 50 A
- Measure 100% of devices under forward and reverse bias using wafer prober
  - Classify devices into passed and failed groups
  - Calculate failure rate
  - Create fail-pass wafer map
- Match wafer maps of device failures to wafer maps of defects in order to understand defect influence on device characteristics



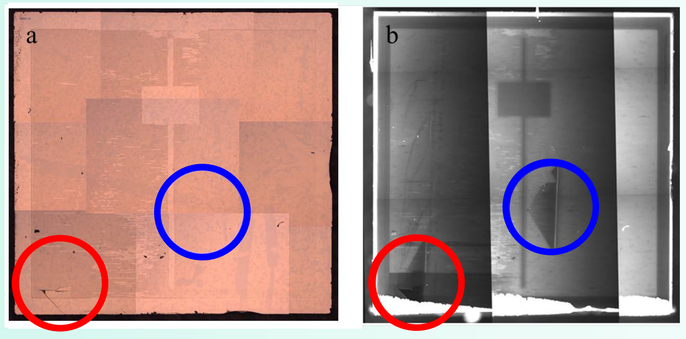
Main findings

- Combination of defect luminescence scanning and electrical measurements of JBS diodes and VDMOS transistors allowed to identify the impact of surface and in-grown triangles on SiC power device characteristics

JBS diodes
- Surface triangles → instant breakdown; abnormal forward characteristics
- In-grown triangles → increase in failure rate by up to 15%

VDMOS transistors
- Surface triangles → instant breakdown; slightly increased failure rate in conduction mode
- In-grown triangles → conduction mode test with low increase in failure rate by 8%
  → no influence in blocking mode test

- No morphological differences were found yet between in-grown triangles that lead to failures and those that show no effect



Optical and DLS images of surface (red) and in-grown (blue) triangles after implantation during VDMOS processing.

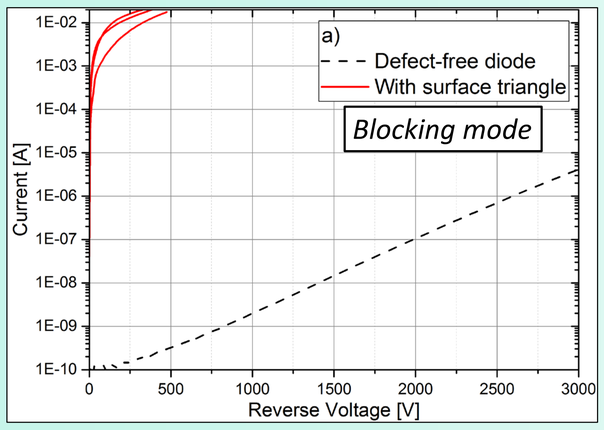
Electrical Characterization & Statistical Approach

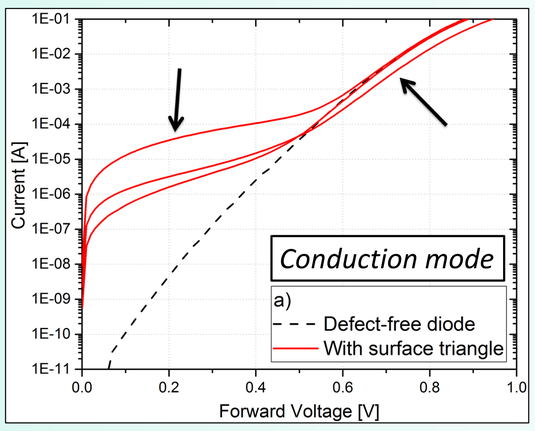
JBS diodes

- Defect-free devices used as reference for electrical characteristics

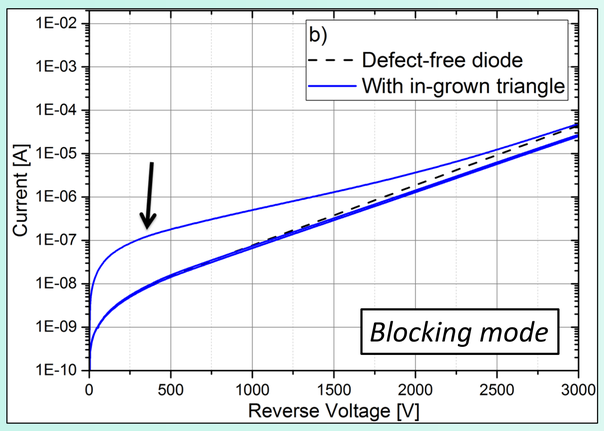
Blocking mode
- In-grown triangles increase leakage current in 20% of diodes
- Surface triangles lead to maxing leakage current limit of 1 mA even below 100 mV

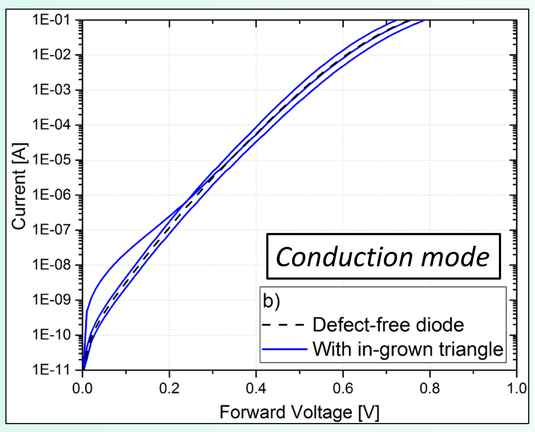
Conduction mode
- In-grown triangles affected 26% of diodes in conduction mode, but at low voltage only
- Surface triangles cause forward characteristic with inhomogeneous barrier height [4]





	JBS diodes			VDMOS transistors		
Triangle defect type	Total	Surface	In-grown	Total	Surface	In-grown
# defects	-	50	266	-	84	220
# afflicted devices	330	23	95	740	45	96
Blocking mode						
No effect	218 (66%)	1 (4%)	49 (51%)	407 (55%)	3 (7%)	51 (53%)
Inhomogeneous ϕ_B	66 (20%)	3 (14%)	27 (29%)	-	-	-
Destructive	46 (14%)	19 (82%)	19 (20%)	333 (45%)	42 (93%)	45 (47%)
Conduction mode						
No effect	277 (84%)	3 (13%)	70 (73%)	496 (67%)	23 (51%)	57 (59%)
Degradation	53 (16%)	20 (87%)	25 (26%)	244 (33%)	22 (49%)	39 (41%)





VDMOS transistors

Blocking mode
- In-grown triangles show similar failure rate as dies without defects
- Surface triangles cause immediate failure already below 1 V

Conduction mode
- Triangle-free dies had failure rate of 33% from other defect types
- In-grown triangles increased failure rate to 41%
- Surface triangles increased failure rate to 49%

References

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