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Monolithically Integrated and Galvanically Isolated GaN Gate Driver

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ABSTRACT In this work, a novel monolithically integrated and galvanically isolated GaN gate driver is presented, which combines the separated power and data link of conventional Si-based solutions. The core is an integrated spiral transformer, which is driven on the primary side by a VHF class-D oscillator with on-off keying modulated by the PWM signal. On the secondary side, the signal is rectified and a network ensures the correct off-state. The driver was operated with PWM signals of up to 2 MHz with only one supply voltage of 8 V on the primary side. This GaN IC shows the potential to be integrated with the power transistor in the future to provide a highly compact isolated driver solution on chip.

INDEX TERMS Gallium nitride, power integrated circuits, monolithic integrated circuit, driver circuits, gate drivers, isolators, isolation technology.

I. INTRODUCTION

ISOLATED gate drivers are essential in power electronics to drive floating power transistors, e.g., the high-side switch in a half-bridge configuration. Galvanic isolation is required in most industrial and automotive applications to ensure safety and reliability [1]. This ensures that the control side is electrically isolated from the power side, preventing dangerous voltages from entering the control side and protecting users in case of faults. It also prevents interference signals from transferring to the sensitive control side, crucial in environments with strong electro-magnetic interference (EMI) [2].

The lateral GaN transistor or high-electron mobility transistor (HEMT) is used in a growing number of power electronic systems [3]. The first products are already available that integrate the power transistor and gate driver monolithically in a GaN technology [3], [4]. However, no commercial isolated GaN gate drivers exist yet. A very common solution is to drive the GaN power transistor with a monolithically integrated GaN driver or external Si gate driver and to isolate the signal by a digital-isolator and supply the secondary side by an isolated DC-DC converter, similar to Fig. 1 in which power and data have separate links.

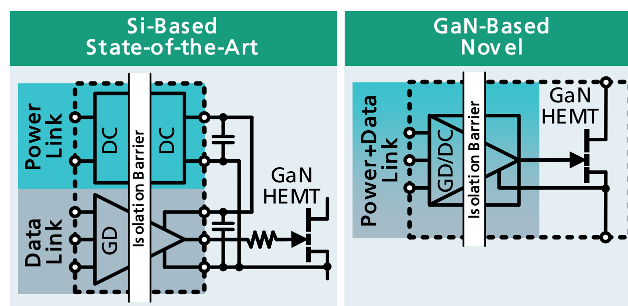

FIGURE 1. Block diagram of a Si-based isolated gate driver and power supply consisting of two separated links for power and data (state-of-the-art). Novel approach to combining the links in a GaN technology.

Isolated gate drivers can be divided into chip or package insulation, which has a direct influence on the isolation between the primary and secondary side. Package-scale isolation consists of at least two but sometimes also three dies. The dies or ICs can be realized completely in the GaN technology (fully-integrated) or consist of a mix between Si-based and GaN technology (partially-integrated). At this point four GaN-based package-scale isolation examples: N. Spina et al.

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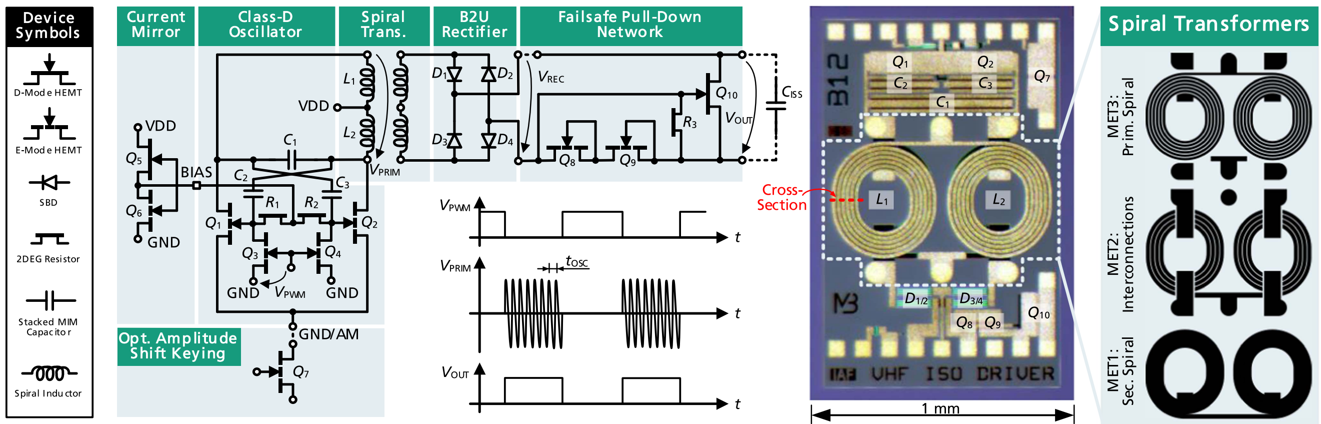

FIGURE 2. Schematic with the circuit groups, legend of the device symbols, and simplified waveforms of the voltages V_{PWM}, V_{PRIM}, and V_{OUT}. Chip photography (size: 1.5 × 1 mm², without power transistor) and insight into the geometry of the double spiral transformer $L_{1/2}$ through the metallization layers.

and S. Spataro et al. realized a two-chip solution of a galvanically isolated data link with integrated antennas in GaN [1], [5], referred to fully-integrated. A partially-integrated approach with combined data and power link was developed by K. Leong et al., where the primary side was realized in an Si-based technology with an integrated transformer and the secondary side in GaN [6]. Another example is [7] by N. Shuichi et al., who developed a GaN-based transmitter and receiver with a PCB butterfly isolation coupler. A distinction can also be made between the isolation method: optical, capacitive [8], inductive [6] or RF-based [1], [5], [7]. However, what has not yet been realized (to the best of author's knowledge) is a combined power and data link fully monolithically integrated into a GaN technology as a chip-scale isolation solution.

In this work, a monolithically integrated and galvanically isolated GaN gate driver is presented, which has a combined power and data link (see Fig. 1). Thus, this isolated driver would be perfectly suited for floating power transistors. Section II describes the circuit implementation and operation of the proposed isolated driver. Section III presents the measurement results of the prototype chip. Section IV concludes this article.

II. CIRCUIT IMPLEMENTATION

Fig. 2 shows the top circuit diagram of the proposed isolated GaN gate driver. The driver consists of a class-D oscillator [9], double spiral transformer, and B2U bridge rectifier, which is for a Si-based technology a common solution of a fully-integrated watt-level power transfer system with on-chip isolation [10], [11], and an additional pull-down network. The realized GaN IC is shown in Fig. 2 and has a total chip area of 1.5 × 1 mm^2 fabricated in a GaN power IC technology of the Fraunhofer IAF [12], [13].

A. VHF OSCILLATOR FOR A COMBINED ISOLATED POWER/DATA LINK

To realize a combined isolated power and data link, a class-D oscillator from [9] with time-variant LC tank is adapted and has an improved power efficiency compared to a class-B oscillator. The mode of operation is described in more detail in [9]. The oscillator provides the RF carrier in the very high frequency (VHF) range from 30–300 MHz, that is on-off keying (OOK)-modulated by the PWM signal and transmitted through the double spiral transformer $L_{1/2}$ [5]. The max. oscillation frequency can be calculated as $f_{OSC,MAX} = (2\pi \cdot \sqrt{L_{1/2PRIM} \cdot C_1})^{-1}$. With designed values of $C_1 \approx 15$ pF (integrated 2DEG-stacked MIM capacitor with capacitance density of 1.2 fF/μm^2 [4], [12], [13]) and $L_{PRIM} \approx 14$ nH, this results in a $f_{OSC,MAX}$ of ∼347 MHz. The drain-source voltage across $Q_{1/2}$ is higher than the max. allowable gate-source voltage, which is why a capacitive coupling through $C_{2/3}$ (1/3 of C_1) is used [5], [10]. This in turn reduces f_{OSC} to ∼200 MHz in combination with the parasitic capacitances of $Q_{1/2}$. The gate width W_G of the transistors $Q_{1/2}$ is 2.5 mm. All HEMTs used in the GaN IC are logic devices with a symmetrical channel design, i.e., gate-source l_{GS}, gate l_G, and gate-drain length l_{GD} are each 1 μm, resulting in a total channel length l_{CH} of 3 μm. The HEMTs do not have a source-connected field plate and have a breakdown voltage of ∼50 V. The bias voltage is realized by a current-mirror $Q_{5/6}$ ($W_G = 5/100$ μm) and the current is adjusted by 2DEG resistors $R_{1/2}$ with a width W/length l of 5/6.5 μm which corresponds to 1.3 times the 2DEG sheet resistance. The turn-off circuitry consists of two further transistors $Q_{3/4}$ ($W_G = 100$ μm), which inverts the output. The transistor Q_7 can be used for an optional amplitude shift keying (ASK), which is often used in half-duplex data communication [11], [14] but was not investigated in this work. The optional ASK detection on the secondary side is not shown in Fig. 2. On the secondary side, the carrier signal is rectified by a common B2U rectifier consisting of four Schottky-barrier diodes (SBDs) $D_{1\text{-}4}$ ($W_G = 1$ mm). The anode-cathode length l_{AC} and the anode length l_A are both 1 μm. The rectifier design and the circuit connected to the output of the rectifier (failsafe pull-down network and input capacitance of the GaN transistors C_{ISS}, here designed for 100 pF) load the transformer differently, which must be taken

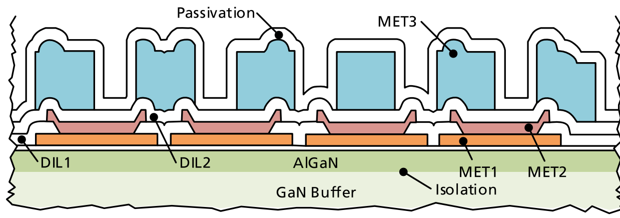

FIGURE 3. Simplified cross-section (not to scale) of the section marked in red in Fig. 2 of the spiral transformer with the metallization's and dielectric interlayers.

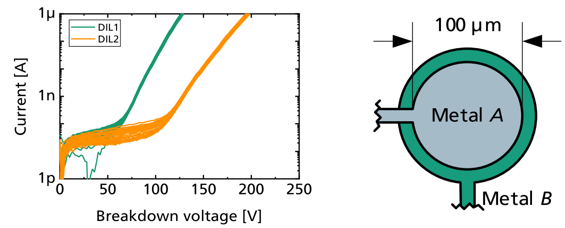

FIGURE 4. Mapped vertical isolation measurements of dielectric interlayers (DILs) of the 37 cells on one 4"-inch wafer of the structure shown on the right.

into account in the transformer design. A design procedure for this is presented in [10] for isolated DC-DC converters. The oscillator is designed for a supply voltage V_{DD} of 6 V and should have a supply current of ~56 mA with a PWM signal of 1 MHz and a duty-cycle of 50%.

B. FAILSAFE PULL-DOWN NETWORK

In the event that the oscillator is not powered or is turned-off by $Q_{3/4}$, a network is required to keep the GaN power transistor in the off-state. The failsafe pull-down network is adapted from [6], [15] and consists of d-mode/normally-on pull-down transistor Q_{10} ($W_G = 2.5$ mm), a clamping circuit consisting of two gate-source short-circuit e-mode/normally-off transistors $Q_{8/9}$ (also known as lateral field-effect rectifiers LFERs) and a 2DEG resistor R_3. The transistors $Q_{8/9}$ have a W_G of 1 mm and the 2DEG resistor a W/l ratio of 10/12.5 μm. The Q_{10} must also be strong enough (i.e., have a low equivalent output resistance) to keep the GaN power transistor in the off-state during dV/dt triggered false turn-on [4].

C. POWER/DATA ISOLATION DOUBLE SPIRAL ON-CHIP TRANSFORMER

The used GaN technology has 3 metallization layers, whereby the gate metallization (MET1) and the interconnect metal (MET2) having a relatively high sheet resistance of ~0.1 Ω/□ and galvanized metallization (MET3) has a significantly lower one of ~0.002 Ω/□. The vertical isolation between the metallization's depends on the SiN passivation thickness and quality, referred to here as dielectric interlayers (DILs). DIL1 is between MET1 and MET2 and has a thickness of 100 nm, while DIL2 is between MET2 and MET3 and is 300 nm thick. Fig. 3 shows a simplified cross-section of the section marked in red in Fig. 2 of one spiral transformer. Isolation measurements are shown in Fig. 4. DIL1/2 has a vertical isolation or breakdown voltage of ~130/200 V. This has a direct influence on the transformer design and isolation class. The GaN technology used has not been specially adapted to achieve a higher insulation class. In the future, a special galvanic isolation thick-oxide backend process for DIL2 similar to [16] can be introduced in the transformer area to increase the isolation rating to >10 kV. Inductive components in this technology and their limitations are investigated in [13], [17]. The transformer is represented as two similar coupled inductors

TABLE 1. Geometrical Parameters of One Spiral Transformer

Spiral	Metal	Turns n	Width w [µm]	Spacing s [µm]	Max. Diameter d [µm]
Primary	3	6	10	7	438/392
Secondary	1	4	20.8	2	446/392

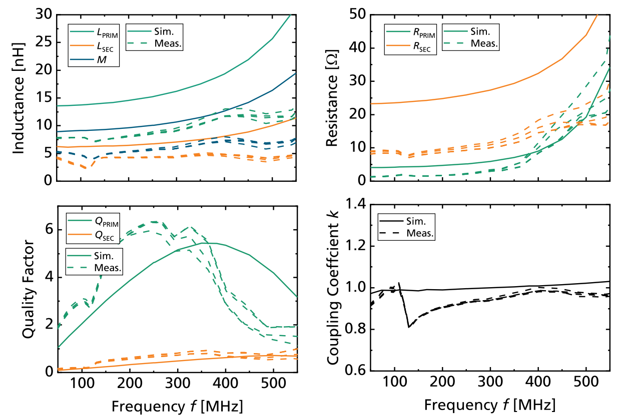

FIGURE 5. Extracted parameters L_{PRIM}, L_{SEC}, M, R_{PRIM}, R_{SEC}, Q_{PRIM}, Q_{SEC}, k (from S-parameter simulation and measurement) of the one spiral transformer $L_{1/2}$.

$L_{1/2}$ with primary L_{PRIM} and secondary L_{SEC} spirals coils. A stacked configuration is used for the transformer. The primary spiral is realized in MET3 and the secondary side in MET1, see Fig. 2. MET2 is used for the return wire of the spirals and to reduce the inductor resistance, as shown in Fig. 2 in the top view and Fig. 3 in the cross-section. The geometrical parameters of one spiral transformer are listed in Table 1. The spiral transformer is optimized with the Momentum 3D planar EM simulator of Advanced Design System ADS for the VHF oscillator, supply voltage and input capacitance of the GaN power transistor and the associated gate-source voltage ratings. The following parameters were extracted from the simulated S-parameters of $L_{1/2}$ as follows $L_{PRIM/SEC}/M = |\text{imag}(Z_{11/22/12})/\omega|$, $R_{PRIM/SEC} = \text{real}(Z_{11/22})$, $Q_{PRIM/SEC} = \omega \cdot L_{PRIM/SEC}/R_{PRIM/SEC}$, $k = M/\sqrt{L_{PRIM} \cdot L_{SEC}}$ and shown in Fig. 5.

III. MEASUREMENT RESULTS

First, 2-port S-parameter measurements are carried out on four one spiral transformer $L_{1/2}$. The structure is measured with two special SG probes and calibrated at on-wafer level. The

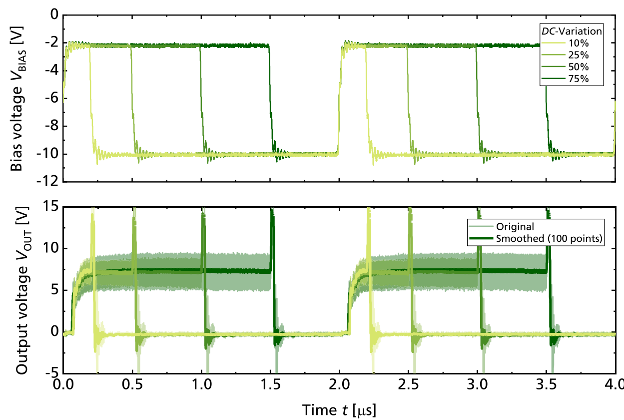

FIGURE 6. Measured bias voltage V_{BIAS} and output voltage V_{OUT} of the isolated GaN gate driver with duty cycle *DC*-variation from 10%-75% at a switching frequency of 500 kHz.

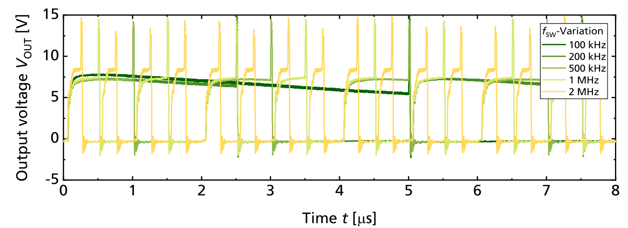

FIGURE 7. Measured output voltage V_{OUT} (smoothed waveforms) of the isolated GaN gate driver with switching frequency f_{SW}-variation from 100 kHz-2 MHz.

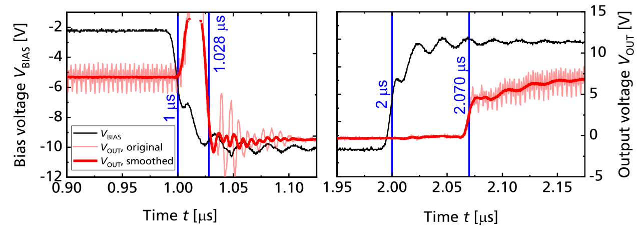

FIGURE 8. Zoom to falling and rising edge of V_{BIAS} and V_{OUT} (left/right axis labeling) at 500 kHz and 50% to determine the propagation delay.

measured S-parameters are transformed into Z-parameters and the extracted parameters are again shown in Fig. 5 (as well as the simulated from Section II-C. The simulated and measured parameters differ, but are of the same order of magnitude. This is due to the choice of a different substrate (SiC compared to Si) and a different GaN buffer structure in the DOE.

The aim is to demonstrate the function of the circuit. The GaN IC was realized in a normally-on GaN technology without a p-GaN gate in comparison to [12], [13] on insulating SiC substrate (typ. $V_{TH} = -2.5$ V), which is why the turn-off circuitry $Q_{3/4}$ and the current mirror $Q_{5/6}$ are not used. The oscillator is turned-on and -off directly via the bias voltage V_{BIAS} and is therefore not inverted as shown in Fig. 2. The PWM therefore corresponds to V_{BIAS} and is provided by a function generator. The circuit is measured on-wafer with two eye-pass probes and one high-voltage needle for V_{DD}, which is additionally buffered with two capacitors (10 μF || 100 nF) very close to the wafer. The voltages on the secondary side are measured with isolated probes. A potentiometer is connected externally between the B2U rectifier and failsafe pull-down network via the probe and set to 1.5 kΩ. The load capacitor (in our case C_{ISS}) is 100 pF, which is roughly equivalent to the input capacitance of a 600 V transistor with on-resistance of 100–200 mΩ. The supply voltage V_{DD} is provided by a source measure unit (SMU) and is set to 8 V.

Fig. 6 shows on-wafer measurements of the bias voltage V_{BIAS} (provided by the function generator) and output voltage V_{OUT} (measured with the isolated probe IsoVu^{TM}) with different duty-cycles *DC* from 10%–75% at a switching frequency f_{SW} of 500 kHz. The oscillation frequency of the oscillator is ~530 MHz, which can be seen on the waveforms on the output volage. Fig. 6 also shows the smoothed (100 points) waveforms. Fig. 7 shows on-wafer measurements of V_{OUT} with different switching frequencies f_{SW} from 100 kHz-2 MHz. The supply current I_{DD} decreases with higher f_{SW}. Fig. 8 shows a zoom to the falling and rising edge of V_{BIAS} and V_{OUT} at f_{SW} = 500 kHz and DC = 50% of Fig. 7. The propagation delay corresponds to 28 ns (high-to-low) and the 70 ns (low-to-high), determined at 50% of the signal amplitude. The fall and rise time are 3.6 ns and 6.1 ns respectively. Overshoots and oscillations can be seen in Figs. 6–8, which can be explained by the on-wafer setup and measurements. The assembly of the GaN IC in a package with a correspondingly closer placement of the decoupling capacitors could solve the problem. With this approach, duty cycles of 0% or 100% can also be achieved. However, small *DC*'s at high frequencies are limited due to the delay times of 70/28 ns. Turn-on times of $<$100 ns must first be verified.

The supply current I_{DD} at V_{DD} = 8 V is very high with several 100 mA, which is why the SMU has achieved the compliance with DC >75%. The reason for the high I_{DD} is that transistor Q_{10} is not completely turned-off in the failsafe pull-down network. Q_{10} turns off if a voltage drops across the clamping circuit consisting of $Q_{8/9}$ and R_3. However, in the normally-on technology there are no p-GaN gates, which is why $Q_{8/9}$ become SBDs, which have a low turn-on voltage V_{T0} of ~1-1.5 V compared to LFERs with V_{T0} of ~1.5-2 V. Thus, a higher current flows via Q_{10} due to the lower voltage drop. In Fig. 8 it can also be seen that the charging process of the output capacitance C_{ISS} continues after the delay time and only reaches the final value after ~150 ns, which is related to the high current flow through Q_{10}. In some GaN-based gate drivers (not isolated), there are high quiescent currents due to static losses [4], which are avoided here and consist only of leakage currents.

Table 2 compares different isolated GaN-based gate drivers/data links. Only data links are realized in [1], [5], [8] by means of voltage pulses (e.g., pulse number, pulse polarity etc.) or by modulated RF signals (e.g., ASK, OOK) [18]. A

TABLE 2. Comparison of Isolated GaN-Based Gate Drivers/Data Links

Reference	[1]	[5]	[6]	[8]	This work
Isolation level	Package	Package	Package	Package	Chip
Isolation method	RF	RF	Inductive	Capacitive	Inductive
Power Link	No	No	Yes	No	Yes
No. of dies	2	2	2	2	1
Technology	GaN	GaN	Si/GaN	Si/GaN	GaN
Max. PWM rate	500 kHz	4 MHz	1.5 MHz	-	≥2 MHz
Propagation delay	>25 ns	30 ns	60-130 ns	7 ns	30-70 ns
Isolation	12 kV_{PK}[1]	12 kV_{PK}[1]	-	20 kV_{PK}	~0.2 kV_{PK}[1]
Supply voltage	5/6 V[2]	6/6 V[2]	8-12 V	-	8 V
Area	2.9 mm^2	2.9 mm^2	-	4.82 mm^2	1.5 mm^2

[1] estimated, [2] TX/RX chip

combined power/data link from [6] uses an OOK with ASK modulation to ensure a higher current or more energy at the beginning of the transistor turn-on. Another possibility for a combined link is to use OOK with edge detection [19]. In this work, only an OOK modulation is used for the combined data/power link due to its simplicity, while a combined solution with ASK modulation could also be used. A special feature of this innovative solution is the chip scale-isolation on a small chip area compared to the state-of-the-art. The max. PWM rate of ≥2 MHz is very high with relatively short propagation delay times. In comparison, the delay times of commercial digital isolators are in the range of 10-30 ns, but sometimes up to 70 ns, which this work also achieves. However, a basis or reinforced galvanic isolation at 10 kV is important for isolated gate drivers. As noted above, the isolation class can be increased by adapting the technology, which is the limiting factor in this current design due to the low thickness of the SiN DIL2 of only 300 nm. With a thick-oxide backend process, the circuit and the transformer would have to be adapted accordingly. Another important parameter for isolated GaN gate drivers is the common-mode transient immunity (CMTI), which is in the order of 200 kV/μs due to the fast-switching GaN transistors [5]. With package-integrated isolated drivers based on RF-signals, this can be ensured quite simply by ensuring a proper distance through isolation (DTI), for example 250 μm between transmitter (TX) and receiver (RX) chip for 12.5 kV isolation rating [1], [5]. The basis for this is the assumption is that typical molding compounds have a dielectric strength in the range of 50–100 kV/mm [1]. A high CMTI for chip-scale isolation approaches is more difficult to achieve and must first be measured for this work. However, for this isolated GaN gate driver, it can be assumed that the CMTI will not be high due to the relatively large coupling capacitance of the micro-transformer in the single-digit pF-range at ≥500 MHz, which can be simulated and extracted from the S-parameter measurements (see Fig. 5). This is also directly related to the currently low isolation voltage. Finally, the isolated GaN driver of this work must also be combined and demonstrated with a power transistor. This final demonstration can then be used to correctly evaluate the galvanic isolation rating and CMTI performance considering both the assembly and the specific application. What is shown, however, is that isolated gate drivers can be integrated into GaN with included power link to drastically reduce the PCB area needed to drive floating GaN power transistors in the future.

IV. CONCLUSION

In this work, a monolithically integrated and galvanically isolated GaN gate driver is proposed, which has a combined power and data link. The operation principle and the circuit design with integrated transformer are described. In this work, the layout was fabricated and investigated in a normally-on GaN-on-SiC technology. The spiral transformer was simulatively optimized and characterized and its parameters extracted. The isolated driver was operated at different duty-cycles and switching frequencies up to 2 MHz and achieves a low propagation delay time at a supply voltage of 8 V and capacitive load of 100 pF. Thus, this novel isolated GaN-based driver solution shows a possibility to reduce the PCB area requirement for isolated interfaces in the future.

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