Toward consistent circuit-level aging simulations in different EDA environments

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***Abstract*—Aging simulations on circuit level allow integrated circuit (IC) designers to verify their circuits with respect to lifetime reliability requirements by considering the degradation of field effect transistors (FETs). To obtain significant analysis results with a reasonable effort, two prerequisites have to be fulfilled. First, reasonable models for FET degradation effects have to be set up. Second, the models have to be implemented into electronic design automation (EDA) environments. In this work, we demonstrate that degradation models can be implemented consistently in different EDA environments by using tool-specific and generic modeling interfaces. Furthermore, we compare the behavior of selected environments based on simulation studies with example degradation models for bias temperature instability (BTI) and hot carrier injection (HCI).**

I. INTRODUCTION

Emerging applications, such as autonomous driving and Industry 4.0, demand for integrated circuits (ICs) with an enormous computing power at a very high reliability [1]. These diametrical requirements should be considered in IC design projects to ensure meeting the product specifications.

Circuit-level aging simulations are a particular feature to verify ICs for potential lifetime reliability issues, and they are available in multiple tools and environments for electronic design automation (EDA) (e.g. [2], [4], [5]). They extend standard circuit simulations to analyze the impact of the degradation of field effect transistors (FETs) on circuit performance. To use this feature during IC design, semiconductor foundries need to characterize the FET aging and implement corresponding models into their process design kits (PDKs). The EDA tools offer own built-in models for FETs aging, but they are tool specific and, partially, confidential. Hence, to support multiple EDA tools, foundries have to extract multiple aging models, which causes an enormous effort and leads to undesired inconsistencies. They can be overcome by implementing custom aging models into tools-specific application programming interfaces (APIs) provided by the simulators. From a foundry perspective, two major tasks have to be addressed to provide reasonable aging models. First, feasible models have to be defined and parametrized based on measurement data with a sufficient accuracy at an acceptable effort. Second, the models have to be consistently implemented into multiple EDA environments and tools. The work presented in this paper is focused on the model implementation by setting up and evaluating example aging models for bias temperature instability (BTI) and hot carrier injection (HCI) in different simulators and by using their specific reliability APIs as well as the upcoming standard interface Open Model Interface (OMI). We run simulation studies and check the different variants with respect to the accuracy of the results of the simulations.

II. BRIEF REVIEW OF TRANSISTOR DEGRADATION

BTI and HCI are FET degradation mechanisms where a gradual charge accumulation in or near the gate oxide dielectric leads to a gradual change of the FET characteristics, mostly to a gradual reduction of drain currents with FET operation time. As a change in FET characteristics puts at risk the functioning of electronic circuits, a proper degradation modeling and circuit aging analysis is essential.

BTI is a major concern for p-channel FETs (PFETs), where it is referred to as negative BTI (NBTI) due to large negative gate-source voltages V_{gs} or elevated temperatures triggering the capture of channel carriers into pre-existing or newly generated oxide defects. A reduction of V_{gs} results in a partial recovery of the BTI degradation. In the context of high-k metal gate technologies, BTI occurs also in n-channel FETs (NFETs) –positive BTI (PBTI) due to being driven by positive gate-source voltages V_{gs}– and often is less pronounced than NBTI.

High lateral electric fields activate HCI degradation: through acceleration, a fraction of channel carriers becomes fast enough to destroy hydrogen-passivated bonds at the oxide interface. Depending on the inversion state, i.e. on V_{gs}, bond destruction is an individual or a collective effort of carriers. As the carrier acceleration involves several scattering processes with different temperature dependencies, the overall HCI temperature dependence can be complex, and a higher temperature can increase or reduce HCI degradation.

Traditionally, experimental constant-stress degradation data is fitted to ansatzes [6],

$$\Delta_1(V,T,t) = A\ \exp\left(\frac{E_{aa}}{kT}\right) V^m t^n, \tag{1}$$

or similar, using an Arrhenius temperature activation with energy E_{aa} and power-law voltage and time dependences.

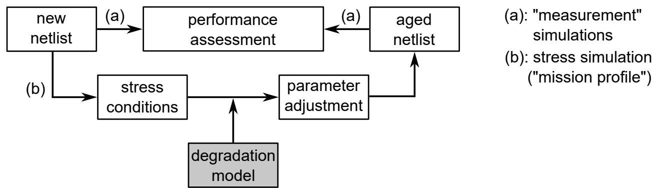

Fig. 1. Flow of circuit-level aging simulations

The ansatz can be generalized to include the experimentally observed saturation of degradation

$$\Delta_2(V,T,t) = \frac{\Delta_1(V,T,t)}{1 + B\ \Delta_1(V,T,t)}, \tag{2}$$

with a saturation level $1/B$. For both ansatzes, convenient generalizations to time dependent stress exist [7], [8].

When looking for high accuracy, degradation models can be extended to include additional features. They may include BTI recovery [9], [10] and variability [11]; voltage-dependent time exponents [12]; full deformation of FET direct current (DC) characteristics; or full dependence on V_{gs} and V_{ds} at HCI.

On the other hand, the accuracy of circuit aging simulations can depend on the model implementation, especially when comparing simulation results obtained from different environments. Potential issues are the availability of identical degradation models in different environments, consistent choice of the time discretization in transient simulations and details on the feed-back of degraded parameters to FET models and circuit simulations.

III. Consistent implementation of degradation models in multiple EDA environments

Fig. 1 depicts a typical aging simulation flow, in which a “new netlist” represents the circuit at time 0. From transient simulations that assume particular usage scenarios (often referred to as “mission profiles”), the stress conditions per FET are extracted in terms of voltages and currents and, potentially, temperatures. Degradation models process the stress information for each individual FET and convert them into adjustments of selected parameters of the underlying device model. With the adjusted parameters, an “aged netlist” is generated to represent the circuit after a pre-defined time of operation. Its simulation allows predicting the performance of the aged circuit and hence assessing the circuit lifetime.

Along with offering aging simulations capabilities, EDA tools usually provide basic transistor degradation models, but they are tool specific and not consistent among different simulators as well as possibly oversimplified or confidential. Furthermore, model extraction procedures are not necessarily publicly available.

For these reasons, it is hard to assess whether a built-in transistor aging model is feasible for a particular semiconductor technology. Furthermore, it appears impossible to consistently support aging simulations in multiple design environments, which can be a serious issue for foundries. These

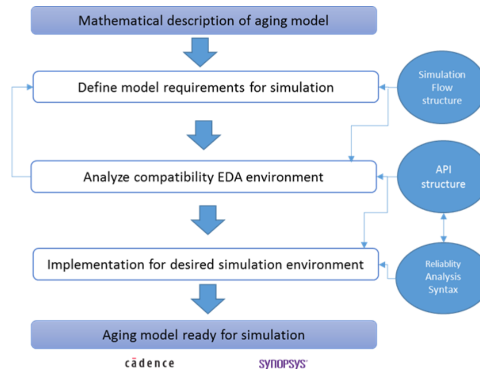

Fig. 2. Necessary steps to integrate aging models across different EDA environments

disadvantages of the built-in transistor aging models can only be overcome by custom models.

EDA tools provide APIs to define and integrate user-defined transistor aging models into their simulation flow. The APIs are a set of functions and data structures in C (programming language) that allow the implementation of the mathematical description of the aging model as well as the exchange of data between model and circuit simulator. Through the API, the model has access to the information it needs to compute the degradation (stress conditions on fresh simulation, model card parameters and reliability control statements) and can send back the degraded parameters to the simulator. As the built-in degradation models, reliability APIs are tool specific. An improved interaction between simulators and aging models is targeted by the emerging OMI API [3].

As outlined in Section II, the implementation of the aging model can have a significant impact in the model accuracy and performance. Since the internal structures of the APIs, as well as the aging simulation flows differ among EDA tools, it is important to follow a methodology, such as the one shown in Fig. 2, to be able to deliver consistent results across different simulators using the same mathematical model description.

First, it is necessary to evaluate and determine the requirements that have to be fulfilled in order to perform an aging degradation calculation in a circuit level simulation. This includes the information that needs to be collected from the simulation environments, available control settings; how the model can back-annotate the information on transistor degradation, and the type of analyses that are supported by the aging models.

Once the requirements are set, a compatibility analysis is performed. To ensure that all requirements can be met, the individual API capabilities are examined with respect to accessing the relevant information from the simulator and how to adapt all parameters that are described by the aging model. Following this approach with a particular aging model, allows to determine if is possible to implement this transistor aging model consistently across multiple design environments and tools. This will be demonstrated by a case study on NBTI and HCI degradation in IV.

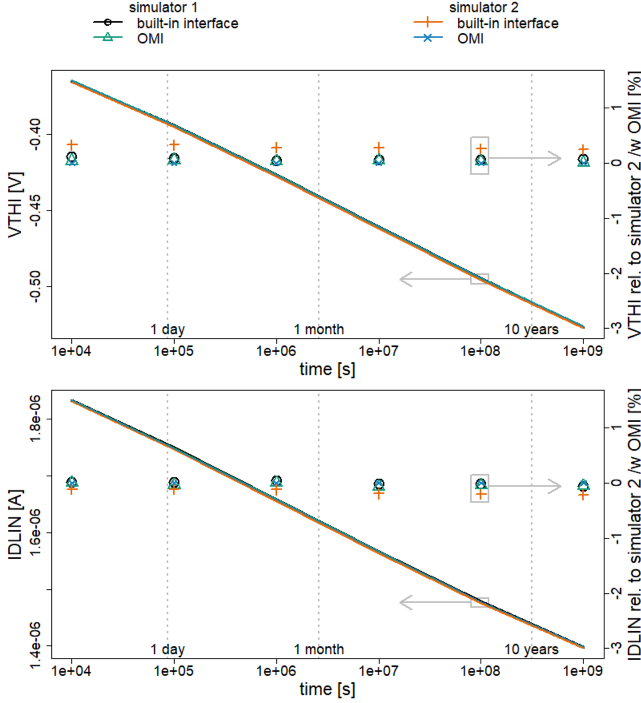

Fig. 3. VTHI and IDLIN of PFET under NBTI

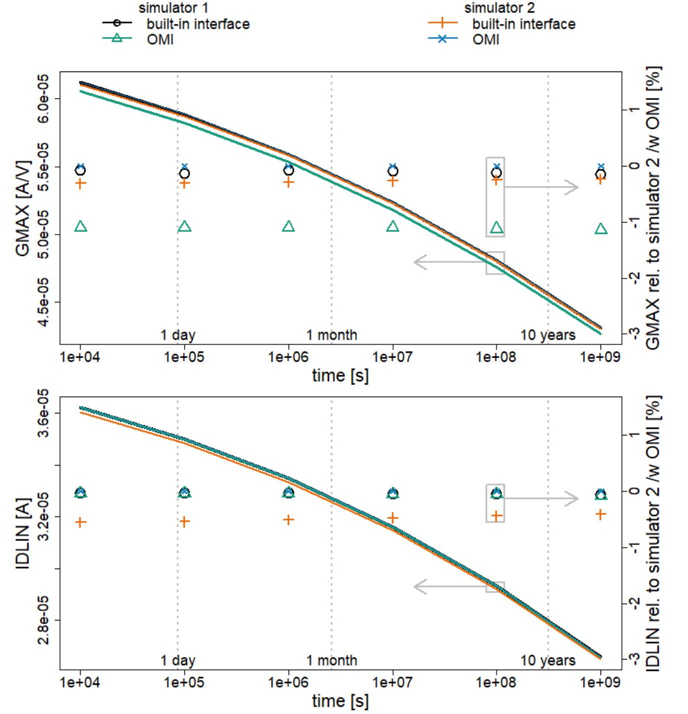

Fig. 4. GMAX and IDLIN of NFET under HCI

IV. Simulation Study and Comparison

The simulation in this study is perform on the basis of 130nm BSIM4 Predictive Technology Models (PTM) for bulk complementary metal-oxide-semiconductor (CMOS) [13]. To closely relate them to previous results achieved by our group in the ADMONT research project [14], transistor degradation is expressed by adapting selected parameters of the underlying BSIM4 model. Furthermore, the approach in Eq. (2) to model FET degradation is applied along with the implementation scheme from [7]. NBTI degradation is mapped of PFETs by shifting the BSIM4 parameter vth0 according to

$$\mathrm{vth0_{aged}} = \mathrm{vth0_{fresh}} - \Delta\mathrm{vth0}, \tag{3}$$

with $\mathrm{vth0_{fresh}} = -0.321$ from the model card and Δvth0 from Eq. (2) with $A = 2.915$, $E_{aa} = -0.2$, $m = 3.5$, $n = 0.15$, and $B = 3$. Similarly, the HCI degradation of NFETs is expressed by adapting the BSIM4 parameter u0 according to

$$\mathrm{u0_{aged}} = \mathrm{u0_{fresh}} - \Delta\mathrm{u0}, \tag{4}$$

using Eq. (2) and,

$$\Delta_1 = A\ \exp\left(\frac{C}{V_d}\right) t^n, \tag{5}$$

with: $\mathrm{u0_{fresh}} = 0.05928$ from the model card with $A = 3.215$, $C = 8.15$, $n = 0.12$, and $B = 13$.

As described in Sec. III, these models were implemented into the URI API of Cadence, the MOSRA API of Synopsys, and OMI. In the following, they will be referred as "simulator 1" and "simulator 2", with their built-in APIs and OMI.

Our simulation study contains the following scenarios: the degradation of electrical figures of merit of single PFET and NFET devices as well as the degradation of the frequency of two different ring oscillators (ROs). In the simulations, we keep all device geometries constant at $L = 260$ nm and $W = 520$ nm.

For PFET NBTI, we stress a PFET instance at $T = 175$ °C as well as $V_{\mathrm{gs}} = -1.2$ V, and observe the evolutions of the threshold voltage VTHI (V_{gs} that causes $I_{\mathrm{d}} = 100$ nA $\cdot\, W/L$ at $V_{\mathrm{ds}} = 0.05$ V) and the linear current IDLIN (I_{d} at $V_{\mathrm{gs}} = -1.2$ V and $V_{\mathrm{ds}} = 0.05$ V). For NFET HCI, we stress an NFET instance at room temperature as well as $V_{\mathrm{ds}} = 1.2$ V, and observe the evolutions of the maximum transconductance GMAX (at $V_{\mathrm{ds}} = 0.05$ V) and the linear current IDLIN.

Figures 3 and 4 respectively show the degradation results for the PFET and the NFET, along with the difference between simulators after arbitrary choosing simulator 2 and OMI as the reference. The largest difference can be seen in HCI GMAX degradation, with a maximal variation of around 1.0 %. For the other figures of merit, the degradations are practically identical, with discrepancies clearly below 1.0 %.

This study continues with two ROs with 3 and 21 inverter stages, forced into oscillation in the simulations by applying reasonable initial conditions. Based on aging simulations, we investigate the expected frequency degradation due to the RO operation at $V_{\mathrm{dd}} = 1.2$ V. The 3-stages RO was aged using the HCI model at $T = 27$ °C, while the NBTI model was used to degraded the 21-stages RO at $T = 175$ °C. The results are shown in Fig. 5 and Fig. 6. As in the case for single

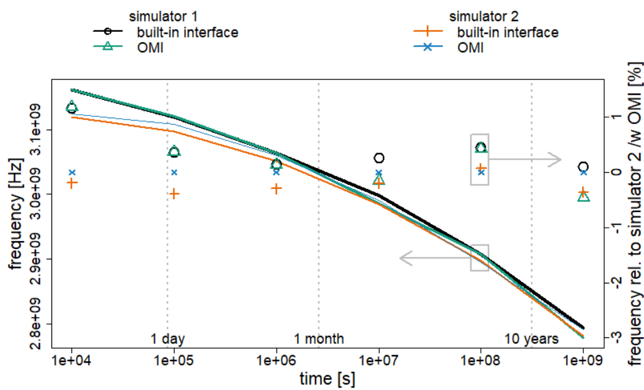

Fig. 5. Frequency degradation of the 3-stages RO under HCI aging.

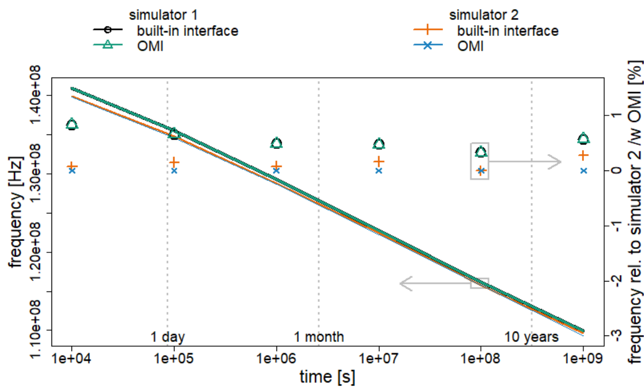

Fig. 6. Frequency degradation of the 21-stages RO under NBTI aging.

transistors, the degradation over time nearly coincide across all the simulators, with a maximal deviation within 1.5 % for the 3-stage ROs and 1.0 % for the 21-stages RO. The difference seen between simulators can be reduced further by fine-tuning the simulator considering time discretization in the transient analysis, internal accuracy of the simulators and signal measurement and control options.

In this study, the transistor degradation was model by adjusting selected model card parameters of the transistor. Larger differences in the results have to be expected when transistor degradation is modeled by subcircuits, e.g. consisting of controlled sources, around the unchanged transistor, since the APIs offer different capabilities in this regard. For example, some API´s have a subcircuit approach, in which external current or voltage sources can be added to the transistor to model the degradation, while others allows to internally change the electrical characteristics of the transistor. The main difference in performance in this study between “simulator 1” and “simulator 2” was the level of support for the OMI model, with one of the simulators showing a better integration to the external API

V. Summary & Conclusions

Aging simulations allow the verification of lifetime reliability for integrated circuit (IC) designs before manufacturing, and their importance is expected to rise due to multiple emerging application fields. Semiconductor foundries face the challenges of: (1) defining reasonable degradation models based on their lifetime reliability data, while trading of accuracy, complexity, and characterization effort and, (2) assuring consistency of the models delivered in their process design kit (PDK), so they yield identical results in different electronic design automation (EDA) environments.

This work focused on the consistent implementation of degradation models in different EDA environments by using their built-in application programming interfaces (APIs) and the emerging standard interface OMI. By applying advanced modeling approaches for negative BTI (NBTI) and hot carrier injection (HCI), we demonstrated that these models can, indeed, be implemented consistently, usually with deviations below 1 %. Fine tuning of simulator accuracy settings and numerical methods probably leads to even smaller differences when required. However, a detailed study of simulator and API performance, especially with larger circuits, remains a subject to future work.

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