Direct Growth of III-V/Silicon Triple-Junction Solar Cells with 19.7 % Efficiency

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Abstract—Monolithic multi-junction solar cells made on active silicon substrates are a promising pathway for low-cost high-efficiency devices. We present results of GaInP/GaAs/Si triple-junction solar cells, fabricated by direct growth on silicon in an MOVPE reactor using a GaAs,P$_{1-y}$ buffer structure to overcome the lattice mismatch between Si and GaAs. A low temperature (750 °C) Si surface preparation process and a SIN$_n$ diffusion barrier at the rear side have been implemented to maintain the minority carrier lifetime in the Si bottom cell. Conversion efficiencies up to 19.7 % have been achieved under AM 1.5g spectral conditions. The cells are compared to identical GaInP/GaAs dual-junction solar cells grown on bulk GaP and GaAs substrates to identify loss mechanisms. Subcell electrical characterization using electroluminescence reveals a significant voltage loss of the III-V subcells on Si, compared to the same structures grown on GaP or GaAs. Electron channeling contrast imaging of the metamorphic GaAs,P$_{1-y}$ buffer shows a three times higher threading dislocation density on Si (1.4×10$^6$ cm$^{-2}$) than on GaP substrates, and atomic force microscopy shows holes in the GaAs,P$_{1-y}$ buffer on Si that are not observed on GaP. Approaches to reach lower defect densities for the III-V layers on silicon are discussed.

Index Terms—multi-junction solar cell, semiconductor materials, III-V on silicon, MOVPE, OMVPE

I. INTRODUCTION

Combining high-quality III-V semiconductors with Si substrates for solar cell applications has been a major research goal for several decades. The approach of building III-V cells on top of active silicon solar cells is attractive due to the high efficiency potential of such multi-junction devices and the low cost of Si substrates. To date, III-V multi-junction solar cells reach the highest sunlight to electricity conversion efficiencies of up to 38.8 % under 1-sun AM1.5 global irradiation [1], and 46.1 % under the concentrated AM1.5 direct spectrum [2]. However, these high efficiency solar cells have only been achieved on expensive Ge, GaAs or InP substrates. Using Si as a substrate for high efficiency multi-junction devices is a promising pathway for decreasing the cost significantly in order to get competitive to state-of-the-art single-junction Si solar cells. In addition, Si has a near-optimal bandgap for the bottom subcell of several multi-junction designs and it can therefore act simultaneously as an active subcell.

The standard III-V alloys with useful bandgaps for Si-based multi-junction cells (such as GaInP, GaAsP, and GaAs) have lattice constants that are approximately 3 - 4 % larger than Si, making material integration a challenge. There have been two successful strategies for overcoming this lattice mismatch: using an epitaxial buffer structure (direct growth) or bonding/gluing/mechanical stacking. By stacking a GaInP/GaAs dual-junction cell onto a Si subcell and operating the device in four-terminal mode, Essig et al. reached a conversion efficiency of 35.9 % [3]. However, the four-terminal operation makes module integration more complex. Cariou et al. achieved conversion efficiencies up to 33.3 % for a two-terminal GaInP/GaAs/Si device using the approach of direct wafer bonding [4]. Bonding is well suited to combine semiconductors with different lattice constants but is quite demanding from a technological point of view. The surfaces have to be extremely smooth and free of particles. Thus, an additional expensive polishing step is required usually.

Direct growth of III-V materials on Si, on the other hand, is the most straight forward approach. But additional challenges are associated with the transition from the non-polar Si to polar III-V crystals [5]. Furthermore, the minority carrier lifetime of the Si substrate has to be maintained during the high temperature growth of the III-V layers [6]. And finally, the difference in thermal expansion coefficients of Si and various III-V alloys may lead to crack formation especially in the case of thick layer structures [7]. Direct growth of GaAs on Si has been studied in detail, but most crystals suffered from high threading dislocation densities above 10$^6$ cm$^{-2}$ [8] without additional treatment like thermocycling. During the last decade, high-quality, anti-phase domain-free GaP layers on Si substrates, which can serve as templates for the growth of III-V solar cells, have been developed by multiple research groups [9]-[11]. GaP has a low lattice mismatch to Si (0.4 % at room temperature) and therefore is a promising transition layer from Si to III-V crystals. By growing a GaAs,P$_{1-y}$ buffer onto such a GaP/Si template Yaung et al. reached a defect density of 4.0-4.6×10$^6$ cm$^{-2}$ for GaAs$_{0.77}$P$_{0.23}$ [12] and Grassman et al. stated a density in the mid to upper 10$^6$ cm$^{-2}$ range for GaAs$_{0.96}$P$_{0.04}$ [13].

Several results have been reported for III-V solar cells on passive Si substrates [12], [14]-[16], but only very few results are available which show the successful implementation of an active Si bottom cell in III-V multi-junction devices using the direct growth approach [13], [17], [18]. One reason is the strong degradation of minority carrier lifetime in the Si substrate during high-temperature treatments which are
necessary for the III-V growth [6]. Soga et al. reached a conversion efficiency of 21.2 % under the AM0 spectrum for an AlGaAs/Si dual-junction cell in 1997 [17] which still represents the highest published value for a directly grown III-V multi-junction solar cell including an active Si bottom subcell. Recently, Grassman et al. have achieved remarkable results and showed the first successful integration of a triple-junction GaInP/GaAsP/Si and a dual-junction GaAsP/Si solar cell on an active Si substrate [13]. However, the performance of these early-stage devices is limited by a high dislocation density above 10⁷ cm⁻², an unbalanced current distribution and a degraded Si bottom cell in the case of the triple-junction device.

In this paper we present the development of a Ga₃₀.₅₁In₀.₄₉P/GaAs/Si triple-junction solar cell which is directly grown by metalorganic vapor phase epitaxy (MOVPE) onto a Si bottom cell with a diffused pn-junction. SiNx is used as a diffusion barrier on the rear surface of the wafer to prevent degradation of the minority carrier lifetime in the Si subcell. A metamorphic GaAsPₓᵧ buffer structure allows increasing the lattice constant from Si to GaAs and serves as template for the growth of the III-V solar cell layers. Results are compared for Ga₁₋₅₁Inₓ₋₄₉Pₓ₋₄₉/GaAs cells on active Si and bulk GaP (including the GaAsPₓᵧ buffer) as well as on GaAs substrates. This allows identifying the origin of losses. A detailed characterization of both the subcell electrical parameters and the crystal quality is performed and a clear pathway towards higher device efficiency is described.

II. Experimental Procedure

The device structures of the three multi-junction solar cells discussed in this paper are shown in Figure 1. For the cells on Si, single-side polished 4-inch 300 μm thick p-type float-zone (100) Si wafers featuring a 2° offcut towards <111> and a resistivity of 2 Ωcm were used. After an RCA cleaning procedure a phosphorous diffusion process (POCl₃) was performed at 790 °C for 60 min to form an n-Si emitter on the front side followed by a high-temperature drive-in step at 1050 °C for 60 min resulting in a 120 Ωsq.cm emitter. The backside of the Si wafer was coated with 5 nm Al₂O₃ via plasma-assisted atomic layer deposition capped by 70 nm SiNₓ via plasma-enhanced chemical vapor deposition. This layer stack is known to provide a low surface recombination velocity [19] and simultaneously serves as a diffusion barrier against impurities from the susceptor in the MOVPE reactor chamber [6]. MOVPE growth was performed in three separate processes and in two different reactors. The GaP nucleation layer and the step-graded GaAsₓᵧ buffer structure were deposited in a CRIUS Close Coupled Showerhead reactor from AIXTRON in a 7x4 inch wafer configuration. The GaP nucleation was performed with the reactor in a clean state with minimal III-V material deposition on the reactor walls. Before loading the substrates into the MOVPE chamber the native oxide was removed by diluted HF (1 %). The in-situ Si surface preparation was performed at 750 °C in order to preserve the Si lifetime. Details of the process including the low-temperature flow-modulated GaP nucleation have been presented in a previous publication [20]. Note that the wafers were loaded out and again into the reactor chamber between the GaP deposition and the GaAsₓᵧ buffer growth. During the buffer growth, a 2 inch n-GaP (100) wafer featuring a 2° offcut towards <111> was loaded additionally for direct comparison of results on both substrates. The step-graded GaAsₓᵧ buffer structure was grown at 700 °C surface temperature (measured via pyrometry) applying a V/III ratio of 10.

![Diagram of multi-junction solar cells](Figure 1: Structure of three different types of multi-junction solar cells on Si, GaP and GaAs substrates which are investigated in this paper.)

Triethylgallium (TEGa), arsine (AsH₃), phosphine (PH₃) and silane (SiH₄) were used as precursors. The buffer consists of 14 individual layers with a thickness of 120 nm, resulting in a grading rate of ~2.4 %/µm. We achieved nominally homogeneous changes in composition from layer to layer by first calibrating the nonlinear mixed anion incorporation. The surface layer was GaAs but due to the grading of the lattice, the in-plane lattice constant (0.5644 nm) was 0.16 % smaller than for a GaAs bulk crystal (0.5653 nm). Some of the samples were set aside after the buffer growth for materials characterization, described later, and did not go through the remaining process steps. The other samples were transferred to an AIX2800 planetary reactor from AIXTRON in an 8x4 inch wafer configuration. A transparent 350 nm thick Alₓ₋₀.₉₀Gaₓ₋₀.₉₀As₀.₀₇ layer was deposited at 640 °C as an overshooting layer to relax the in-plane lattice-constant and avoid any further formation of misfit dislocations during the growth of the solar cell layers. For the tunnel-junctions, a p⁺ AlGaAs/n⁺-GaInP hetero structure was implemented. The Ga₉₀.₅₁In₀.₄₉/P/GaAs (nominal composition) tandem cell was grown at 640 °C with a total thickness of 0.63 µm (GaInP) and 1.2 µm (GaAs), respectively. The accumulated thickness of deposited III-V material on the Si substrate is 4.75 µm which did not lead to formation of cracks in any of the process steps. As a reference, the same cell structure (without buffer) was grown on a 4 inch GaAs (100) substrate featuring a 6° offcut towards <111>°A. In the case of the 4 inch Si and GaAs substrates, the wafers were processed to solar cell devices with an area between 0.05 and 4 cm² via standard photolithographic methods including a wet-chemical mesa etch for III-V and Si (in the case of Si substrate). On the 2 inch GaP wafer, cells with an area between 0.05 and 1 cm² were processed. A dual-layer anti-reflective coating consisting of
Ta₂O₅ and MgF₂ was applied to the front surface of all cells to reduce optical losses. The backside of the triple-junction device on Si was covered by 2 μm of aluminum followed by a laser fired contact process [21] to form local ohmic contacts to the p-Si wafer through the SiNx and Al₂O₃ layers. This structure allows for the backside of the p-Si wafer to be passivated and at the same time have local ohmic contacts without the need for removal of any of the layers. On the backside of the other two cell structures full area Pd/Au/Ge/Ti/Pd/Ag/Pd ohmic contacts were evaporated.

The solar cells were characterized in the CalLab at Fraunhofer ISE using a 3-zone solar simulator adjusted to AM1.5g spectral conditions. Spectral mismatch factors were determined from external quantum efficiency (EQE) measurements. The best cell on each wafer was selected for detailed investigation. During the I-V measurement of the triple-junction solar cell on the active Si substrate a mask was applied to avoid the generation of excess current in the Si solar cell outside of the dedicated cell area. Electroluminescence measurements were taken on small concentrator cells (0.05 cm²) on the same wafers to extract subcell voltages of the multi-junction devices. The electroluminescence data was calibrated via I-V measurements under concentration.

For material characterization, the samples, which were put aside after the GaAsP₁₋ₓ buffer growth, were investigated by electron channeling contrast imaging (ECCI) and atomic force microscopy (AFM). ECCI measurements were performed in a Hitachi SU-70 scanning electron microscope equipped with a four quadrant backscatter detector. The images were taken under g=(040) diffraction conditions. A Park XE-150 AFM setup in non-contact mode was used to characterize the surface morphology. In addition, we carried out high resolution scanning transmission electron microscopy (STEM) using an aberration corrected JEOL JEM-2200FS operated at 200 kV. The imaging mode applied utilizes the so called low angle annular darkfield (LAADF) in which the scattered transmitted electrons are collected by a ring shaped detector. In order to visualize the effect of lattice distortions we have chosen an inner detection angle of about 38 mrad and a sampling of 70 pm/pixel.

III. RESULTS AND DISCUSSION

A. GaInP/GaAs on GaAs and on GaP

The impact of the GaAsP₁₋ₓ buffer structure on the performance of the GaInP/GaAs tandem cell is studied by comparing the GaInP/GaAs structure on GaAs and on GaP substrates. I-V measurements are shown in Figure 2. The black squares represent the values of the GaInP/GaAs on GaAs reference design. The characteristic values are listed in Table 1. An open-circuit voltage of \( V_{OC} = 2.41 \) V, a short-circuit current density of \( J_{SC} = 12.7 \) mA/cm² and a fill factor of FF=88.3 % result in a conversion efficiency of \( \eta = 27.0 \% \) under AM1.5g spectral conditions. When the nominally same GaInP/GaAs cell structure is grown on the metamorphic GaAs on GaP virtual substrate, a significant decrease in performance is observed. The open circuit voltage drops by 370 mV to \( V_{OC} = 2.04 \) V and the short-circuit current density decreases to \( J_{SC} = 11.0 \) mA/cm². A significant parallel resistance which can be seen in the negative slope of the I-V curve (red open circles) leads to a decreased fill factor of FF=78.1 %. The reason for this low shunt resistance has not been identified yet but it could be correlated to a high density of threading defects resulting in current path with lower resistance. The resulting conversion efficiency of \( \eta = 17.5 \% \) is much lower than the value of the reference structure on GaAs.

The best cell on each wafer was selected for analysis. The observed losses, EQE measurements for the final devices and ECCI measurements after the GaAsP₁₋ₓ buffer growth on GaP were performed. The latter one enables the direct determination of the threading dislocation density at the end of the GaAsP₁₋ₓ grading. The obtained image (with locally enhanced contrast) is shown in Figure 6b). The threading dislocation density on the shown image is \( 4.9 \times 10^7 \) cm². As those threading dislocations will penetrate through the active regions of the subsequent GaInP/GaAs cell, the diffusion length and hence the open-circuit voltage is limited by those crystal defects. This explains the observed decrease in device performance. The EQE measurements in Figure 3 (integrated current densities are inserted) reveal a significant decrease of the quantum efficiency for the structure on GaP compared to GaAs. The GaInP cell shows an average decrease of 9 % and the GaAs cell an even stronger average decrease of 13 % in. These results correlate with a degradation of the diffusion length throughout the GaInP top and GaAs middle cell which is expected for the high dislocation density observed after the buffer growth.

![Figure 2: Light I-V data for the GaInP/GaAs/Si triple-junction and the GaInP/GaAs dual-junction solar cells on GaP and GaAs substrates. The measurements were performed under calibrated AM1.5g spectral conditions.](image)

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B. GaInP/GaAs/Si

The GaInP/GaAs/Si triple-junction cell structure features the same GaInP/GaAs top cell structure as the tandem devices discussed in the previous section. However, the substrate is different. By investigating this cell structure, the influence of the GaP on Si nucleation layer on the performance of the GaInP/GaAs tandem cell can be determined. Since it is a triple-junction device, the characteristic values like open-circuit voltage, short-circuit current density and fill factor cannot be compared directly. However, the EQE which is shown in Figure 3 can be compared. The GaAs sub-cell (600<λ<860) shows exactly the same behavior for both metamorphic GaInP/GaAs/Si and GaInP/GaAs on GaP devices. Small differences are only observed in the short wavelength part between 300 nm and 650 nm where the light is absorbed in the GaInP top cell. These differences are not considered to be significant and it can be concluded that the metamorphic growth on GaP or Si leads to similar device characteristics in terms of quantum efficiency. The EQE of the Si bottom-cell (λ > 900 nm) peaks at 90 % and maintains a high value in the long wavelength region due to the Al$_2$O$_3$/SiN$_x$ passivation stack on the backside. The short-circuit current densities of the subcells have been calculated under AM1.5g spectral conditions by integration of the EQE. The lowest current density of 10.0 mA/cm$^2$ is found for the Si bottom cell. This junction consequently limits the overall current and conversion efficiency of the triple-junction device. The GaInP top cell has a current density of 13.0 mA/cm$^2$ resulting in a strong current mismatch. This explains the high fill factor of 84.3 % in comparison to similar published devices [4], [13], [16]. The I-V measurement (see Figure 2, blue triangles) and the open-circuit voltage of $V_{oc}$=2.32 V confirm the successful integration of the Si bottom cell in the GaInP/GaAs/Si triple-junction device. To compare the open-circuit voltages of the individual sub-cells, EL measurements were performed. The evaluated data is shown in Figure 4.

![Figure 4: Subcell voltages as a function of the current density (proportional to sunlight concentration) extracted from electroluminescence measurements for the GaInP/GaAs/Si triple-junction, GaInP/GaAs on GaP and GaInP/GaAs on GaAs dual-junction reference devices.](image)

For the structure on GaAs, EL signals were obtained for a wide range of current densities (13 to 6540 mA/cm²). Due to enhanced non-radiative recombination, the structures on GaP and Si showed measurable EL signals only for high current densities. As expected, the reference structure on GaAs (black squares) has the highest voltages for the GaInP and GaAs subcells. The subcell voltages for the metamorphic structure on GaP (red open circles) are significantly lower but increase slightly faster with higher current densities than in the case of the reference structure on GaAs. This can be explained by saturation of non-radiative recombination centers at higher irradiation intensities. This effect is even more pronounced for the GaInP cell in the GaInP/GaAs/Si structure (blue triangles) which starts at even lower values for the open-circuit voltages. This is in contrast to the EQE which did not show any significant difference between the structures grown on GaP and Si.

To identify the origin of the even lower sub-cell voltages, STEM, ECCI and AFM measurements were performed on the GaAs$_{0.5}$P$_{0.5}$ buffer of the structure on Si. The LAADF STEM cross-sectional image is shown in Figure 5. Most dislocations are located at the interfaces of the individual layers. However, there are several threading dislocations visible which penetrate into the active GaAs layer. In order to determine the threading dislocation density accurately, ECCI (plane-view) measurements of the final layer of the GaAs$_{0.5}$P$_{0.5}$ buffer were performed. The image shown in Figure 6a) reveals a threading dislocation density of $1.4\times10^5$ cm$^{-2}$, a factor of three higher compared to the structure on GaP. Other researchers have also found an increased threading dislocation density for GaAs$_{0.5}$P$_{0.5}$ buffers on Si compared to GaP [12], [22]. They assume that different dislocation dynamics lead to the observed effect. AFM scans, see Figure 7a), additionally show pits with a depth exceeding 500 nm after the GaAs$_{0.5}$P$_{0.5}$ buffer growth on Si. Such holes are not found for the same buffer on GaP as shown in Figure 7b).

![Figure 3: EQE measurement of three different solar cell devices: GaInP/GaAs tandem cell grown on GaP or GaAs and GaInP/GaAs/Si triple-junction. The integrated current densities of the individual subcells (@AM1.5g) are given in mA/cm$^2$.](image)
We assume that remaining anti-phase-domains on the 60 nm GaP nucleation layer lead to small holes during the heat-up procedure for the regrowth of the GaAs$_{1-y}$P$_y$ buffer which then increase in size during further growth. Those holes and the increased threading dislocation density explain the lower sub-cell voltages for the structure on Si.

According to the EL measurements, the Si bottom cell shows an (extrapolated) voltage of approximately 550 mV at a current density of 10 mA/cm$^2$ (1 sun). Subtracting this voltage from the open-circuit voltage of the triple-junction cell of 2.32 V leads to 1.77 V for the combined GaInP/GaAs subcells. In a former publication by the authors an open-circuit voltage of 1.94 V was achieved for a GaInP/GaAs tandem cell on a passive n-Si substrate [16]. The lower voltage in the recent triple-junction cell is again attributed to the presence of holes after the growth of the GaAs$_{1-y}$P$_y$ buffer and tandem cell structure on GaP/Si templates. Thus, a significant increase in open-circuit voltage can be expected in future devices if the formation of those holes is suppressed.

The rather low voltage of 550 mV for the Si bottom cell can be explained by the implementation of a low doped 120 Ω/sq. n-Si emitter which is very sensitive to the GaP/Si interface recombination velocity. As we have shown in [19] the GaP/Si interface exhibits a recombination velocity above $10^5$ cm/s leading to a significantly reduced open-circuit voltage compared to a highly doped 19 Ω/sq. emitter. A close investigation of the GaP/Si interface via LAADF STEM shown in Figure 8 reveals a high density of threading and misfit dislocations. They can contribute to the high recombination velocity and thus the reduced $V_{OC}$ in the Si bottom cell. This interface may be improved in the future by introducing a dislocation blocking layer. GaNP can be grown lattice-matched to Si and could potentially stop dislocations to penetrate down to the GaP/Si interface during subsequent GaAs$_{1-y}$P$_y$ growth. Nitride containing layers have already been shown to act as blocking layers for threading dislocations [23].

Alternatively, a better shielding of minority carriers in the Si from this interface could be obtained by heavier doping of the n-Si emitter as shown in [19].
Ga₀.₅₁In₀.₄₉P/GaAs/Si triple-junction solar cells have been successfully realized by direct MOVPE growth of the III-V layer structure onto a diffused silicon junction. The devices with an area of 4 cm² reach an efficiency of 19.7% under AM1.5g spectral conditions, which is currently the highest reported efficiency for a directly grown triple-junction cell on silicon. The silicon bottom cell has an external quantum efficiency close to 90% and a voltage of approximately 550 mV at 1000 W/m². These values are encouraging towards the full integration of III-V/Si multi-junction cells. The overall device performance is still limited by a high density of defects which originate from two sources. One component to the defect density is the lattice grading which leads to a threading dislocation density of 4.9x10⁶ cm⁻² found for GaAsₚ₁.₇ buffer growth on GaP. Additional defects are introduced by the growth on silicon and they may originate from anti-phase boundaries in combination with the overgrowth of nucleation layers in a separate process. This has resulted in overall defect densities for GaAs on Silicon in the order of 1.4x10⁷ cm⁻² as determined by electron channeling contrast imaging. These values correspond well with losses observed in the quantum efficiency and voltage of the top cells. Other research groups have reported on defect-free GaP/Si templates [10] and did not see pits during overgrowth. Thus, this issue can be solved by appropriate growth conditions. Yaung et al. reached a density of 4.0-4.6x10⁶ cm⁻² for GaAs₀.₇ₓP₀.₃ₓ on GaP/Si [12] and Grassman et al. stated a density in the mid to upper 10⁶ cm⁻² range for GaAs₀.₉₀P₀.₁₀ on GaP/Si [13]. Those very promising results show that it is possible to obtain significantly lower threading dislocation densities in the active III-V layers with compositions close to the ones presented. When reaching a similar density as already achieved by those groups we expect a significant increase in efficiency towards 30%.

V. ACKNOWLEDGMENT
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REFERENCES


