THE RTCVD160 – A NEW LAB-TYPE SILICON CVD PROCESSOR FOR SILICON DEPOSITION ON LARGE AREA SUBSTRATES

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ABSTRACT

Fast and cost effective silicon deposition is a fundamental requirement for the preparation of crystalline silicon thin-film solar cells. Pursuing the high-temperature approach, chemical vapor deposition (CVD) of silicon layers by thermal decomposition of chlorosilanes is often applied. At Fraunhofer ISE we develop optically heated ("rapid thermal") RTCVD processors, where substrates are mounted in two parallel rows for deposition. In this paper we present a new RTCVD generation which is capable of depositing silicon on two rows of substrates, each up to 125x300 mm^2 in size. This RTCVD160 was specially designed for laboratory type purposes. The deposition process based on $SiHCl_3$, H_2, B_2H_6 and PH_3 is completely computer controlled. The optical heating system enables fast temperature ramps and stable process temperatures up to 1300°C. Epitaxial growth rates exceeding 5 µm/min can be reached with this system.

1. INTRODUCTION

The availability of fast silicon deposition techniques is essential for any approach of crystalline silicon thin-film (CSiTF) solar cells. At Fraunhofer ISE we pursue the high-temperature route, where heat resistant substrates allow process temperatures up to the melting point of silicon. Epitaxial silicon deposition from inexpensive precursors with deposition rates up to 10 µm/min are therefore possible [1].

In principle, silicon deposition and silicon epitaxy is a well-known topic in semiconductor industry. In this area, reactors have been designed aiming at extremely good process control in terms of homogeneity of layer thickness and doping density, as well as very low defect levels. To achieve these goals, high process gas flows and e.g. sample rotation is used, resulting in comparatively low utilization rates of the process gas, complex machine setup and thus high costs for the deposited layer.

For an industrial scale deposition of inexpensive silicon layers for solar cells, the processors have to operate within some boundary conditions different from those important for semiconductor industry:

- the throughput of the processor has to be very high (~10 m^2/h)
- the silicon conversion efficiency, defined as the quotient of silicon atoms deposited on the substrate and silicon atoms contained in the precursor gas, must be very high (>~30 %)
- the processor setup has to be inexpensive and very robust.

On the other hand, the needs in layer quality are relaxed for an application in CSiTF solar cells: both doping and layer homogeneity can have some tolerances and higher defect densities are allowed.

To address the needs of silicon deposition for solar cells, we develop deposition processors using the principle of chemical vapor deposition (CVD) at atmospheric pressure for years. Our latest development, the RTCVD160 was designed for testing these requirements. It is an optically heated processor specially designed for lab-type depositions on various substrate types with maximum sample size of up to 125x300 mm^2.

2. SETUP OF THE RTCVD160 PROCESSOR

2.1 Total system

Fig. 1 shows a photograph of the RTCVD160. It is a compact system using only 2.2x1 m^2 of floor space, including power supply, gas system, $SiHCl_3$ storage case, optically heated furnace, quartz reactor tube, manual loading stage as well as control and security systems. Despite of this compact setup, all parts are easily accessible for maintenance.

Fig. 1: Front view of the RTCVD160 system. In the lower part the gas system is visible. The upper part houses the optically heated furnace and the reactor tube.

The RTCVD160 was designed for laboratory purposes where short process cycles are necessary to enable a quick

parameter variation. The design of the single parts described in the following sections is based on this preliminary requirement.

2.2 Optically heated furnace

Fast heating ramps and cooling time enables several deposition runs per day featuring totally different deposition parameters if necessary. Therefore we designed a furnace which is optically heated by 30 linear halogen lamps of 4.5 kW maximum power each. They are mounted vertically in two arrays of 400 mm length and 250 mm height inside a water cooled, mirrored lamp house. Together with the appropriate thyristor power supply, the furnace is capable to heat up the silicon substrates to 1300°C for at least 30 min. Power and therefore temperature profiles can be realized along the lamp array by adjusting the signal gain at the thyristor units.

2.3 Deposition principle, reaction chamber and deposition control

The setup of the RTCVD160 adapts the principle shown in Fig. 2. Together with the carrier, two parallel vertical rows of substrates form a closed reaction volume which is only open on two ends for gas inlet and exhaust outlet. The carrier is located inside a quartz tube, and is heated by the surrounding furnace. The process gas is injected into the process chamber formed by the substrate rows, where it is decomposed and silicon is deposited on the inner surface of the substrate wafers. The exhaust gas is extracted via the end plate of the process chamber. During the deposition the reactor tube is flushed with hydrogen or inert gas. For a production of CSiTF solar cells, this principle can be applied for building a continuous in-line CVD processor featuring high throughput and low deposition cost.

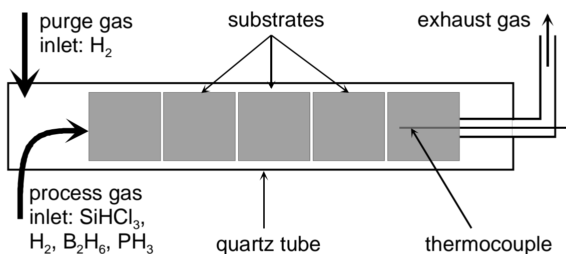

Fig. 2: Principle of reaction chamber setup.

The first CVD reactor where the described wafer-setup for deposition was realized is the RTCVD100 built at Fraunhofer ISE. It was designed to deposit silicon on samples of a maximum width of 80 mm. This processor was characterized in detail and showed excellent electronic properties of deposited Si layers. Solar cell efficiencies of up to 17.6 % could be achieved for thin epitaxial base layers grown on inactive Cz-Si wafers [2].
In Fig. 3 the quartz carrier developed for the RTCVD160 is illustrated. Samples of up to 100 mm in width can be mounted vertically in two rows up to 500 mm in length. The process gas is first introduced into the gas conditioning zone for homogenizing the gas flow, and then enters the deposition zone, where gas decomposition and silicon deposition occurs at a length of approximately 300 mm. A simple modification of the quartz carrier enables the processing of larger substrates with up to 125 mm in width.

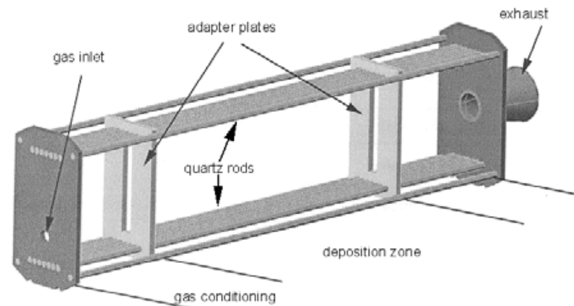

Fig. 3: Quartz process chamber of the RTCVD160

Deposition homogeneity can be varied and optimized by variation of process gas composition, temperature and temperature profiles in the reactor as well as the application of gas showers. Therefore process gas flows are all measured and controlled by mass flow controllers. $SiHCl_3$ is carried to the process chamber by bubbling with H_2, where a “Source VI” controller regulates the mass flow of $SiHCl_3$. P- or n-type silicon layers can be grown by adding a B_2H_6/H_2 or PH_3/H_2 mixture respectively to the process gas. The quartz process chamber can be in situ cleaned by HCl etching.

The whole deposition process is controlled by a programmable logic controller and a PC, with a wide range of parameter variability, specially adapted to the needs of R&D applications.

3. EXPERIMENT AND RESULTS

3.1 Temperature homogeneity

Among other parameters, temperature and temperature profiles determine homogeneity and defect structure of the deposited silicon layer. In a first experiment, we investigated the temperature homogeneity as a function of different temperature profiles, which can be realized by the optically heated furnace. For this purpose, a defined temperature of 1273 K was set and measured by a fixed thermocouple. A second thermocouple was scanned along the centerline of the deposition zone while measuring the local temperature in between the substrate rows. During the measurements, the process chamber was purged with a 5 l/min N_2 flow.

In Fig. 4 the temperature profiles measured for two different power profile settings are shown. Using a constant lamp power profile, the temperature on the first 70 mm of the 300 mm long deposition zone is up to 60 K lower than the setpoint of 1273 K. Within the main deposition zone (200 mm length) the temperature variation is determined to ±5 K. Application of a parabolic power profile leads to a significant reduction in temperature variation along the entire deposition zone. On a length of 200 mm, a temperature deviation of only ±2 K around the setpoint can be achieved which corresponds to a variation of only 0.16 %.

Measurements of the vertical temperature homogeneity showed that the lower and upper edges of the substrates have a significantly lower temperature than the center regions. This temperature drop affects the edges on a scale of ~10 mm with a difference in temperature compared to the middle of the wafer estimated to be in the

range of 10-15 K. We assume that shadowing of the substrate edges by the quartz rods of the reaction chamber, and direct contact to the “cold” quartz parts are responsible for the observed decrease in temperature. However, the observed vertical temperature homogeneity is in the same order of magnitude than the longitudinal homogeneity. Therefore we expected that the deposition homogeneity will be mainly influenced by flow and distribution of the process gas in the deposition zone.

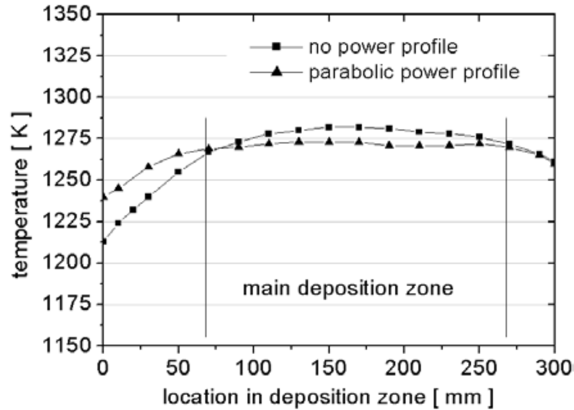

Fig. 4: Temperature profile in between the wafer rows with and without lamp power profile.

3.2 Silicon deposition at low temperatures

Within the high-temperature approach of CSiTF solar cells usually two silicon deposition steps are applied:

- first, epitaxial films have to be grown to form the active base of the solar cell in nearly all used concepts
- second, in concepts which employ recrystallization, highly doped, thin “seeding” layers have to be deposited at low temperatures.

The seeding layer should be of high thickness homogeneity, since all liquid phase recrystallization procedures usually are comparatively sensitive to thickness variations. In the zone-melting recrystallization for example, film thickness variations indirectly influence solidification front morphology and thus type and density of intragrain defects, which determine strongly the quality of the silicon base layer deposited epitaxially on the recrystallized seeding layer.

Although the RTCVD160 was designed for depositing both epitaxial and seeding layers, main effort in the beginning was put in process optimization for silicon seeding layer deposition with respect to thickness homogeneity. The following section reports the respective results.

We put our first attention to the question of symmetry of deposition rates concerning left and right substrate row. In principle there should be no difference between the two rows, since furnace and reaction chamber setup is completely symmetrical to the longitudinal middle axis. This assumption was proved by numerous experimental data as shown in Fig. 5: on both rows, deposition rates are very close or even identical. In consequence, further analysis of thickness homogeneity was only done on one of the two substrate rows.

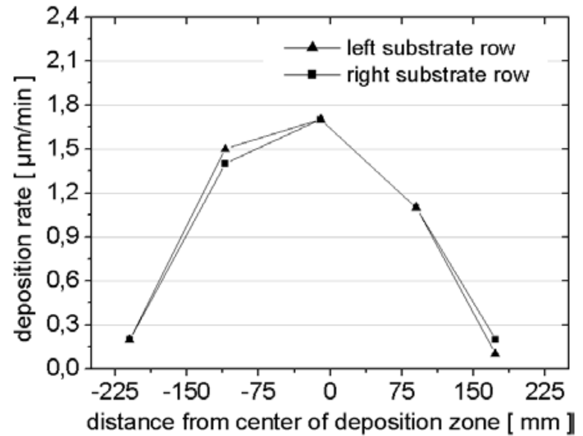

Fig. 5: Comparison of deposition rates of left and right substrate row, respectively.

A uniform distribution of the process gas across the whole deposition area is essential if excellent thickness homogeneity is to be reached. Wafer geometry, gas inlet, total gas flow and gas composition play a key role on that score [3, 4]. In a first step the effect of total gas flow and gas composition on the thickness distribution within the deposition zone was evaluated by systematic variation of these parameters. The deposition temperature was fixed to 1223 K with no lamp power profile applied. This temperature is our standard process temperature for silicon growth on SiO_2 encapsulated substrates, since at a higher temperature the SiO_2 layer would be decomposed in the hydrogen atmosphere. A simple quartz tube served as gas inlet and a constant power profile was applied. Only the samples positioned on a length of 300 mm in the deposition zone were used for characterization. For an analysis of the layer thickness the samples were cut into stripes by laser scribing and analyzed by inspecting the edge using Nomarski microscopy.

In Fig. 6 two examples are shown to illustrate the effect of total gas flow on thickness uniformity. The Cl/H-ratio was fixed to 0.165 and the total gas flow rate was adjusted to 5.6 and 11.2 l/min for the top and bottom figure respectively. In the top figure the onset of maximum deposition rate is approx. in the middle of the deposition zone, and persists until the end of the deposition zone. This asymmetry can be attributed to an asymmetric temperature profile of the substrate wafers due to the heating up of the process gas stream. In addition a substantial reduction in growth rate can be observed towards the upper and lower edges of each wafer. Assuming laminar flow the gas velocity distribution within the reaction volume follows a parabolic profile with zero velocity at the boundaries and maximum velocity in the center of the main gas stream. Therefore the decrease in growth rate towards the edges is mainly a consequence of inhomogenous gas distribution.

The thickness distribution of the deposition at large gas flow of 11.2 l/min is shown in the bottom part of Fig. 6. Compared to the deposition with lower flow rate, two main differences attract attention:

- First, a cold finger is visible at a vertical position of -20 mm, reaching ~180 mm into the deposition zone. This effect can be clearly attributed to the cooling effect of the process gas injected with high velocity (~1.6 m/s) into the carrier.

- Second, an increased thickness can be observed in the upper part of the middle wafer, which may be due to a roll back cell formed at high gas flow.
- An overall better vertical homogeneity, presumably due to a better gas supply at the edges.

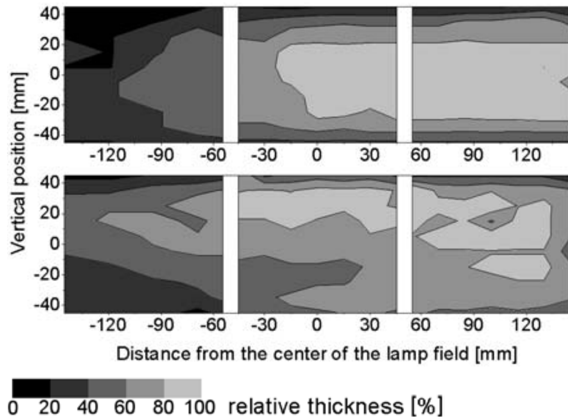

Fig. 6: Relative thickness distribution for fixed Cl/H ratio and different total gas flow.

Maximum growth rates of approx. 1.1 µm/min were determined for both processes.

The comparison shows that the vertical thickness homogeneity is mainly limited by an insufficient distribution of the process gas. Therefore the gas inlet geometry and thus the gas distribution was varied in a second step. Experiments were carried out using either a simple quartz tube, an inlet strainer attached to the adapter plates or a nozzle.

Fig. 7 shows the thickness distribution achieved when using the nozzle as gas inlet. The process parameters were identical to those in Fig. 6 (top).

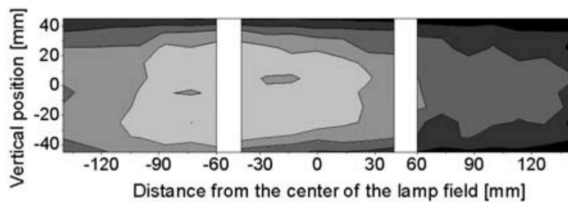

Fig. 7: Relative thickness distribution for silicon seeding layers. A nozzle has been used for gas distribution. Thickness scale is identical to that of Fig. 6.

Compared to Fig. 6 (top) the onset of the homogeneous area within the deposition zone has shifted towards the gas inlet. In gas flow direction the deposition rate decreases because of the depletion of process gas. The deposition profile in vertical direction is almost symmetric. Similar to Fig. 6 the decrease in layer thickness towards the upper edge of the wafer is greater compared to the bottom edge. This effect can be attributed to the asymmetric position of the gas inlet relative to the vertical center of the carrier.

The implementation of a nozzle for gas distribution leads to a significant improvement in terms of vertical thickness homogeneity. However an adjustment of the process parameters to the changed gas distribution is necessary to further optimize the thickness uniformity.

Up to now the best homogeneity was reached for a Cl/H-ratio of 0.165 using a nozzle as gas inlet. Under these process conditions the mean deviation of layer thickness was determined to be 32 % over a deposition area of 80x150 mm². Considering a smaller area of 70x150 mm² in the middle of the deposition zone, thus eliminating the edge effects leads to a reduced mean deviation of 17 % in thickness uniformity. Using this deposition process a maximum growth rate of 1.5 µm/min was measured and a chemical yield of 17 % was achieved.

Further improvement is expected if more sophisticated gas distribution systems are used. For this aim new gas inlet geometries are currently being developed.

The suitability of the deposited seeding layers for zone-melting recrystallization was investigated by recrystallizing a seeding layer grown on a 100x100 mm² mc-Si sample with SiO_2 intermediate layer. A maximum width of 90 mm for the recrystallized area could be achieved for a melting zone width of 2 mm. Coarse-grained crystals of high quality on this sample proved the suitability of the seeding layers grown in the RTCVD160 for ZMR.

4. CONCLUSION

The RTCVD160 realizes a CVD principle which is characterized by high silicon conversion efficiencies and high throughput necessary for solar cell applications. It was specially designed for laboratory purposes. High variability in substrate types and deposition conditions as well as robustness are its main features. Substrates up to 125 mm in width and up to 300 mm in length can be coated with silicon. With a quartz carrier designed for 100 mm wide substrates, polycrystalline silicon layers can be deposited with a homogeneity of 68% on 120 cm^2 area. Process optimization for epitaxial layers is currently under investigation.

5. ACKNOWLEDGEMENTS

The authors gratefully acknowledge the support of the Fraunhofer ISE mechanical and electrical workshop for their invaluable construction work.

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