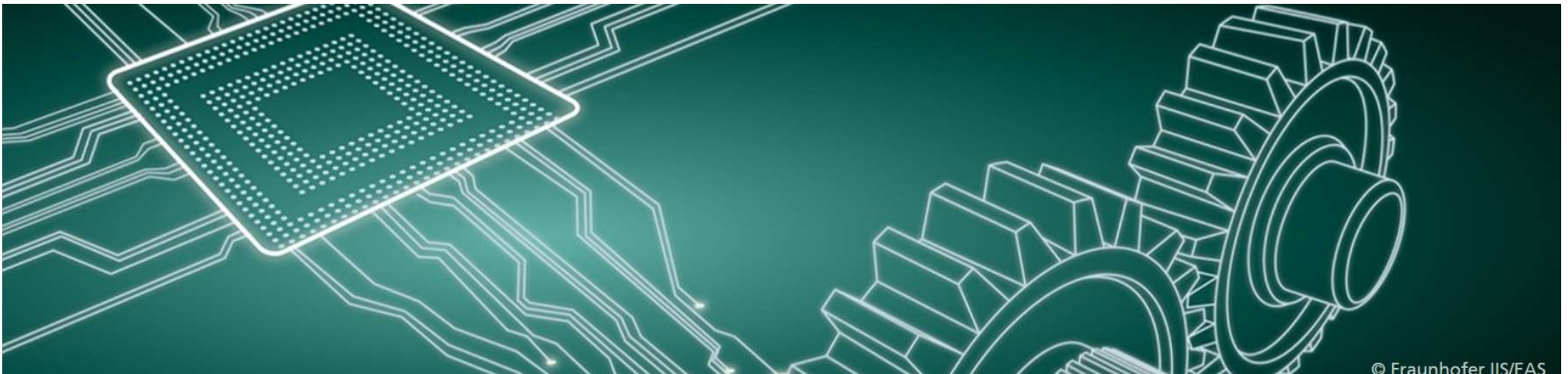

EASE DESIGN SUCCESS IN NM ANALOG USING GENERATORS

Fraunhofer Institute for Integrated Circuits IIS
Division Engineering of Adaptive Systems EAS



© Fraunhofer IIS/EAS

Benjamin Prautsch
Group Manager Advanced Mixed-Signal Automation

The Fraunhofer Institute for Integrated Circuits IIS



Division Engineering of Adaptive Systems EAS

Founded	1992
Employees	approx. 110
Budget	approx. 12.5 million €
Director	Dr. Peter Schneider

Fraunhofer IIS

Founded	1985
Employees	approx. 1,000
Budget	approx. 184 million €
Directors	Prof. Dr. Albert Heuberger Dr. Bernhard Grill

Fraunhofer IIS – Division EAS

Business Areas & Research Topics

Challenges in the development of adaptive systems

- Complexity of the systems
- Functional safety and reliability
- Security and privacy
- Variable application scenarios
- Human-machine interaction



Design methodology

- Reliability and robustness of ICs
- Functional safety



Efficient electronics

- Integrated sensor electronics
- System integration
- Optical sensor technologies

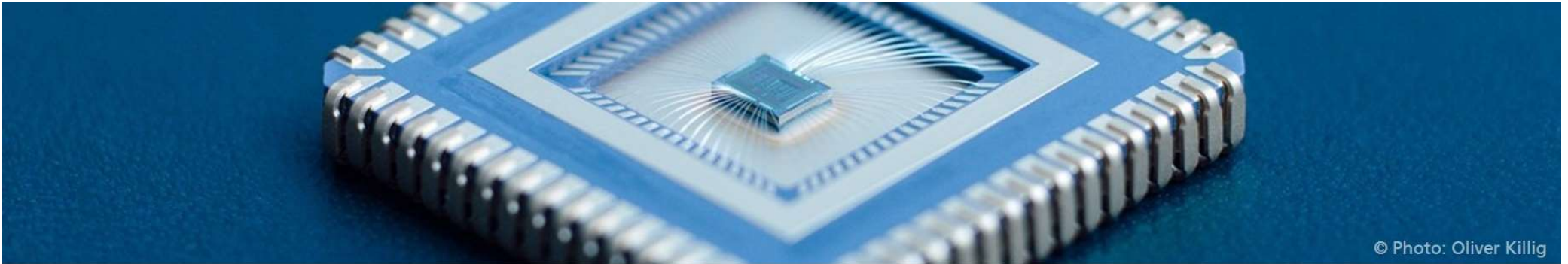


Distributed data processing and control

- Industrial data analysis
- Wireless-networked automation
- Energy management

Fast Analog Design Using Generators – Intelligent IP

What are Your Challenges in A/MS IC Design?



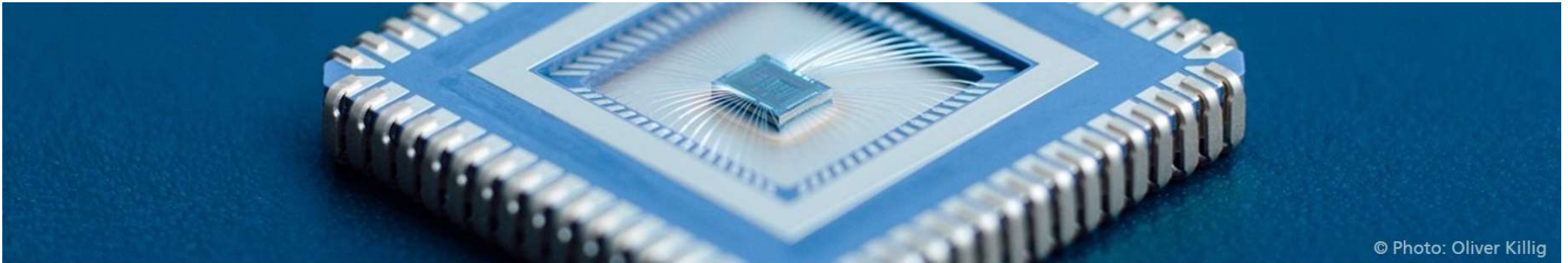
Questions – please give some feedback

- What is your mayor challenge in design?
- Which automation tools do you use?
- What do you use automation for?
- Which nodes are you working in?

Thank you!

Fast Analog Design Using Generators – Intelligent IP

Analog Design: Challenges We See and Our Approach



© Photo: Oliver Killig

Today's challenges

- **Low level of automation** in analog circuit design
- **Miniaturization increases complexity** and susceptibility to errors
- Only **limited reuse** of designs

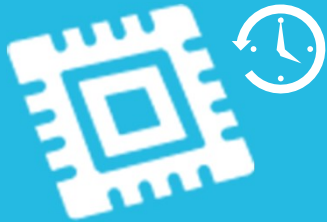
Our approach

- Analog design using **Intelligent IP (IIP)**
- **Accelerated technology migration** through automated reuse
- **Increased design speed&safety** through standardized knowledge-based routines

Fast Analog Design Using Generators – Intelligent IP

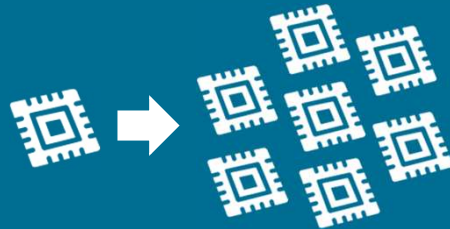
Our IIP Offers

Design Aid: Base-Level IIP



- Accelerate your design process

IP Reuse



- Reuse & migrate your designs

Full-Custom IIP



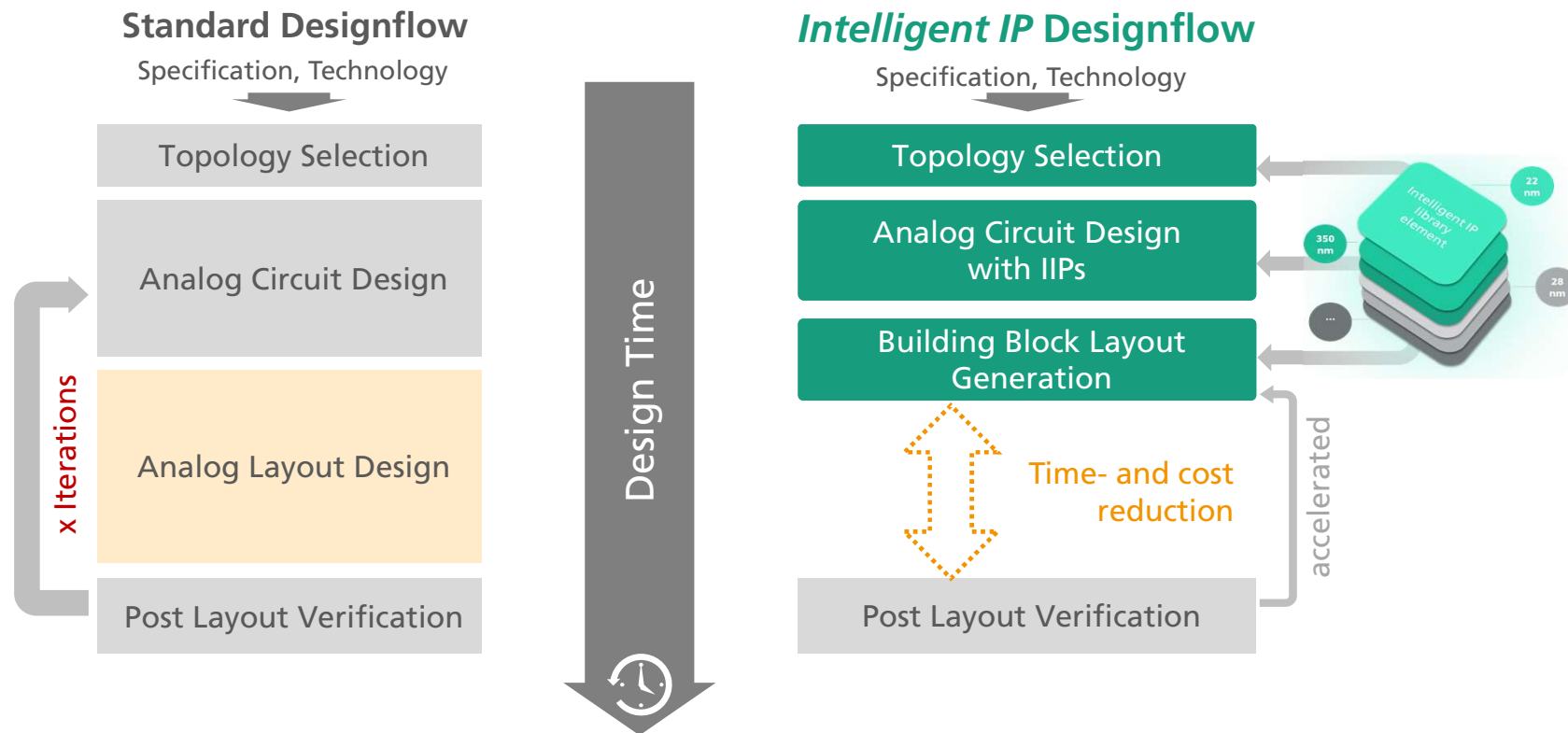
- Get your problem automated

+ IIP Framework and Support

+ TechSetups, Customization Support (not included in licensing fees)

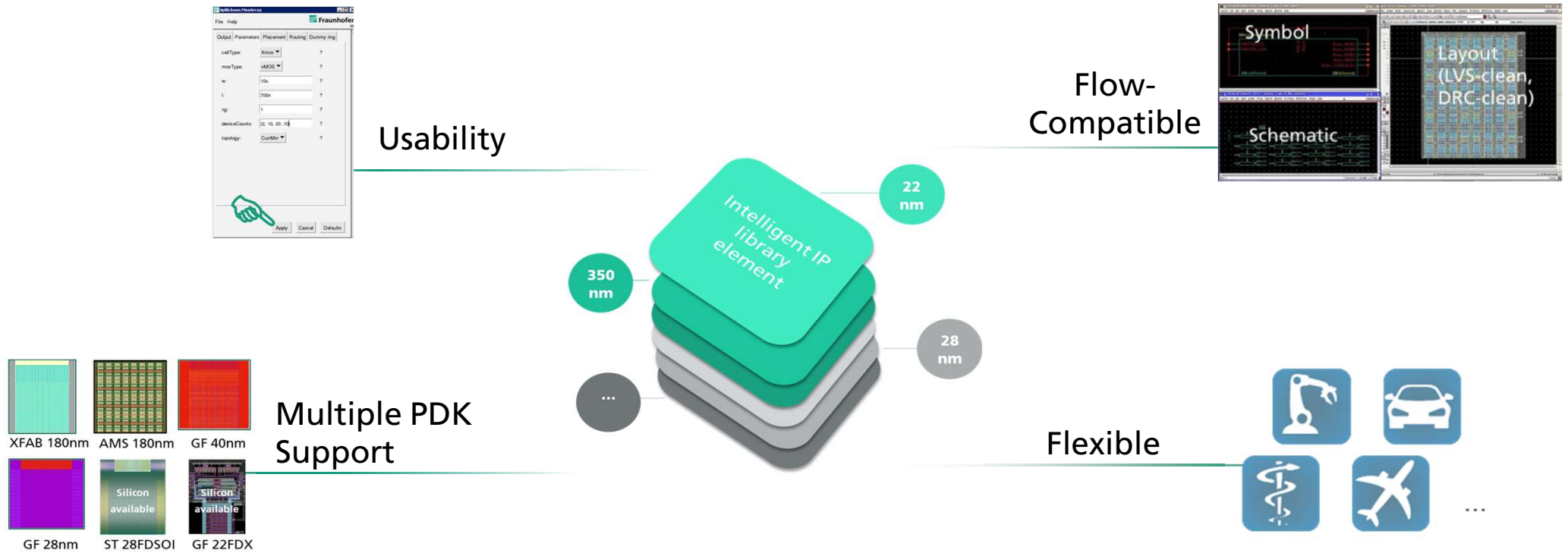
Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: IIP-Based Design Flow



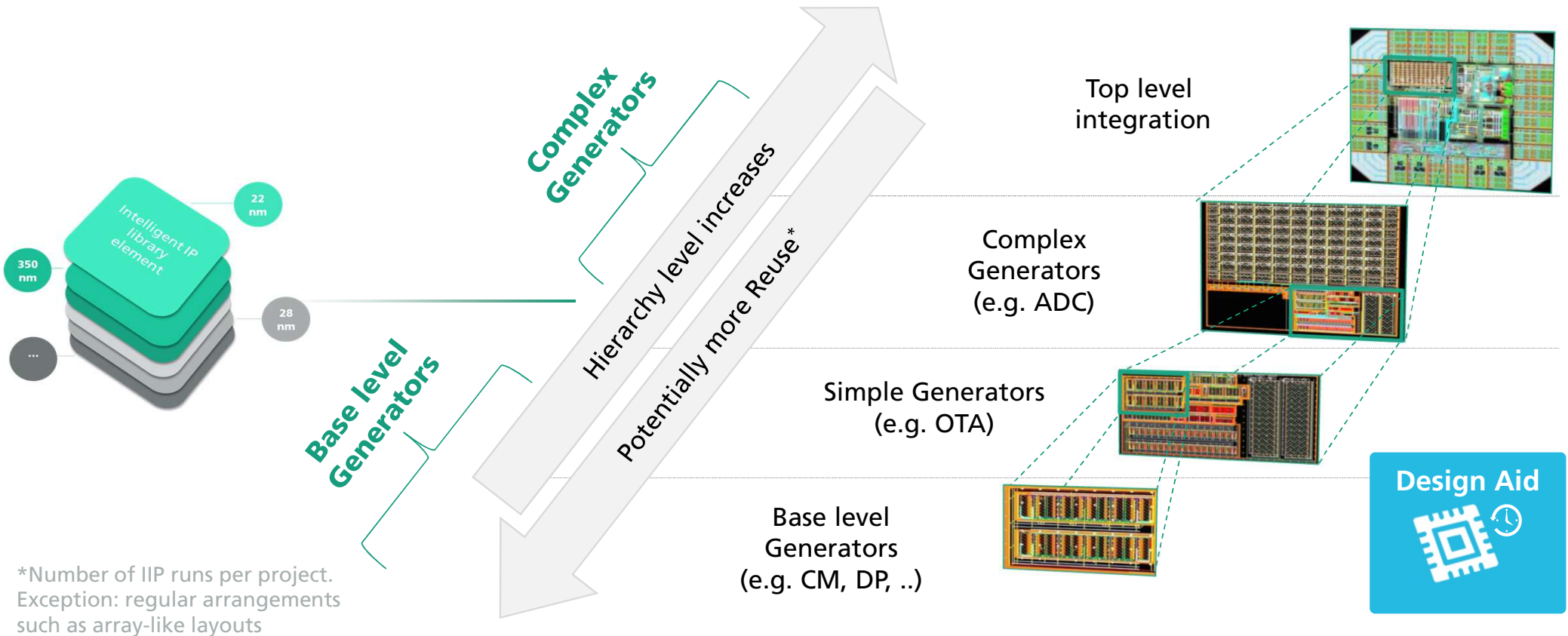
Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: The IIP Library (I)



Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: The IIP Library (II)

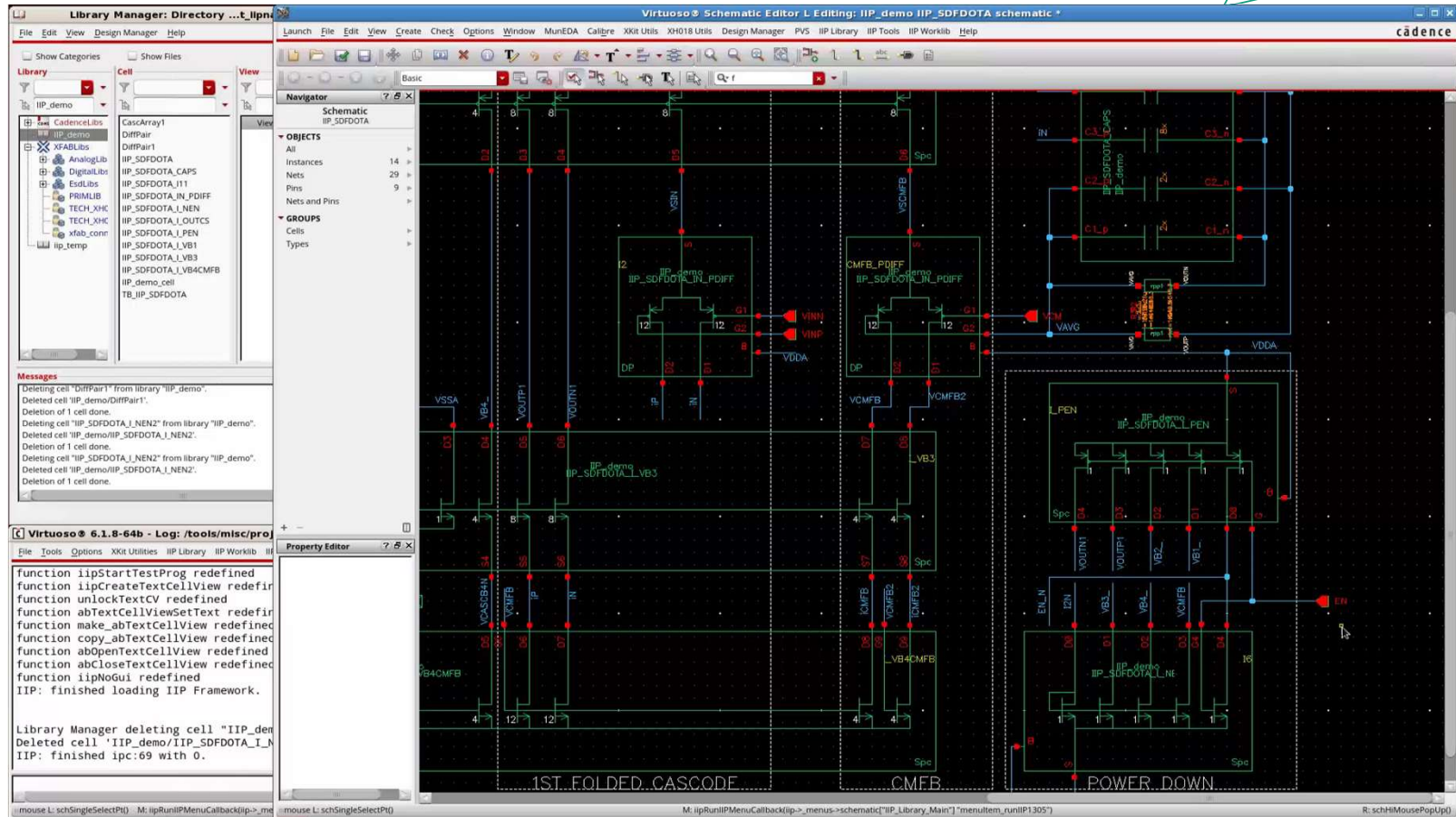


*Number of IIP runs per project.
Exception: regular arrangements
such as array-like layouts

Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Usability for Editing

Screencasts available on:
www.intelligent-ip.org



Library Manager: Directory ...t.iiipn

Virtuoso® Schematic Editor L Editing: IIP_demo IIP_SDFDOTA schematic *

Library

- CadenceLibs
- IIP_demo
 - CasArray1
 - DiffPair
 - DiffPair1
 - IIP_SDFDOTA
 - IIP_SDFDOTA_CAPS
 - IIP_SDFDOTA_I11
 - IIP_SDFDOTA_IN_PDIFF
 - IIP_SDFDOTA_IN_NEN
 - IIP_SDFDOTA_I_OUTCS
 - IIP_SDFDOTA_I_PEN
 - IIP_SDFDOTA_LVB1
 - IIP_SDFDOTA_LVB3
 - IIP_SDFDOTA_LVB4CMFB
 - IIP_demo_cell
 - TB_IIP_SDFDOTA
- XFABLibs
- AnalogLib
- DigitalLib
- EsLibs
- PRIMLIB
- TECH_XHC
- TECH_XHC
- xfab_conn
- ip_temp

Navigator

Schematic IIP_SDFDOTA

OBJECTS

- All
- Instances: 14
- Nets: 29
- Pins: 9
- Nets and Pins

GROUPS

- Cells
- Types

Messages

Deleting cell 'DiffPair1' from library 'IIP_demo'.
Deleted cell 'IIP_demo/DiffPair1'.
Deletion of 1 cell done.
Deleting cell 'IIP_SDFDOTA_I_NEN2' from library 'IIP_demo'.
Deleted cell 'IIP_demo/IIP_SDFDOTA_I_NEN2'.
Deletion of 1 cell done.
Deleting cell 'IIP_SDFDOTA_I_NEN2' from library 'IIP_demo'.
Deleted cell 'IIP_demo/IIP_SDFDOTA_I_NEN2'.
Deletion of 1 cell done.

Virtuoso® 6.1.8-64b - Log: /tools/misc/pro

```
function iipStartTestProg redefined
function iipCreateTextCellView redefin
function unlockTextCV redefined
function abTextCellViewSetText redefin
function make_abTextCellView redefin
function copy_abTextCellView redefin
function abOpenTextCellView redefin
function abCloseTextCellView redefin
function iipNoGui redefined
IIP: finished loading IIP Framework.

Library Manager deleting cell "IIP_den
Deleted cell 'IIP_demo/IIP_SDFDOTA_I_N
IIP: finished ipc:69 with 0.
```

Property Editor

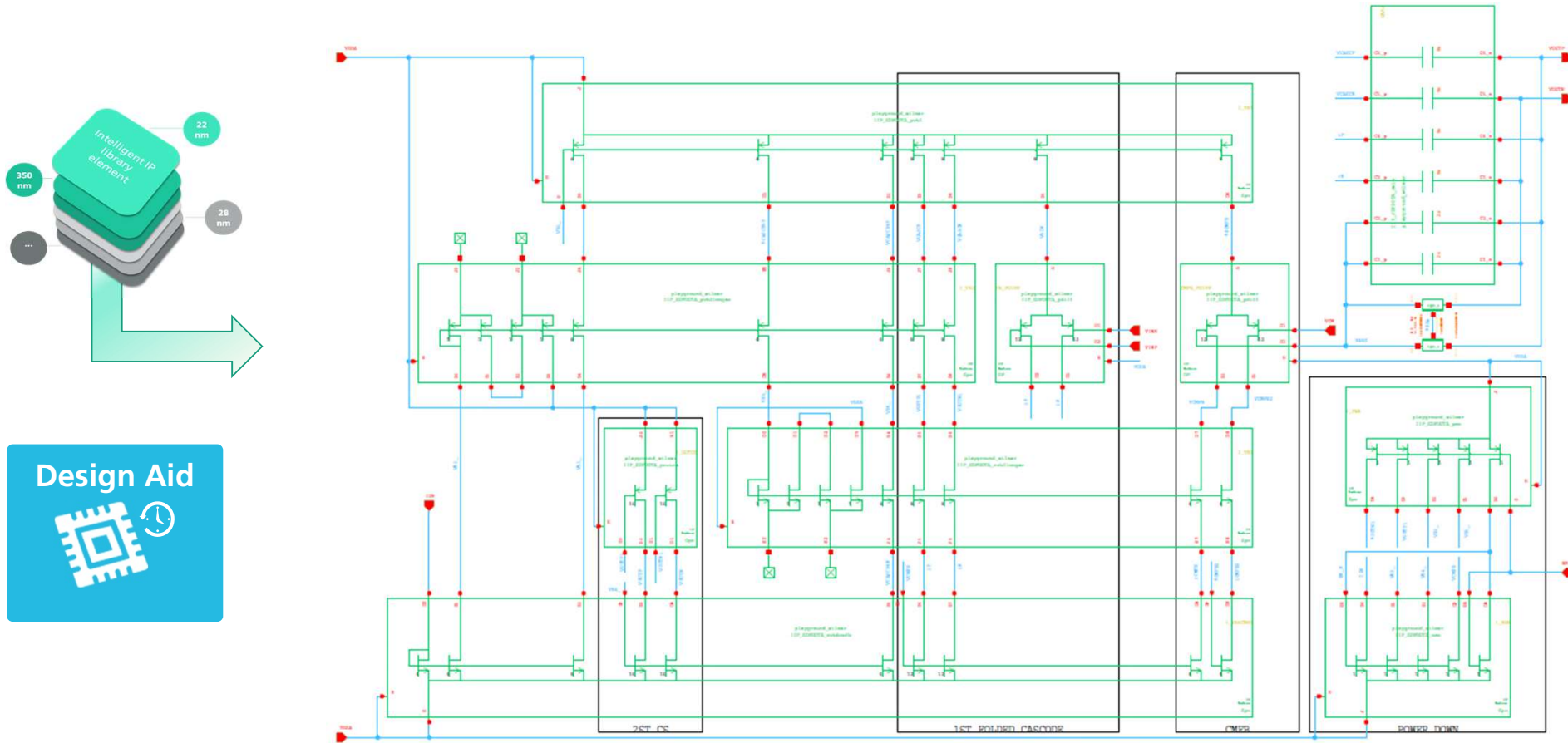
1ST_FOLDED_CASCODE

CMFB

POWER_DOWN

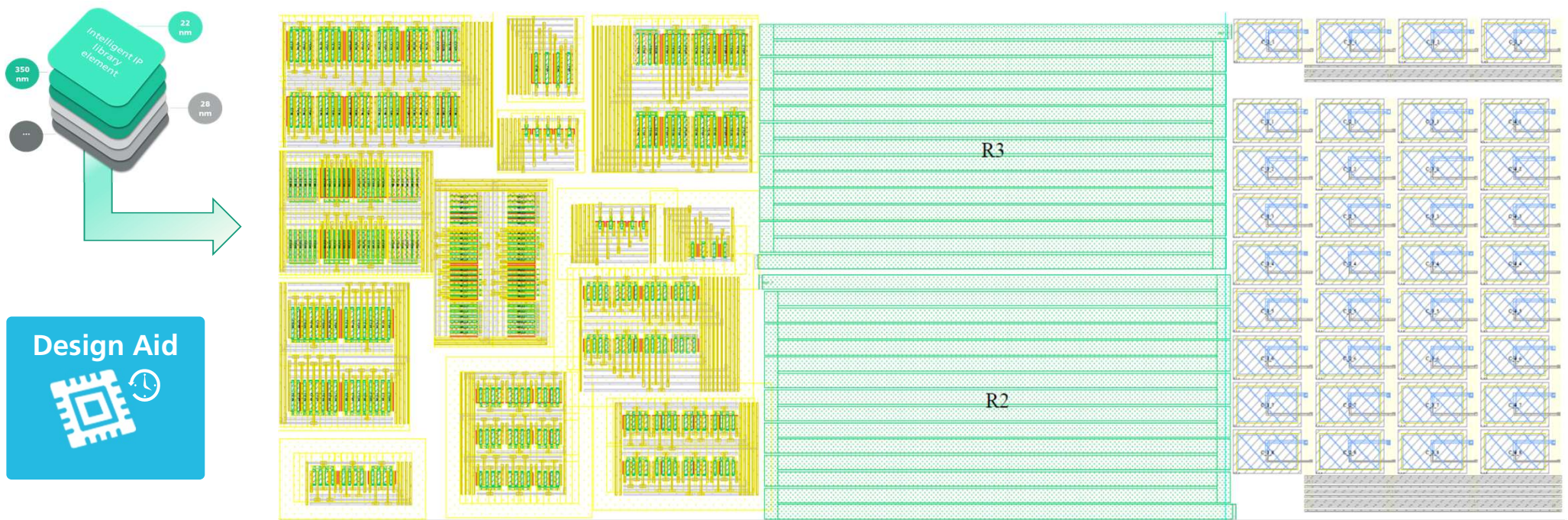
Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Base Level Generators (Schematic)



Fast Analog Design Using Generators – Intelligent IP

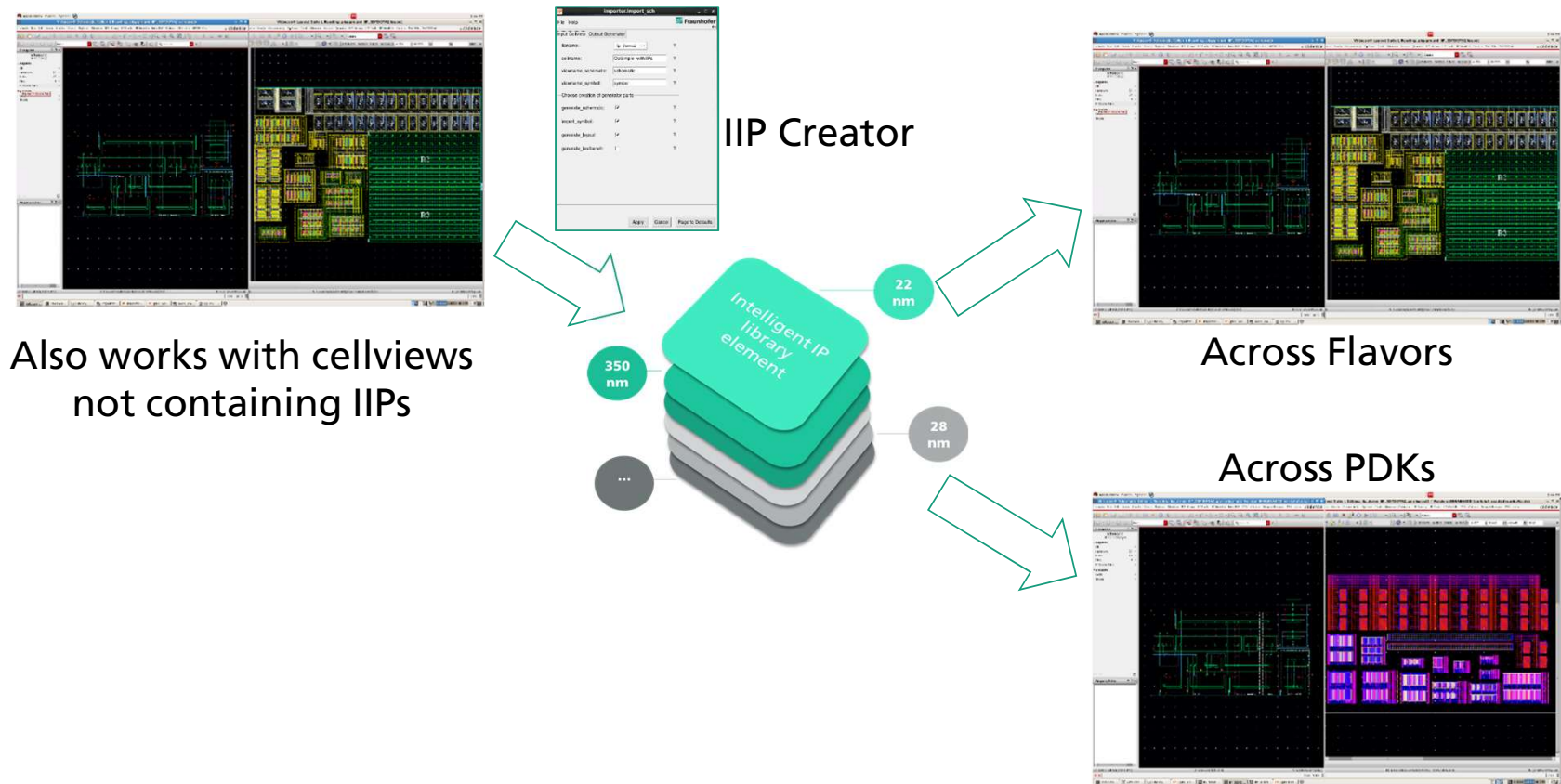
More Efficiency in Design: Base Level Generators (Layout, placed)



Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: “Copy-Paste” Schematic Migration

Screencasts available on:
www.intelligent-ip.org

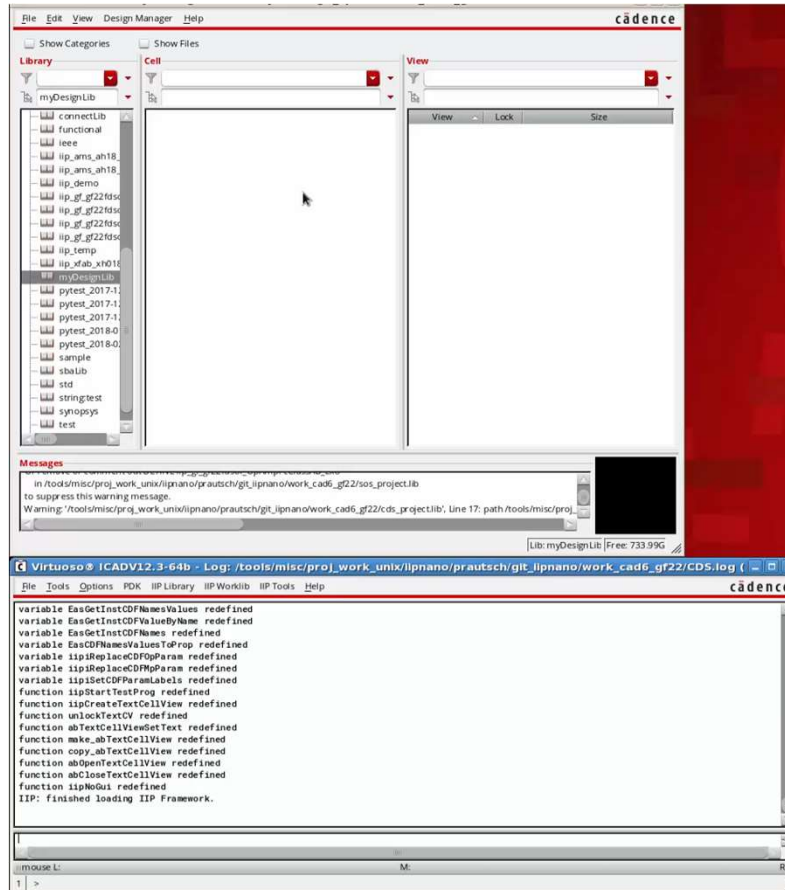
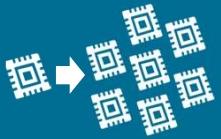


Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Generation of all Design Data

Screencasts available on:
www.intelligent-ip.org

IP Reuse

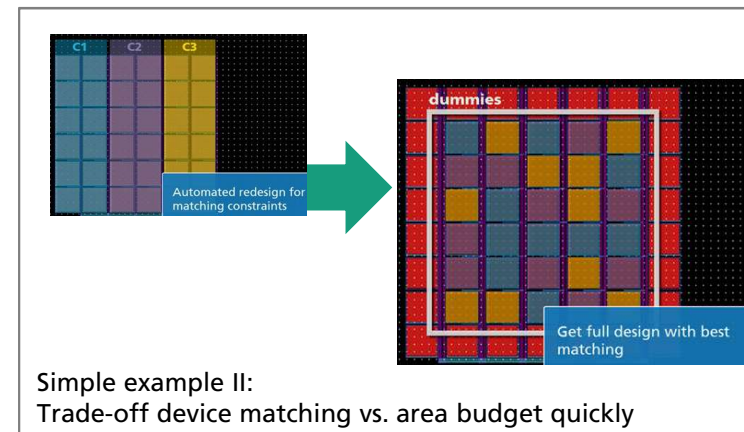
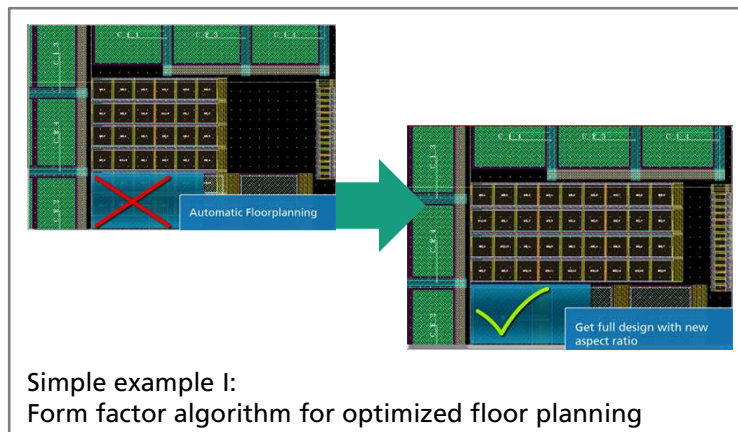


Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Base Level Generators Flexibility Example



Use Intelligent IP for automatic placement, routing, matching ...



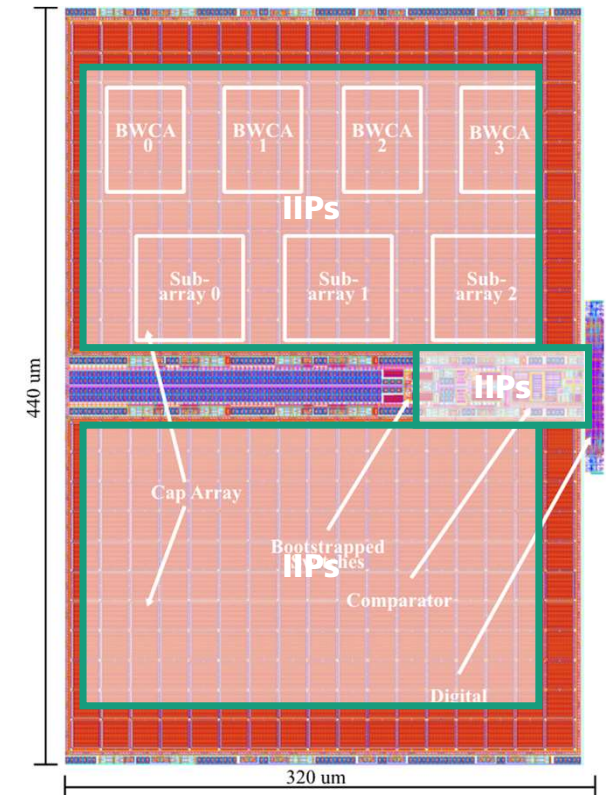
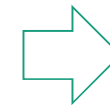
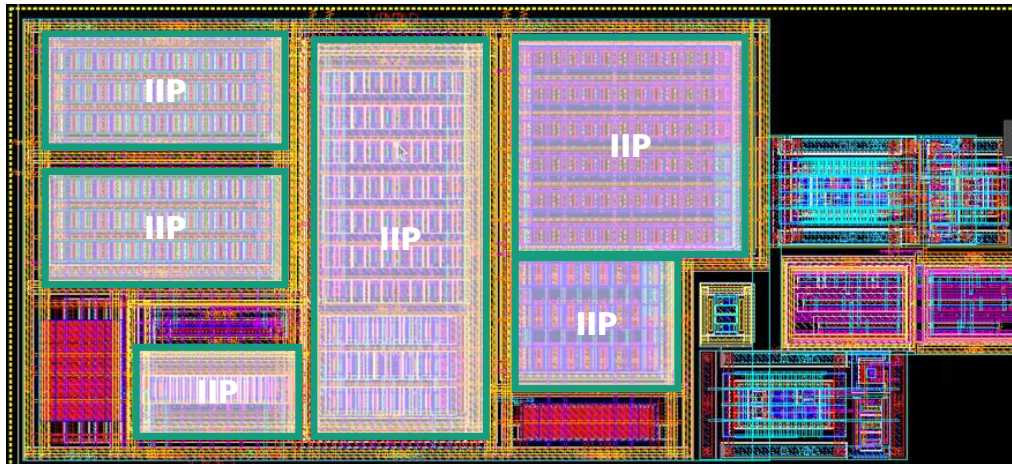
... and speed up design steps

Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Base Level Generators Design Example

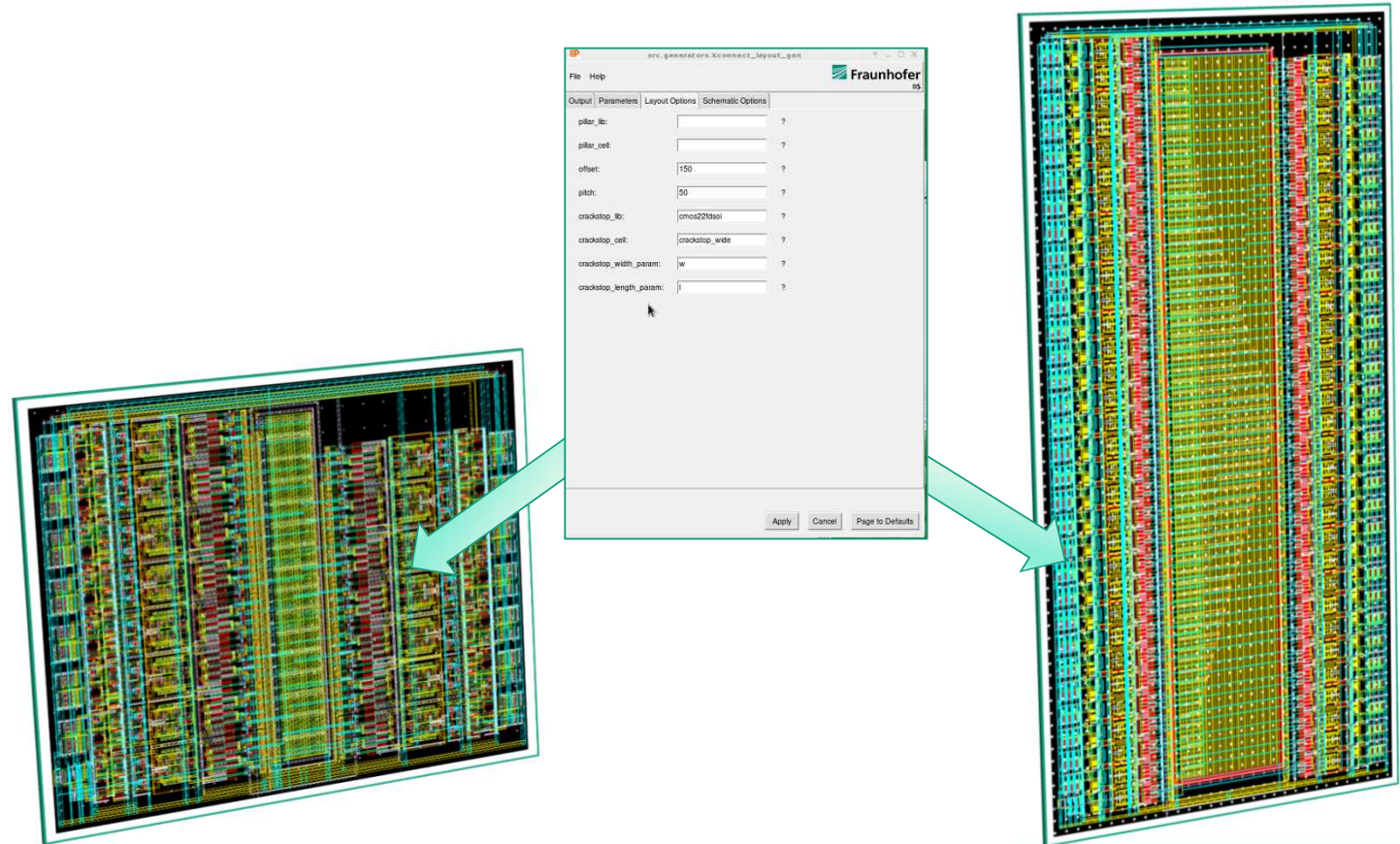


- Example: Automation for SAR-ADC design (PDK: **22nm FDX**)
 - Building blocks automated for comparator & capacitor array
 - Layout design about **60 % faster**
 - Design better reusable



Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Full Custom IIP Example (I)

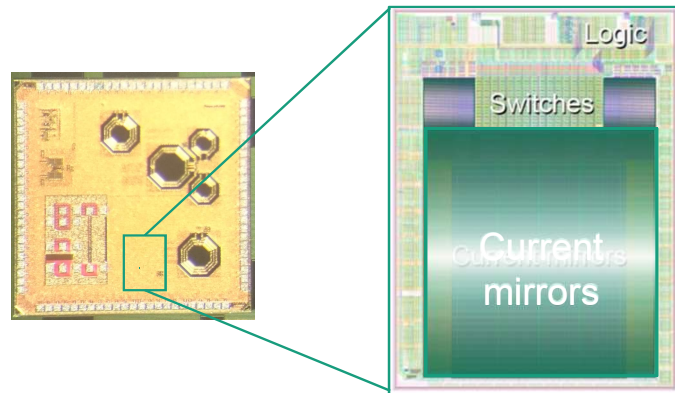


Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Full Custom IIP Example (II)

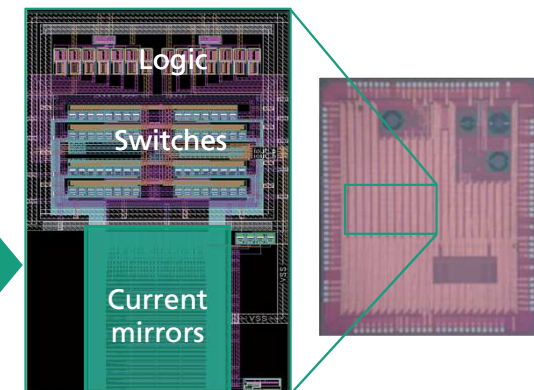


12-bit DAC in STM 28nm FDSOI



- Initial IIP development in ~4 weeks
- Layout generation: **~3 min**
- Silicon available

10-bit DAC in GF 22FDX



- IIP reuse for tech node shrinking
- Layout generation: **~2 min**
- Silicon available

IIP-based Migration

[Source (28 nm): <http://publica.fraunhofer.de/documents/N-426412.html>]

Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Full Custom IIP Example (III)



- Copper pillar design
 - Fast generation (secs)
 - Correct-by-construction

A composite image showing the design process. On the left is a circuit schematic with components like resistors and capacitors. On the right is a top-down layout of a copper pillar array. A central dialog box titled "fra_generators_xconnect_layout_gen" is shown, containing parameter settings for the layout. A large blue arrow points from the dialog box to the layout image.

fra_generators_xconnect_layout_gen

File Help Fraunhofer IIS

Output Parameters Layout Options Schematic Options

pillar_lib: ?

pillar_cell: ?

offset: 150 ?

pitch: 50 ?

crackstop_lib: onco22ktool ?

crackstop_cell: crackstop_wide ?

crackstop_width_param: w ?

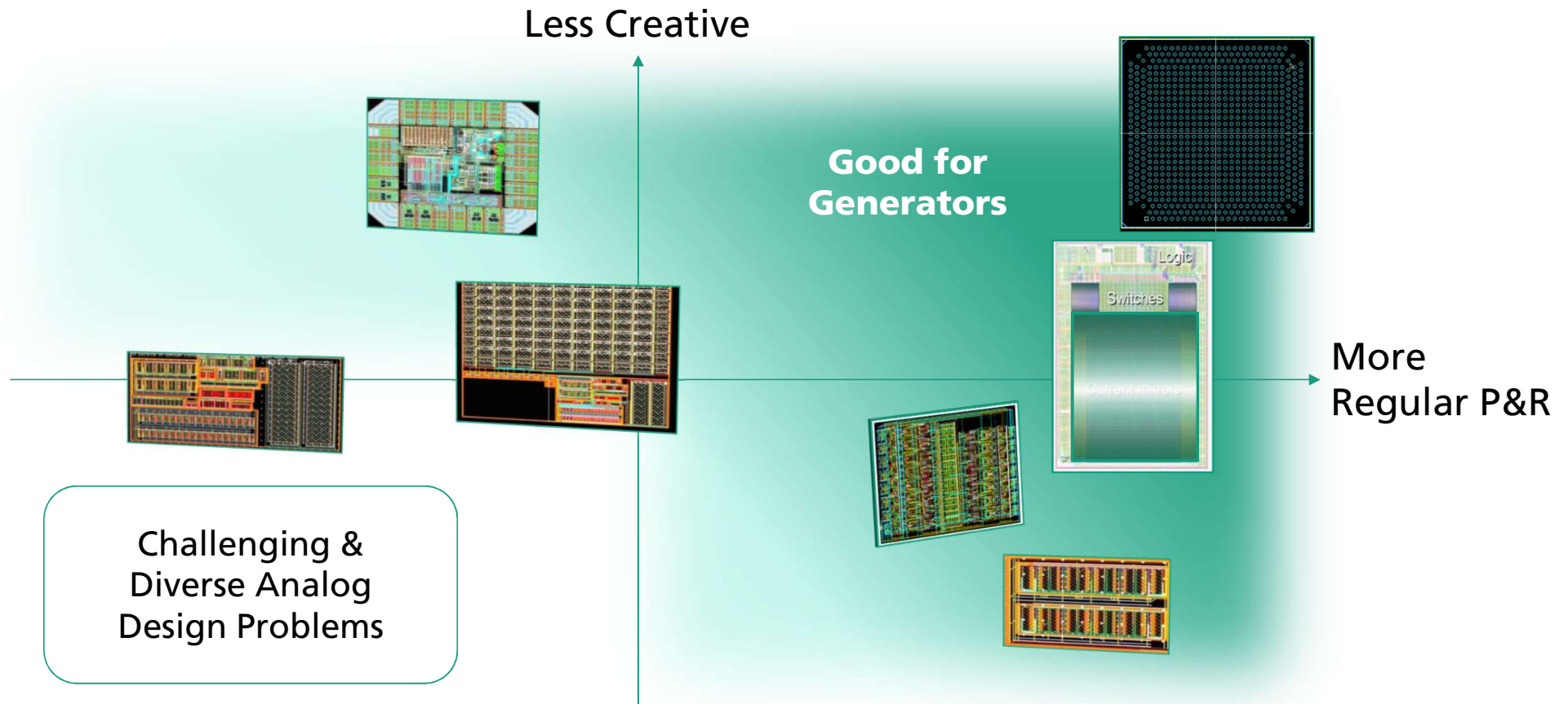
crackstop_length_param: l ?

Apply Cancel Page to Defaults

Fraunhofer IIS	File	fra_generators_xconnect_layout_gen	Confidential
Integrated Circuitry & Systems	Ctrl	fra_generators_xconnect_layout_gen	Copyright (c) Fraunhofer IIS
an 10/18/2018 02	View	Parameters	
11/08/2018 02	Date: Nov 29 09:28:01 2018		025 Ver
11/08/2018 02	Project	Tools	File
11/08/2018 02	Version	View	Status

Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Which IIP Approach to Use When?

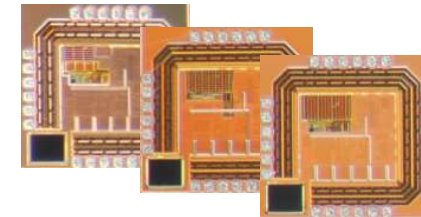


Fast Analog Design Using Generators – Intelligent IP

More Efficiency in Design: Success Stories

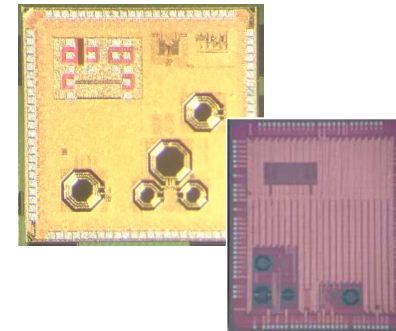
2012 SMART sensor ASICs XFAB 180nm

➔ 50% cost reduction



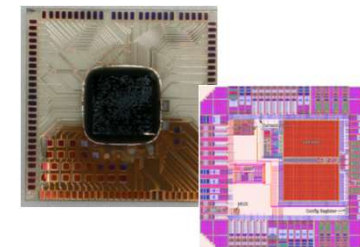
2015 80MSps 12-bit DAC in STM 28FDSOI

➔ 40% cost reduction



2017 500MSps 10-bit DAC in GF22FDX

➔ 60% cost reduction



2019 **5 μ W**, 11 bit, 10 – 100 kS/s, in GF22FDX

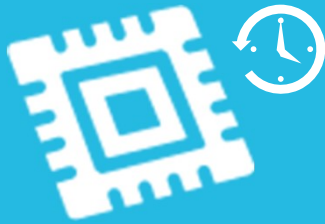
➔ 30% cost reduction



Fast Analog Design Using Generators – Intelligent IP

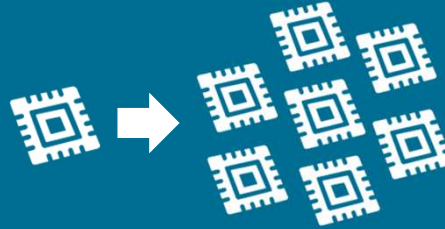
More Efficiency in Design: Our Methods

Design Aid



- Faster design process
- Design safety

IP Reuse



- Faster design reuse & estimation

Full-Custom IIP



- Get your specialized IIP
- Eliminate overhead

+ IIP Framework and Support

+ TechSetups, Customization Support (not included in licensing fees)

THANK YOU FOR YOUR ATTENTION

YOUR CONTACTS



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