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Fraunhofer Institute for Integrated Circuits IIS
Division Engineering of Adaptive Systems EAS

Chiplets for future automotive application

Andy Heinig, Head of Department Efficient Electronics
Fabian Hopsch, Advanced System Integration

Introduction - Use Cases

- **Data center**
  - High speed data processing
  - Contains:
    - **Different processing unit**
    - **Memory**
    - **Interfacing**
  - High speed data processing
    - **E.g. 3/5/7 nm for digital processing**
    - **E.g. 12 nm for IO interfaces**

  - Production volume: mid size volume
  - Budget for exploration: available

Introduction - Use Cases

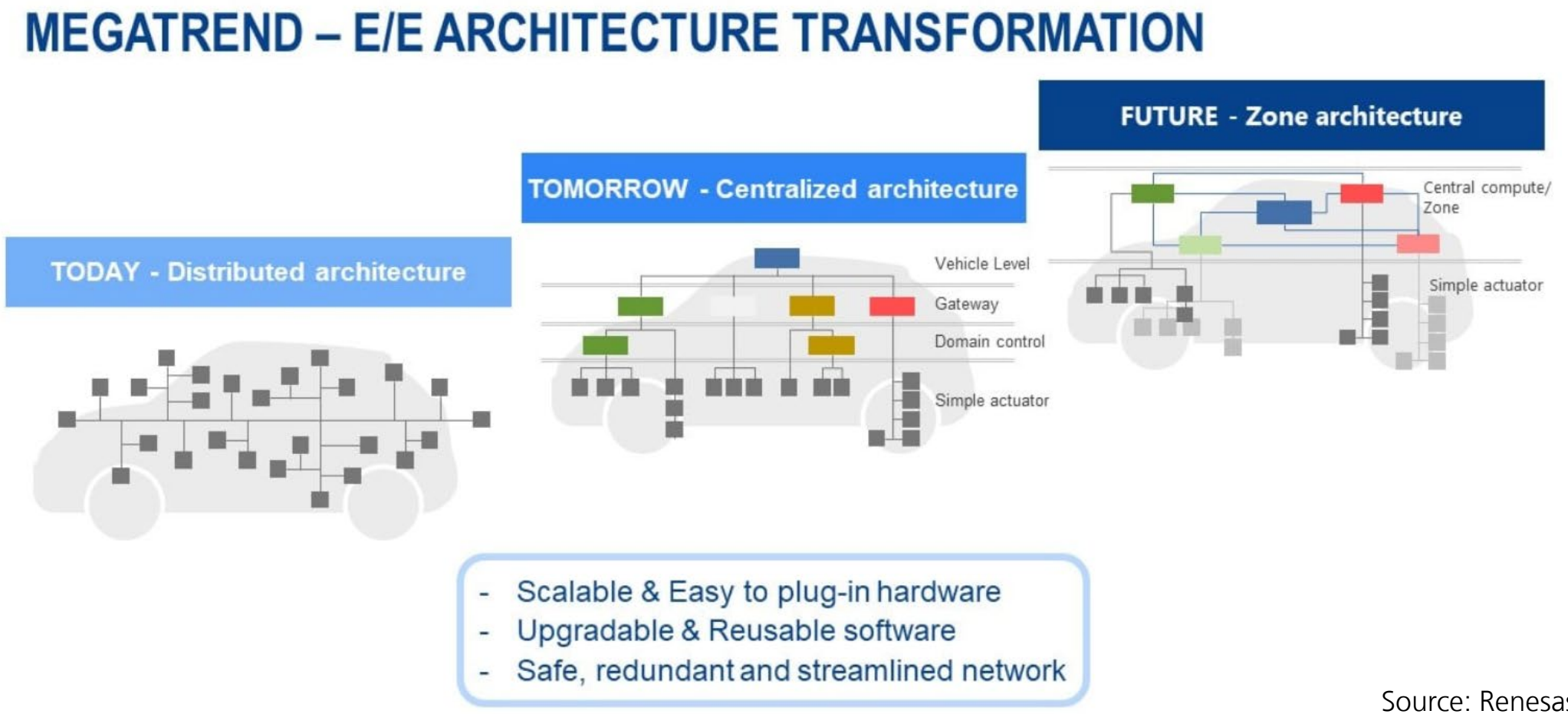
- **Measurement equipment**
  - High speed data acquisition in the range of Gbit/s or Tbit/s from small number of channels
  - Contains:
    - **Analog-to-digital Converter (ADC)**
    - **Digital pre-processing eFPGA (flexible, …)**
    - **Digital processing DSP (FFT, …)**
  - High speed data acquisition needs heterogenous integration approaches with highly specific technologies
    - **E.g. SiGe for data acquisition**
    - **E.g. 5/7 nm for digital processing**
  - Production volume: very small volume
  - Budget for exploration: not available

Introduction - Use Cases

- **Automotive**
  - High speed data acquisition in the range of Gbit/s or Tbit/s from a large number of channels (Lidar, Radar, Kamera, …)
  - Contains:
    - Sensors: Lidar, Radar, Kamera
    - Digital pre-processing eFPGA (flexible, …)
    - Digital processing DSP
    - Digital processing CPU
  - Automotive needs a building block for flexible configurations

  - Production volume: low/mid size volume
  - Budget for exploration: available

EE-architectures



Source: Renesas

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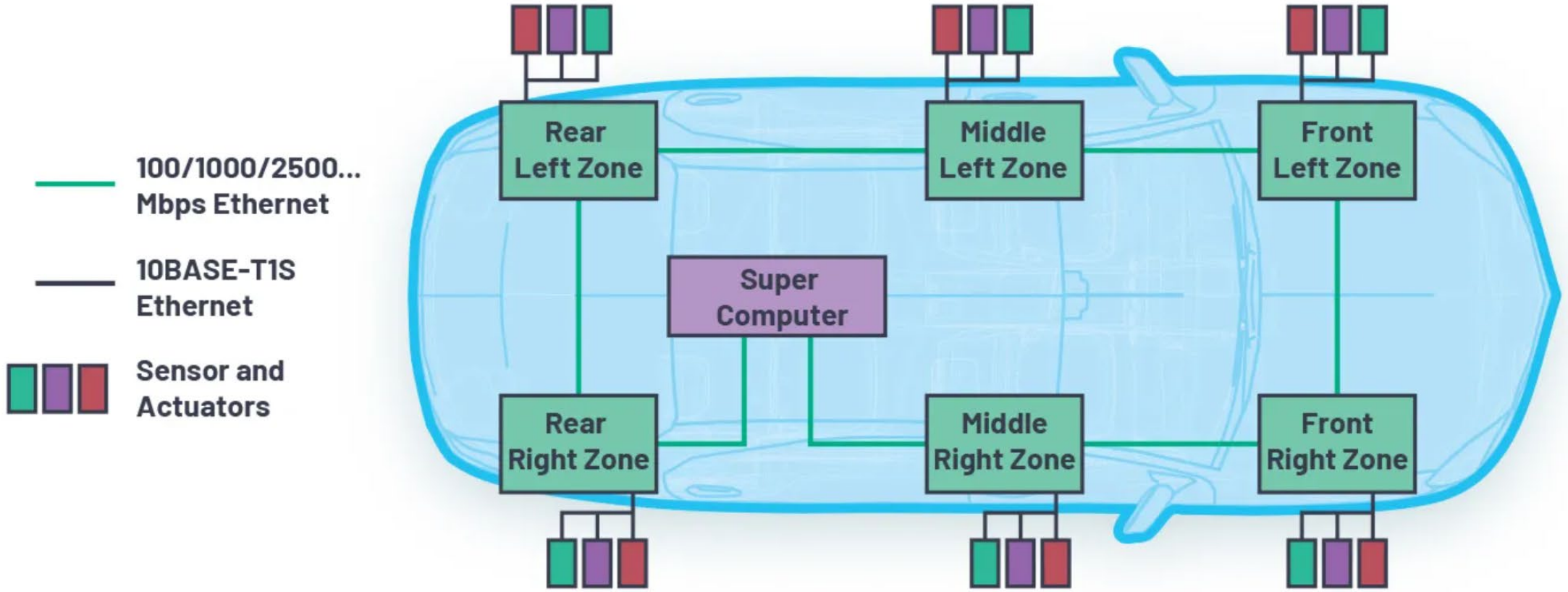
EE-architectures



Source: Analog Devices

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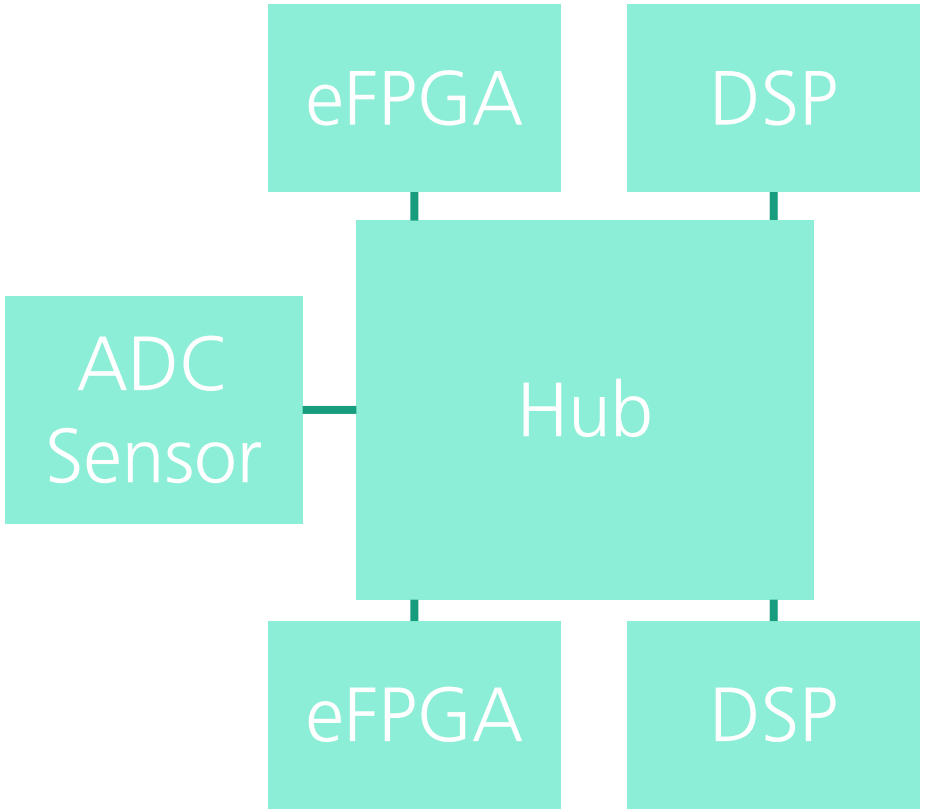
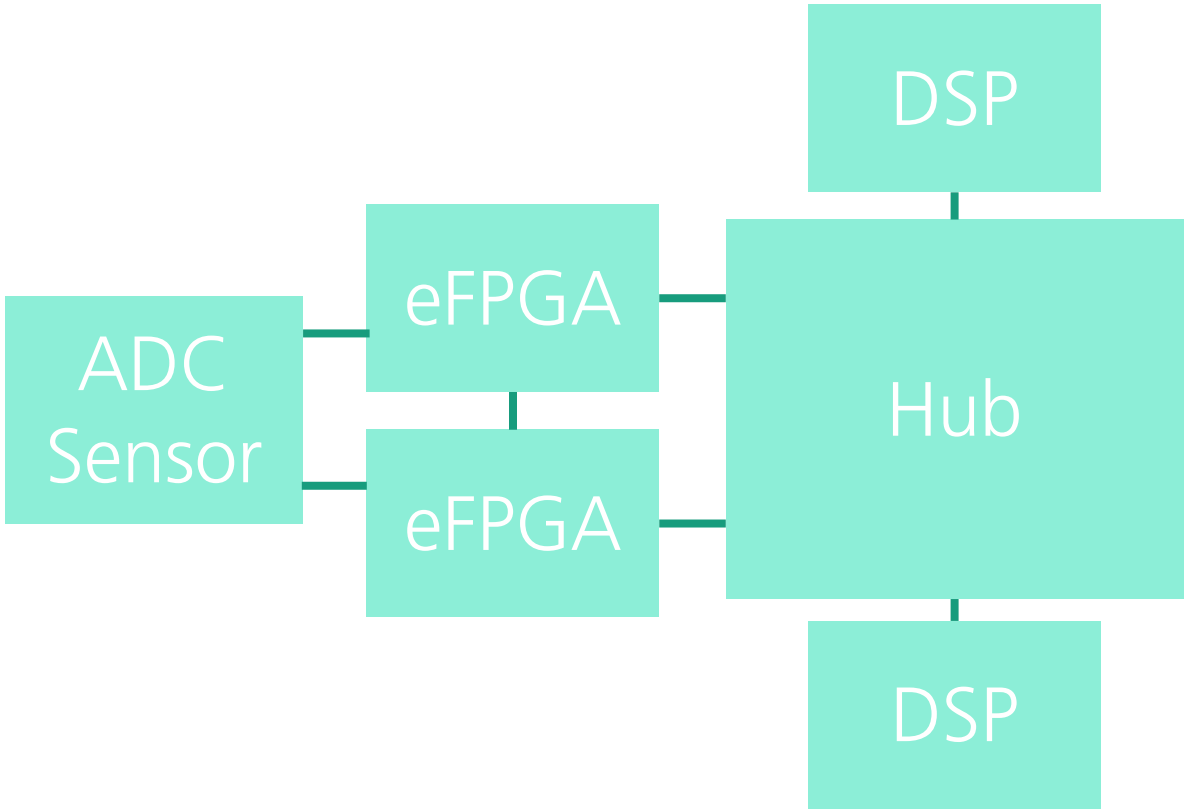
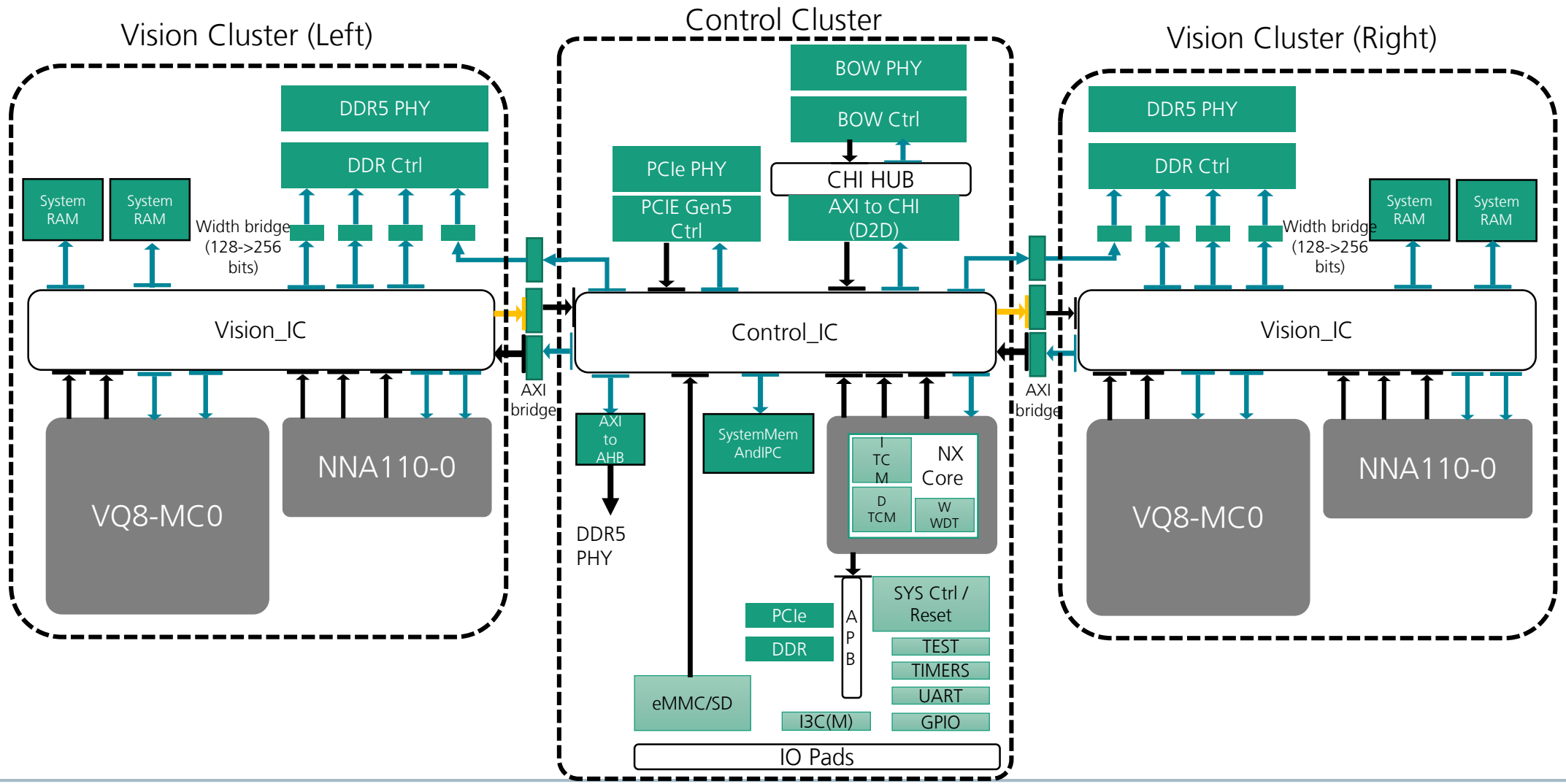
Architectures for Zone controller and HPC





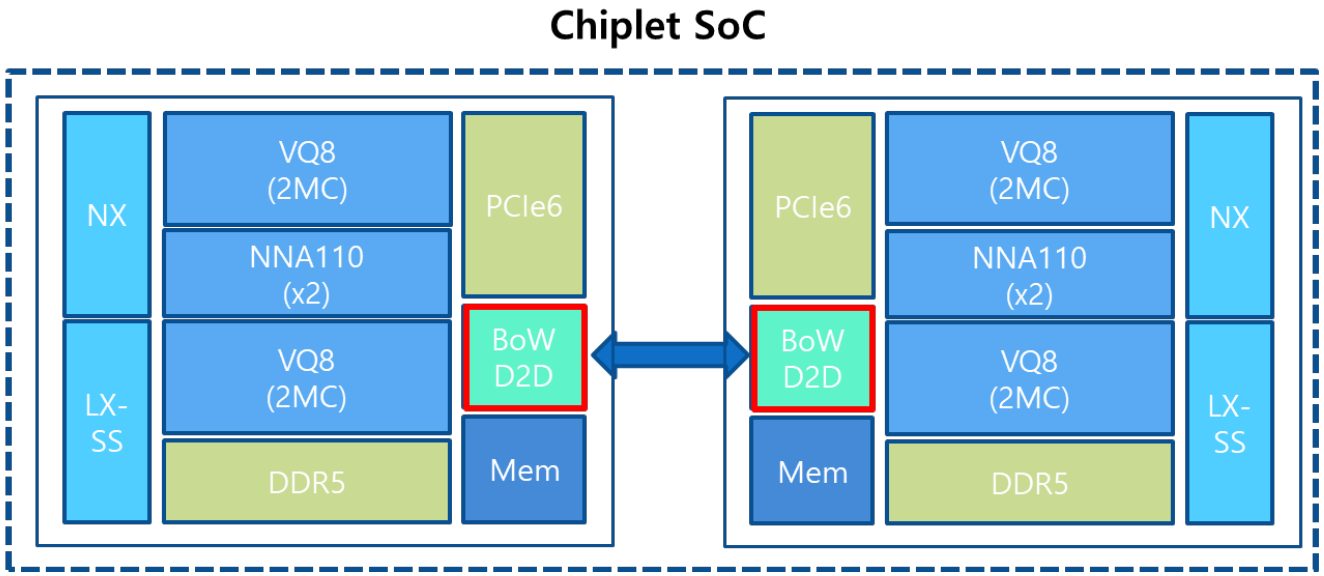
Test/reference system



Test/reference system

- Samsung Advanced SF5A Process
- Cadence NNA110 & Q8 Vison Core
- IO/Memory Core: PCIe6 and DDR5
- System Memory: Xenergic
- Chiplet I/F: BoW D2D

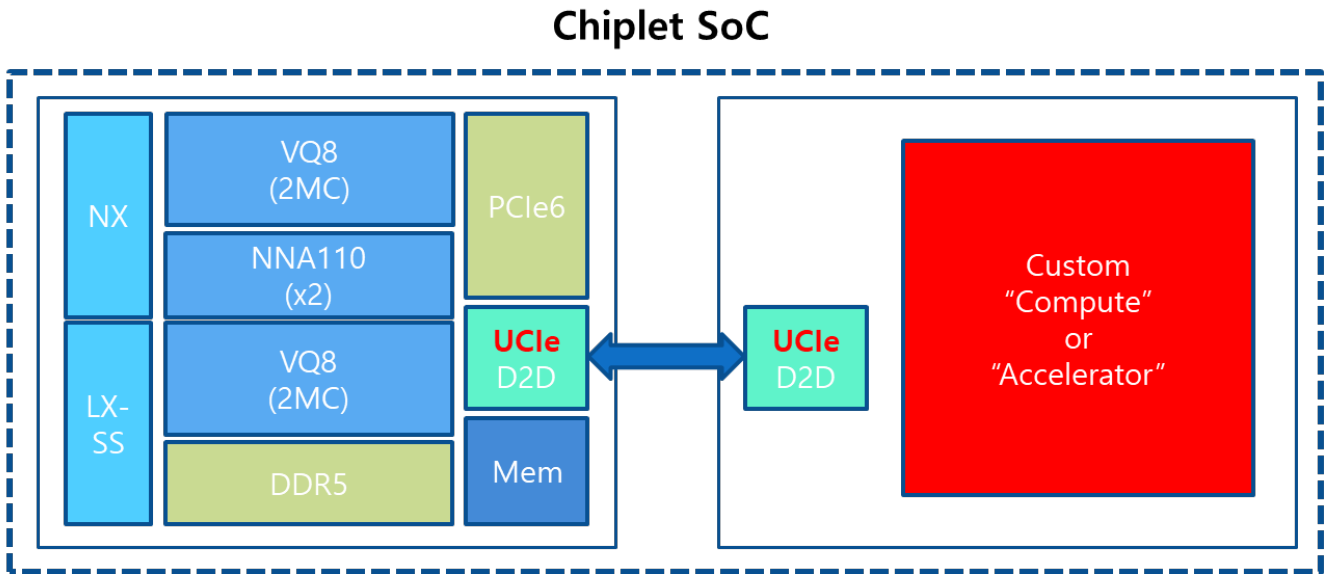
- Chiplet – leverage multiple dies in the same package
- Leverage chiplet and IP reuse
- Highlight Cadence Multi Die tools
- Utilize Samsung Multi Die Packaging



Test/reference system

- A Samsung 5nm IO Hub Platform
- Proven architecture and interoperability
- Leverage SW built on Tensilica DSP
- Ability to change/customize blocks

- D2D: BoW → UCIe
- PCIe: PCIe6 → PCIe5 or more lanes
- DDR: 5600 → 6400/7200/8400 or LPDDR/GDDR/HBM
- System Memory: change size or config.
- Cores: select from AI/ML to Vision to Audio



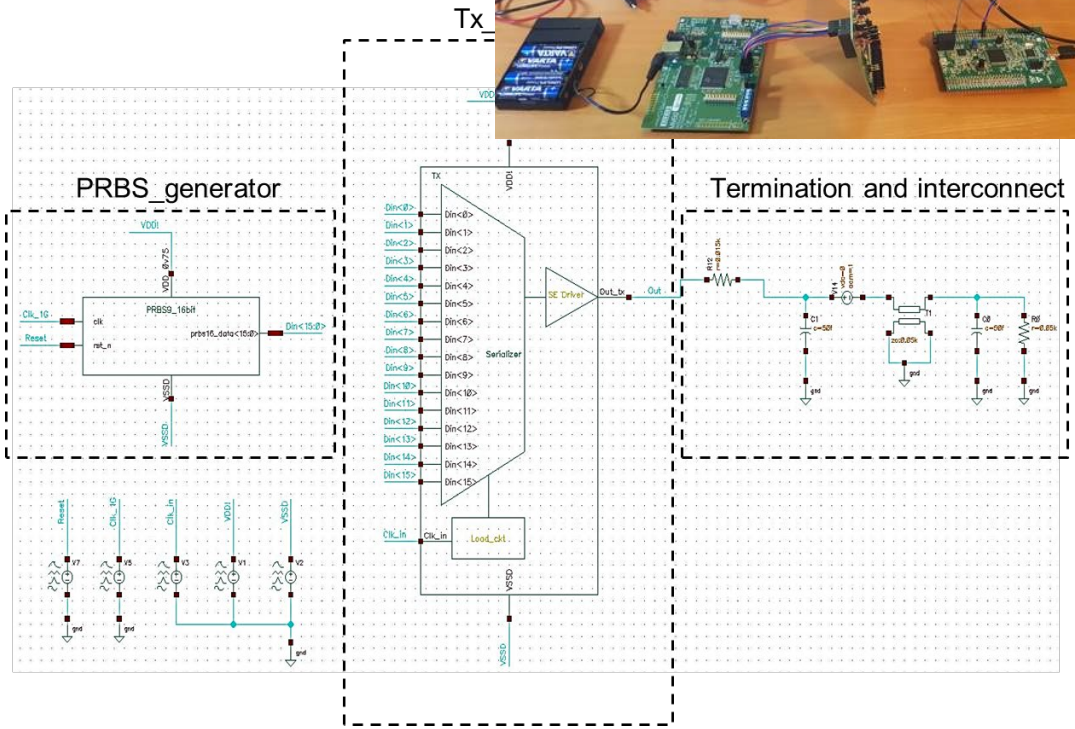
Die to Die Interface (BoW, UCIe)

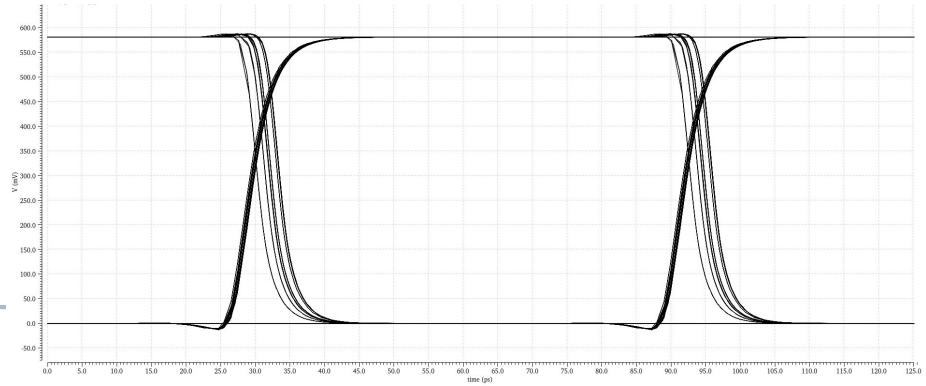
- TX single operates at a clock frequency of 16 GHz and consists of three main blocks:
  - **Parallel-in-Serial-out (PISO)** to serialize the incoming input data.
  - **Loading circuit** which generates the control signal for PISO.
  - **Single-ended (SE) Driver** operates at a adata frequency of 16 Gbps.

- A **PRBS_generator** generates a 16 bits of PRBS-9 input signal. It operates at 1GHz.

- A **Termination resistance** of 15Ω is connected in series to the SE Driver.

- VDD = 0.75 V
- Unit Interval (UI) = $^{1}/_{\text{Data rate}}$ = 62.5 ps





Contact

Andy Heinig
Head of Department Efficient Electronics
Tel. +49 351 45691-250
andy.heinig@eas.iis.fraunhofer.de

Fraunhofer Institute for Integrated Circuits IIS
Division Engineering of Adaptive Systems EAS
Münchner Straße 16
01187 Dresden; Germany
www.eas.iis.fraunhofer.de

Contact

Fabian Hopsch
Advanced System Integration
Tel. +49 351 45691-263
fabian.hopsch@eas.iis.fraunhofer.de

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Division Engineering of Adaptive Systems EAS
Münchner Straße 16
01187 Dresden; Germany
www.eas.iis.fraunhofer.de