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High Throughput Low Energy Industrial Emitter Diffusion and Oxidation

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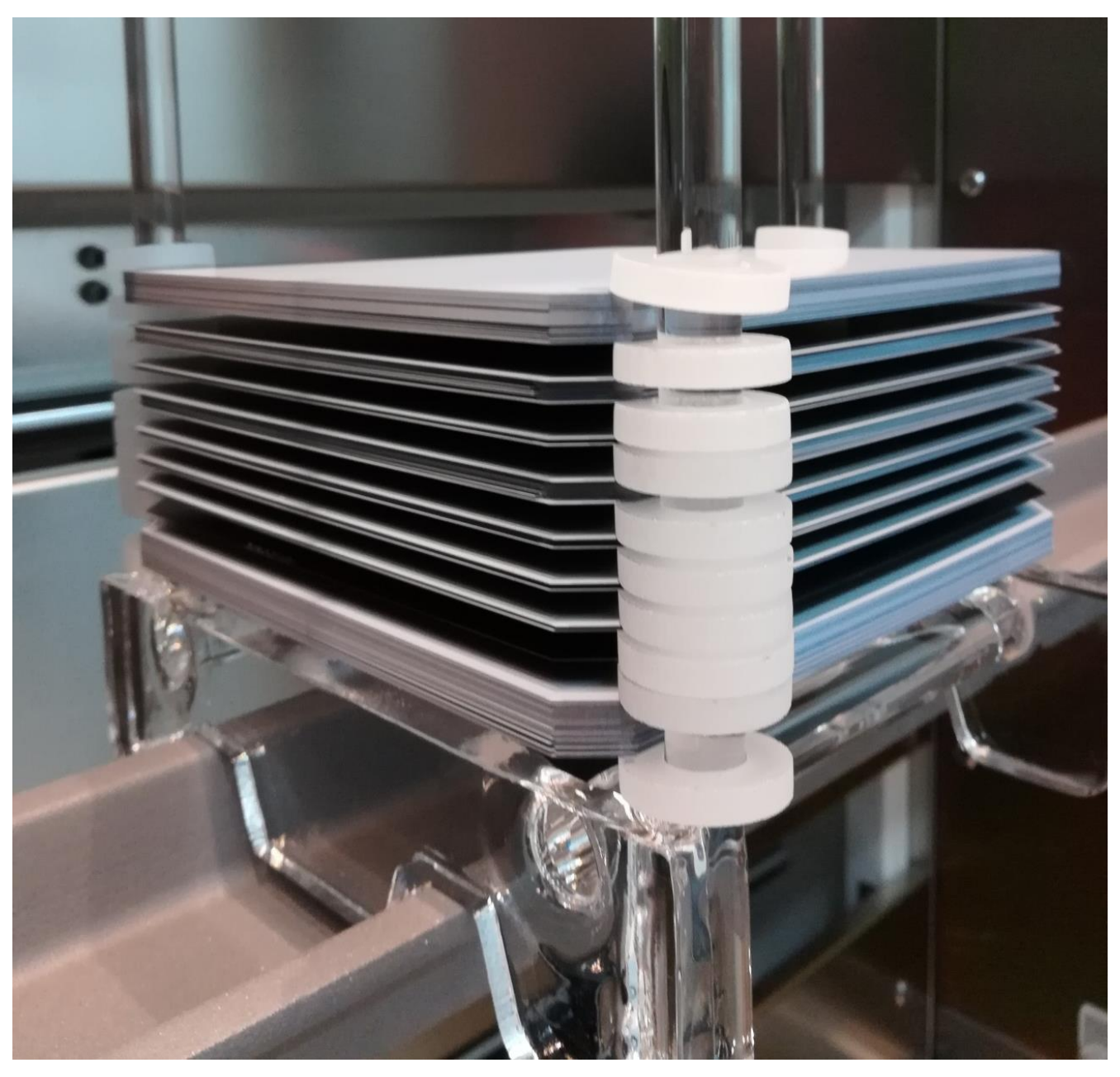
MOTIVATION

- The cost and energy consumption for the emitter formation and thermal oxidation contributes to a significant proportion in the total industrial manufacturing sequence of PERC solar cells
- Aim: Reduce both, the energy consumption and the specific cost with an adapted diffusion and a high throughput oxidation by stacking wafers [1, 2]



Experimental setup: quartz boat with stacked wafers (200 wafers in total)

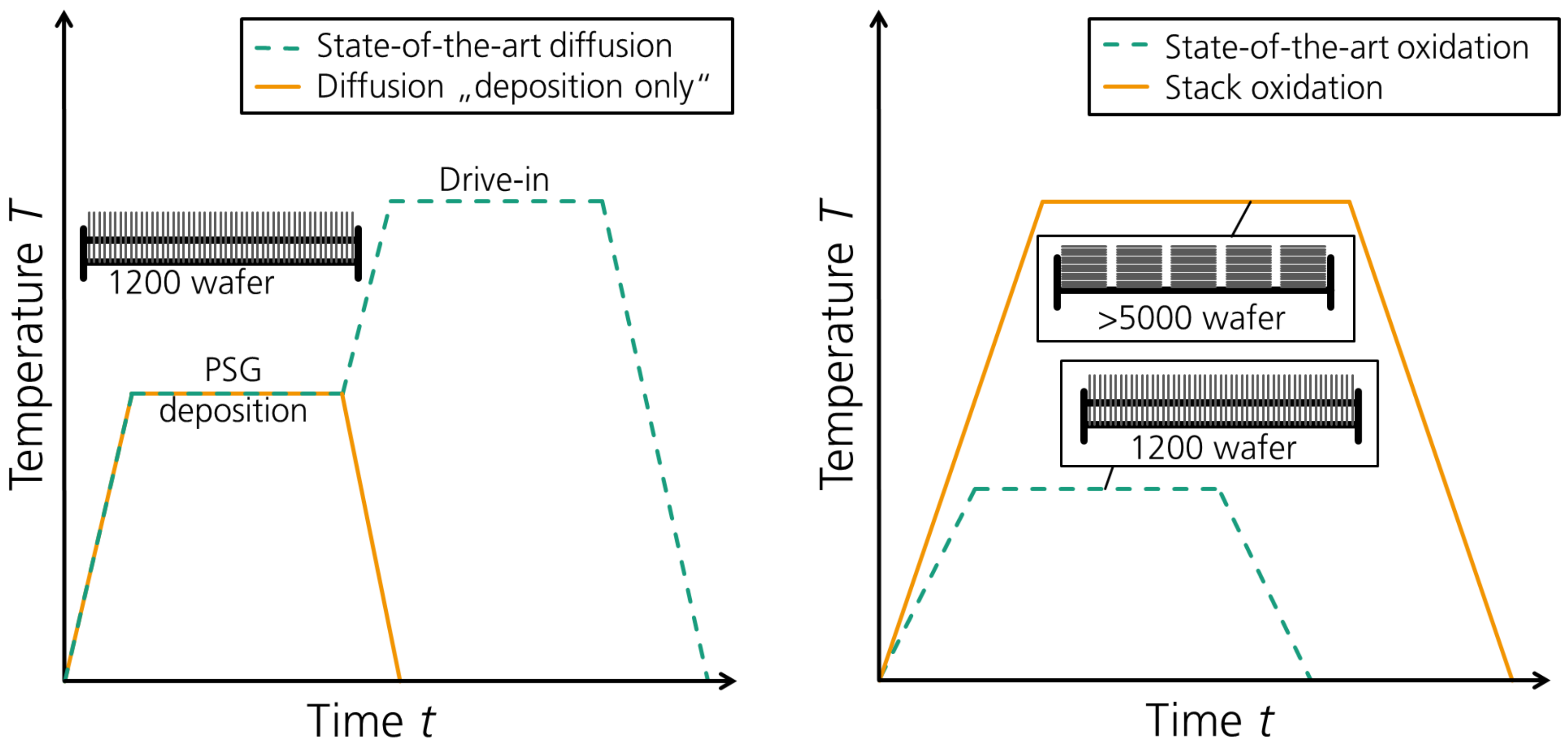
HIGH THROUGHPUT APPROACH

Low pressure (LP) $POCl_3$ diffusion

- Only PSG deposition, no drive-in
- Removal of the phosphosilicat glass (PSG)/SiO_2 layer before thermal oxidation

Thermal oxidation

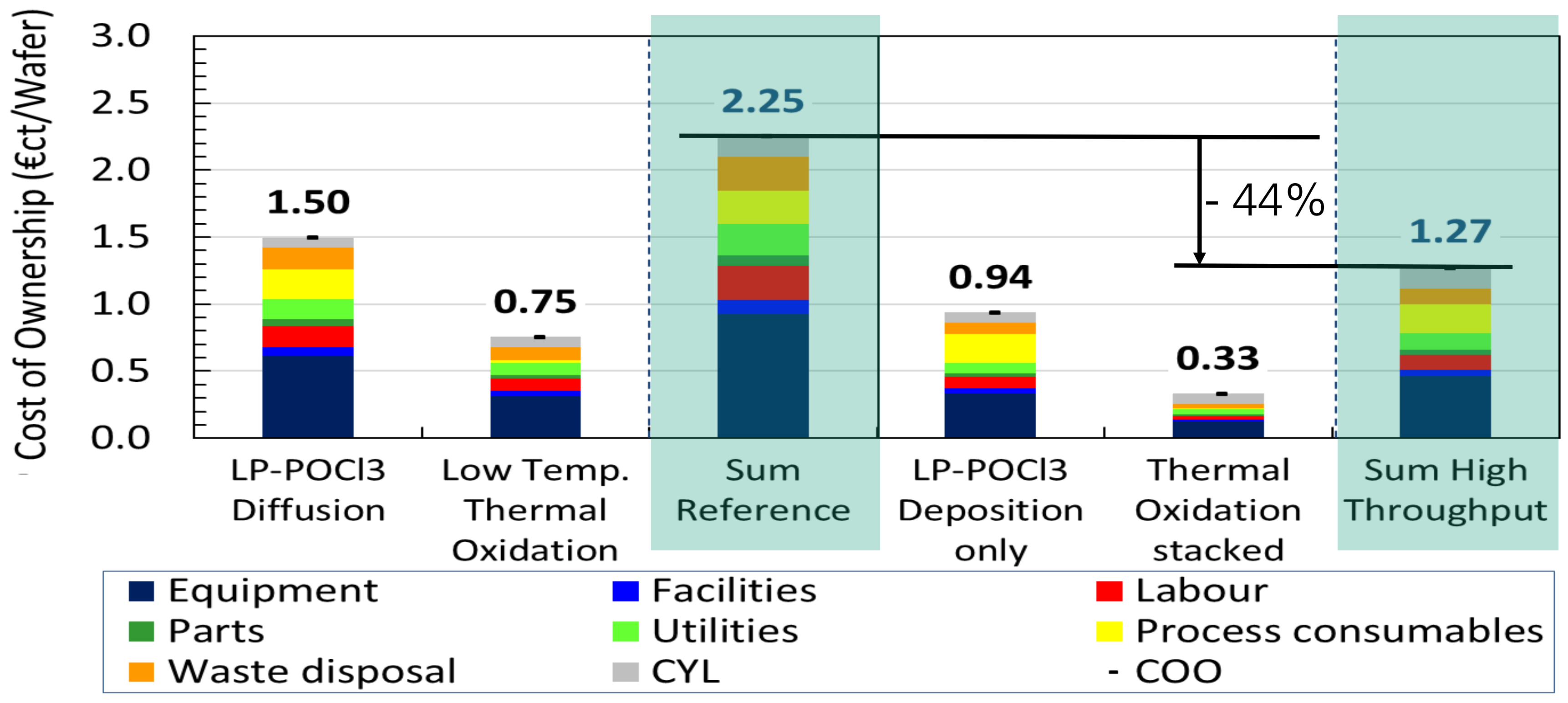
- Adapted process (t↑, T↑), wafer stack
- Redistribution of dopants in Si and oxidation of the surface at the same time



Schematic illustrations of the state-of-the-art processes and of the approach presented in this investigation. Left side: $POCl_3$ diffusion, right side: thermal oxidation

COST CALCULATION

- Cost of ownership (COO) calculated for the state-of-the-art process and our high throughput approach
- Reduction of the COO by 44% *(further details given in paper)*
- The specific power consumption is expected to be reduced by approx. 50%



Cost of ownership calculation for the state-of-the-art processes (left side) and the approach presented in this investigation (right side)

References
[1] K. Breuer *et al.*, DE 10 2011 000 973 A1, Aug. 30, 2012
[2] J. Horzel *et al.*, WO 2010/066626 A2, Dez. 03, 2009

SUMMARY AND OUTLOOK

- High throughput emitter diffusion and oxidation approach by stacking wafers shows lower COO by 44%
- Homogeneous growth of silicon oxide layer is possible within stacks
- Suitable emitter passivation quality with emitter saturation current densities down to $j_{0e} \approx 33$ fA/cm², no negative impact of stacking
- Integration into PERC solar cells with additional laser doping pending

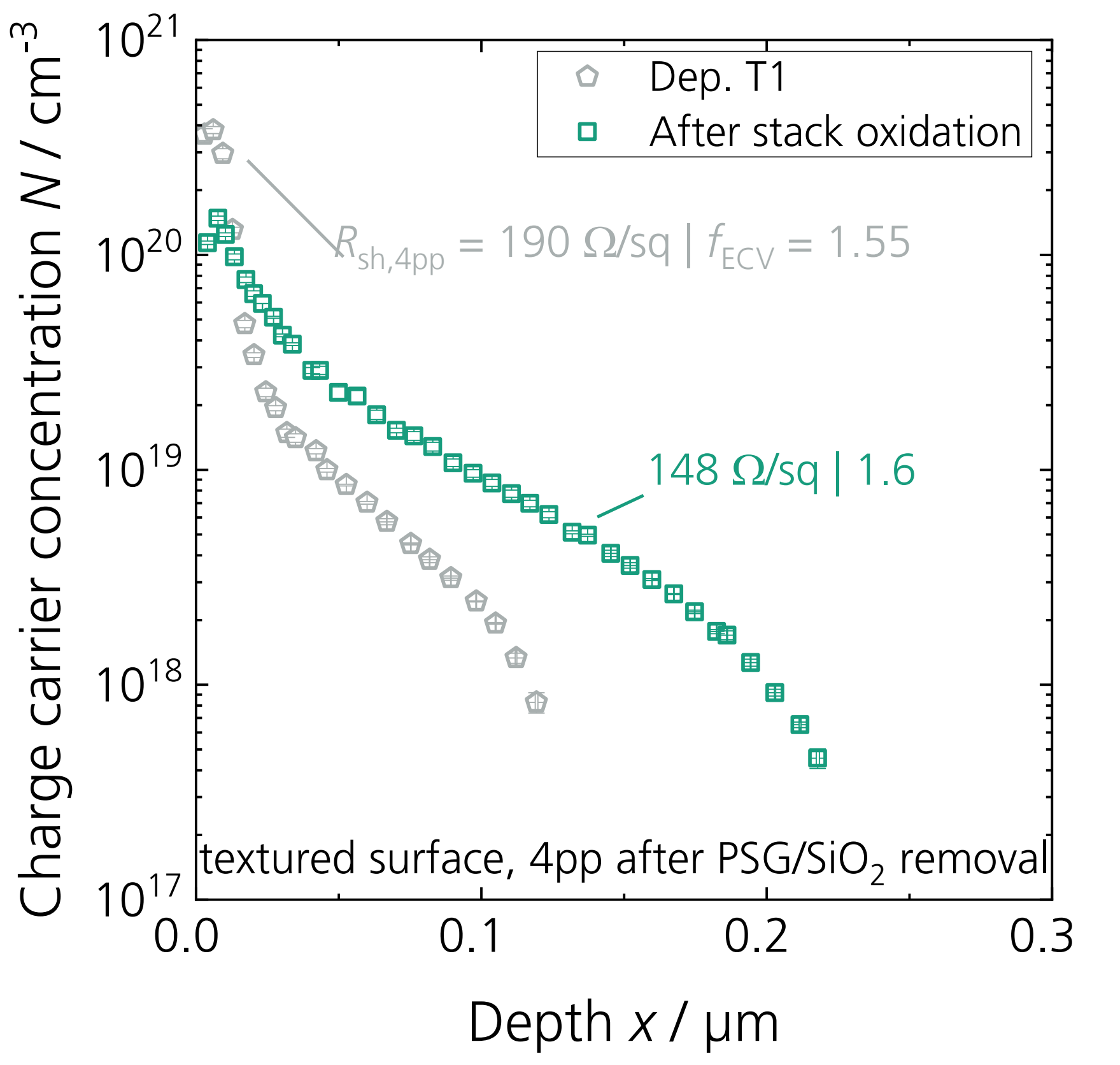
DOPING PROFILES AND EMITTER RECOMBINATION

LP $POCl_3$ diffusion variation

- Variation of the deposition temperature: $T_1 > T_2 > T_3 > T_4$

Electrochemical Capacitance Voltage (ECV) measurements

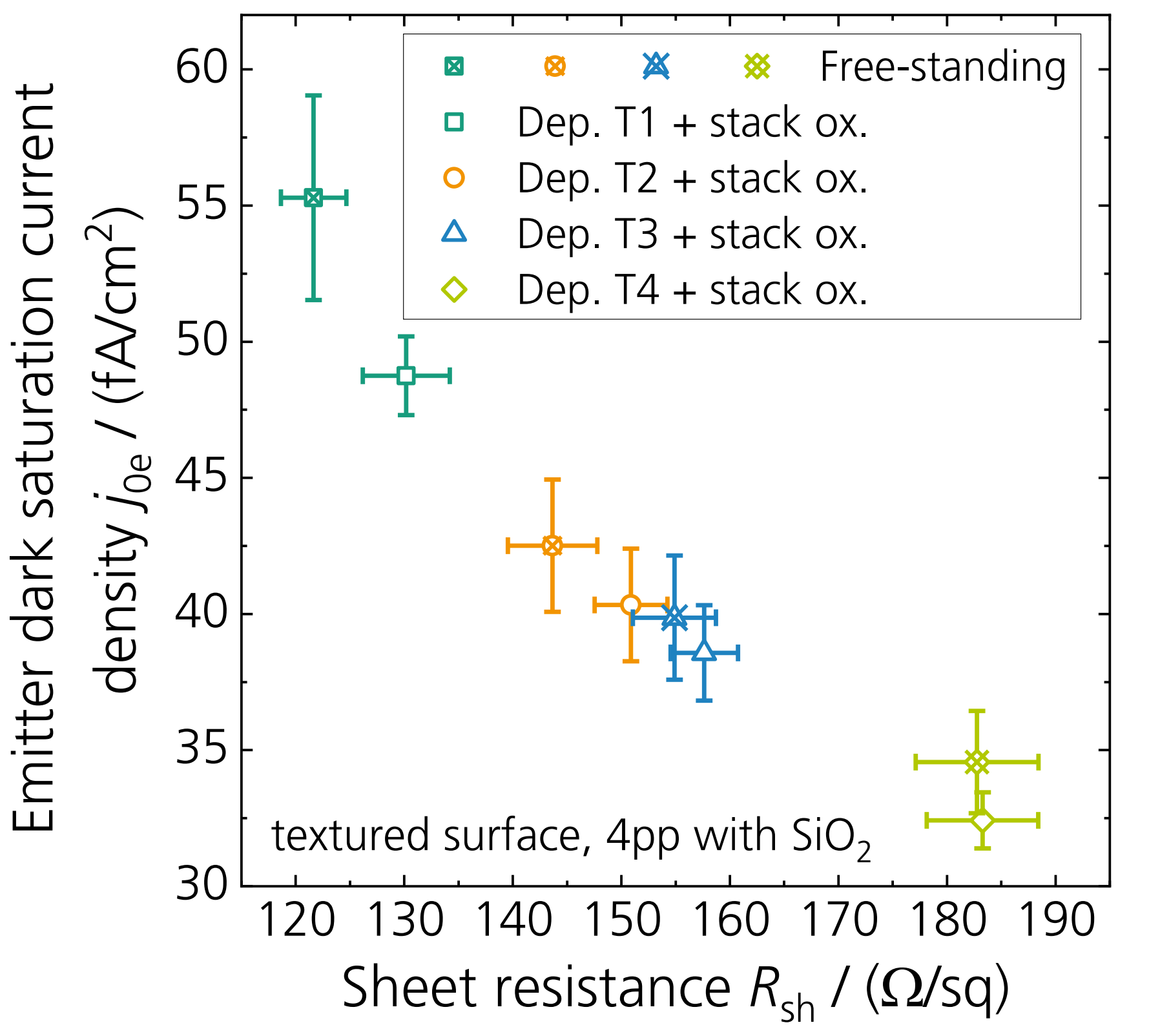
- Four-point-probe (4pp) measurements after PSG/SiO_2 etch on textured surface
- Decrease of the surface concentration N_s with the oxidation from $N_s = 4 \cdot 10^{20}$ cm^{-3} to $N_s = 1.5 \cdot 10^{20}$ cm^{-3}
- Increase of the profile depth with the oxidation process



ECV measurement after diffusion and oxidation

Emitter dark saturation current density j_{0e}

- Sheet resistance R_{sh} measured with 4pp with SiO_2 on textured surface
- Decreasing j_{0e} from j_{0e} = 48 fA/cm² to j_{0e} = 33 fA/cm² (SiO_2/SiN_x passivated and fired) with decreasing deposition temperature while R_{sh} increases
- Comparable j_{0e} for stacked and free-standing wafers

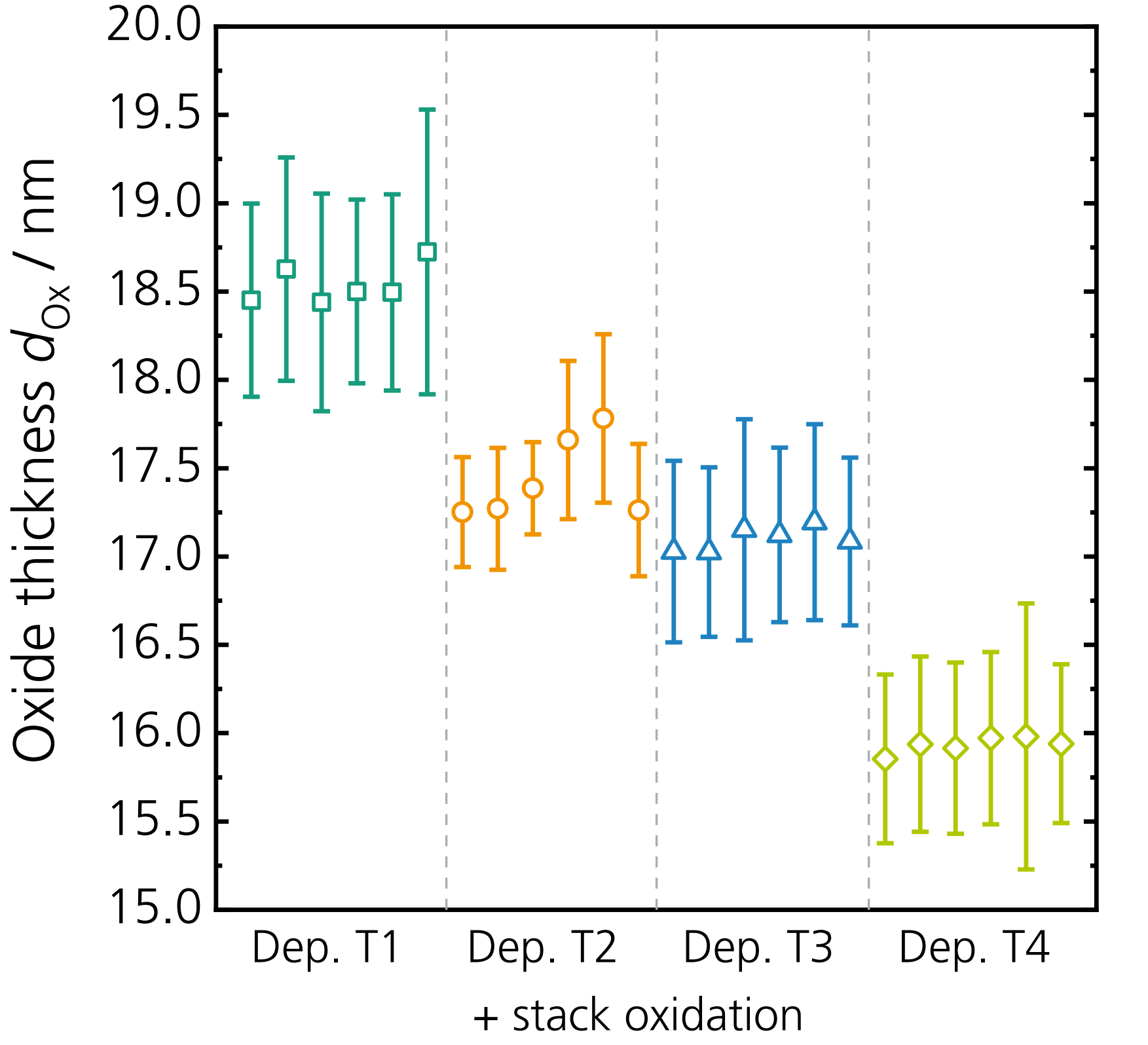


Quasi-steady-state photoconductance measurement

HOMOGENEITY OF OXIDE LAYER THICKNESS

Oxide layer thickness d_{Ox}

- Alternating planar and textured wafers in a stack
- Measured with laser ellipsometer (25 measurements over planar wafer)
- Homogeneous oxide growth over stack and within wafer
- Decreases in d_{Ox} with decreasing deposition temperature due to surface doping



Ellipsometer measurement on planar surfaces

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