NBTI degradation and recovery in analog circuits: accurate and efficient circuit-level modeling

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***Abstract*—We investigate the NBTI degradation and recovery of pMOSFETs under continuously varying analog-circuit stress voltages, and thereby generalize existing digital-stress NBTI studies. Starting from our ultra-fast NBTI measurements and an extensive TCAD analysis, we study two physics-based compact models for analog-stress NBTI including recovery. The high accuracy of both models is evidenced from single-FET analog-stress and circuit-level ring oscillator experiments. Their numerical efficiency allows a direct coupling to circuit simulators and permits to accurately account for NBTI already during circuit design. Furthermore, one of the models calculates the time-dependent NBTI variability of single-FET and of circuit performance parameters. We demonstrate our NBTI models on a ring oscillator and calculate the mean drift and statistical distribution of its oscillation frequency.**

I. Introduction

Recovery is a characteristic trait of the negative-bias temperature instability (NBTI) mechanism [1–3] and distinguishes it from many other transistor degradation mechanisms. However, modeling the (partial) decrease of NBTI degradation during phases of low stress is a considerable challenge. From a circuit designer perspective, investigating this feature in detail is desirable for several reasons. On the one hand, an accurate analog-stress NBTI model allows the controlled reduction of margins away from costly over-designs of analog circuits. Naturally, analog-stress models can also be used in digital design, as the digital signals can deviate from an idealized two-level shape, and features such as overshoots or finite signal edges can have an impact on the NBTI-induced drift of gate delay times and other gate characteristics.

On the other hand, an accurate NBTI model is essential in circuit topologies that rely on matching FETs. Imagine a differential pair circuit subject to NBTI-induced drifts Δ_1 and Δ_2 of its constituent FETs. Conservative degradation models can provide worst-case bounds A and B such that $0 \leq \Delta_1 \leq A$ and $0 \leq \Delta_2 \leq B$. The resulting estimate of the NBTI-induced mismatch $|\Delta_1 - \Delta_2| \leq \max\{A, B\}$ is usually prohibitively large, as designers expect the mismatch to be much smaller than single-FET drifts A, B. Notice that such models cannot bound the mismatch to $|A - B|$. One reason for the unattractive estimate is the lack of a lower bound on Δ_1, Δ_2 better than just 0. Such issues are resolved by NBTI models that fully account for recovery.

Worst-case NBTI models traditionally consider time-independent stress voltages [4]. Further empirical models, in parts proposed for hot carrier degradation, still neglect NBTI recovery but improve the degradation bound by accounting for time dependent stress voltages [5–7]. Models including recovery were first proposed for digital stress voltages, such models use capture-emission-time (CET) maps [2, 8] or otherwise exploit the fact that the stress voltage takes on only two values [9–11]. In the CET map framework, periodic digital stress results in a closed-form solution [12]. Furthermore, it has been shown that stress patterns with a complicated periodic structure have an efficient numerical solution [13]. In analog circuits, the continuous stress voltage levels necessitate a more complex model of the defect dynamics: the differential equation of the Markov two-state NBTI model [2] has an efficient numerical solution for periodic analog stress voltages [14–16]. A complementary approach parametrizes the gate-source voltage (V_{gs}) dependence of CET maps [8] and traces an occupancy map during analog-stress [17].

Here, we discuss two accurate NBTI compact models including NBTI recovery for analog design [18, 19], and we compare their application focus. The present analog-stress study combines the results of experiments, TCAD simulations and the compact modeling approaches. After summarizing our methods, we compare experimental and theoretical results on the NBTI aging of single transistors due to analog gate-source voltages. One of the analog-stress NBTI models was already validated against single FET measurements, and its application to a differential pair (without a validation) was shown [18]. Here, we go several steps further and finally validate the models also against circuit-level (ring oscillator) experiments; moreover, we provide an error estimation of our NBTI predictions, and we give a detailed comparison of the defect-centric and the non-defect-centric NBTI model. We finally demonstrate how our model provides access to the NBTI variability of analog circuits.

II. Technical approach

A. Experimental setup

Both single FET measurements and ring oscillator measurements were performed on production quality MOSFETs of a 130 nm technology with a 2.2 nm thick plasma-nitrided gate oxide. Single FET measurements on pMOSFETs with analog

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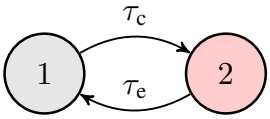

Fig. 1: Two-state defects undergo transitions between a neutral state "1" and a positively charged state "2" with (mean) capture time τ_c and emission time τ_e. These defect-specific times sensitively depend on gate voltage and on temperature. Charging state "2" contributes to NBTI aging.

stress patterns were performed using the ultra-fast measure-stress-measure (MSM) technique [20] with a measurement delay of 1 µs. Different analog-stress patterns (digital AC, sine, sawtooth and inverse sawtooth) at a frequency of 0.5 kHz and 2 kHz were applied at a stress temperature of $T = 125°\mathrm{C}$ and maximum stress voltages of $V_{\mathrm{high}} = -2.8\,V$.

Furthermore, we use two different ring oscillators (INV and NOR) to study the impact of NBTI on a circuit. The ring oscillators are placed between heater stripes to accelerate degradation with temperature and avoid the need for heating the chuck, which enables fast in-line measurements at the process control monitor. The experimental sequence includes frequency measurements before as well as after stress at operation voltage (room and stress temperature). After the temperature reaches the target temperature, the stress bias is applied and the frequency at stress voltage is measured in situ during stress without any introduced recovery. In addition, the frequency measurements at operation conditions before and after stress serve as reference for the first frequency read-out at stress conditions.

B. TCAD modeling of NBTI

The extraction of defect properties and the simulation of defect kinetics with TCAD tools [21, 22] enable the parametrization and verification of the defect centric compact simulations presented in this work. For the extraction of defect properties, we use extensive BTI data measured on devices with large gate areas to obtain the mean degradation which holds information on a large ensemble of defects. The extended Measure-Stress-Measure (eMSM) scheme is usually applied here because the measurement cycles with stress phases followed by extended recovery phases for up to 100 ks comprise detailed information of both degradation and recovery [23]. Typically, two dominant degradation mechanisms are reported for such BTI experiments: a) Charging and discharging of pre-existing oxide defects, causing a recoverable shift which can be described by the four-state non-radiative multi-phonon (NMP) model [2] and b) a more permanent degradation which is probably due to hydrogen relocation in the near-interfacial region. Due to its complexity, the latter is modeled phenomenologically with a simple double-well (DW) model [24]. The distributions of the parameters of these two models are then optimized to obtain one set of defects which gives consistent results for all experiments with different stress times, temperatures, and voltages conducted on the technology of interest and is in line with physical values obtained from ab-initio studies [25].

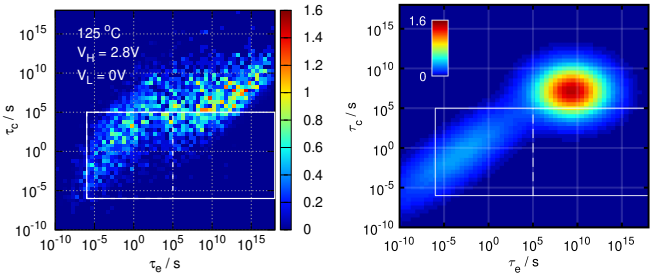

Fig. 2: Visualization of the CET maps in the NBTI defect sampling model (left) and the approach of fitting to a CET map ansatz function (right). The dimension of the z axis is mV. The white rectangles mark the windows of experimental characterization.

C. Compact modeling of NBTI

The NBTI two-state Markov model projects out metastable defect states and considers uncoupled oxide (NMP) and interface (DW) defects to cause NBTI aging (see e.g. [2]). Each defect occupies either an electrically neutral or a positively charged state, and transitions between the two states occur with characteristic capture and emission times that depend on V_{gs}, temperature and defect properties (Fig. 1). The threshold voltage shift ΔV_{th} results from a change of the oxide electric potential due to charged defects, and its (mean) value reads

$$\Delta V_{\mathrm{th}}(t) = \sum_k \eta_k \times \big(w_k(t) - w_k(t_0)\big), \qquad (1)$$

with $w_k(t)$ the probability that defect k is charged at time t, and η_k its ΔV_{th} contribution.

The properties of the contributing defects play an essential role. We account for their distribution by two distinct models: on the one hand, we employ a database with defect properties obtained in a TCAD analysis of experimental NBTI data (defect sampling model, DS). On the other hand, we model the "collective" defect behavior by a fit of experimentally obtained capture-emission-time (CET) maps to an ansatz function (CET map based model, CB). Both models calculate the mean ΔV_{th} independently but are calibrated to the same experimental data set. Both models assume a periodic $V_{\mathrm{gs}}(t)$. In applications, stress patterns can also feature multiple periodicities on different time scales, corresponding to e.g. different IC power states, day-night cycles, mission profile requirements; the DS model efficiently calculates also the effect of such patterns [13]. Table I compares both approaches to TCAD, Fig. 2 compares an exemplary CET map for the two models.

1) NBTI compact model based on defect sampling (DS): To be more specific, the DS model employs a TCAD-generated database that discretizes the dependence of the capture and emission time constants τ_c, τ_e on V_{gs} and temperature ϑ for $\sim 10^4$ technology-characteristic defects (see Sec. II-B). For each defect, we then solve the differential equation governing the time evolution of the occupation probability w_k,

$$\dot{w}(t) = a(t)w(t) + b(t), \qquad w(t_0) = w_0 \qquad (2)$$

with $a(t) = -\tau_e^{-1}(t) - \tau_c^{-1}(t)$ and $b(t) = \tau_c^{-1}(t)$, using a numerically efficient algorithm [14]. Notice that the coeffi-

Tab. I: Comparison of the defect sampling and CET map based NBTI compact models to the TCAD reference. In the simulation effort column, the example time corresponds to calculating 100ks of sine stress (100 MHz) on single-core hardware. The fast parametrization of the CB model allows its application to a large number of transistor types. The additional experimental effort for the parametrization of the DS model enables the calculation of NBTI variability. Using TDDS information or estimating mean defect step heights η, prediction of NBTI variability with the CB model is currently studied.

Model	base	defect states	degrees of freedom	experimental effort [time / FET]	simulation effort [time / FET]	feasible V_{gs} patterns/ stress times	NBTI variability	V_{ds} dep.	freq. dep.	advantage
TCAD	10^4 individual defects	2 and 4	24	TDDS + eMSM [1000h]	too high for Spice	any / small	yes	yes	yes	fundamental physical simulation
DS		2	24 (via 10^4 defects)		closed-form for each defect [10ms]	periodic, nested periods [13] / any	yes	no	no	faster than TCAD, NBTI variability, nested-periods stress
CB	V_{gs} dep. AEMs		20	TA-MSM [50h]	closed-form for each CET bin [10ms]	periodic / any	in dvp.	no	no	faster than TCAD, fast parametrization

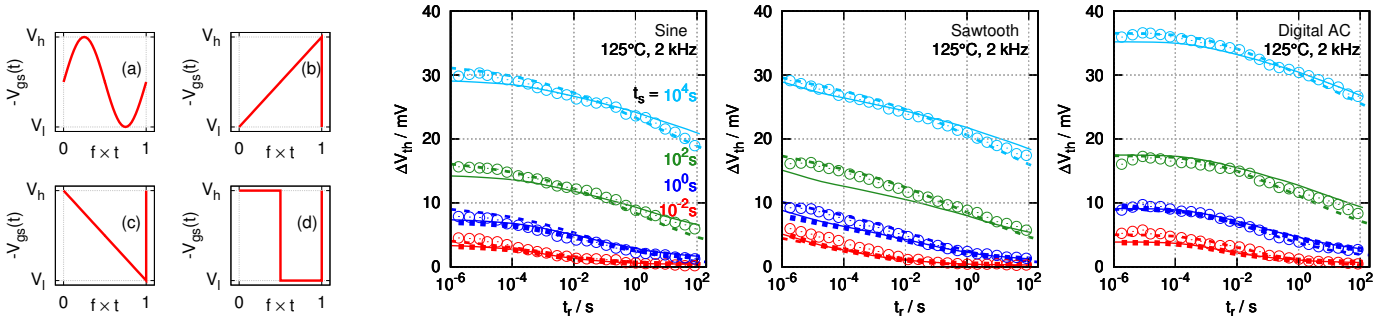

Fig. 3: The analog-stress MSM experiments periodically apply one of the four stress patterns: sine, sawtooth, inverse sawtooth, digital AC (a to d, ***left***). The stress voltage oscillates between the values $V_l \leq -V_{gs}(t) \leq V_h$. ***Right (three plots):*** The MSM ΔV_{th} recovery curves after four stress durations 10^{-2}s, 10^0s, 10^2s and 10^4s (bottom-up in the plots) show a good agreement between experimental data (symbols), TCAD results (thick dashes) and compact model results (defect-sampling model: solid, CET-map based: dashed lines). The present setup uses a stress frequency of 2kHz, a temperature of 125°C and stress voltages between $V_l = 0.5$V and $V_h = 2.8$V.

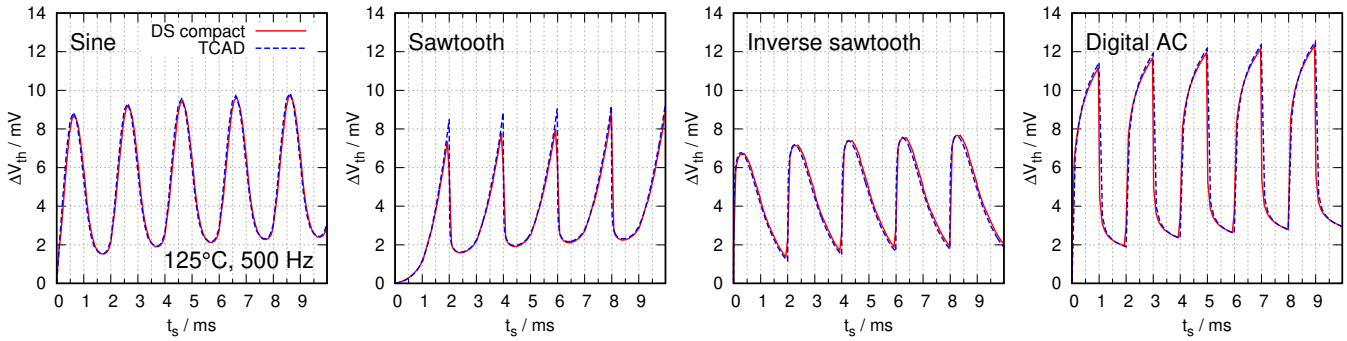

Fig. 4: Threshold voltage shift during analog stress. We compare the DS model results on ΔV_{th} (solid line) to their TCAD reference (dashed line), for the first five periods of the stress phase. For all four stress patterns, both methods are in excellent agreement. The calculations use a stress frequency of 500Hz, a temperature of 125°C and voltage values $V_l = 0.5$V and $V_h = 2.8$V.

cients in the above equation depend on the FET's stress signal $t \mapsto V_{gs}(t)$ and therefore are time dependent. The sum in eq. (1) provides the time dependent shifts $\Delta V_{th}(t)$ for each pFET in the investigated circuit.

2) NBTI compact model based on CET maps (CB): The CB approach rewrites the sum in eq. (1) in terms of CET maps [2, 8]. Measurements on wide FETs with a large number of defects allow a fast parametrization of these maps [17], replacing the single time constants of each individual defect by an analytical form of the capture and emission time map (see Fig. 2 b) [8]. With the temperature-accelerated MSM (TA-MSM) technique, the temperature and stress voltage dependence of the CET maps can be obtained with very low measurement effort and one activation energy map (AEM) is used to describe all dependencies [17]. The stress signal is approximated by a digital stress pattern for N_V stress voltages and the charging and de-charging of the defects is described analogously to the charging function of a single RC element [12], eq. (2). Furthermore, the defect occupancy is described in a closed, stress time and frequency independent form [19]. The threshold voltage shift contributed from each N_V differential activation energy maps is calculated as the integral of all defects being charged up to the stress time and not yet discharged at the recovery time. The total threshold

voltage shift is then the sum over all threshold voltage shifts of the N_V discrete stress voltages. A detailed description of the model can be found in [19].

D. HCI empirical model

Furthermore, to estimate the full degradation in the ring oscillator experiments, the effect of hot carrier stress on carrier mobility is independently considered using the empirical model proposed by Takeda [26] with a polynomial covering the gate-voltage dependence [27].

III. Experimental Model Validation

The NBTI compact models were calibrated to measurements at time-independent stress voltages, using a large number of combinations of V_{gs} and temperature. We validate our model by comparing to additional NBTI measurement results: in a first step to single FETs under time dependent stress voltages, in the second step to a whole ring oscillator circuit.

A. Single FETs under analog stress

Our MSM experiments apply the analog V_{gs} patterns of Fig. 3 (left), namely a sine, sawtooth, inverse sawtooth and digital pattern, during four different stress times (10^{-2} to 10^4s) and then measure the NBTI relaxation. Fig. 3 (right) shows the good agreement between the measurement results (symbols) and the compact models (solid and dashed lines) as well as the TCAD simulation (thick dashes).

Although the degradation during the NBTI stress is experimentally inaccessible in the ultra-fast measurement setup, we compare the predictions of the DS compact model to the more fundamental TCAD simulation: Figure 4 shows the results for the first 5 stress periods and an excellent agreement. Figure 5 displays in detail the relative ΔV_{th} difference between TCAD and DS model simulations for the first 10^4 to 10^5 stress periods, separately for the fast NMP (left) and the slow DW defects (right). Increasing the time discretization of the stress pattern from ~ 100 (dashes) to ~ 200 points per period (solid lines) pushes the error to essentially below 5%. Presumably, the error is even much lower if compact model and TCAD use exactly the same stress pattern discretization scheme (linear grid plus logarithmic grid near discontinuities of the stress pattern). The DW defects at small stress times (shaded region) show a larger deviation, but their ΔV_{th} contribution is very small then; their V_{th} contributions larger than 1mV have an error $< 5\%$ as well. The high accuracy of the DS model comes with the advantage of a few seconds vs. several hours (TCAD) runtime for 10^4 stress periods.

B. Ring-oscillator aging

We further validate the NBTI models for the use in circuit simulators with ring oscillator frequency measurements at accelerated stress conditions. Simulations are performed with the previously described BTI and HCS models integrated into the *Spectre* circuit simulator. To observe a measurable change in the ring oscillator frequency, we stress at a temperature of $T = 175°C$ and at $V_{dd} = 2.4\,V$, which is way above the

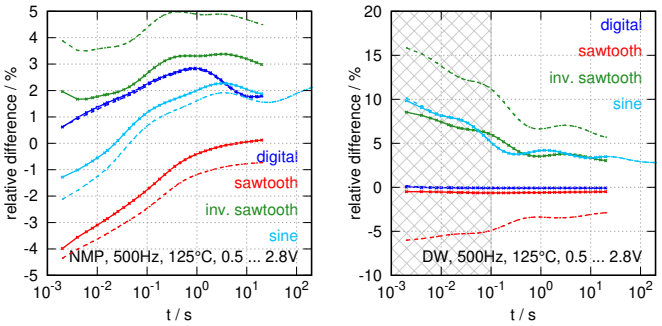

Fig. 5: Threshold voltage shift for 10^4 and 10^5 analog-stress periods (patterns of Fig. 3 left). The plots show the relative difference between the TCAD and the DS compact model results for the NMP defects (left) and the DW defects (right). Symbols mark the considered stress times. Whereas the time discretization of the stress pattern with $\sim$ 100 samples (dashes) has a larger error, $\sim$ 200 samples per period (solid lines) push the error to essentially below 5%. Besides high accuracy relative to TCAD, the DS model furthermore has the advantage of a few seconds vs. several hours (TCAD) runtime for 10^4 stress periods.

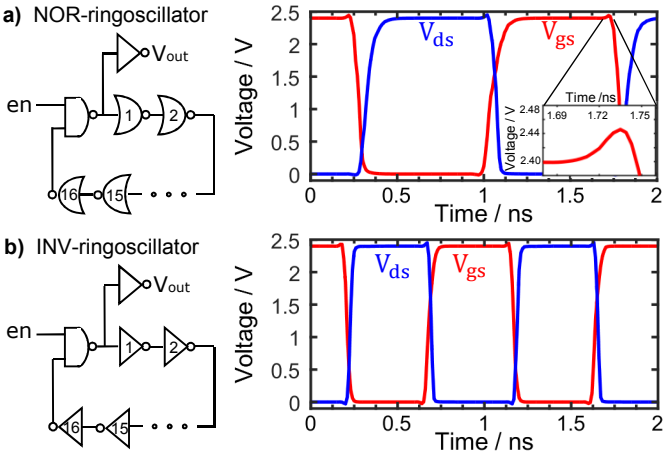

Fig. 6: Sketch of the schematic (left) and plot of the time-dependent pFET stress voltages V_{gs}, V_{ds} (right) for the 17-stages **a)** inverter ring-oscillator and **b)** NOR ring-oscillator. The inset in the top-right plot shows the voltage overshoot in the oscillation pattern.

use conditions of $V_{dd} \leq 1.5\,V$. The resulting ring oscillator stress patterns are shown in Fig. 6 a) and b). For each type of ring oscillator, eight fresh chips are measured and all measurement traces are shown in Fig. 7. Already after a short stress time (increase of V_{dd} to the stress voltage), the ring oscillator frequency during the first in situ read-out decreases. Therefore, measurements and simulation at use condition before and after stress are used to determine the frequency $f(t = 0)$ at $V_{dd} = 2.4V$ for the unstressed ring oscillator, which is then used as a reference for the in situ frequency read-outs. The obtained initial ring oscillator mean frequencies and standard deviations at stress conditions are $630 \pm 10\,$MHz and $990 \pm 15\,$MHz for the NOR and INV ring oscillator, respectively. Note that ring oscillator frequencies are very sensitive to FET variability. Variability of the initial frequencies is mainly due to different test chip positions on the wafer. Measurement uncertainty is $0.1\,$MHz.

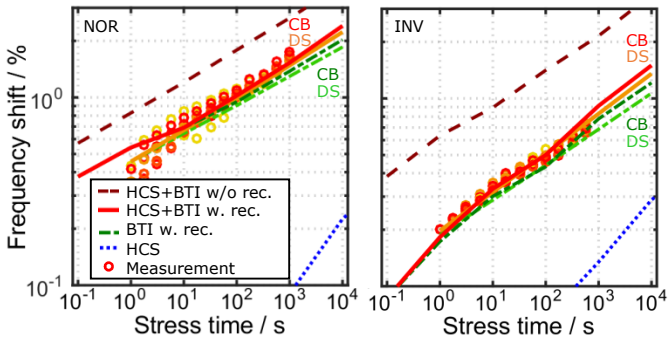

Fig. 7: Measurements of the relative frequency change over stress time in comparison with simulations for three different BTI models for the NOR ring oscillator (left) and the INV ring oscillator (right). Measurements of 8 chips are shown as open circles, lines correspond to simulation with the models. The simulated frequency shift solely due to BTI is shown as dashed green lines (pure BTI including recovery, CB dark green, DS bright green) and solid lines (BTI and HCS with recovery: CB red, DS orange and dashed dark red line corresponds to the empirical model disregarding recovery). The frequency shift solely due to HCS is indicated with blue dotted lines. Measurements and simulation with both BTI recovery models show a very good agreement for all measured stress times.

The relative frequency decrease for the *in situ* measurements (open circles) during stress at $V_{\mathrm{dd}} = 2.4\,\mathrm{V}$ and $T = 175°\mathrm{C}$ and the corresponding simulation results (lines) are shown in Fig. 7 on the left for the NOR and for the INV ring oscillator on the right. The frequency decrease due to aging of the INV ring oscillator is clearly lower than that of the NOR ring oscillator for all stress times. This is due to the design of the two ring oscillators with the number and position of the aged transistors influencing the frequency: The NOR gate contains two stacked PMOS and two NMOS, whereas the INV gate consists only of one PMOS and one NMOS. After $1000\,\mathrm{s}$ of stress, the NOR and INV ring oscillator frequency decreased by $1.65 \pm 0.05\,\%$ and $0.79 \pm 0.03\,\%$, average and sigma of all 8 chips respectively. In addition, the effect of the aged MOSFETs is even more enhanced switching back (switching time: $\sim$ 1ms) to use conditions $V_{\mathrm{dd}} = 1.5\,\mathrm{V}$ (at $T = 175°\mathrm{C}$), showing a frequency shift of $3.8 \pm 0.2\,\%$ and $2.2 \pm 0.1\,\%$, for the NOR and INV ring oscillator, respectively, in accordance with simulations. Both NOR ring oscillator and INV ring oscillator are sensitive to NBTI degradation, HCS is nearly negligible due to a low $V_{\mathrm{gs}}/V_{\mathrm{ds}}$ crossing point for the NOR as well as the INV ring oscillator stress pattern (compare voltage intersections in Fig. 6 a and b). For the sake of completeness, even though HCS is nearly negligible for these circuits and stress conditions, we account for HCS (blue dashed lines). First findings indicate that the actual degradation is less than the addition of the single effects [28], but due to the low HCS component, this is not the focus of this study.

We compare three NBTI simulations to the measurements: the DS and CB models (accounting for recovery, see Sec. II-C) and an empirical model without recovery (V_{gs} and T dependent power law, measurement delay $1\mu\mathrm{s}$). In addition, we simulate the frequency decrease due to HCS. As seen in Fig. 7, both recovery models, the CB (dashed dark green lines) and DS (dashed bright green lines) model, show a very good agreement with the measurement data. The dependence on stress time as well as the magnitude is perfectly covered by both NBTI recovery models and shows the applicability of single transistor aging models to circuit aging simulations. The differences between the two models are small: the BTI induced frequency shift of the CB model (red line) lies slightly above the DS model (orange line) but with very similar dependence on the stress time. In contrast, the empirical model disregarding BTI recovery (dashed dark red lines) overestimates the frequency shift by a factor of two for both ring oscillators (see Fig. 7). This demonstrates the necessity for an accurate recovery model. Hence, our BTI models accounting for recovery strongly improve the accuracy of circuit aging simulations.

IV. NBTI Variability and Ring-Oscillator Aging

Our defect-sampling model allows to calculate the full distribution function [18] of the NBTI-induced ring oscillator frequency decrease, beyond the mean decrease calculated in the previous section. For simplicity, we focus on the NOR ring oscillator, and we neglect the small HCI contribution, parasitics and additional load gates in the circuit.

NBTI variability results from fluctuations in the density of NBTI-relevant defects as well as in the defect properties. We calculate the NBTI variability in a Monte Carlo (MC) simulation with Poisson distributed defect numbers and exponentially distributed step heights [29–31]. Each NOR gate in the oscillator comprises two pFETs, one of them (M16) is exposed to constant stress $V_{\mathrm{gs}} = V_{\mathrm{dd}}$ and the other one (M17) to the oscillating pattern of Fig. 6. Figure 8 (left) shows the ΔV_{th} distribution after different oscillator operation times in the range of 10s to 10^5s (left to right). Employing 10^5 MC samples resolves the ΔV_{th} distributions up to 4 standard deviations away from the mean, and ΔV_{th} turns out to be normally distributed in that range. A spice-level simulation provides the delay of a single NOR gate as a function of M16 and M17 V_{th} shifts (second plot in Fig. 8). From that information, the distribution of the period T of the 17 stages ring oscillator is calculated, for operation times 10s to 10^5s (third plot). The inset shows that the relative shift of T is essentially normally distributed in a wide range. Whereas the mean shift μ of T increases with operation time, the broadening σ of the distribution levels off (right plot).

V. Conclusions

We compared compact and TCAD models for NBTI including recovery. Even though the models have a simple parametrization from constant-stress MSM experiments, they correctly predict the analog-stress experimental results for single FETs and for entire circuits. From our analysis, we estimate that the DS model error for non-negligible degradation is below 5%. The compact model complexity is linear in the number of pFETs and in the number of single-FET stress-period time samples. However, in contrast to the TCAD

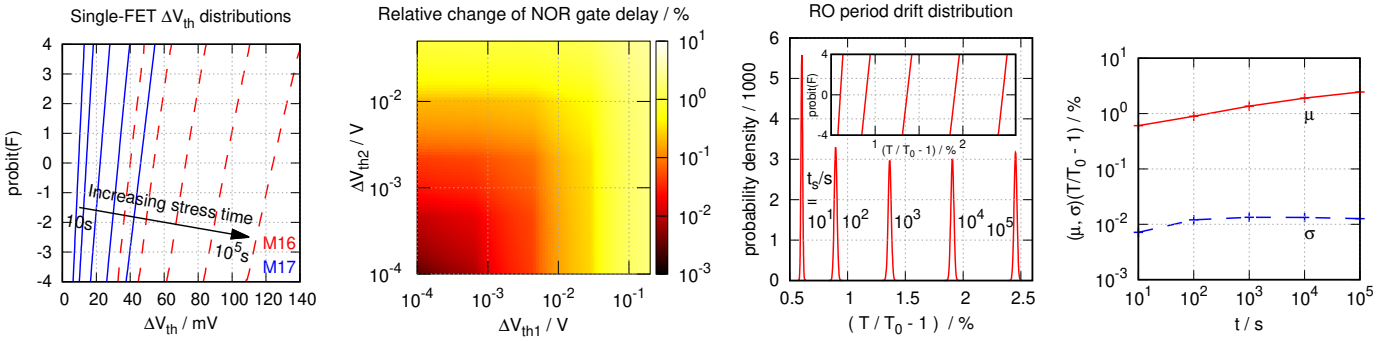

Fig. 8: Simulation of NBTI variability for the NOR ring oscillator at 170°C and 2.4V, using the DS model: NBTI variability leads to a *distribution* of threshold voltage shifts for the two pFETs M16 and M17 within each NOR gate, depending on operation time 10^1, 10^2, 10^3, 10^4, 10^5s (from left to right in the leftmost plot). The V_{th} shifts cause an increase in the delay of each single NOR gate (second plot). This results in a distribution of the ring oscillator period T depending on operation time (third plot), which is well approximated by a normal distribution (inset plot). As calculated before, the distribution's mean μ shifts to longer periods with increasing stress time, whereas its root mean square deviation σ levels off at large stress time (rightmost plot). While the broadening of the ΔV_{th} distributions seems to be unbounded (left plot), the spread of the period durations T is bounded from above (right plot).

reference, the compact model complexity is independent of the stress time such that lifetime studies (several years of stress time) can be simulated as fast and accurately as short-time stress. The NBTI simulation runs equally fast as nominal Spice simulations and applies also to large analog circuits: the presently simulated circuits consist of $\sim$ 300 pFETs in the ring oscillator, additional load gates and frequency dividers. The simulation with a model disregarding NBTI recovery overestimates the oscillator frequency reduction by a factor of two and emphasizes the significance of the presented compact models. Our future work on Spice-level NBTI models includes accounting for the metastable defect states [2, 32, 33] as well as for the NBTI V_{ds} dependence.

Acknowledgments

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References

[1] V. Huard, M. Denais, and C. Parthasarathy, "NBTI degradation: From physical mechanisms to modelling," *Microel. Rel.*, vol. 46, no. 1, pp. 1–23, 2006, 10.1016/j.microrel.2005.02.001.

[2] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microel. Rel.*, vol. 52, no. 1, pp. 39–70, 2012, 10.1016/j.microrel.2011.09.002.

[3] J. H. Stathis, S. Mahapatra, and T. Grasser, "Controversial issues in negative bias temperature instability," *Microel. Rel.*, vol. 81, pp. 244 – 251, 2018, 10.1016/j.microrel.2017.12.035.

[4] JEDEC, "JEP122G: Failure Mechanisms and Models for Semiconductor devices," 2010.

[5] M. M. Kuo, K. Seki, P. M. Lee, J. Y. Choi, P. K. Ko, and C. Hu, "Simulation of MOSFET lifetime under AC hot-electron stress," *Trans. El. Dev.*, vol. 35, no. 7, pp. 1004–1011, 1988, 10.1109/16.3358.

[6] A. J. Scholten, D. Stephens, G. D. J. Smit, G. T. Sasse, and J. Bisschop, "The Relation Between Degradation Under DC and RF Stress Conditions," *Trans. El. Dev.*, vol. 58, no. 8, pp. 2721–2728, 2011, 10.1109/TED.2011.2153854.

[7] A. Kerber, S. Krishnan, and E. Cartier, "Voltage Ramp Stress for Bias Temperature Instability Testing of Metal-Gate/High-k Stacks," *El. Dev. Let.*, vol. 30, no. 12, pp. 1347–1349, 2009, 10.1109/LED.2009.2032790.

[8] T. Grasser, P. J. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, and B. Kaczer, "Analytic modeling of the bias temperature instability using capture/emission time maps," in *Proc. IEDM*, 2011, p. 27.4.1, 10.1109/IEDM.2011.6131624.

[9] G. Wirth, R. da Silva, and B. Kaczer, "Statistical Model for MOSFET Bias Temperature Instability Component Due to Charge Trapping," *Trans. El. Dev.*, vol. 58, no. 8, p. 2743, 2011, 10.1109/TED.2011.2157828.

[10] G. Wirth, J. Franco, and B. Kaczer, "A unified model for AC bias temperature instability," in *Proc. IIRW*, 2013, pp. 84–87, 10.1109/IIRW.2013.6804164.

[11] X. Chen, Y. Wang, Y. Cao, and H. Yang, "Statistical analysis of random telegraph noise in digital circuits," in *Proc. ASP-DAC*, 2014, pp. 161–166, 10.1109/ASPDAC.2014.6742883.

[12] H. Reisinger, T. Grasser, K. Ermisch, H. Nielen, W. Gustin, and C. Schlünder, "Understanding and modeling AC BTI," in *Proc. IRPS*, 2011, p. 6A.1.1, 10.1109/IRPS.2011.5784542.

[13] K. Giering, A. Lange, B. Kaczer, and R. Jancke, "BTI variability of SRAM cells under periodically changing stress profiles," in *Proc. IIRW*, 2016, pp. 1–5, 10.1109/IIRW.2016.7904888.

[14] K.-U. Giering, C. Sohrmann, G. Rzepa, L. Heiß, G. Rott, H. Reisinger, W. Gustin, T. Grasser, and R. Jancke, "NBTI modeling in analog circuits and its application to long-term aging simulations," in *Proc. IIRW*, 2014, pp. 29–34, 10.1109/IIRW.2014.7049501.

[15] F. Alagi, M. Rossetti, R. Stella, and E. Viganò, "A reversible first-order dispersive model of parametric instability," *Microel. Rel.*, vol. 54, no. 3, pp. 561–569, 2014, 10.1016/j.microrel.2013.10.020.

[16] F. Alagi, M. Rossetti, R. Stella, E. Vigano, and P. Raynaud, "Compact model for parametric instability under arbitrary stress waveform," in *Proc. ESSDERC*, 2014, pp. 270–273, 10.1109/ESSDERC.2014.6948812.

[17] K. Puschkarsky, H. Reisinger, C. Schlünder, W. Gustin, and T. Grasser, "Voltage dependent activation energy maps for analytic lifetime modeling of NBTI without time extrapolation," in *Trans. El. Dev.*, 2018, pp. 4764–4771, 10.1109/TED.2018.2870170.

[18] K.-U. Giering, G. Rott, G. Rzepa, H. Reisinger, A. Puppala, T. Reich, W. Gustin, T. Grasser, and R. Jancke, "Analog-circuit NBTI degradation and time-dependent NBTI variability: An efficient physics-based compact model," in *Proc. IRPS*, 2016, 10.1109/IRPS.2016.7574540.

[19] K. Puschkarsky, H. Reisinger, C. Schlünder, G. Rott, W. Gustin, and T. Grasser, "An efficient analog compact NBTI model for stress and recovery based on activation energy maps," to be published.

[20] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI degradation and recovery behavior based on ultra fast VT-measurements," in *Proc. IRPS*, 2006, pp. 448–453, 10.1109/RELPHY.2006.251260.

[21] T. Binder, K. Dragosits, T. Grasser, R. Klima, M. Knaipp, H. Kosina, R. Mlekus, V. Palankovski, M. Rottinger, G. Schrom, S. Selberherr, and M. Stockinger, *MINIMOS-NT User's Guide*, Institut für Mikroelektronik, TU Wien, 1998.

[22] See www.globaltcad.com.

[23] B. Kaczer, T. Grasser, P. Roussel, J. Martin-Martinez, R. O'Connor, B. O'Sullivan, and G. Groeseneken, "Ubiquitous Relaxation in BTI Stressing – New Evaluation and Insights," in *Proc. IRPS*, 2008, pp. 20–27, 10.1109/RELPHY.2008.4558858.

[24] G. Rzepa, J. Franco, B. O'Sullivan, A. Subirats, M. Simicic, G. Hellings, P. Weckx, M. Jech, T. Knobloch, M. Waltl, P. Roussel, D. Linten, B. Kaczer, and T. Grasser, "Comphy — A Compact-Physics Framework for Unified Modeling of BTI," *Microel. Rel.*, vol. 85, pp. 49–65, 2018, 10.1016/j.microrel.2018.04.002.

[25] W. Goes, Y. Wimmer, A. El-Sayed, G. Rzepa, M. Jech, A. Shluger, and T. Grasser, "Identification of Oxide Defects in Semiconductor Devices: A Systematic Approach Linking DFT to Rate Equations and Experimental Evidence," *Microel. Rel.*, 2018, 10.1016/j.microrel.2017.12.021.

[26] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *El. Dev. Let.*, vol. 4, no. 4, pp. 111–113, 1983, 10.1109/EDL.1983.25667.

[27] G. A. Rott, H. Nielen, H. Reisinger, W. Gustin, S. Tyaginov, and T. Grasser, "Drift compensating effect during hot-carrier degradation of 130nm technology dual gate oxide P-channel transistors," in *Proc. IRPS*, 2013, pp. 73–77, 10.1109/IIRW.2013.6804162.

[28] B. Ullmann, M. Jech, K. Puschkarsky, G. A. Rott, M. Waltl, Y. Illarionov, H. Reisinger, and T. Grasser, "Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on MOSFET Characteristics–Part I: Experimental," *Trans. El. Dev.*, pp. 1–9, 2018, 10.1109/TED.2018.2873419.

[29] B. Kaczer, T. Grasser, P. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, "Origin of NBTI variability in deeply scaled pFETs," in *Proc. IRPS*, 2010, pp. 26–32, 10.1109/IRPS.2010.5488856.

[30] B. Kaczer, P. Roussel, T. Grasser, and G. Groeseneken, "Statistics of multiple trapped charges in the gate oxide of deeply scaled mosfet devices – application to nbti," *El. Dev. Let.*, vol. 31, no. 5, pp. 411–413, 2010, 10.1109/LED.2010.2044014.

[31] D. Angot, V. Huard, L. Rahhal, A. Cros, X. Federspiel, A. Bajolet, Y. Carminati, M. Saliva, E. Pion, F. Cacho, and A. Bravaix, "BTI variability fundamental understandings and impact on digital logic by the use of extensive dataset," in *Proc. IEDM*, 2013, pp. 15.4.1–15.4.4, 10.1109/IEDM.2013.6724636.

[32] L. Heiß, A. Lachmann, R. Schwab, G. Panagopoulos, P. Baumgartner, M. Y. Virupakshappaa, and D. Schmitt-Landsiedel, "New methodology for on-chip RF reliability assessment," in *Proc. IRPS*, 2016, pp. 4C–5–1–4C–5–7, 10.1109/IRPS.2016.7574541.

[33] X. Yu, R. Cheng, W. Liu, Y. Qu, J. Han, B. Chen, J. Lu, and Y. Zhao, "A Fast V_{th} Measurement (FVM) Technique for NBTI Behavior Characterization," *El. Dev. Lett.*, vol. 39, no. 2, pp. 172–175, 2018, 10.1109/LED.2017.2781243.