HIGH CAPACITY INLINE ANNEALING FOR HIGH EFFICIENCY SILICON SOLAR CELLS

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ABSTRACT: Most high-efficiency concepts for silicon solar cells utilise passivated surfaces and/or novel metallisation approaches. For these devices an anneal step, preferential in forming gas ambient, is beneficial or even crucial. Annealing is known to activate or improve surface passivation, facilitate metal-silicide formation, improve adhesion of metal contacts and cure potential crystal damage. Challenges for industrial solutions of anneal processes are a precise control of the process atmosphere and temperature, as well as a high throughput and easy integration into production lines. We present a high capacity inline annealing system that addresses these tasks with a throughput of over 1000 wafers per hour. The gas locks, located at the entrance and exit of the furnace, allow for an effective separation of laboratory and forming gas process ambient, which results in a residual oxygen concentration of a few ppm. Inline annealed silicon solar cells with a thermal oxide passivated rear surface show the same conversion efficiency as reference cells, which are annealed in a single wafer reactor. The specific cost of inline annealing in forming gas is calculated to be below 1.1 €ct/W_p.

Keywords: Annealing, Passivation, Contact, Silicon Solar Cell

1 INTRODUCTION

Anneal steps are vital for device performance in a wide variety of applications, e.g. metallisation or surface passivation. Hoex *et al.* used annealing in nitrogen to fully activate the passivation of plasma-assisted atomic layer deposited Al_2O_3 layers [1]. A forming gas anneal (FGA) or post-metallization anneal is also beneficial or even mandatory for thermal oxide or other passivation layers covered by an aluminium layer [2-5]. Moreover, Alemán *et al.* used a FGA to form metal silicides from wet-chemically deposited Ni seed layers [6]. Reinwand *et al.* showed the positive influence of a FGA on sputtered metal seed layers [7]. Schubert *et al.* and Kontermann *et al.* were able to reduce the contact resistance of screen-printed Ag fingers by a FGA [8, 9]. For laser fired contacts (LFC), annealing cures laser-induced crystal damage [4].

Compared to batch processing, inline annealing has the advantage of skipping the loading and unloading of a carrier and purging of the tube, which consumes a considerable amount of time, especially for short process times of a few minutes. Inline anneal steps therefore enable a high throughput and a high system utilisation ratio. To our knowledge, inline anneal steps are not used in silicon PV manufacturing yet, but might become important for future high-efficiency silicon solar cells.

2 FURNACE LAYOUT AND THROUGHPUT

We use a prototype high capacity inline annealing system built by centrotherm photovoltaics AG. Figure 1 shows a photograph of the furnace. The two track system has a small footprint (7500 mm x 1550 mm), the temperature plateau zone is around 2 m long. The chamber itself is made from stainless steel and heated by a surrounding resistance heating; process temperatures of up to 550 °C are reached. The system features the possibility of performing the anneal step in different atmospheres, N_2, cleaned dry air (CDA) or forming gas (FG). An in-situ temperature measurement and detection of oxygen partial pressure in the furnace chamber during operation allow for a precise process control. Gas locks effectively separate the process atmosphere from the ambient. The inline annealing furnace uses the walking string principle for wafer transport [10]. The prototype system features two tracks; however, it can be easily scaled up to larger systems with more tracks.

Apart from the need for tight temperature and atmosphere control, easy implementation into production lines and high throughput are important for industrial manufacturing. Figure 2 shows the temperature profile of a 2 min anneal process at 350 °C measured with a thermocouple attached to a wafer sample. Depending on temperature and string speed, the heating rate is in the order of several hundred K/min, before the wafer enters the plateau zone. We define the anneal time as the time during which the actual wafer temperature is within 5 K of the set plateau temperature. The anneal time also defines a plateau zone for the process. Before unloading, the samples are cooled in a controlled ambient.

Figure 1: Inline annealing furnace located at Fraunhofer ISE. The system was built by centrotherm photovoltaics AG.

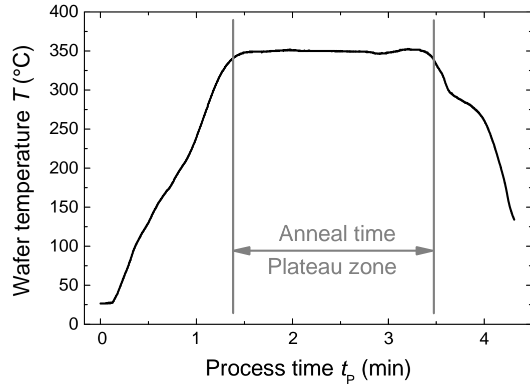

Figure 2: Exemplary temperature profile for a 2 minute anneal process, measured with a thermocouple attached to a wafer. Additional process duration arises from gas locks and controlled cooling. Anneal time is defined as the time during which the actual wafer temperature is within 5 K of the set plateau temperature.

Figure 3 shows the calculated throughput versus the process time for an industrial realisation of the anneal process using the existing two track or a predicted larger five track furnace. With such a system, throughput is expected to exceed 1000 wafers/hour for anneal plateau times of 3 min or less. Kontermann *et al.* showed that an optimum post-metallisation anneal for thermal oxide rear surface passivated solar cells with laser-fired contacts can be as short as one to two minutes [9], which would increase throughput of a five track system to over 2000 wafers/hour. Throughput is increased further by elongating the plateau zone from currently ~2 m to 4 m. When keeping the anneal time constant, throughput directly depends on string velocity and thus the length of the plateau zone. For such a system and assuming an anneal plateau time of 2 min, throughput would exceed 3000 wafers/hour.

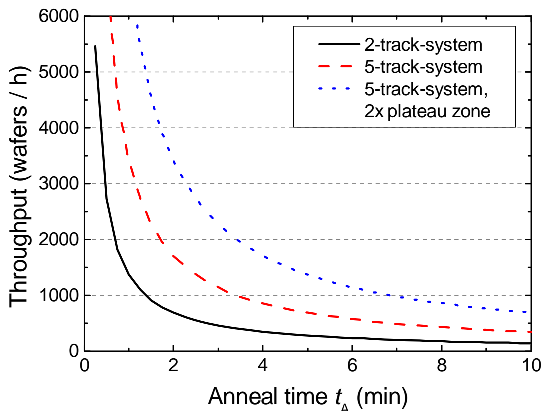

Figure 3: Calculated throughput in wafers per hour versus anneal plateau time. The calculation is based on a plateau zone length of 2 m, wafers of 156 mm dimension with 20 mm spacing and a furnace with 2 (realized) or 5 tracks (predicted), respectively. Throughput is increased further by elongating the plateau zone from currently 2 m to 4 m (prediction). Anneal plateau time as defined in Fig. 2.

3 EXPERIMENTAL AND RESULTS

3.1 Annealing of Ni seed layers

Ni seed layers in combination with Ag light induced plating form a promising alternative to established screen-printing technology for the contact formation to phosphorous diffused emitters, due to the improved aspect ratio and the possibility to contact emitters with a reduced phosphorous surface concentration [11, 12]. Several authors report the necessity to perform a sintering step after plating to form a Ni silicide layer and improve contact adhesion and contact resistivity [11-14]. A high oxygen concentration during sintering might lead to oxidation of Ni at the surface, which increases the contact resistance. Therefore, annealing of Ni contacts can be used to detect residual oxygen in the process ambient. In case of an inline system, it further allows testing the effectiveness of the gas locks, which are located at the furnace entrance and exit and allow for very low oxygen concentration in the process chamber during processing.

We investigate the influence of different anneal ambients (FG, N_2, and CDA) during sintering at 300 °C for ten minutes on the formation of Ni oxide layers on Ni contacts and analyse the ratio of the atomic concentration [O] / [Ni] by energy dispersive X-ray spectroscopy (EDX) at a scanning electron microscope (SEM) operated at an acceleration voltage of 5 kV.

Table 1 lists the results of EDX spectroscopy measurements, performed after annealing of samples in different atmospheres at 300 °C using the presented inline system and a small-scale quartz tube furnace as a reference process.

Before annealing, a [O] / [Ni] ratio of 0.07 is extracted. Apparently the use of a batch anneal process in forming gas leads to a increase in the [O] / [Ni] ratio, indicating oxide formation on the Ni surface, whereas an inline annealed sample exhibits a factor of ~ 2 lower ratio. For the batch process, the samples are removed from the furnace without prior cooling, which promotes nickel oxide formation. Samples annealed in the inline furnace are cooled in controlled atmosphere before unloading, as apparent from Figure 2, which does not lead to a increased [O] / [Ni] ratio. Therefore, for annealing of Ni contacts, inline processes are as qualified as established batch processes in quartz tube furnaces, or even superior, to prevent an oxidation of the contacts.

As expected, samples annealed in CDA applying the inline furnace show a increased [O] / [Ni] ratio compared to the sample annealed in N_2 or FG, again indicating Ni oxide formation. As for the use of N_2 or FG a similar

Table 1 Surface concentration ratio [O] / [Ni] for Ni contacts measured before and after annealing in different furnaces and ambients extracted from EDX measurements using an acceleration voltage of 5 kV.

	furnace	ambient	$[O_2]$	[O] / [Ni] ratio
before annealing	-	-	-	0.07
annealed	batch	FG	?	0.13
annealed	inline	FG	< 10	0.07
annealed	inline	N_2	< 100	0.07
annealed	inline	CDA	210000	0.11

[O] / [Ni] ratio is extracted as before annealing, the gas locks effectively shield the process ambient from the laboratory atmosphere, which enables the use of forming gas also for inline systems.
Measurements of residual oxygen $[O_2]$ during annealing yield concentrations of a few ppm for use of FG, and slightly higher values for N_2. In contrast, for the use of CDA, $[O_2]$ is 210000 ppm.

3.2 Annealing of symmetric lifetime samples

Forming gas anneal steps are known to strongly decrease the surface recombination velocity at thermal oxide layer passivated silicon surfaces, especially if the thermal oxide layer is covered by an Al layer. This aluminium post-metallization anneal (PMA) liberates hydrogen by the chemical reaction of aluminium with trace amounts of water at the SiO_2/Al interface to AlO_x [15, 16] that passivates dangling bonds at the Si/SiO_2 interface.

For this experiment we use 125*125 mm² (pseudo-square) large boron doped floatzone (FZ) as-cut wafers with a resistivity $\rho_{bulk} = 1$ Ωcm and a thickness $W = 200$ µm. After removing the saw-damage in KOH solution, the samples are subject to a RCA wet chemical cleaning sequence. We then grow a 100 nm thick thermal oxide layer in pyrolytic steam at 950 °C and deposit a 2 µm thick Al layer by means of electron beam evaporation onto both sides, before the samples are subject to an anneal variation. To allow for an effective carrier lifetime measurement, the Al layers are wet chemically removed.

For all symmetric samples we measure the effective minority carrier lifetime τ_{eff} applying the QSSPC method at an injection density of $\Delta n = 5*10^{14}$cm^{-3}. From τ_{eff} we calculate the surface recombination velocity [17]

$$S = \frac{W}{2}\left[\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)^{-1} - \frac{1}{D}\left(\frac{W}{\pi}\right)^{2}\right]^{-1} \qquad (1)$$

using an intrinsic recombination-limited bulk lifetime $\tau_{bulk} = 2.14$ ms at $\Delta n = 5*10^{14}$ cm^{-3} [18] and a diffusion coefficient $D = 27.0$ cm^{2}s^{-1} [19] for the 1 Ωcm p-type material used.

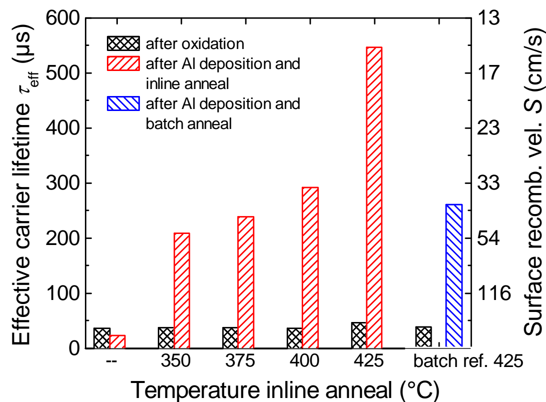

Figure 4: Effective carrier lifetime τ_{eff} and surface recombination velocity S for thermal oxide passivated 1 Ωcm FZ wafers measured after an inline anneal step for 3 min 40 s (plateau time) at different temperatures in forming gas. A batch annealed sample (425°C, 5 min) acts as reference. Each bar represents one sample.

Figure 4 shows τ_{eff} and S measured on symmetric samples, before and after the anneal step, and plotted versus the inline anneal temperature. Also shown are a sample without anneal and a reference annealed in a batch furnace.

For the sample without anneal step, aluminium deposition and subsequent etching of the layers marginally reduces τ_{eff} and therefore can not be accounted for the strong increase in τ_{eff} observed after inline annealing. For all samples subject to inline annealing, an anneal time of 3 min 40 s is chosen. Increasing anneal temperatures lead to a pronounced increase in τ_{eff} and thus a lower S down to 15 cm/s for an anneal temperature of 425 °C. The high surface passivation quality after inline annealing also becomes visible in comparison to the batch reference, which is annealed in a small scale quartz tube furnace at 425 °C for a total process time of 5 min. The lack of a precise wafer temperature measurement during batch annealing however impedes the specification of a plateau time for this process.

Anneal temperatures above 425 °C were not tested, however might lead to higher interface trap densities at the Si/SiO_2 interface [22].

3.3 Annealing of solar cells

Figure 5 shows a schematic sketch of the cross-section of a thermal oxide rear surface passivated solar cell with local contacts. The solar cells are produced from 156 mm large boron-doped Czochralski (Cz) grown wafers using the Silicon Nitride Thermal Oxidation (SiNTO) approach [20, 21]. Front end processes until SiN_x deposition are performed in an industrial production line at SolarWorld facilities, whereas back end processing including thermal oxidation is performed at Fraunhofer ISE’s pilot line PV-TEC. The process sequence is described in detail in Ref. [21]. A final anneal step in forming gas ambient is required to activate the surface passivation and cure damage induced by laser-fired contact formation (LFC) [23]. Two groups of samples are processed identically except for the final anneal step, which is performed either in a laboratory-type single wafer reactor with pyrometric temperature control or the previously described inline annealing furnace.

Table 2 depicts the cell parameters extracted from IV curves measured with an industrial cell tester after the fabrication process. Before annealing, cell efficiency is

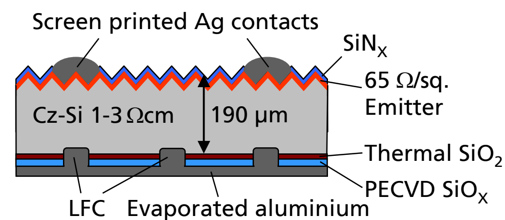

Figure 5: Schematic sketch of the cross-section of the SiNTO device [20, 21]. The rear surface is passivated by a thin thermal oxide layer. A laser forms the local rear contacts (LFC). A final anneal step in forming gas ambient is required to activate surface passivation and cure damage induced by laser-fired contact formation.

Table 2 Values for the best cell and mean values of solar cell parameters extracted from IV measurements in an industrial cell tester, before and after annealing of SiNTO solar cells. Either the inline annealing furnace or a single wafer reactor is used for the final forming gas anneal. Apart from annealing, all cells are processed identically. The cell area is 238.7 cm^2, the devices are not stabilised before the measurement. *: measured under constant light

Annealing furnace	V_{oc} (mV)	J_{sc} (mA / cm²)	FF (%)	η (%)	pFF (%)
Before annealing *					
Mean of 4 cells	587±0	32.8±0.1	74.7±0.3	14.4±0.5	-
Inline furnace					
Best cell	636	37.3	77.9	18.5	82.9
Mean of 41 cells	635±2	36.9±0.3	77.4±1.1	18.1±0.3	82.2±1.3
Single wafer reactor					
Best cell	637	37.5	77.4.	18.5	82.4
Mean of 34 cells	635±3	36.8±0.2	77.6±0.3	18.1±0.2	82.4±0.4

around 14.5 %. Annealing in FG using either inline furnace or single wafer reactor leads to a strong increase in V_{oc} of ~ 50 mV and J_{sc} of ~ 4 mA/cm^2 due to the hydrogen release during this step (see Figure 4 [15, 16]). Both systems allow for a conversion efficiency of up to 18.5 % (as processed) confirming the high performance of the inline anneal process. Also a comparison of the arithmetic mean of up to 40 samples for the two anneal processes shows no significant difference in all cell parameters. Thus using inline instead of single wafer annealing allows for a strongly increased throughput, while showing the same cell results as laboratory type single wafer equipment. Inline annealing was also applied for the fabrication of large-area p-type silicon metal wrap through solar cells (149 cm^2, total area) featuring conversion efficiencies exceeding 20% [5, 24].

4 COST CALCULATION

For industrial manufacturing, cost-effectiveness must be assured. We evaluate the economic feasibility of inline annealing by calculating the specific process cost (cost of equipment ownership) [25] for 156 mm large boron-doped Cz wafers. For annealing, we assume an automated industrial two or five track furnace with a plateau length of 2 or 4 m and a spacing of 20 mm between each wafer. Annealing takes place in forming gas. For the calculation, we assume a solar cell conversion efficiency of 19.5% as reported by several authors [5, 26-29], which is a high value for current large-area high-efficiency p-type silicon solar cells. The calculations include a depreciation of seven years and take into account the cost for machine, automation, imputed interest, floor cost, material, energy, labour, maintenance and machine downtime.

Table 3 Calculated cost of equipment ownership for inline annealed wafers assuming an inline furnace with two or five tracks, a plateau length of 2 or 4 m and for anneal times of 1 min or 2 min in forming gas.

Tracks	Cost of equipment ownership (€ct / W_p)			
	2 m plateau zone		4 m plateau zone	
	1 min anneal	2 min anneal	1 min anneal	2 min anneal
2	0.6	1.1	0.4	0.8
5	0.6	1.1	0.3	0.7

The results, listed in Table 3, indicate that inline annealing is a cost-competitive process with specific costs in the range of 0.3 to 1.1 €ct / W_p, depending on furnace layout. A reduction of the anneal time of 2 min to 1 min has a stronger impact on the specific process cost than up scaling of the machine to 5 tracks due to increased invest for the latter. It has to be remarked that the specific process cost in a production line depends on a large number of factors. The exact values of Table 3 therefore rank as an estimate.

5 SUMMARY

We successfully introduce high capacity anneal processes using an inline furnace to silicon solar cell fabrication. Inline anneal processes are applicable for improving dielectric surface passivation and contact resistance reduction, as well as for the formation of metal-silicides. The existing two track system already allows for a throughput of 1000 wafers/h at an anneal plateau time of 1 min and 20 s. An even higher throughput is expected by enlarging the system to five tracks and/or increasing the plateau zone length from currently 2 m to higher values. Thermocouple measurements reveal wafer heating and cooling rates in the range of several hundred K/min. EDX measurements performed on Ni contacts do not reveal an increase in the [O] / [Ni] ratio due to inline annealing in forming gas ambient, which shows the effectiveness of the gas locks located at the entrance and exit of the system. For the use of a forming gas ambient, a residual oxygen concentration of a few ppm is measured.

Samples passivated by a thick thermal oxide layer yield surface recombination velocities down to 15 cm/s after Al deposition and inline annealing. A comparison of anneal steps using either the inline furnace or a single wafer reactor with pyrometric temperature control shows no difference in cell parameters for large area thermal oxide rear surface passivated solar cells with local laser-fired rear contacts and screen-printed front contacts. Both systems yield cell efficiencies of up to 18.5 %

confirming the high quality of the new inline anneal process. In our cost calculation we show the cost-effectiveness of inline anneal processes. The specific cost of an inline anneal process in forming gas is calculated to lie between 0.3 and 1.1 €ct / W_p.

6 ACKNOWLEDGMENTS

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