UV nanoimprint lithography process optimization for electron device manufacturing on nanosized scale

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Abstract

Imprint specific process parameters like the residual layer thickness and the etch resistance of the UV polymers for the substrate etch process have to be optimized to introduce UV nanoimprint lithography (UV NIL) as a high-resolution, low-cost patterning technique for research and industry into electron device manufacturing. Additionally, UV NIL processes have to be compatible with conventional silicon (Si) semiconductor processing. Within this work, the minimization of the residual layer thickness by using a multi drop ink-jet system, which was integrated into the imprint stepper NPS300 from S.E.T. (formerly SUSS MicroTec), in combination with a low viscous UV polymer from Asahi Glass Company is shown. The etch resistance of different UV polymers against the poly-Si etch process was increased by 50% with an appropriate post exposure bake. A poly-Si dry etch process was used to pattern the gates of short channel MOSFETs. After optimizing the poly-Si etch, properly working short channel MOSFETs with a minimum gate length of about 90 nm were fabricated demonstrating successfully the compatibility of UV NIL with conventional Si semiconductor processing on nanosized scale.

Keywords: UV nanoimprint lithography, residual layer thickness, UV polymers, etch resistance, electron devices, MOSFET

1. Introduction

UV nanoimprint lithography (UV NIL) is an attractive technique to transfer nanosized patterns without using expensive optical exposure tools [1] for applications in different fields like photonics, biotechnology, organic electronics, high-density data storage, and electron devices. The success of this technique depends on the availability of appropriate templates [2-4], on the imprint specific process parameters like antisticking of the UV polymer to the template or adhesion of the UV polymer to the substrate [5], and on the life time of the antisticking layer [6]. It is also mandatory that the imprint process parameters such as residual layer thickness (RLT) and etch resistance of the UV polymers for the substrate etch process are optimized to further assure a transfer of the imprinted patterns into a substrate with a high dimensional accuracy. Finally, the UV NIL processes have to be compatible with conventional Si semiconductor processing for its adoption into the manufacturing of electron devices like short channel MOSFETs.

Within this work, results are presented to decrease the RLT using an ink-jet system in combination with a low viscous UV polymer. The etch resistance of different UV polymers was optimized by a post exposure bake to achieve a transfer of the imprinted patterns into the substrate with a high dimensional accuracy. To finally fabricate short channel n-MOSFETs, reactive ion etching (RIE) and further Si semiconductor processes were optimized. In the end, MOSFETs with a minimum gate length of 90 nm were fabricated. The MOSFETs were subsequently characterized optically by scanning electron microscopy (SEM) and electrically by measuring the transfer and output characteristic.

2. Residual layer thickness

In earlier investigations, the minimum RLT achieved for the imprint stepper NPS300 was about 400 nm, which was attained by dispensing the medium viscous resist PAK-01 (viscosity: 50 mPa·s) with the integrated single drop dispenser [5]. Such rather high RLT is not sufficient for a feasible pattern transfer of nanosized patterns into the substrate. To minimize the RLT, a multi drop ink-jet system was integrated into the NPS300. This ink-jet system in combination with the low viscous resist NIF-A-5b from Asahi Glass Company (viscosity: 8.5 mPa·s) provides a droplet volume of 60 pl, which means an essential droplet volume reduction by two orders of magnitude compared to the single drop dispenser. Therefore, the amount and the distribution of the initial dispensed UV polymer droplets could be adjusted to the patterns on the template. By optimizing the amount and the distribution of the UV polymer, the RLT could be decreased to about 30 nm (see Fig. 1). The UV polymer volume (5.4 nl) corresponding to the RLT of 30 nm was the minimum volume to achieve a closed resist layer. By increasing the volume, also the RLT increases.

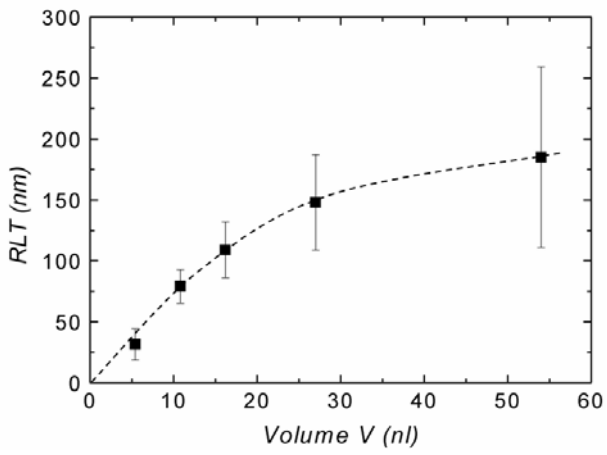

Fig. 1. Residual layer thickness for different amounts of dispensed UV polymer NIF-A-5b.

For a pattern transfer into the substrate with a high dimensional accuracy, the RLT has to be removed by RIE and, therefore, the residual layer has to be thin and uniform for all imprints. In Fig. 2, the RLT for 25 imprints on a poly-Si layer, deposited on an oxidized 150 mm double side polished Si substrate is shown. The mean value of the RLT for all imprints was about 50 nm with a standard deviation of about 12 nm. The higher value for the RLT of 50 nm (compared to 30 nm from Fig. 1) was caused by a slightly higher dispensed volume in order to level substrate waviness. The thickness and the homogeneity of the residual layer were sufficient to achieve an uniform transfer of the imprinted patterns into the substrate by RIE, which will be discussed in chapter 3.

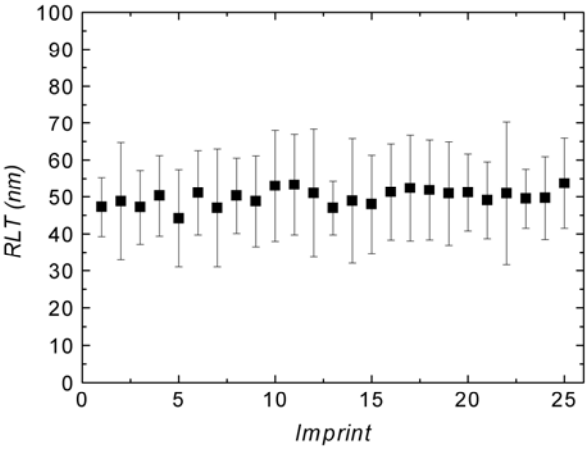

Fig. 2. Residual layer thickness for 25 imprints on a Si substrate. The resist used was NIF-A-5b.

3. Substrate patterning

After the minimization of the RLT and the evaluation of its uniformity, a homogeneous removal of the RLT is essential. The RLT was removed by a physical Argon sputtering process. The etching rates of five different UV polymers (suited for different applications) treated with different post exposure baking (PEB) conditions are shown in Fig. 3. The knowledge about the RLT etching rate is important to precisely remove the RLT. The etching rates of the different UV polymers decreased by about 30% with a PEB of 120°C or 160°C for 120 min. The temperature treatment resulted in a densification of the resist which increased the UV polymer etch resistance.

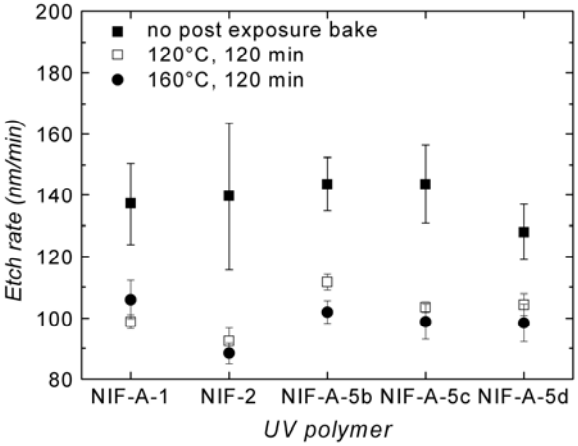

Fig. 3. UV polymer etch rates for different post exposure bake conditions against the RLT etching process.

The RLT etch process is followed by the substrate (poly-Si) etch process. Here, the UV polymers have to exhibit an appropriate etch resistance against the poly-Si RIE process in order to achieve a pattern transfer with a high dimensional accuracy. The poly-Si thickness for obtaining the gates was about 110 nm and the UV polymer thickness (after RLT etch) was about 90 nm. Therefore, the selectivity (poly-Si etch rate divided by UV polymer etch rate) for the poly-Si

RIE process has to be higher than 1.2. In Fig. 4, the selectivities of five different UV polymers treated with different post exposure baking conditions for the poly-Si etch process are shown. For a PEB of 120°C for 120 min, the highest selectivity (at least 1.5) for all UV polymers could be found, which is sufficient for patterning the poly-Si gates.

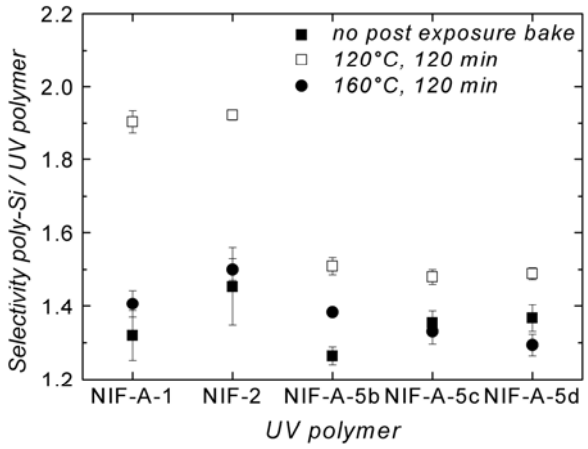

Fig. 4. UV polymer etch resistance for different post exposure bake conditions against the poly-Si etch process.

4. Electron device manufacturing

After the successful patterning of the poly-Si gates by UV NIL and RIE, the fabrication of the short channel n-MOSFETs (see Fig. 5) was continued by conventional processing and lithography using maskaligning technique (mix and match).

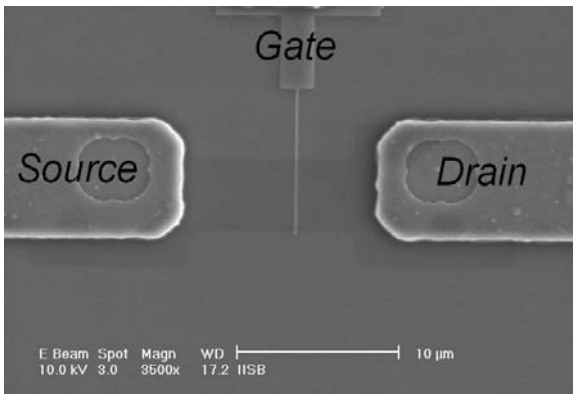

Fig. 5. SEM top view image of the fabricated short channel n-MOSFET.

In Fig. 6, a SEM cross section image of a poly-Si gate with a channel length of about 90 nm is shown. The minimum gate length was limited by the resolution of the electron beam lithography during the template fabrication process.

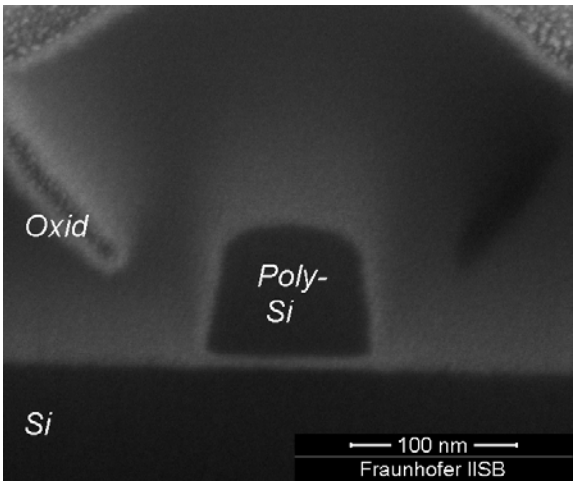

Fig. 6. SEM cross section image of a poly-Si gate, patterned by UV NIL and RIE. The channel length is around 90 nm.

The final transistors were characterized electrically by measuring the transfer characteristics (see Fig. 7). The threshold voltage V_{Th} for the 90 nm MOSFET was 0.14 V, which is in good agreement with simulations that were performed before the MOSFET fabrication.

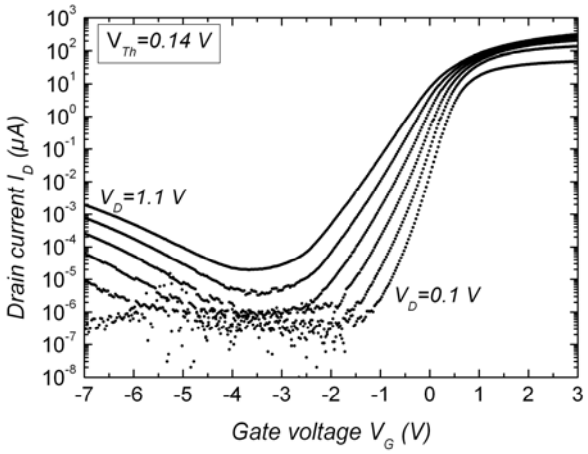

Fig. 7. Transfer characteristic of the short channel n-MOSFET shown in Fig. 6 with a channel length of about 90 nm.

5. Summary

In this work, the optimization of imprint specific process parameters like the minimization of the RLT to 30 nm, the UV polymer etch resistance, and finally the patterning and manufacturing of short channel MOSFETs with a channel length of 90 nm and a V_{Th} of 0.14 V by UV NIL and conventional Si semiconductor processing was successfully demonstrated. The UV NIL patterning approved a very good compatibility to conventional semiconductor processing and is applicable for sub-100 nm electron device manufacturing.

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