Lateral Drift-Field Photodiode for Low-Noise, High-Speed, Large Photoactive-Area CMOS Imaging Applications

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Abstract

In this work a theoretical concept and simulations are presented for a novel *lateral drift-field photodetector* pixel to be fabricated in a 0.35µm CMOS process. The proposed pixel consists of a specially designed *n*-well with a non-uniform lateral doping profile that follows a square-root spatial dependence. "Buried" MOS capacitor-based collection-gate, a transfer-gate, and an *n*-type MOSFET source/drain n^+ floating-diffusion serve to realize a non-destructive readout. The pixel readout is performed using an in-pixel *source-follower* pixel buffer configuration followed by an output amplifier featuring correlated double-sampling. The concentration gradient formed in the *n*-well employs a single extra implantation step in the 0.35µm CMOS process mentioned and requires only a single extra mask. It generates an electrostatic potential gradient, i.e. a lateral drift-field, in the photoactive area of the pixel which enables high charge transfer speed and low image-lag. According to the simulation results presented, charge transfer times of less than 3ns are to be expected.

Keywords: CMOS imaging, lateral drift-field photodetectors (LDP), high-speed imaging, large pixels, low-noise

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1. Introduction

Charge-coupled devices (CCD) have been the dominant technology in the field of solid-state imaging for a couple of decades due to their capability to perform very efficiently and uniformly over large photoactive areas the photon conversion into electrical charge, the charge collection, and the charge transfer into readout electronics at low noise [1]. But today, the maturity of *complementary metal-oxide-semiconductor* (CMOS) technology based photodetectors has been firmly established while offering significant advantages, such as random *x-y* pixel addressing, in-pixel amplification and signal processing, and cointegration of control and interface electronics [2]. Moreover, modern deep sub-micron standard CMOS processes are perfect candidates for implementation of imagers for an increasing number of imaging applications, as they enable cointegration of numerous highly complex circuit functions. Nevertheless, the use of high doping profiles, thin gate-oxides and low power supply voltages necessary in modern sub-micron CMOS technologies affects adversely the performance of many analog circuits and photodetectors and thus inhibits implementation of high-performance imagers.

To alleviate the situation, we use a 0.35µm *n*-well 4 metal layers CMOS process which combines *low-voltage* (LV) and *high-voltage* (HV, up to 80V) MOSFETs and is normally used for automotive applications. It features thin LV and thicker HV gate-oxides, two polysilicon layers with two different work-functions (n^+ or p^+ doped), as well as five different well and substrate concentrations. The process offers the possibility of fabricating at least eight different reverse-biased *p-n* junction-based photodiodes (PD) and also different MOS capacitor based photogates (PG) by combining the different *n*- and *p*- wells, or using the non-doped epitaxial layer, as well as the two polysilicon layers (and their high-resistivity versions).

For high-performance imaging, e.g. for industrial, scientific, and medical applications, often large-area low-noise image sensors are required (hence, low dark currents are required, too). This is still difficult to realize, especially if a high speed should be also provided. Here a typical example is represented by the three dimensional (3-D) *Time-of-Flight* (ToF) range imaging [3] requirements. A 3-D image sensor must exhibit an extremely low noise, a high *signal-to-noise ratio* (SNR)), and very high speed. To achieve these goals, it is normally required that the generated charge carriers in a photodetector are collected away from the silicon surface to avoid the trapping and entrapping effects of the *Shockley-Read-Hall* (SRH) [4] generation/recombination centres located there. Moreover, it is desirable that the collected photocharge should stay under control of electrical fields to avoid any losses due to recombination mechanisms taking place inside the silicon. And in addition, the readout node capacitance should be kept low, as it affects the amount of *noise equivalent charge* (NEC) generated in most active pixel configurations [3]. For near infra-red (NIR) radiation and radiation at longer wavelengths, or for particle detection applications, the electrical field should expand as much as possible throughout the photoactive area substrate, as used in *monolithic active pixel sensors* (MAPS) [5]. More cannot be achieved, as CMOS technology results incompatible with any other approach in which there is a back-contact in the photodetector and the entire silicon bulk (or high-resistivity epitaxial layer) is depleted.

All these requirements mentioned are difficult to meet using a standard CMOS process, even in its enhanced automotive version described above. Thus, special process modifications (additional implantation steps, special masks, etc.) have been lately developed in the mentioned 0.35µm CMOS process for realization of high-performance imagers. Nevertheless, the process still retains its original characteristics as far as standard electronic devices are concerned and thus enables proper design and fabrication of the readout, processing, control, interface, and other circuitry on the same chip.

2. Standard Active Pixel Configurations

The development of photogate (PG) active pixels (Fig. 2(a)) to be fabricated in CMOS technology started in the early 1990's, based on the well known and mature CCD technology. Just as it happened with *p-n* junction-based photodiodes, although they are not

novel inventions, its intended use enabled over the years the appearance of a wide range of different CMOS image sensor configurations [6].

The CMOS technology based PG active pixels [7] offer several advantages in comparison to conventional *p-n* junction photodiode based ones. Their main advantage comes from the improved noise suppression provided by the combination of non-destructive readout in conjunction with the *source-follower* (SF) pixel buffer stage, which also enables the use of *correlated double-sampling* (CDS) readout technique. This approach allows the reduction of the low-frequency correlated noise generated in the pixel.

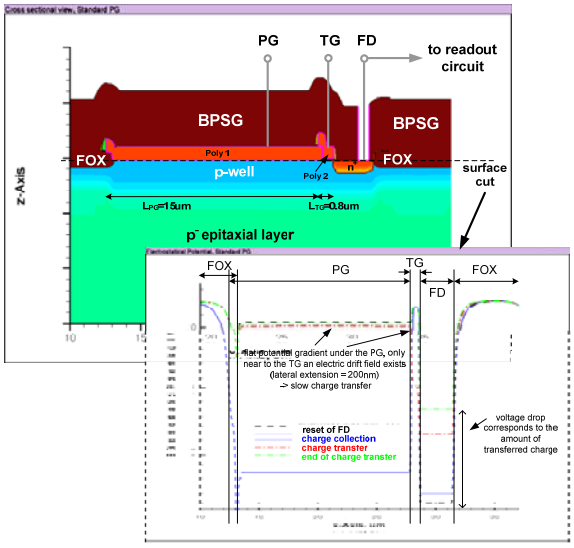

Fig. 1. 2-D simulation (TCAD) results of the standard photogate pixel: electrostatic potential profiles at the wafer surface for reset, charge collection, and charge transfer phases, respectively [8].

Moreover, the *kTC*-noise at the pixel output does not depend here on the capacitance of the photodetector. It is defined by the much smaller capacitance of the readout node, the so called *floating diffusion* (FD), which is charge-coupled to the PG through a MOS capacitor-based *transfer gate* (TG), preferably overlapping it to increase the *charge-transfer efficiency* (CTE), as it can be observed in Fig. 1 [8]. Having separated photoactive and readout node areas enables charge readout from the FD while performing an additional charge-to-voltage conversion and amplification.

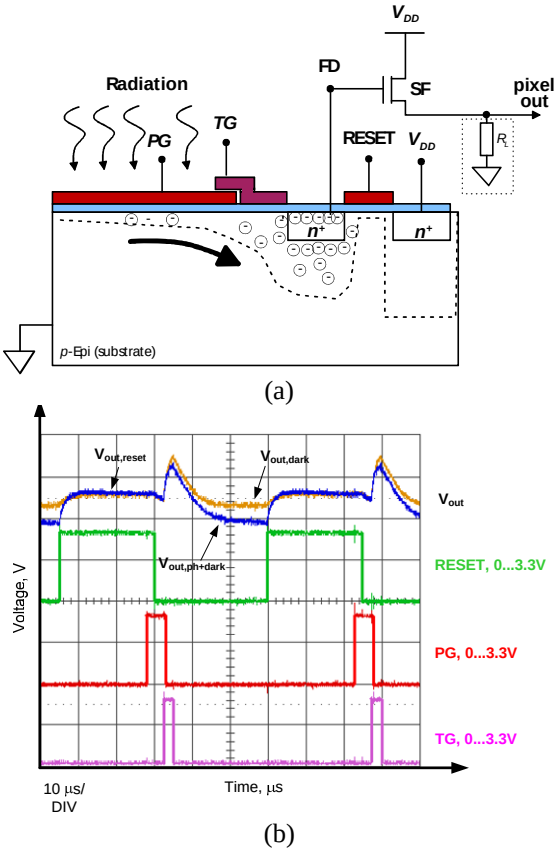

Fig. 2. (a) Schematic representation of a PG active pixel in the charge transfer phase; (b) oscilloscope graph showing the RESET, PG and TG signals and the voltages at the source follower output for an illuminated PG (λ=700nm, E=1.69×10^{-3} W/m²) and under dark conditions, respectively.

Unfortunately, the use of a radiation absorbing polysilicon layer on top of the photoactive area reduces its quantum efficiency of the pixel, specially in the blue and ultraviolet part of the spectra. Also, as the electrostatic potential maximum is located directly on the Si-oxide interface, the dark current surface component and the interface traps degrade the SNR performance of the pixel [4]. This is the reason why “buried” CCD or PG have been developed.

For the analysis of the speed performance of PG-based pixel structures (Fig. 2(a)), two types of currents must be taken into account: the *drift* and the *diffusion* currents induced during charge transfer

from the PG to the FD across the TG. A really fast transfer of collected photogenerated charge carriers can be only implemented if there is a lateral electrostatic potential gradient beneath the PG and the TG which generates a lateral drift field in that area. The presence of the so called “fringe-fields” [1] helps, but their influence reaches only the first 300nm – 400nm of the PG closest to the TG, or the same part of the TG closest to the FD, a feature mainly taken advantage of in modern PG pixels fabricated in deep submicron technologies, with reduced pixel pitches. The latter is true for both, the “surface channel” and the “buried” PGs.

For longer PGs (15µm in Fig. 1), the electrostatic potential beneath the PG remains constant, as it can be observed in the two-dimensional (2-D) electrostatic potential simulation result shown in Fig.1, which means that the minority carriers collected beneath the PG can be moved toward the FD by thermal diffusion only. This makes this transport much slower if compared with the drift transport mechanisms, and increases the probability of image-lag effects drastically for most readout rates. Readout times, closely related to the charge transfer times, of around 20µs or more can result (see Fig. 2(b)) in this kind of photodetectors.

Another analysis of this phenomena was performed for PG active pixels fabricated in the same 0.35µm CMOS process, where a PG based active pixel was illuminated by a 905nm wavelength laser pulsed illumination, for several laser pulse widths (T_{pulse}), while varying the collected photocharge transfer time (T_{TG}) from the PG to the FD via the TG. The measured pixel has a photoactive area of 30x30µm² (i.e. PG area), a 3µm long transfer gate and a 20x1.5µm² FD, with a 12fF capacitance at 3.3V bias.

As expected from the previously explained results (Fig. 2(b)), the transfer times of several nanoseconds are too short to transfer the complete amount of photogenerated charge collected under the PG to the FD due to the absence of strong electrical drift fields, even if an optimized SF stage and sensor output buffer are respectively used, as it is the case here. For T_{TX} of 30ns only around 20% of signal charge reaches the FD. This can be observed in Fig. 3 in terms of the FD output voltage measured after the SF buffering stage in the pixel. If the transfer time is extended to 60ns, the transfer loss is reduced to 50% (Fig. 3).

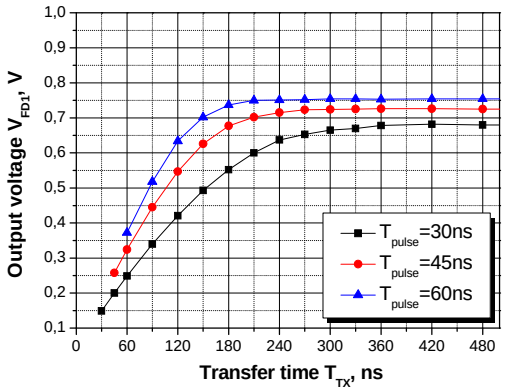

Fig. 3. Output voltage measured at the FD for different transfer times and laser pulse widths (measurement performed with a single laser pulse).

A special type of “buried” photodetectors is used in the well-known *pinned* photodiode (PPD) [7] active pixel configuration. It solves the problem of the fast surface states present in surface channel PG pixels (Fig. 1), as it uses a shallow (≤1µm deep) *n*-well fabricated on the *p*-type epitaxial layer as a *p*-*n* junction based photodetector, sandwiched between this epi-substrate and an additional grounded p^+ implantation on its surface [6]. This can be seen in Fig. 4, where a 2-D TCAD simulation is shown for a PPD structure fabricated in the 0.35µm CMOS process described above. The *n*-well doping profile is optimized in such a way that it generates an electrostatic potential maximum, the so called “pinned” voltage that completely depletes the entire photodiode of majority carriers. The p^+ layer “pushes” the electrostatic potential maximum away from the silicon surface, thus avoiding all the already discussed effects of the surface fast states. It also reduces the recombination rate of the minority carriers at the surface, as they are almost immediately drifted into the electrostatic potential maximum generated below.

The rest of the pixel configuration is identical to the one described for the PG pixel, as far as the TG,

the FD, the SF buffer stage, and the CDS readout are concerned. Both configurations share the image-lag [9] and charge transfer speed problems. On the one side, this is due to the lateral flat potential profile in the photoactive area, where the collected charge is being transferred to the FD only by thermal diffusion (see Fig. 4), on the other side - in the case of PPDs – it is caused by the high resistance of the fully-depleted *n*-region.

The major source of dark current in the PPD pixels is the part below the TG, where the space charge region (SCR) of the *n*-region reaches the silicon surface, as investigated in [10], the same effect which should be avoided, hopefully without losing all the other advantages of this pixel configuration. One additional problem in the PPD pixels, however, is the limited full-well capacity of their *n*-regions.

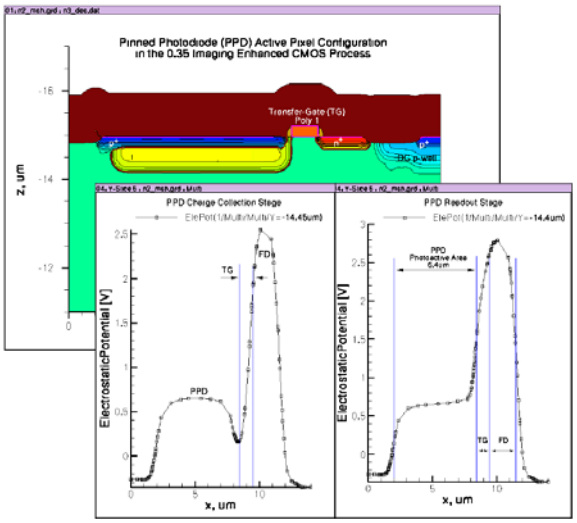

Fig. 4. 2-D simulation (TCAD) result of the standard PPD active pixel configuration fabricated in the 0.35µm CMOS process using an additional "shallow" *n*-well implantation. Below left, electrostatic potential cut made at the electrostatic potential maximum (just below the p^+ layer) during the charge collection phase can be observed. Below right, the charge transfer stage.

In the open literature, several approaches have been reported which pursue the increase of the charge transfer speed in the pixel by introducing a lateral drift-field by various means. As an example, the semiconductor *drift-chamber* [11] and the drift-chamber based JFET and DEPFET photosensors developed during the last 15 years that follow the same approach are used in particle and high-energy radiation detection: they consist of concentrically placed segmented electrode rings biased at a voltage gradient that creates a drift-field across the entire completely depleted wafer. Unfortunately, as it was already explained above, this approach cannot be directly applied in CMOS technology. Nevertheless, a very similar idea was very successfully developed in [12], where a pixel based on static drift fields was successfully fabricated in a CCD/CMOS hybrid planar technology. This was developed for high-speed demodulation pixels used in ToF range imaging. Another approach, reported in [13], makes use of the modulation of drift fields in the substrate by changing the substrate voltages within the pixel, which compromises the correct functionality of the neighbouring circuitry and requires fabrication of good isolation structures for each pixel.

Following the entire analysis just presented, a novel approach based on a lateral drift-field induced in the photoactive area by a concentration gradient is proposed. This gradient is created using a non-uniform lateral doping profile of an extra designed *n*-well to be fabricated in the 0.35µm CMOS process described above. This is the essential idea behind the *lateral drift-field photodetector* (LDP) introduced below.

3. Lateral Drift-Field Photodetector (LDP)

The just mentioned extra *n*-well with a non-uniform lateral doping profile is located on the epitaxial substrate, as shown in Fig. 5(a). It remains fully depleted during operation if sandwiched between the substrate and a grounded p^+ layer. A collection-gate (CG), a transfer-gate (TG), and a floating-diffusion (FD) also form part of this photodetector, two-dimensional layout example of which can be found in Fig. 5(b).

A metal-oxide-semiconductor (MOS) capacitor-based *collection-gate* (CG) is fabricated on the one end of the sandwiched well, which remains biased at a certain voltage (e.g., V_{DD}) and induces an additional electrostatic potential maximum in the system, where the photo- and thermally- generated carriers are finally collected. The fact that the CG is fabricated on

top of the same well resembles a “buried” photogate, where the electrostatic potential maximum, if a perpendicular cut is made across the CG, is located away from the silicon surface (Fig. 8), thus reducing the amount of charge carriers that are caused by the rapid surface-states to be mixed with the already collected photocharge. This potential maximum, as well as the extension of the CG are optimized to accumulate the desired amount of collected charge.

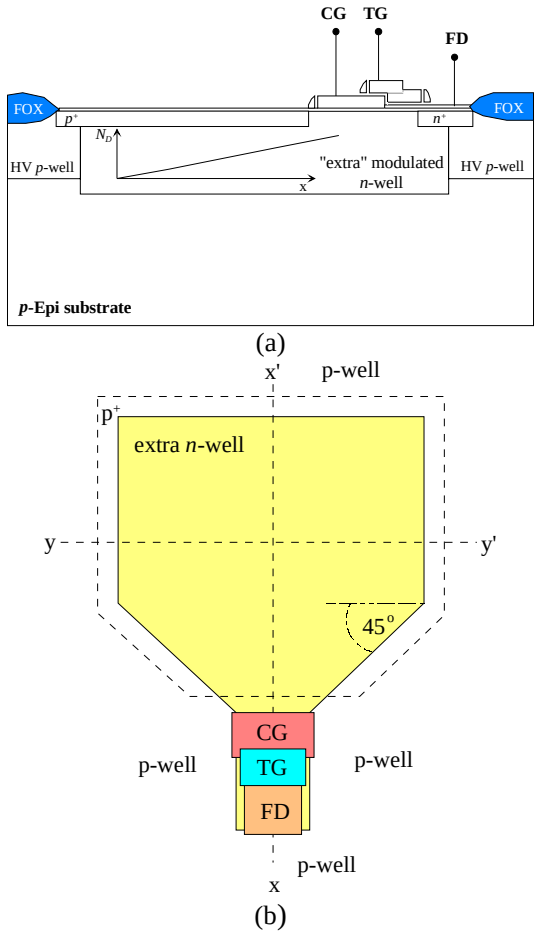

Fig. 5. (a) Schematic representation of the proposed CMOS compatible, low-noise and high-response speed *lateral drift-field photodetector* (LDP); (b) layout presentation of the LDP proposed.

Finally, a transfer-gate (TG) has been added which – by applying an adequate gate voltage - serves to create a potential barrier in the well to prevent the collected charge to be transferred into the floating-diffusion (FD) during the charge collection cycle. On the other hand, when properly biased it enhances the drift field mechanism when the collected charge is being transferred into the FD during the readout and the reset cycles (Fig. 7). The FD is used as a photodetector readout and reset node.

The extra *n*-well with a non-uniform lateral doping profile is fabricated using a single extra mask and a single extra *n*-type implantation step. As no additional annealing steps are allowed to be introduced in the process because of the changes in the thermo-electrical characteristics of all the neighboring electronic devices (specially MOSFETs) they would inevitably follow, the degrees of freedom for designing the extra well consist in choosing the proper moment during the fabrication process at which this extra implantation is to be performed, as well as the implantation energy and dose.

As proposed in [14] for high-voltage semiconductor devices, the shape of a non-uniform lateral doping profile is controlled by the geometry of the implantation mask and the characteristic length for diffusion, directly proportional to the number and sort of the following high-temperature annealing steps present in the 0.35µm CMOS process. A square-root function was here chosen for the concentration gradient generated in the *n*-well. Adapting the mathematical model developed in [14] for the case of interest here, and if L is the p^+/substrate sandwiched *n*-well extension, a the mask openings center-to-center distance, n number of mask openings, w_i the width of the i-th mask opening, and x_i the exact location of the center of the i-th mask opening, as it can be observed in Fig. 6(a), Eq. (1) [14] is used to determine a, for a given n, and Eq. (2) defines the different magnitudes of w_i, if a square root relation is followed, where i=1, 2, 3, …, n, and the calculated a remains constant.

$$a = \frac{(x_n - x_i)}{(n-1)} \tag{1}$$

$$w_i = a \cdot \sqrt{\frac{x_i}{L}} \tag{2}$$

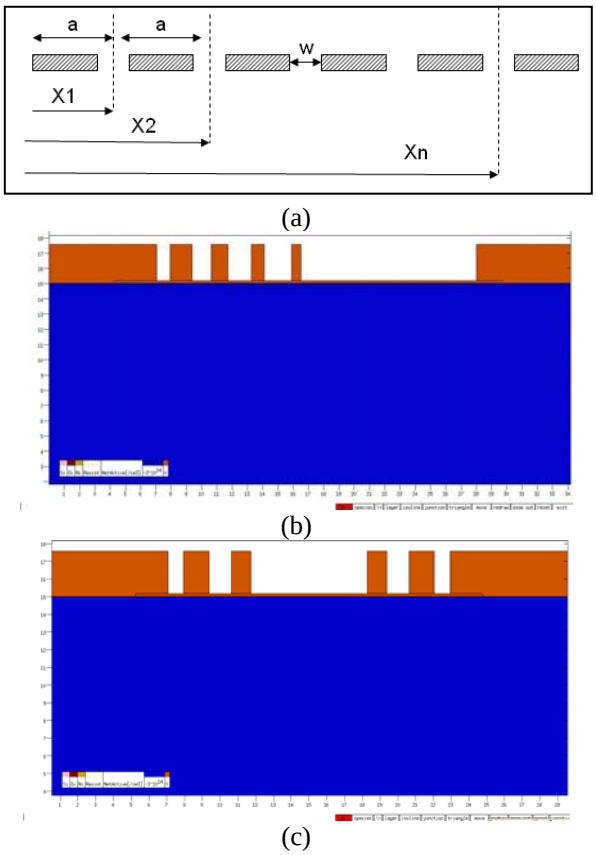

Fig. 6. (a) Schematic representation of the features defining the mask used for a non-.uniform lateral doping profile; (b) the mask used for the TCAD simulation of the extra *n*-well implantation in the 0.35µm CMOS, following the x-x' plane (Fig. 5(b)); (c) the mask used for the *n*-well implantation following the y-y' plane shown in Fig. 5(b).

Taking into account the very important photolithographic limitation of the 0.35µm CMOS process used, according to which the minimum mask geometric feature should be ≥ 0.5µm (i.e. w_i and the mask parts dividing these mask openings) for the ion implantation chosen, geometry values have been obtained, which can be observed translated into the applied mask itself in Fig. 6(b), referred to the plane x-x' shown in Fig. 5(b). Here, the defined features are: L=20µm (arbitrarily chosen), n=5, minimum mask opening of 0.63µm, and minimum mask feature between the openings of 0.9µm. On the other hand, to induce a similar square-root doping concentration dependence inside the *n*-well also along the y-y' plane shown in Fig. 5(b), the symmetrical mask shown in Fig. 6(c) was designed, using L=20µm, and n=3.

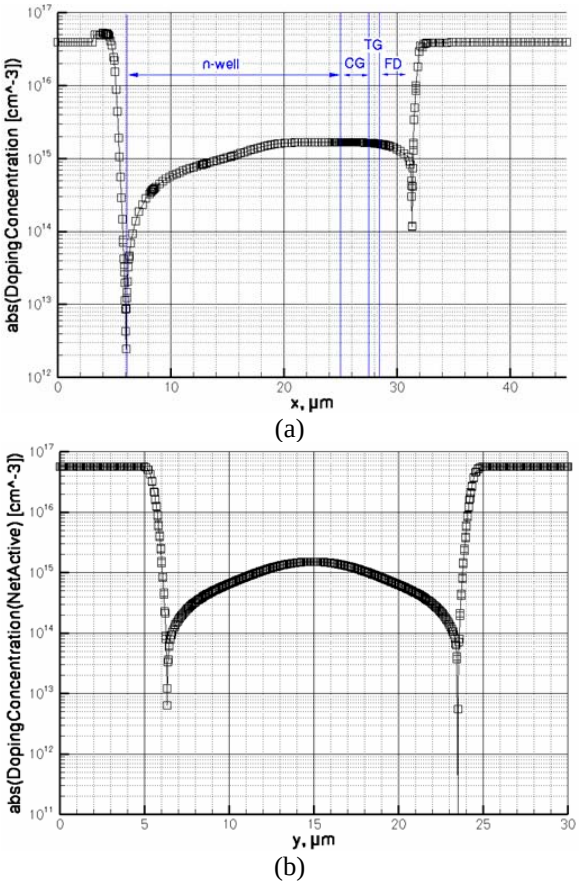

Fig. 7. (a) Square-root function dependent concentration gradient inside the extra designed *n*-well, obtained as a cut parallel to the wafer surface made to the 2-D TCAD doping profile simulation along the plane x-x' (Fig. 5(b)); (b) the doping profile cut made parallel to the wafer surface along the y-y' plane (Fig. 5(b)).

The final result of the LDP simulation, once all the 0.35µm CMOS process fabrication steps have been simulated, can be observed in Fig. 7. A cut made to the 2-D doping simulation result, parallel to the wafer surface, at an approximately 500nm depth along the x-x' plane (Fig. 5(b)) shows a doping concentration depicted in Fig. 7(a) and clearly exhibits the desired square-root function dependence of the concentration gradient caused by the extra designed *n*-well. The

desired doping profile can be observed also in Fig. 7(c) for the y-y' plane shown in Fig. 5(b).

Electrostatic potential simulations were then performed for the LDP pixel structure using (*Synopsys*) TCAD software tools. The results of the LDP reset/charge-transfer operation, performed biasing the CG at 3.3V, the TG at 5V, and 7V the FD at 7V are to be found in Fig 8, where the white line in the Fig. 8(a) indicates the SCR limits inside the p-type epitaxial layer. Fig. 8(b) shows cuts made to the 2-D electrostatic potential simulation result which are perpendicular to the silicon surface at different *x* coordinates. Here, the electrostatic potential increases along the LDP, as expected, and its maxima are "pushed" away from the Si surface. In Fig. 8(c), the electrostatic potential gradient induced in the LDP can be seen parallel to the silicon surface at two different depths: at the approximated depth of the vertical potential maxima and immediately below the p^+ layer depth.

If the transfer-gate is biased at 0V, an electrostatic potential minimum is induced between the CG and the FD, and the charge-collection time can be in this way controlled in the pixel.

In this solution, the designed *n*-well generates a depletion region which reaches quite deeply in the silicon substrate (depending on the electrostatic potential induced in the well); which is particularly important for near infra-red (NIR) radiation detection. On the other hand, once separated from the majority carriers due to the effect of the induced electrical field, the minority charge-carriers are immediately drifted to the local electrostatic potential maximum in the well or beneath the CG (Fig. 8(a)), and then laterally drifted further into the system electrostatic potential maximum located beneath the CG. This means that, in contrast to what happens in surface-channel or even buried-channel photogates, the CCD, or even *pinned photodiodes*, where the charge transfer depends primarily on thermal diffusion and fringe-field mechanisms, the charge transport in this solution depends almost exclusively on drift mechanism.

This principle of later drift-field photodiode has a potential to yield an ultra low-noise, high-speed, and highly versatile CMOS compatible photodetector. The charge transfer times present in this pixel, following a similar analysis as the one performed in [12], should be around 3ns. Note that this technique allows attaining high speed even for photodetectors featuring large photoactive areas.

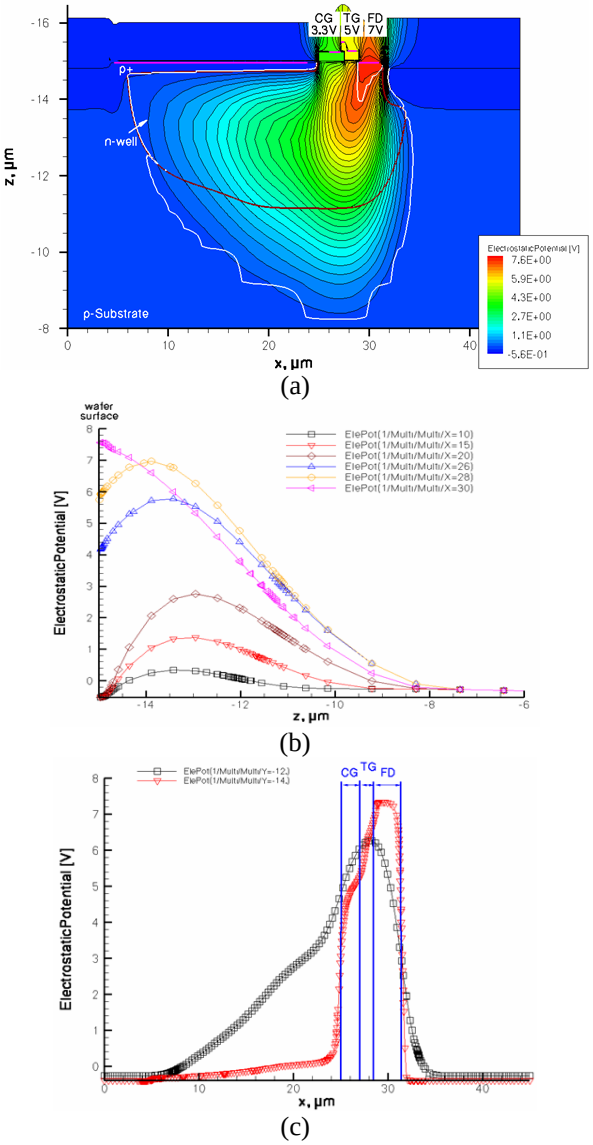

Fig. 8. (a) Lateral Drift-Field Photodetector (LDP) electrostatic potential 2-D simulation result performed using TCAD software tools for the reset/readout condition. Here, CG is biased at 3.3V, TG at 5V, and the FD at 7V. (b) Silicon surface perpendicular cuts made to (a) at different *x* coordinates showing the electrostatic potential increase along the LDP and its maximum being "pushed" away from the Si surface. (c) Electrostatic potential cuts made parallel to the silicon surface in (a) at the potential maxima (black boxes), and below the p^+ layer (red triangles).

The SNR can be further enhanced in this device by using special readout techniques, such as charge accumulation multi-readout averaging, special CDS applications or in-pixel signal processing.

4. Conclusion

Theoretical concept and simulations have been presented for a novel *lateral drift-field photodetector* (LDP) pixel to be fabricated in the 0.35µm CMOS process available at the Fraunhofer IMS. The proposed photodetector features a specially designed *n*-well with a non-uniform lateral doping profile that follows a square-root spatial dependence. The pixel based on this principle contains a "buried" MOS capacitor-based collection-gate, a transfer-gate, and a floating-diffusion. The concentration gradient formed in the *n*-well requires a single extra implantation step and generates a lateral drift-field in the photoactive area of the pixel which enables a high transfer speed of photogenerated charge carriers at low noise. According to the simulation results presented, charge-transfer times of less than 3ns are to be expected.

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