Micro Structure Analysis for System in Package Components - Novel Tools for Fault Isolation, Target Preparation, and High-resolution Material Diagnostics

M. Petzold¹, F. Altmann¹, M. Krause¹, R. Salzer³, C. Schmidt¹, S. Martens², W. Mack³, H. Dömer³, A. Nowodzinski³
¹) Fraunhofer Institute for Mechanics of Materials, Walter-Huelse-Str. 1, 06120 Halle, Germany
²) Infineon Technologies AG, Wernerwerkstrasse 2, 93049 Regensburg, Germany
³) Carl Zeiss NTS GmbH, Carl-Zeiss-Strasse 56, 73447 Oberkochen, Germany
Matthias.Petzold@iwmh.fraunhofer.de

Abstract

In this paper we introduce novel tools for an improved failure analysis process flow for complex packaged microsystems. This failure analysis process flow starts with a non-destructive defect localization using an improved Lock-In Thermography (LIT). After fault isolation, a highly efficient target preparation can be performed using cross-sectioning by combined pulsed-laser ablation and high-current Focused-Ion-Beam (FIB) milling in a specifically modified FIB device. The sample quality achieved is high enough to enable improved high-resolution material analysis of cross-sectioned structures using Scanning Electron Micrography (SEM) and Electron Back-Scatter Diffraction (EBSD), particularly for the analysis of highly resistive bonding interconnects, intermetallic compound identification, and texture analysis. To illustrate the complete workflow of the approach, a failure analysis of a vertically integrated microsystem using a microinert technology is described. The particular benefit of each step is compared to conventional approaches in failure analysis. In addition, the potential of the new failure analysis methodology for future applications using System in Package (SiP) technologies is highlighted.

Failure analysis workflow

Technologies for the assembly of complex SiP solutions and 3D integration as well as for embedding of active and passive components into built-up layers of substrates have attracted increasing attention during recent years. In addition to the technological aspects, the reliability properties are also of paramount importance.

Due to these new systems’ complex designs, dimensions, and materials, traditional failure-analysis methods established for semiconductor front-end technologies are either not applicable or have to be adapted to the specific requirements of SiP and 3D integration technologies. The need for failure identification in stacked or buried components has to be taken into account, including information on vertical fault position and the broad variety of material combinations involved. Thus, it is essential to develop new methods to detect reliability-limiting or failed structures in highly integrated systems. These methods must be able to be applied during technology development, quality testing, reliability assessment, and failure analysis of field returns. The paper aims at demonstrating novel tools that can be implemented into a stepwise fast and efficient failure analysis process flow for complex integrated microsystems. In the first section of the paper, we show the application of non-destructive localization of defects by improved LIT method. Due to the transparency of Si to infrared radiation, this technique allows the detection of defects directly in the interface between stacked Si components. The technique is therefore particularly well-suited for fault isolation in vertically integrated systems.

In many failure analysis cases, the preparation of metallographic cross-sections of the localized defect site is necessary to investigate the mechanism causing the failure. In addition to the need to remove large quantities of materials, a typical problem of mechanical cross-sections is the smearing of soft materials such as tapes, gold metallization, or solder into cracks and delaminations. This normally requires the application of ion polishing for a significant increase in sample quality, and the use of FIB techniques [1]. However, especially for packaged microsystems, the time required for the FIB preparation is the limiting factor due to the relatively slow ion milling process. The ablation rate of silicon is typically as low as 2.7 µm/s for a beam current of 10 nA. This is sufficient for target preparations on the Integrated Circuit (IC) level, but for typical packaging dimensions, a huge amount of time is necessary. A so-called High-CURRENT FIB (HC-FIB) can achieve beam currents up to 100 nA and ablation rates of up to 30 µm/s. Another approach is the additional insertion of reactive gases by a Gas-Injection System (GIS) to increase the etch rate by one or two orders of magnitude [2]. Recently, Inductively Coupled Plasma (ICP) ion sources were applied for package preparation. Compared to a conventional Liquid Metal Ion Source (LMIS), ICP ion sources have significant higher beam currents in the µA- and even mA-range. Tesch et al. demonstrated several applications such as cross-sections in a Through Silicon Via (TSV) or through a 750-µm solder ball [3].

In this paper, we demonstrate how target preparation using a combination of rapid pulsed-laser ablation and precise HC-FIB milling could be used for SiP cross-section preparation to analyze the localized defects traced by the preceding LIT-based fault isolation. For this purpose, a novel tool has been developed combining the excellent ablation rates of pulsed-laser ablation with the high accuracy of FIB milling. Therefore, an FIB device was equipped with a new high-current ion-beam column and a laser ablation device directly attached to the FIB lock chamber.

For comparison, Table 1 lists the typical ablation rates of silicon for various ion-beam technologies compared to the removal rate by a pulsed Diode-Pumped Solid-State (DPSS) laser with an optical wavelength of 355 nm. Also, the time needed to ablate a volume of 0.3 mm³ is shown, which...
corresponds to the removed material in the following application presented. In particular, the combination of laser ablation and HC-FIB promises to enable rapid, high-efficiency preparation of cross-sections for failure spot access to buried components. This approach can help to close the gap between large-scale metallographic preparations, and slow but highly accurate FIB preparations.

Table 1: Comparison of removal rates of different ion beam technologies and pulsed laser ablation

<table>
<thead>
<tr>
<th>Method</th>
<th>Ablation rate of silicon [µm³/s]</th>
<th>Time needed to remove 0.3 mm³</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIB</td>
<td>2.7</td>
<td>3.5 years</td>
</tr>
<tr>
<td>HC-FIB</td>
<td>30</td>
<td>116 days</td>
</tr>
<tr>
<td>FIB combined with GIS</td>
<td>250</td>
<td>14 days</td>
</tr>
<tr>
<td>ICP ion source</td>
<td>2000</td>
<td>1.7 days</td>
</tr>
<tr>
<td>355-nm DPSS laser</td>
<td>$1 \cdot 10^6$</td>
<td>5 minutes</td>
</tr>
</tbody>
</table>

Nevertheless, the feasibility of this approach may be affected by any potential material alterations due to the laser ablation step, such as local melting, chemical reactions, phase formation, recrystallization, surface contamination, increased diffusion rates or any other material transformation processes in the Heat-Affected Zone (HAZ), as well as the possible formation of preparation-induced cracks, surface roughening and other damage processes. Therefore, in a discussion of practical application cases, it is important that the original defect to be analyzed must not be removed or altered. Furthermore, the actual total process time of preparation will depend on how long it takes to remove the laser-induced HAZ by FIB preparation until a high-resolution SEM analysis becomes possible. This is particularly important if the grain microstructure and intermetallic phase formation of interconnecting components in SiP and vertically integrated systems, such as lead-free solder microbumps or wirebond contacts, have to be analyzed by EBSD techniques. The detection of EBSD patterns in sufficient quality requires a specifically high-end polishing that reduces any preparation-induced defect zone in the sample surface to a thickness of less than 10 nm.

To illustrate the complete workflow of the approach mentioned above, a failure analysis of a vertically integrated microsystem using a flip-chip-like microinsert technology is described. The particular benefit of each step is compared to conventional approaches in failure analysis. In addition, the potential of the new failure analysis methodology for future applications using System in Package (SiP) technologies is highlighted.

Ni microinsert technology

The samples fabricated by an innovative Ni microinsert technology were used as a case study to demonstrate the potential of the failure-analysis workflow for components based on highly integrated 3D approaches. The Ni microinsert technology is a flip-chip-like process for face-to-face interconnection of heterogeneously integrated systems. While solder bumps are used for conventional flip-chip technology in many cases, here small spikes of Ni are formed at the point of interconnection between the two dies. The microinserts are formed either at a bond pad or at the termination of a rerouted interconnection by using a combination of photolithography and electrolytic plating (Fig. 1). An appropriate glue layer is required as an under-fill. Thermo-compression bonding is then applied to achieve a robust connection (Fig. 2). A detailed general description of the Ni microinsert technology is given by Mathewson et al. [4]. In terms of bonding quality and reliability, the choice of glue layer and the device-to-wafer co-planarity are crucial to avoid regions with open circuits or high-resistance contacts. In the investigated system, 32 contact pads forming a daisy-chain structure were used with each pad containing 16 isolated microinserts with a diameter of 5 µm. Specimens that showed a significantly increased ohmic resistance after assembly were analyzed to detect the failure mechanism involved.

Fig 1: (a, top) Electrolytically deposited Ni microinserts on a metal pad; (b, bottom) System assembly by thermo-compression bonding [4]
Defect localization of buried defects using Lock-In Thermography

LIT was used to localize the failed contacts inside the device. This method pulses the supply voltage of the device under test with a certain frequency. The resulting thermal response is imaged by a highly sensitive infrared camera in the spectral range of 1.5-5 µm. Using two different correlation functions, a sin-function and a cos-function, splits the thermal response into one part that has no phase shift with respect to the electrical excitation signal (so called 0°-signal), and a second part that is 90° phase-shifted. This phase-correlation approach allows high spatial resolution and sensitivity that is even higher than the thermal noise of the camera detector itself. The resulting 0° and 90° signals are integrated and make it possible to derive either the amplitude or the phase image.

\[
\text{Amplitude} = \sqrt{(S_{\text{in-phase}})^2 + (S_{\text{out-of-phase}})^2} \\
\text{Phase} = \arctan \frac{S_{\text{out-of-phase}}}{S_{\text{in-phase}}}
\]

where \( S \) represents the intensity of the temperature-dependent signal. The amplitude image has the advantage that the signal-to-noise-ratio is increased and therefore defect-related hot spots are detectable while the phase image leads to a dynamic suppression and removes the influence of the material emissivity. This offers an opportunity to identify even weak hot spots in the vicinity of very intensive signals. Furthermore, by analysing the defect’s depth-related phase shift, 3-dimensional defect localization within fully packaged and complex devices is possible. The first investigations of this topic were published in [5].

Using both resulting images, the amplitude and the phase image, it is possible to detect thermally active defects with a spatial resolution down to approximately 1 µm and a thermal energy sensitivity down to a few µW. In addition, due to the fact that silicon is transparent in the infrared range, LIT can easily be applied from the chip’s front or back sides and hence thermal active failures in the chip-to-chip contacts can be imaged directly through the Si substrate. Therefore, an allocation of the detected hot spot to the topography of the daisy-chain structure in the bonding interface between both dies is possible. In order to allow navigation for the following target preparation, the distance from the defect area to the edge of the upper die was determined for each failure spot.

The measurements were done at a current of 50 mA. In this case, with a dissipation power of a few mW, it was possible to image the thermal response of the device within a few minutes at a lock-in frequency of 25 Hz (Fig. 2).

In Fig. 2, defect-related thermal emissions indicating the presence of high resistance contacts between the dies can be seen at the spots (1) and (2) compared to a reference contact (3) which shows no heat dissipation. For the following target preparation step, high spatial resolution is required. A resolution improvement for the thermal emission signal itself can easily be achieved by using a Gaussian fit. However, for a precise allocation of the thermal emission to the defective structure, a high spatial resolution of the topography pattern in the sample is also necessary. Therefore, LIT was used with a recently developed high-resolution infrared objective. Fig. 3 shows that the resulting spatial resolution allows the identification of single defective Ni plugs with 5 µm diameter inside the chip-to-chip interface. The lower temperature sensitivity of high-resolution imaging can be compensated for by an increased measurement time.

![Fig. 2: LIT amplitude image showing a defect-related thermal emission at the interconnect areas (1) and (2) between two dies in comparison to a reference contact (3)](image)

![Fig. 3: High-resolution imaging using LIT of a contact area allows the exact localization of single defective Ni plugs](image)
Combined laser-FIB target preparation

The feasibility of laser-based target preparation with a single laser source was demonstrated recently for molding compound, silicon dies, and metal interconnects in 3D integrated devices. Various laser technologies such as ultrashort-pulse lasers, Excimer lasers, and DPSS lasers with different wavelengths and pulse durations were evaluated. For the target preparation of stacked silicon dies, the laser wavelength was the most important factor with respect to artifact-free thinning. With the ultraviolet 355-nm DPSS laser, a distinct ablation of the stacked silicon dies was possible with resulting surface roughness of around 5 µm [6]. Furthermore, the HAZ during laser preparation was analyzed, which is extremely important to help determine if visible cracks or delaminations are artifacts caused by the thermal load during laser preparation, or real defects in the device. A molten region only 1-2 µm thick was found. After estimation of the amount of absorbed energy, the spatial and transient temperature profiles were calculated by finite element simulations. These thermal simulations confirmed that the molten material, here silicon, cools down to a few degrees above ambient temperature in the time interval of tens of µs until the next laser pulse is deployed. A significant temperature increase occurs only within a distance of 5-6 µm close to the laser edge. Therefore, the extension of the HAZ is limited to the order of the surface roughness [7].

Laser preparation was applied to perform a cross-section through those Ni microinserts that showed hot spots during LIT measurements, thus indicating highly resistive contacts. Fig. 4 shows the area of laser preparation, which was a square of 1 mm²; the depth of the laser cavity was 300 µm. Laser parameters were chosen which resulted in an ablation rate for the silicon of around $1 \times 10^6$ µm³/s. The processing time to remove the silicon volume of 0.3 mm³ was 300 seconds. An ablation rate of $6.5 \times 10^6$ µm³/s is achievable for silicon with this laser system [8].

Fig. 5 shows a more detailed view of a corner of the laser-prepared cavity. The 4- to 5-µm-thick glue layer between the 180-µm-thick upper die and the silicon substrate is clearly observable. The emerging edges during laser ablation in silicon are not perpendicular. An edge angle of around 12 degrees occurs, which is very advantageous during subsequent FIB polishing. This edge angle has to be also considered as an offset during laser navigation, which can currently be done with a position accuracy of around 10 µm.

Fig. 4: SEM image of the 1 mm² area of laser preparation. After a processing time of 300 seconds, the cavity depth is 300 µm

Fig. 5: Corner of the laser-prepared cavity with the clearly observable 4- to 5-µm-thick glue layer below the 180-µm-thick upper die

The remarkable small corner radius of the laser cavity is shown in Fig. 6. Despite the fact that a single laser impact has a diameter of more than 40 µm, due to the mentioned edge angle, the corner radius decreases down to 2-3 µm. The Ni microinserts, the glue layer, and the metallization are clearly observable immediately after laser preparation. No cleaning or polishing has been applied at this stage of preparation.

Fig. 6: Detailed view of the Ni microinserts and the cavity corner radius directly after laser preparation without any additional cleaning or polishing
Fig. 7 shows the corner of the laser cavity after a few minutes of subsequent FIB polishing with a beam current of 10 nA. In the region of the Ni microinserts, the material is removed to a depth of 3-4 µm.

Fig. 7: Ni microinserts after a few minutes of FIB polishing

The high current capability of the device is shown in Fig. 8. It shows an increased cross-section at the edge of the laser cavity which is prepared with an ion current of 50 nA and subsequent polishing at 10 nA and 2 nA.

Fig. 8: Ni microinserts and metallisation after HC-FIB preparation and FIB polishing

SEM and EBSD analytics

The detailed view of two Ni microinserts in Fig. 9 and Fig. 10 shows the root cause of the hot spot signal detected by LIT. A glue-filled gap is observable between the Ni microinsert and the top die while the contact between the galvanically deposited Ni and the bottom die is intact. The reduced contact area to the top die results in an increased current density and causes the hot spots observed by LIT measurements. This result was also confirmed by conventional mechanical cross-section preparations followed by FIB analysis.

Fig 9: Cross-section of highly resistive Ni microinserts with glue-filled gap (arrow) between electrolytically deposited Ni and upper silicon die (overview)

Fig 10: Highly resistive Ni microinserts (left) with glue-filled gap (arrow) compared to an electrically intact reference contact (right), detail

For a more detailed material analysis, SEM-based microstructure diagnostics are typically combined with additional methods such as Energy-Dispersive Spectroscopy (EDS), Wavelength Dispersive Spectroscopy (WDS) and EBSD. Particularly for the EBSD analysis, the quality of the obtainable results is directly related to the quality of the prepared sample surface. In particular, contamination caused by smearing or distortions of the crystal lattice near the surface due to work hardening as well as the formation of HAZs must be avoided to provide reliable measurement results for an appropriate failure analysis. This is essential when applying EBSD, for example, to a multitude of different materials including grain structure analysis of lead-free solder materials (Fig. 11), common wire-bond materials, or even to the identification of intermetallic compounds (Fig. 12) [9]. In the case of the Ni microinserts, no further EBSD investigations were performed. However, the required sample surface quality can also be achieved for laser-ablated specimens by refined ion polishing processes allowing the HAZ to be completely removed.

Thus, due to the high milling rates of the combined laser/FIB preparation, the use of EBSD for similar cases is no longer limited to metallographic cross-sections or surface near areas. In fact, the geometrical requirements of EBSD analysis could be fulfilled by specific removal of material along the direction of the diffracted beam, enabling high-resolution texture analysis with spatial resolution in the range of tenths of
Summary and Conclusions

To improve the quality and reliability properties of 3D integrated components, it is not only necessary to detect a failed device or to localize the failed structure. Determining the detailed root cause of the failure mechanism is also essential. This paper presents novel tools for the failure analysis of current microsystems. Their application and beneficial potential is demonstrated for Ni microinsert interconnects between two Si dies. The benefits of using LIT as the first step of the failure analysis flow for non-destructive defect localization were demonstrated, including high-resolution thermal imaging through the top Si die to detect highly resistive Ni interconnects directly in the bonded interface. The isolated failed interconnects were subsequently prepared in cross-section using an additionally developed new combination of fast laser-based ablation and highly accurate FIB. It was proven that the material changes introduced by the laser process did not affect the failure analysis results, provided the use of appropriate laser parameters and precise removal of the 6-µm-thick HAZ by FIB. This procedure made it possible to detect incomplete bonding between the Ni microinserts and the metallization of the top Si die, leading to the identification of highly resistive interconnects as the root cause for the significantly increased ohmic resistance and the related hot-spot signals found during the LIT analysis. In addition, also EBSD is, in principle, possible on such similarly prepared contacts. Due to its excellent milling rates, the combined laser/HC-FIB preparation routine offers unrivaled capabilities in terms of speed and efficiency for SEM failure analysis, as well as for local texture analysis and phase identification in 3D-integrated devices. As a result, a new FIB demonstrator with a high-current ion-beam column and integrated laser ablation is under construction.

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