Monolithic RC-Snubber for Power Electronic Applications

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***Abstract*-In this work, we present a monolithic RC-snubber for power electronic applications that outperforms state of the art RC-snubbers in terms of characteristic electrical parameters. The principle device structure as well as the process technology is presented. The outstanding properties of the device are a high capacitance per area (1.5 nF/mm^2), a low temperature coefficient of the capacitance value (85 ppm/°C) and a low leakage current (<1 nA) for voltages up to 250 V. Characteristic electrical parameters of the single device and in a typical application are shown. In comparison to a SMD snubber, the monolithic RC-snubber shows a significant reduction of overvoltage during switching and enhanced electromagnetic noise suppression.**

I. Introduction

System complexity and contribution of power electronics, in mobile systems, like automobiles, are constantly increasing [1, 2]. Therefore, the topic of passive device integration becomes more and more important.

A RC-snubber, which is necessary to attenuate unwanted oscillations in circuits, consists of a resistor and a capacitor in series. The attenuation effect is provided by the resistor which is operative during switching. In the stationary case, the resistor is decoupled by the capacitor. A low inductive coupling to the oscillating circuit which has to be damped is important for the effectiveness of the RC-snubber. Otherwise, the parasitic inductance of the electric line decouples the resistor from the oscillating circuit during switching and degrades the efficiency of the attenuation drastically. For the design of the RC-snubber, dissipation of heat due to thermal losses, generated in the resistor during switching, is another important factor.

The specification of the resistor and the capacitor of a RC-snubber are defined by above described properties. For optimal attenuation, the resistor and the capacitor of the RC-snubber have to be adapted to the characteristic impedance of the oscillating circuit which has to be attenuated. Furthermore, efficient cooling of the resistor in the RC-snubber has to be achieved and assembling of the RC-snubber has to be done with low inductive coupling. Additionally, the RC-snubber has to sustain high voltages for short periods of time. For a low inductive coupling and to simplify the mounting process, the assembly of the RC-snubber and the circuit which has to be attenuated should be done with the same mounting technique.

To meet all these requirements, monolithic integration of the RC-snubber on a silicon chip is a promising way. This approach enables the mounting of the RC-snubber in direct vicinity to the power switch to be attenuated by the same mounting process on a DBC (Direct Bonded Copper) substrate. Alternatively, the RC-snubber and the power unit can be processed on the same silicon wafer where a low inductive coupling can be easily realized. The heat sink function of the DBC can be used for the resistor of the RC-snubber.

In this work, a technology to fabricate MIS (Metal Insulator Semiconductor) capacitors for a subsequent monolithic integration is developed. A dielectric layer and a metal electrode are deposited on a silicon wafer to form the capacitor. Similar to the processing of trench type DRAMs in which the information is stored as charge in a capacitor, also trench capacitors with high aspect ratios are used for this approach. Trench capacitors have significantly higher capacitance per area in comparison to planar capacitors. However, for DRAMs the operating voltage is limited to a maximum of 5 V [3]. For power electronics applications, much higher voltages are applied and, therefore, significant higher dielectric strengths have to be achieved. To enhance the dielectric strength, the applicability of different dielectric layer stacks with larger (physical) thickness in trenches was investigated in a previous work [4]. Realization of the RC-snubber is done using the silicon substrate as a resistor in series to the MIS capacitor.

II. Device and Process Description

A. Device structure

A schematic of our monolithic RC-snubber can be seen in Fig. 1.

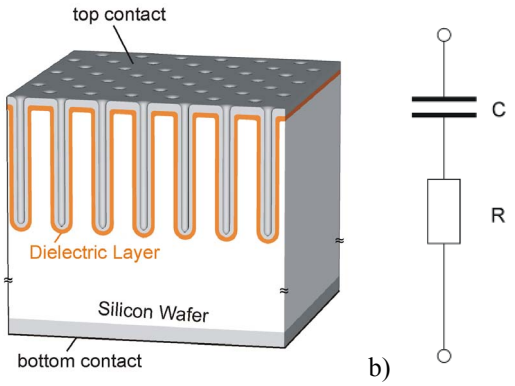


Fig. 1. a) Schematic device structure of the monolithic RC-snubber for power electronic applications, b) equivalent circuit

A large number of deep trenches enlarge the effective area of the silicon substrate which serves as the bottom contact of the MIS capacitor and simultaneously as the resistor of the RC-snubber. The trenchwalls are coated with the dielectric layer stack and afterwards filled with highly doped polysilicon. A metal contact on top of the structure is used for the connection of the RC-snubber by wire bonding. For the backside contact of the RC-snubber, a metal stack consisting of Al,

Ni, and Ag is deposited on the backside of the silicon wafer which forms a solderable or sinterable bottom contact. The bulk of the silicon in between the bottom contact and the trenches mainly determines the value of the resistance of the RC-snubber. Due to this design, the resistor has a large-area thermal contact to the DBC.

In this work, RC-snubbers with a silicon wafer area of 1, 12.5, and 25 mm^2 were manufactured and characterized. In addition, planar RC-snubber devices as reference were analyzed.

B. Process technology

Manufacturing of the trench RC-snubbers was done based on silicon semiconductor processing technology. A simplified process flow is depicted in Fig. 2 a-f.

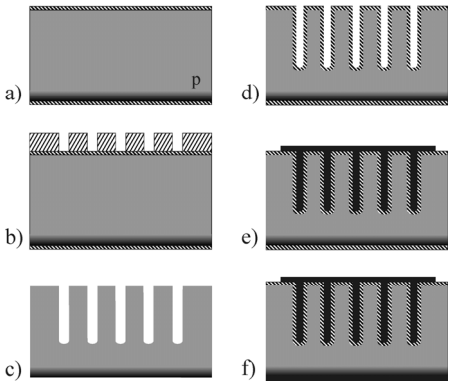


Fig. 2. Simplified process flow for a monolithic RC-snubber. a) thermal oxidation, back side doping and annealing, b) first lithography of the trenches, c) dry etching and removal of the photo resist and SiO_2, d) processing of the dielectric stack, e) processing and patterning the top electrode, f) cleaning of back side and processing the bottom electrode

First, a 20 nm silicon dioxide (SiO_2) layer is thermally grown on a 150 mm p-doped ($N_A \approx 1.3 \cdot 10^{15}$ cm^{-3}) silicon wafer and the back side is highly p-doped by ion implantation (boron, $5 \cdot 10^{14}$ cm^{-2}, 50 keV) and a subsequent anneal (N_2, 1050°C, 30 min.) to form a good ohmic contact (Fig. 2 a). Then, the trench positions are defined by lithography (Fig. 2 b). Next, the trenches are etched with a depth of about 31 µm, using the ASE (Advanced Silicon Etch) process which is a derivate of the "Bosch" process [5]. Subsequently, the photo resist and the 20 nm SiO_2 layer are removed (Fig. 2 c). Next, the insulators for the MIS-capacitors are formed. As insulator, the wafers receive a dielectric stack consisting of 20 nm thick SiO_2 grown by dry thermal oxidation and a 500 nm thick layer of silicon nitride (Si_3N_4), deposited by LPCVD (low pressure chemical vapor deposition) (Fig. 2 d). The top electrode is formed by deposition of poly-silicon using LPCVD and subsequent doping by a thermal treatment in phosphorus oxychloride ($POCl_3$) atmosphere. On top of the device, aluminum is deposited and the top contact is patterned to define the area of the devices (Fig. 2 e). Next, the deposited layers are removed from the back side of the wafer to expose the highly p-doped silicon and the bottom contact metallization is deposited by PVD (physical vapor deposition). Finally, the wafers are annealed in forming gas at 430°C for 30 min. (Fig. 2 f).

III. Device Characteristics

For the electrical characterization of the RC-snubber, capacitance, resistance, leakage current, and impedance were measured over a wide range of frequencies and operation temperatures.

A. Series capacitance and series resistance

To analyze the capacitance and the resistance of the monolithic RC-snubber, capacitance voltage (C-V) measurements were performed using an HP 4277 LCZ-meter at a frequency of 1 MHz and a test signal level of 1 V_{rms} applying a dc voltage of -40 V at room temperature. Figure 3 shows the cumulative percentage of the capacitance and the resistance values for 33 RC-snubbers with an area of 25 mm² spread across a 150 mm wafer. The 3D structuring of the devices leads to capacitance values in accumulation of around 38 nF which is a magnification of a factor of 12.7 in comparison to the planar references. Next to the mean value of the capacitance of 37.9 nF and the mean value of the resistance of 0.75 Ohm, a tolerance range of ±5% is designated. Regarding the capacitance, 67% of the devices and regarding the resistance, 84% of the devices lie within this tolerance range.

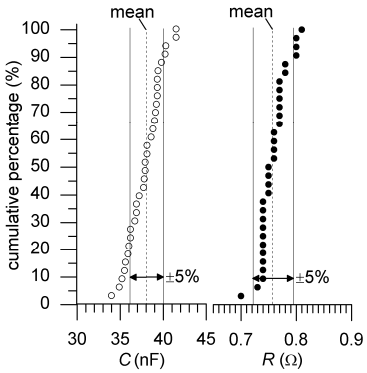


Fig. 3. Cumulative percentage of the capacitance and of the resistance for 33 RC-snubber with an area of 25 mm² over a 150 mm wafer

B. Temperature dependence of the capacitance and the resistance

To analyze the temperature dependence of the capacitance as well as of the series resistance, C-V measurements were recorded at temperatures between 25°C and 125°C.

Fig. 4 shows the deviation of the capacitance in accumulation (ΔC) and the deviation of the resistance (ΔR) in dependence on the temperature normalized to the capacitance and the resistance at 25°C (C_{25}, R_{25}). Linear regressions for the measured values of the capacitance and the resistance were done, respectively. Using the slope of the linear regressions, the linear temperature coefficients of the capacitance α_C and of the resistance α_R can be calculated. For the RC-snubber investigated in this work, a linear temperature coefficient of the capacitance, α_C, of 85 ppm/K and a linear temperature coefficient of the resistance, α_R, of 3269 ppm/K were determined. Hence, the temperature dependence of the series resistance is much more pronounced than the one of the capacitance. For the latter, the temperature dependent conductivity of the semiconductor (i.e., the temperature dependent charge carrier mobility and charge carrier density) is the dominant factor. The temperature coefficient of the resistance corresponds to the

range for p-doped silicon with a similar doping concentration as found by Norton [6]. Metal film resistors used in the target application typically possess a temperature coefficient of the series resistance in the range of ±25 to ±100 ppm/K [7]. For most application fields, a temperature coefficient of the series resistance of the RC-snubber around ±5000 ppm/K is acceptable. In comparison to ceramic capacitors which possess a temperature coefficient of up to 1500 ppm/K and which are used in the target application of our RC-snubber, the temperature dependence of the capacitance of the RC-snubber is very low.

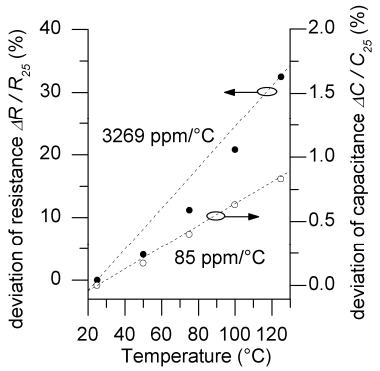


Fig. 4. Temperature dependent deviation of the capacitance (ΔC) and the resistance (ΔR) normalized to the values at 25°C (C_{25}, R_{25}), for temperatures between 25°C and 125°C

C. DC-Current-voltage measurements

For the assessment of the dielectric strength of the RC-snubber, current-voltage (I-V) characteristics were measured using a Keithley 237 source measurement unit. Fig. 5 shows typical I-V curves of the RC-snubber devices with a dielectric layer consisting of 20 nm SiO_2 and 500 nm Si_3N_4 and an area of the devices of 1 mm^2. Curves of planar RC-snubber devices with the same area are shown for comparison.

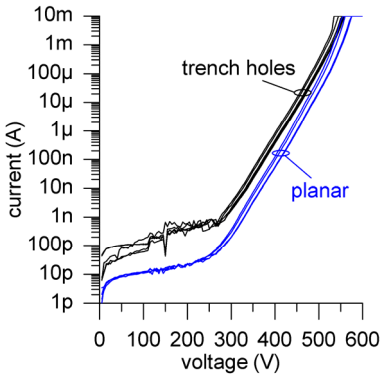
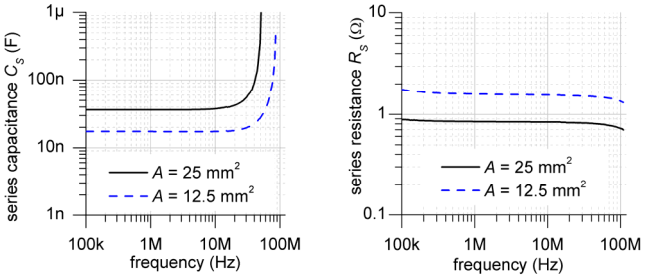


Fig. 5. *I-V* curves of planar and trench RC-snubbers with an device area of 1 mm^2

No dielectric breakdown could be seen for the RC-snubber up to a voltage of 530 V. At these voltages, leakage current through the RC-snubber amounts to 10 mA. The trench RC-snubbers show significantly higher leakage current compared to the planar references for low voltages. This may be due to the higher effective area of the 3D structured devices compared to the area of the planar references. Furthermore, the thickness of the dielectric layer may be lower in the trenches, especially at the bottom of the holes, than on the silicon surface in the planar reference [4]. For both, the trench RC-snubber and for the planar RC-snubber, Poole-Frenkel emission is the dominant leakage current mechanism for voltages higher than 300 V [4].

D. Impedance measurements

To assess the high frequency characteristics of the RC-snubber, the absolute value of the impedance and the angular phase shift were measured versus the frequency using a Agilent impedance analyzer 4294A. For the measurements, diced RC-snubbers were mounted in an Agilent test fixture 16034G which is designed for SMD devices. The applied dc bias was -20 V (accumulation), the ac voltage had a frequency in the range from 100 kHz to 110 MHz. Fig. 6 a) shows the series capacitance and Fig. 6 b) the series resistance plotted against the measurement frequency. A frequency dependence of the series capacitance is only observed for frequencies higher than 20 MHz for a device area of 25 mm^2 and for a frequency higher than 30 MHz for a device area of 12.5 mm^2, respectively. A slight change of the series resistance starts at 50 MHz for both device areas.



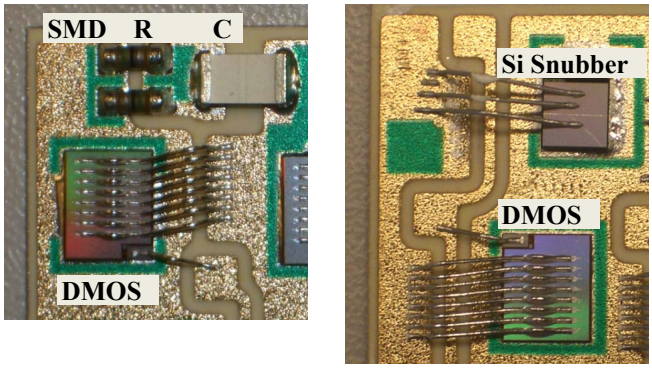
a) b)

Fig. 6. a) Capacitance and b) resistance of diced RC-snubbers with a device area of 12.5 mm^2 and 25 mm^2 over a frequency range of 100 kHz to 110 MHz

IV. Application

A straight forward application for monolithic integrated snubber chips is in power electronic systems. On the one hand, they can be used to limit over voltage during switching the power transistors (i.e., DMOS transistors or IGBTs). On the other hand and even more important, they suppress the electromagnetic noise of the power switches. In both cases the snubbers have to be operated in parallel to the power switches and in best case located as close as possible to the switches to minimize parasitic inductances. For this reason, it is an important fact that these snubbers have to withstand high ambient temperatures (i.e., above 110°C or even more) depending on application. A third very important advantage of monolithic integration is a reliability improvement by the assembling processes and, therefore, the whole system reliability. And last but not least, heading towards novel assembly technologies as sintering processes, it is a necessity to use snubber chips, because SMD technology can hardly be applied.

As mentioned before the snubber chips have to be located as close as possible to the power switches, the best suited place is to assemble them directly together with the power switches on the power hybrid, shown in Fig. 7 a) as SMD variant, b) as monolithic silicon chip snubber.



a) b)

Fig. 7. Power hybrid with power switch and a) SMD snubber, b) monolithic silicon snubber

The power hybrids are then combined in a three phase inverter module. In this module, they are directly mounted on a heat sink and the driving logic is also integrated. A typical application for those inverter modules are battery driven electrical vehicles (e.g., forklifts).

In the following Fig. 8a)-d) the impact of a monolithic silicon RC snubber on the inverter is shown. In the before discussed application the MOS transistor without (figures a, c) and with (figures b, d) the RC snubber was simulated, with the modeled parasitic devices for this application. As can be seen, comparing the V_{DS} overvoltage during switching, it can be reduced significantly using an optimized set of RC parameters.

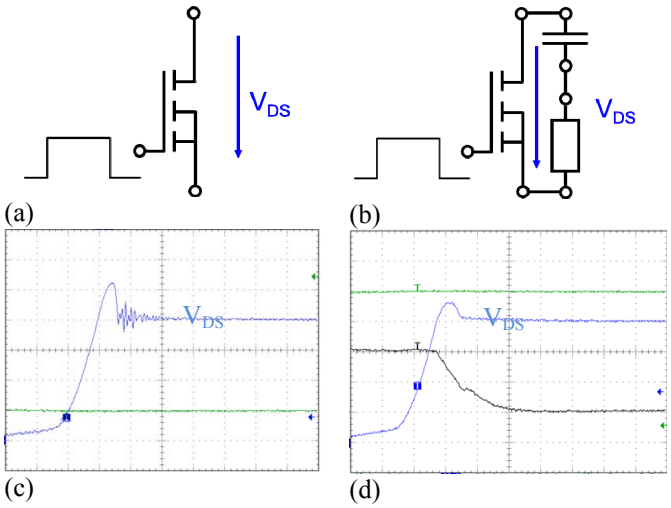


Fig. 8. MOS power switch a) without snubber, b) with RC snubber; simulated time dependent voltage during switching c) without snubber, d) with silicon chip snubber

For comparison of the electromagnetic behavior, the monolithic silicon snubber and the SMD snubber were assembled on the same power hybrid, as shown in Fig. 7. During each measurement, just the corresponding variant was actively connected to the power switches. As reference, a measurement was conducted without a connected snubber. The measurement results are depicted in Fig. 9. The frequency range of interest for the electromagnetic noise in this application is starting at 30MHz.

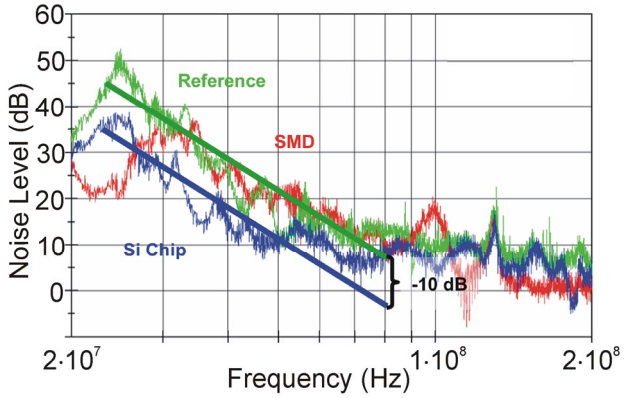


Fig. 9. Comparison of electromagnetic behavior of one phase of an module with silicon chip snubber to SMD snubber and without snubber

As shown in Fig. 9 the monolithic silicon chip snubber shows best electromagnetic noise suppression compared to the SMD variant and the reference without snubber. The suppression is increased by 10dB on average.

V. Conclusion

In summary, monolithic RC-snubber with a high capacitance per area (1.5 nF/mm^2), a low temperature coefficient of the capacitance value (85 ppm/°C) and a low leakage current (<1 nA) for voltages up to 250 V were successfully manufactured and characterized. Applying a monolithic integrated snubber chip in a power electronic module, results in a significant reduction of overvoltage during switching and a noticeable reduction of electromagnetic noise of about 10dB mean, compared to a SMD solution or even without using a snubber.

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