RF small-signal modeling of HCI degradation in FDSOI NMOSFET using BSIM-IMG

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***Abstract*—The increasing demand for reliable CMOS devices in high-frequency applications brings new challenges in the modeling of aging effects in transistors, with the need to also capture degradation of RF performance. In this paper, we explore the possibilities of using BSIM-IMG parameters to model HCI degradation under DC stress on a 22FDX™ FDSOI n-channel transistor. First, a selection of parameters is used to model HCI degradation and its impact on RF performance is analyzed. Furthermore, the "extension resistance model" within BSIM-IMG is used to broaden the model possibilities to capture RF performance degradation**

Keywords—HCI, FDSOI, RF reliability, S-parameters, BSIM-IMG

I. Introduction

Advantages offered by Fully Depleted Silicon on Insulator (FDSOI) technologies such as very good electrostatic control of short channel effects, low power consumption, decrease in junction capacitance, low leakage, back-bias tuning, and scalability have made FDSOI a strong candidate for 28 nm and beyond, as well as for radio frequency (RF) and Internet-of-things (IoT) applications [1],[2]. Hot carrier injection (HCI) is a reliability issue and has been shown to present similar behavior in FDSOI and bulk devices [1]. Although HCI has been known and analyzed for a long time, its effect on RF characteristics has rarely been studied, although it has gained importance in recent years for FDSOI technologies.

A. HCI degradation on FDSOI N-MOSFET

In [3], the first study of the degradation of small-signal parameters due to HCI in FDSOI n-type metal oxide semiconductor field-effect transistors (MOSFETS) is presented for an n-MOSFET fabricated in 22FDX™ technology of GLOBALFOUNDRIES, where the degradation of both DC and RF small-signal characteristics have been measured on wafer level.

As described in [3] for FDSOI and in [4] and [5] for bulk devices, the degradation of small-signal parameters can be partially explained by the degradation of important DC characteristics such as the threshold voltage, the maximum trans-conductance, and the drain current in the linear and saturation regimes. Therefore, to correctly model the HCI degradation of RF small-signal figures of merit (FOMs), the first step is to have an accurate modeling of the degradation of key DC parameters and analyze its effects in the device RF small-signal behavior. Then, the model can be extended to cover the effects not explained by the DC parameter shift.

B. Modeling the degradation for circuit-level simulations

The main commercial electronic design automation (EDA) vendors offer lifetime reliability capabilities in the form of aging simulations. Typically with two transient simulations, the circuit behavior after a pre-defined time of operation can be predicted. In the first simulation all the stress conditions (temperature, voltages, etc.) for each transistor in the design are captured by the simulator. This information is used by the aging model to individually calculate the degradation of each device and back annotate it to the simulation netlist. Finally, a second simulation with the degraded devices is performed, and its behavior compared to simulations of fresh devices. The degraded transistor can be modeled with a subcircuit approach that uses voltage and current sources around an unaltered device to mimic the degraded behavior or with a model card approach, where transistor degradation is modeled by drifting parameters of the intrinsic model card [6]. A third possibility is to extend the compact model of the transistor to account for aging effects.

Although HCI models degrading only DC FOMs can be used to evaluate some RF reliability characteristics [7], [8], extending the model for a more complete RF analysis is advantageous. In this paper, the measurement and characterization work in [3] is extended, by exploring the model card approach to model the degradation of several DC FOMs as well as the RF small-signal behavior, using selected parameters of BSIM-IMG, the industrial standard compact model for FDSOI.

II. Modeling of the DC Degradation

BSIM-IMG is a surface potential-based compact model, capable of modeling independent double-gate and the variation of the threshold voltage due to back-gate bias [9]. Adapting BSIM-IMG parameters for aging modeling takes advantage of the physics implemented in the transistor's compact model to capture the HCI degradation.

The studied device is an NMOSFET with a channel length (L) of 20 nm and channel width (W) of 1 um realized with 16 fingers in parallel, fabricated in the 22FDX™ technology of GLOBALFOUNDRIES. Details of the utilized measurement setup and procedure can be found in [3]. First, a sensitivity analysis was performed to determine the BSIM-IMG parameters that have a significant impact on the DC FOMs of interest: the threshold voltage and the drain current in linear

Table 1. Summary of the BSIM-IMG parameter combinations used for DC degradation modelling.

Name	Parameters	DC FOMS	R^2 IDSAT	R^2 IDLIN	R^2 VTSAT	R^2 VTLIN
BSIM A	U0 PHIG1	IDSAT VTSAT	0.99834	0.97120	0.99777	0.99350
BSIM B	U0 PHIG1	IDLIN VTLIN	0.98896	0.99956	0.99233	0.99988
BSIM C	U0 PHIG1 VSAT DSUB	IDLIN VTLIN IDSAT VTSAT	0.99988	0.99959	0.99975	0.99988

and saturation regimes (VTLIN, VTSAT, IDLIN and IDSAT). The selected parameters are: the low field mobility (U0), the work function of the front gate (PHIG1), the saturation velocity in the saturation region (VSAT) and the Drain Induced Barrier Lowering (DIBL) exponent coefficient (DSUB).

The measured degradation of DC FOMs can be mapped into shifts of model card parameters and to obtain a function to calculate aged BSIM-IMG parameters as a function of the stress conditions. The simulation results after mapping each point of the measured DC degradation into optimized values of the different parameter combinations in Table 1 can be seen in Fig. 1. The combination BSIM C offers the best *coefficient of determination* (R^2) scores (ideally 1.0) for all DC FOMs (see Table 1). The combination "BSIM A" offers R^2 scores close to "BSIM C" for FOMs in saturation, although slightly worsening for the linear FOMs, still offers acceptable results. Likewise, using the combination "BSIM B" optimizes results in the linear regime. This opens the possibility to develop an HCI model with different levels of complexity and a different number of parameters to be used.

Next, we investigate the impact of the DC degradation on the RF small-signal performance; Fig. 2 to Fig.6 show the comparison of simulation results against measurements for operating points of interest (V_{GS} from 0.3 to 0.8 V and V_{DS}=

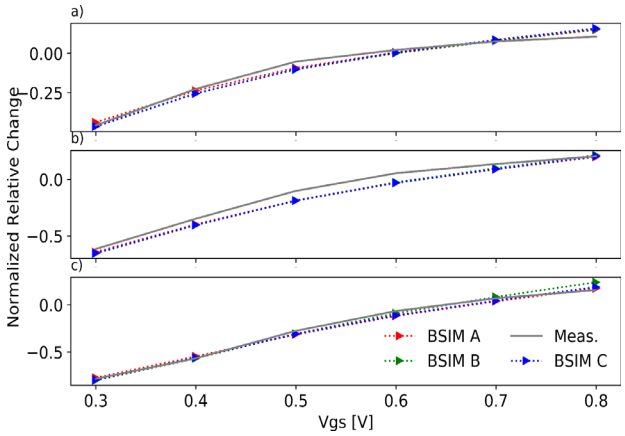

Fig. 2. Simulated and measured relative change in FMAX after 10^4s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V

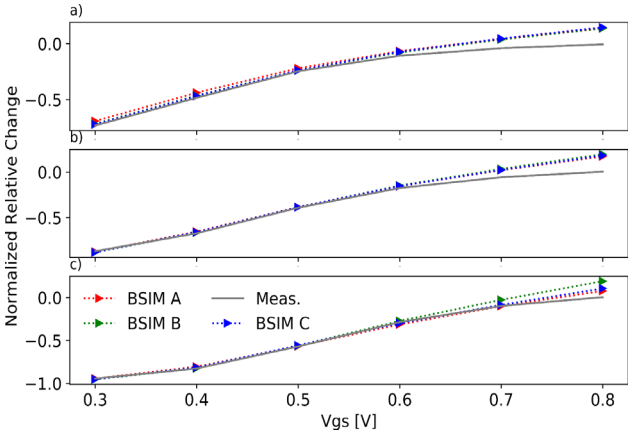

Fig. 3. Simulated and measured relative change in FT after 10^4s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V.

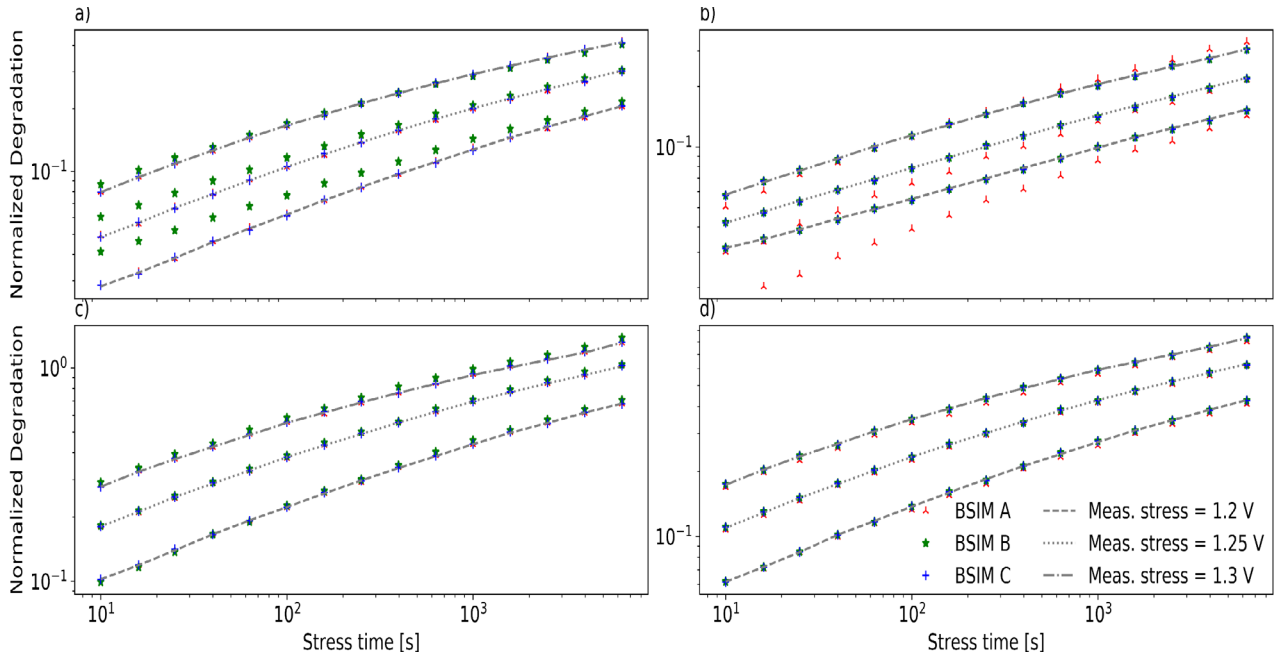

Fig. 1. Time evolution of measured and simulated degradation of : a) IDSAT, b) IDLIN, c) VTSAT, d) VTLIN for different stress voltages: 1.2, 1.25 and 1.3 V at 125 °C . Simulated values for different BSIM parameter combinations (Logarithmic scale in both axis)

0.8 V) for the RF small-signal FOMS: cut-off frequency (f_t), maximum oscillation frequency (f_{max}), and the small-signal characteristics: gate-source capacitance (C_{GS}), gate-drain capacitance (C_{GD}) and AC transconductance (Gm_{AC}), defined as:

$$Gm_{AC} = Re(Y_{21}), \quad (1)$$

$$C_{GS} = \frac{Im(Y_{11}+Y_{12})}{2\pi f}, \quad (2)$$

$$C_{GD} = \frac{-Im(Y_{12})}{2\pi f}. \quad (3)$$

It can be seen from Fig 2 to Fig 6, that the difference in simulation results between the 3 BSIM-IMG parameter combinations presented in this paper is minor throughout all the analyzed RF small-signal FOMs in saturation, with "BSIM B" showing a stronger deviation since it fits linear regime DC FOMS.

Fig. 2 to Fig. 4. compare the relative change in f_{MAX}, f_t and Gm_{AC} between measurements and simulations results for different stress voltages ($V_{GS,STRESS}$ =$V_{DS,STRESS}$ = 1.2, 1.25, 1.3 V) respectively. For f_t and Gm_{AC}, the simulations underestimate the degradation as V_{GS} increases and become significant at V_{GS}= 0.8 V. The simulation results of f_{MAX} show a larger degradation than the measurements for lower V_{GS}, this overestimation decreases as V_{GS} increases, showing a lower degradation in simulations at V_{GS}= 0.8 V.

Fig. 5. and Fig. 6. compare degradation results for the capacitances C_{GD} and C_{GS}. In this case, the difference between simulations and measurements is significant, since

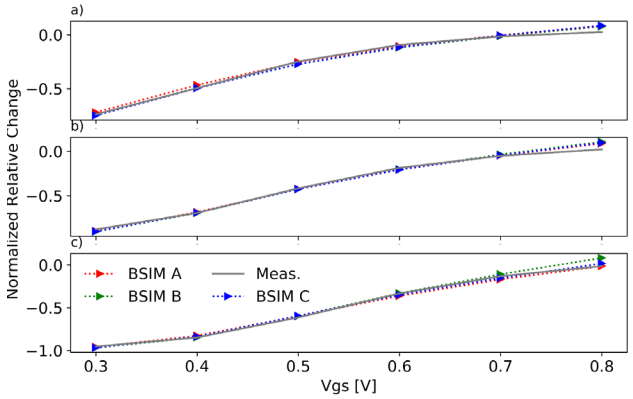

Fig. 4. Simulated and measured relative change in Gm_{AC} after 10^4 s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V

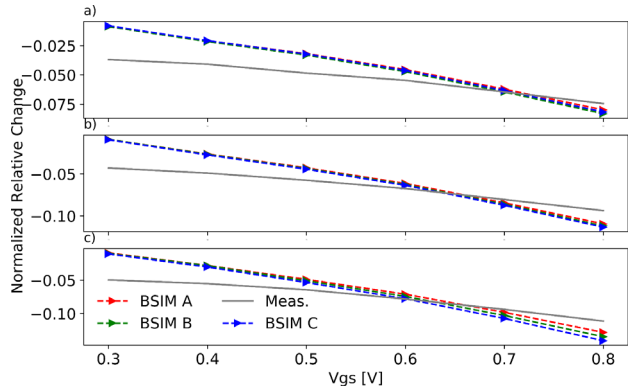

Fig. 5. Simulated and measured relative change in C_{GD} after 10^4 s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V

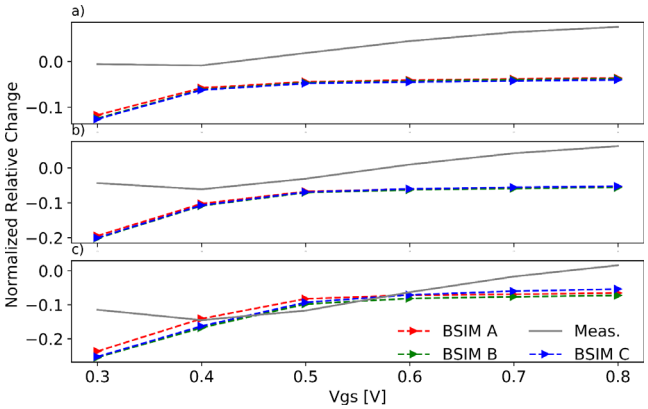

Fig. 6. Simulated and measured relative change in C_{GS} after 10^4 s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V

the measurements show an increase C_{GS} that the simulations cannot capture. The reduction in C_{GD} is larger in the measurements than in the simulations. As mentioned in [3], the degradation of the capacitances cannot be explained by the shift in the threshold voltage, but by trapped electrons close to the drain, resulting in a local change of the flatband voltage. This effect is more significant in the linear regime, but it is still present in saturation, which is the region of focus of this paper.

III. EXTENDING THE DC MODEL TO IMPROVE RF SMALL-SIGNAL DEGRADATION MODELING

The use of parasitic resistances has been proposed to model the observed effects of HCI on RF small-signal performance [5], [10]. Adding passive elements in the netlist to model the aging degradation brings difficulties in the integration of the model into the PDK and the extra nodes can affect simulation performance [6]. The BSIM-IMG compact model allows the definition of an extension resistance R_D, which can be connected between the external and the internal drain nodes of the transistor, making improvements in RF simulations possible without adding passive elements [10]. To improve RF small-signal degradation modeling with R_D, the parameter for the drain extension resistance per unit (RDWMIN) has been selected in combination with BSIM A, since it delivers practically the same results as BSIM C in saturation, using only 2 parameters.

Fig 7. shows the results of fitting R_D to improve the gate capacitance (CGS+CGD) degradation for each V_{GS} in saturation, at $V_{GS\ STRESS}$ =$V_{DS\ STRESS}$ = 1.2. Although having a bias-dependent shift in RDWMIN brings optimal results, it would be difficult to integrate into the aging simulation. As a compromise, an operating point (V_{GS} = V_{DS} = 0.8 V) has been selected to fit CGS+CGD for every stress condition with a

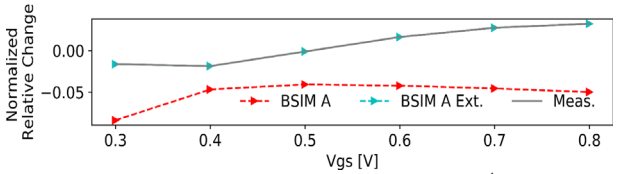

Fig. 7. Simulated relative change in CGS+CGS after 10^4s stress time for different V_{GS} (Saturation) and Stress voltage 1.2 Simulation results before and after extending BSIM A using a RDWMIN for each V_{GS}

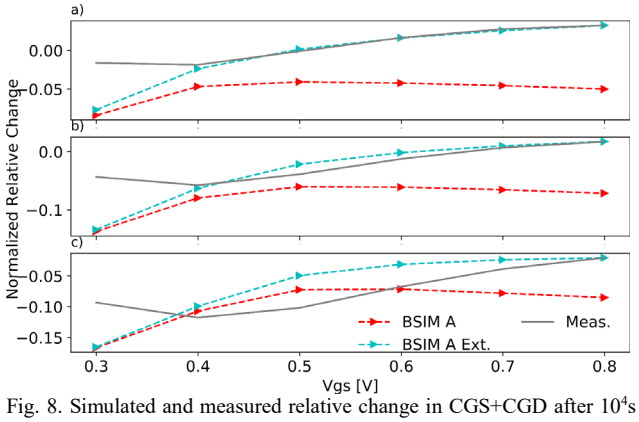

Fig. 8. Simulated and measured relative change in CGS+CGD after 10^4s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V. Simulation results before and after extending parameter combination BSIM A using fixed RDWMIN for each stress voltage.

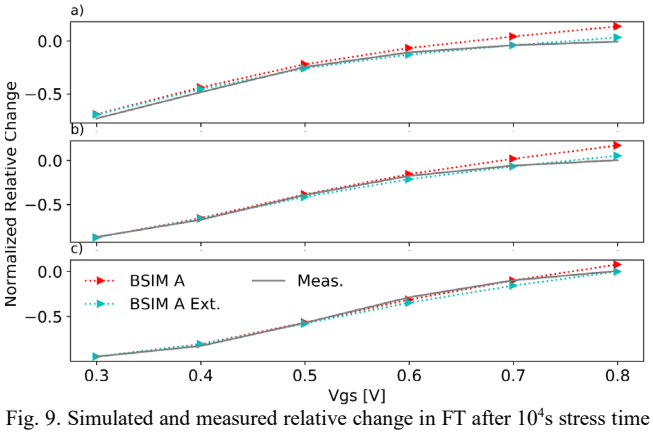

Fig. 9. Simulated and measured relative change in FT after 10^4s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V. Simulation results before and after extending combination BSIM A with a fixed RDWMIN for each stress voltage.

fixed R_D. The results for CGS+CGD, f_t , f_{MAX} and Gm_{AC} are presented in Fig 8. to Fig. 11, respectively.

Fig 8 shows that still with a bias independent R_D, it is possible to improve the modeling of the gate capacitance degradation for different V_{GS}, especially for smaller relative changes (V_{STRESS} = 1.2 , 1.25 V), but with an underestimation of the degradation for larger relative changes (V_{STRESS} = 1.3 V). Fig 9. shows an improvement in f_t by using R_D, reducing the underestimation of degradation at higher $V_{GS.}$ For Gm_{AC} (see Fig. 10) simulation results improve slightly and for f_{MAX} simulation results overestimate the degradation (see Fig.11).

Increasing the drain resistance can affect the DC behavior of the simulations, but the values used to improve the RF performance at 10^4s have minor effect in the DC characteristics (see Fig. 12).

IV. Conclusions

The use of BSIM-IMG compact model parameters to capture the HCI degradation on a 22FDX™ FDSOI NMOSFET, including RF small-signal performance degradation, has been presented.

First, different combinations of model card parameters were used to reproduce the measured degradation of DC FOMs. It was demonstrated that an accurate modeling of the DC degradation can partially represent the RF performance degradation, as previously reported. Furthermore, it was shown that it is possible to improve the modeling of the RF

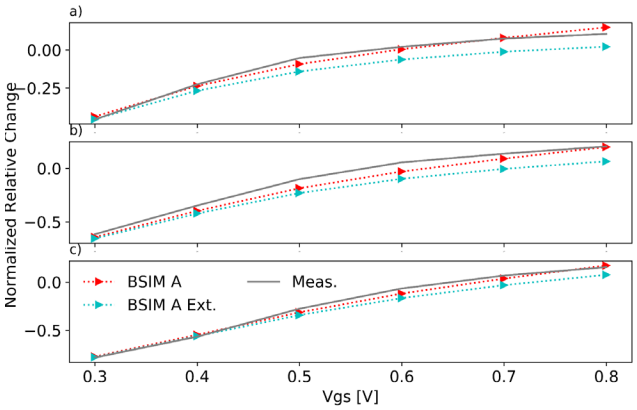

Fig. 10. Simulated and measured relative change in FMAX after 10^4s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V. Simulation results before and after extending combination BSIM A with a fixed RDWMIN for each stress voltage.

degradation by using the extension drain resistance R_D within BSIM-IMG, without adding external elements in the netlist In this paper we explor e the usage of an R_D for each stress condition at a fixed operating point. Accurate modeling of the complete RF performance under different operating and stress conditions is a complex task, making further extensions of the model necessary.

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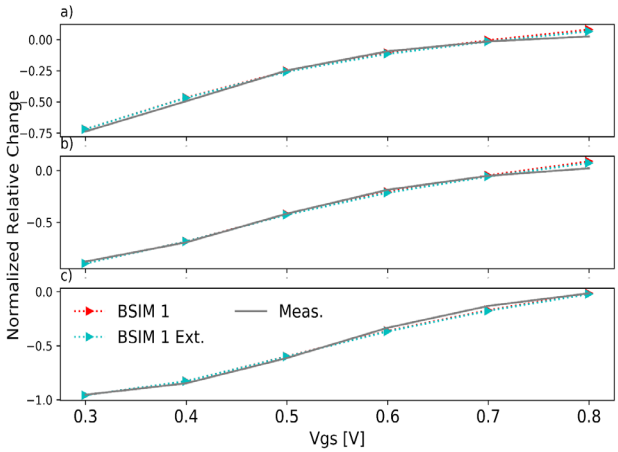

Fig. 11. Simulated and measured relative change in Gm_{ac} after 10^4s stress time for different V_{GS} (Saturation). Stress voltages: a) 1.2, b) 1.25 and c) 1.3 V. Simulation results before and after extending combination BSIM A with a fixed RDWMIN for each stress voltage

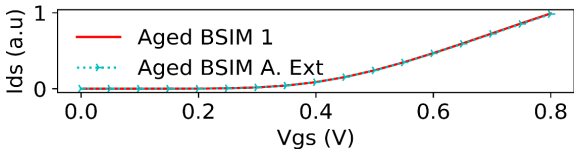

Fig. 12. Simulated Aged Ids in saturation with and without the use of R_D. Stress voltage 1.2 V.

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