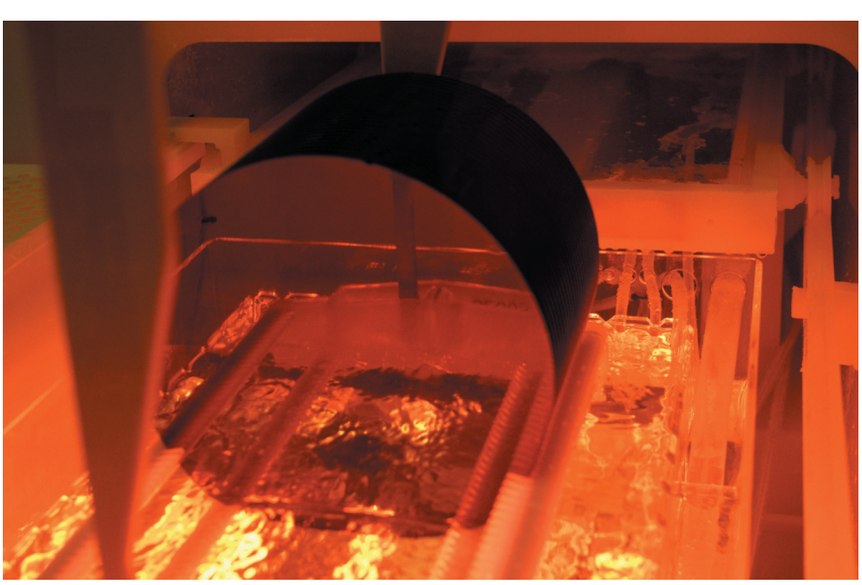
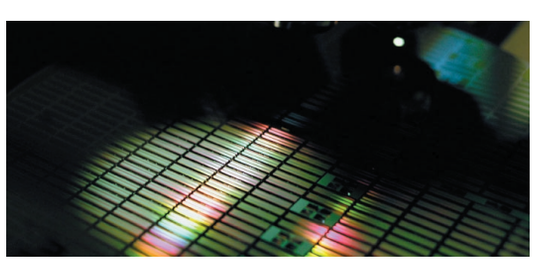
IMS

Fraunhofer Institut
Mikroelektronische
Schaltungen und Systeme

Annual Report 2004





Annual Report of the
Fraunhofer-Institut
für Mikroelektronische
Schaltungen und Systeme IMS
Duisburg
2004

Preface

The 20th year of IMS has opened new gateways for our future on the one hand side, and it has been a summit of results achieved on the other hand side.

Revenues from industry of more than 50 % of our budget, resulting in more than 7,5 MEUR, this is one of our three best results in all the 20 years. The CMOS production for our customers made by far the biggest contribution to this.

Our enlargement building of 1500 square meters utilizable floor space has been structurally completed; important for our production throughput is the ground floor with parameter test and circuit test labs and assembly and mounting cleanroom. In our central court the basement of the multipurpose conference and assembly hall has been finished. It will be surrounded by kitchen facilities for the needs of our employees and visitors. So, next year, our site will be well filled with buildings those give us possibilities for new activities for the demands of the future.

During 2004 our CMOS-Line, after the big investment in new equipment in 2003, was switched over from 6" to 8" wafer production. So our customers now profit from the more rational way of our production, leading to shorter delivery terms, and from new processes installed. The actual throughput of about 8000 waferstarts per year is expected to be increased considerably during the next two years.

Our successful "inHaus" (intelligent building) activities led to a subsequential project "Smart Living NRW", where 600 flats shall be equipped with these new technologies. On the other hand side, we put effort on the stimulation of a big internal project "GAIN" that helps to find fast solutions by novel inter departmental cooperation.

In December, the common "Professor Appointment Committee of Universität Duisburg-Essen" and Fraunhofer decided in a common list for the position "Director of IMS". We hope that this will lead to the result that, from October 2005 on, the new director will guarantee the continuity of IMS after retirement of the actual director for our customers and our employees.

In this year we have all reasons to thank our customers and the public authorities for their continuous confidence. We also thank our employees for their never falling effort, care and curiosity in our new fields and tasks. All our activities are directed at reinforcing the competitive strength of our customers in their relative region and market segment by developing technological innovations and system solutions with Microelectronics, Microsensors, Wireless Chips and distributed Systems; this will further be supported by related research activities.

Günter Zimmer
(Director of IMS)

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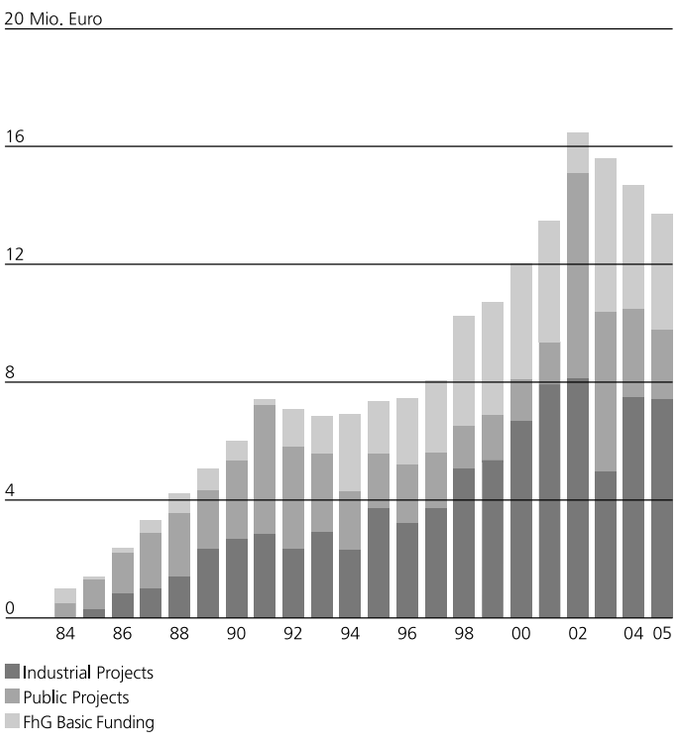

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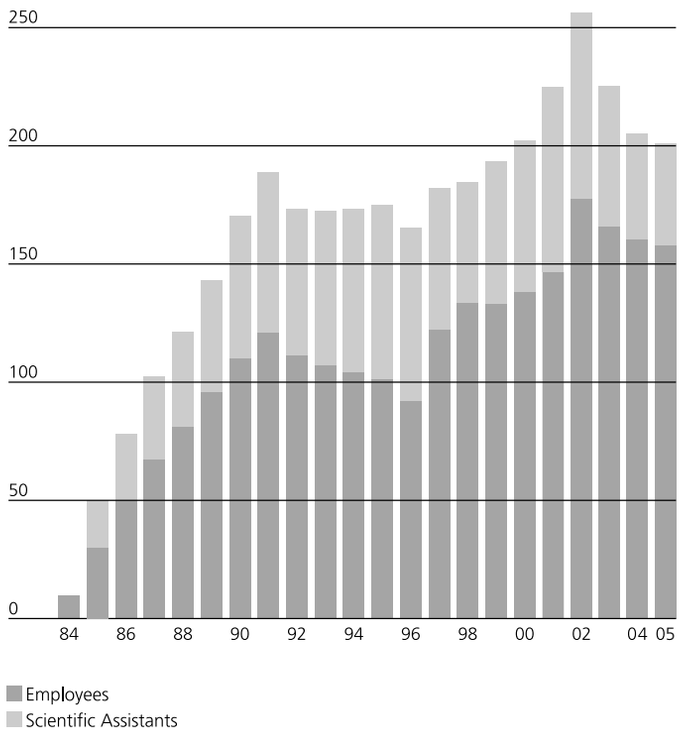

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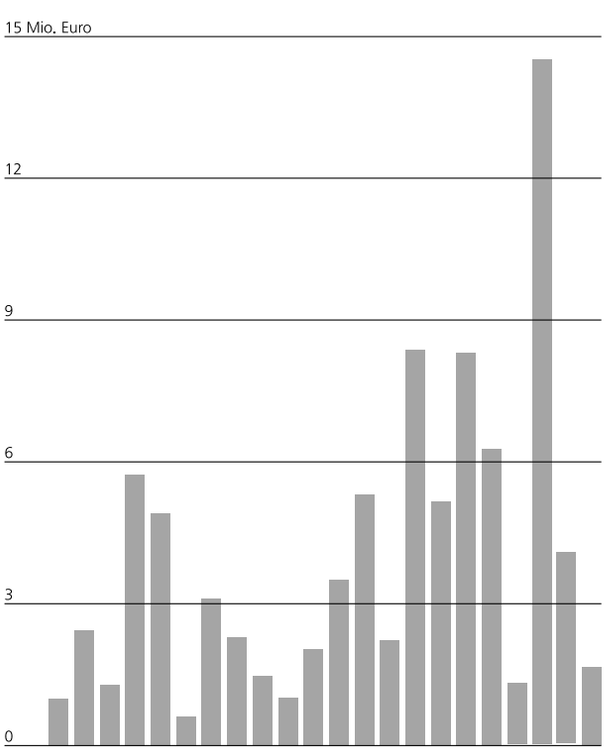

Selected Projects of the Year 2004

200 mm Conversion of IMS Fab Completed

H. Vogt, K. Debusmann, H. Awater, S. Weyers

Modern microelectronics has progressed at high pace. Feature size is becoming smaller and smaller, wafer size increases. To retain compatibility and to provide modern equipment and facilities to our customers for process development and device fabrication, IMS had decided to upgrade its semiconductor factory towards 0.25/0.18 µm capability and 200 mm diameter wafers. These plans were fostered by the fact that many of the IMS customers in the semiconductor industry have already switched their fabs to 200 mm or are in the final planning stages to do so. Modern semiconductor equipment no longer supports 150 mm wafers, thus further pushing the conversion plans.

In the semiconductor industry large high volume manufacturers now open 300 mm wafers fabs. Therefore we had carefully to consider if the 200 mm conversion has adequate future potential. Application specific design and processing, automotive electronics with it's highly specialised medium volume products, power electronics and many other applications will take the optimum advantage of 200 mm fabs for long time to come. The integration of sensors and actuators with CMOS on these wafers even today poses a challenge. Thus 200 mm factories are going to have a long lasting potential.

A first milestone has been achieved at IMS in 2002 with the opening of the cleanroom extension building, which provides a high quality environment for the IMS CMOS activities. The then existing cleanroom was upgraded, new supporting facilities installed (ultra pure water, air conditioning, chemical and waste management, and others). IMS now uses about 1000 m^2 of cleanroom floor space with all front end and backend facilities required.

In 2002 a new project was launched, funded by BMBF, European Union and the State Government of Northrhein-Westfalia, to convert the IMS facility from 150 mm wafers to 200 mm wafers. We selected the equipment suitable for 0.18 µm processing, taking into account new but also high quality refurbished machines. Thus we achieved a very cost efficient toolset. Equipment hook-up took place in 2003, in parallel to the running 150 mm factory. Figure 1 shows the resulting clean room floor plan with the major machine tool groups. A few examples are highlighted in the following: Chemical mechanical polishing is available for shallow trench isolation and the Al and W based multilevel metal system. Wet cleaning comprises of fully automated bath processors as well as single cassette spray tools. Implanters cover medium and high ion currents. The lithography includes i-line and 248 nm excimer laser steppers. For high temperature processing we use horizontal and vertical furnaces as well as rapid thermal annealing. Deposition and plasma etching processes apply single wafer cluster tools.

Process step and process installation commenced in the fourth quarter of

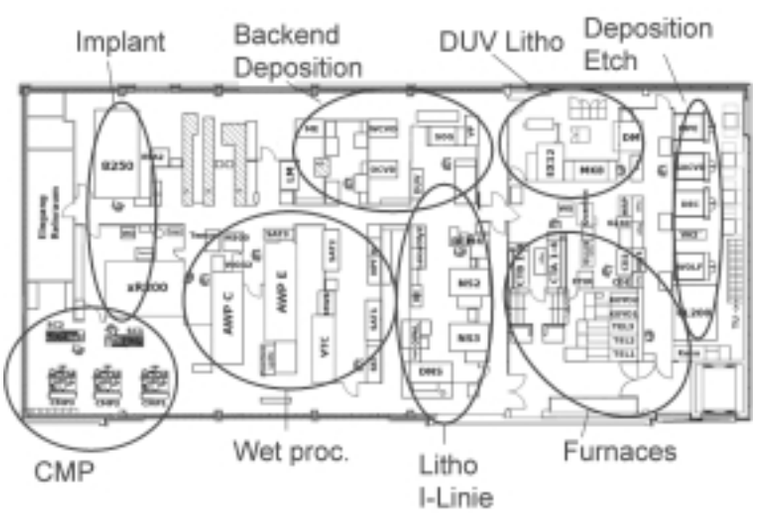

Figure 1: Cleanroom at IMS

2003. Parallel to the ongoing 150 mm activities we ramped up the new tools with 200 mm wafers (Figure 2). The goal was to have as many process steps ready before switching the whole fab to the new wafer size. Thus we presented the first 200 mm wafer with complete MOS processing and functional devices in February 2004. A few process steps (e.g. metal sputtering) were obtained from fabs outside, but most of the process step necessary in a CMOS flow were available during summer 2004 when the switchover was due. Based on the already available finished lots parameters were chosen to preprocess wafer lots until the metal backend waiting for the machine conversion.

150 mm processing finished mid of July with the delivery of the final wafers to our customers. To prevent any delivery shortcuts, some devices had been produced on stock for later delivery. Immediately we began the hardware conversion of the remaining tools (implanter, wafer stepper and others) to allow 200 mm wafer handling. The final new 200 mm equipment, a sputtering cluster tool, was moved into the cleanroom end of July. Thus the conversion of the whole fab took place without any factory downtime. New lots were started continuously, the preprocessed wafers were finished when the sputtering machine was ready for process.

Since August 2004 the "new" factory is up and running. All process steps are installed. CMOS processes ranging from a 1.2 µm robust, automotive proven CMOS process over 0.8 µm to 0.6 µm have been transferred. Qualification of selected devices has begun. In parallel, with the availability of the 200 mm equipment, we have started the development and installation of a 0.25 µm CMOS process. First silicon is due in the final quarter of 2004.

Figure 2: 200 mm wafer processing

High Temperature CMOS on SOI for Harsh Environments

U. Paschen

Introduction

Many modern applications for integrated circuits and systems are characterized by an increasing demand for high temperature capability. While standard CMOS devices are able to operate at temperatures up to about 125 °C (and with reduced performance and reliability up to about 150 °C) many interesting harsh environment fields can only be addressed with circuits working at significantly higher temperatures. These fields include, for example, the automotive industry, aviation and space technology, chemistry, oil drilling and geophysical exploration. In order to satisfy the demands in these important markets IMS develops a high temperature CMOS process that is able to operate at temperatures up to 250 °C.

Process

The main reason for the limitations of standard CMOS processes with regard to high temperature operation is the increase of the leakage currents of the pn-junctions in the devices (see Figure 1). At temperatures above around 125 °C these leakage currents reach values that are detrimental for the circuit performance and in the end lead to malfunctions. In addition to the increase of the leakage currents the metallization, which is made of Aluminum in standard CMOS processes, poses severe reliability risks at high temperatures. High current density levels lead to material transport in the metal wires of an integrated circuit. This phenomenon, which is called electromigration, increases exponentially with increasing temperature and thus can lead to premature failure of the metal lines through interruption.

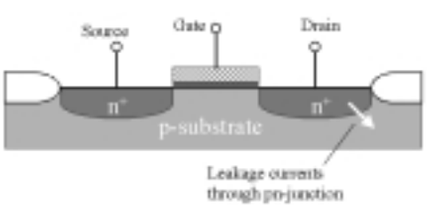

Figure 1: Schematic cross section of an NMOS transistor in a standard CMOS process. Note the large pn-junction areas responsible for excessive leakage currents at high temperatures

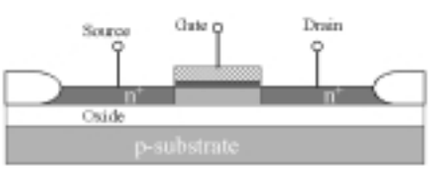

Figure 2: Schematic cross section of an NMOS transistor in a high temperature CMOS process based on SOI substrates

Figure 2 shows the principal cross section of the process employed at IMS to realize the high tempertature CMOS process. The process is based on silicon on insulator (SOI) wafer material. Here a thin silicon film (around 120 nm thick) is separated from the bulk wafer by an oxide layer. The devices are realized within this thin silicon film. Therefore, the devices are dielectrically isolated from the bulk of the wafer and the total pn-junction areas (and consequently the leakage currents) are dramatically decreased, enabling operation at temperatures far beyond the limit of standard CMOS devices. In addition, we employ tungsten as the material for wiring in this process because the electromigration stability of this element at high temperatures is much better than for Aluminum. This ensures long time stability and reliability of the devices with regard to electromigration.

Besides the standard active and passive devices this process also features several interesting add-ons. For advanced analog and mixed signal design voltage independent capacitors are provided. Also a reprogrammable non volatile memory (EEPROM) is available for storage of data. This is a very important feature for all applications where sensors are involved, because it enables the storage of calibration data on the chip. As an example the chip photo of a 32 kBit high temperature EEPROM is shown in Figure 3. Special circuit design and layout of the EEPROM cell ensure proper function and long time data retention even at 250 °C. The process also features an integrated pressure sensor, which is fully compatible with all the CMOS fabrication steps. Thus, the sensor can be integrated together with electronics for signal conditioning and processing (linearisation and temperature compensation of the sensor signal, AD-conversion, bus functionality, ...) on one chip. In addition to reduced packaging volume and cost this also ensures very short signal paths, thus increasing accuracy and immunity

to electrical noise in harsh environments. A chip photo of an integrated pressure sensor is depicted in Figure 4.

The process is currently under development, first lots have already been fabricated. Process qualification will take place in the second half of 2005. Since bare dies can only in very few cases be directly used in applications IMS in parallel to the process development also develops packaging solutions for the integrated circuits and pressure sensors for high temperature applications.

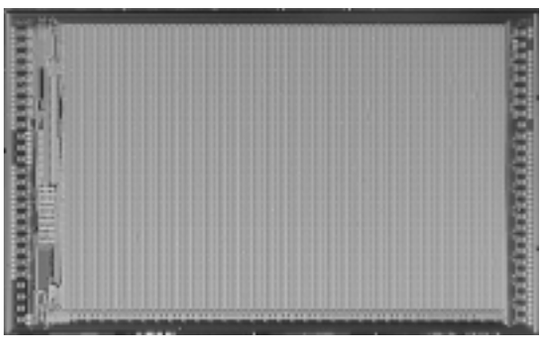

Figure 3: Chip photo of a 32 kBit high temperature EEPROM

Summary

A high temperature CMOS process is currently being developed at IMS for operation at temperatures up to 250 °C. The process offers full capability for analog and mixed signal design. It also features reprogrammable nonvolatile memories (EEPROM) and an integrated pressure sensor. Currently only very few companies worldwide are able to realize high temperature electronics for this temperature range. None, however, offers nonvolatile memory or integrated sensors, which makes the process a unique selling point.

Figure 4: Chip photo of an integrated high temperature pressure sensor

Sensors and Actuators for Micro Reactor Application

H. K. Trieu

Introduction

Experts in industry and universities have discussed microreaction technology for several years. The advantages of this technology are well known. The first important step in the beneficial use of microreaction technology for the chemical and pharmaceutical industries is the development of suitable microfluidic components. These components might be used for mixing/separation, heating/cooling or heat exchange. But there are only few real applications in industrial production. One of the reasons for this is that besides the microfluidic structure a lot of peripheral equipment as known in process controlling for conventional chemical reactors is also needed to run such a microreactor under controlled condition. Most of these control electronics on the microscale are still not commercially available for microreactors. This report describes how microelectronic and microsystem technology will be used to manufacture monolithically integrated sensors/actuators for use in microreaction systems. Thus, a simplification of the whole system is gained by using the silicon chips for measurement of temperature, flow, pressure, concentration, for heating or cooling and for system regulation and controlling.

Microreactor

Microreactors are miniaturized reaction systems containing one or more reaction channels with sub-millimeter dimensions. Figure 1 gives an idea

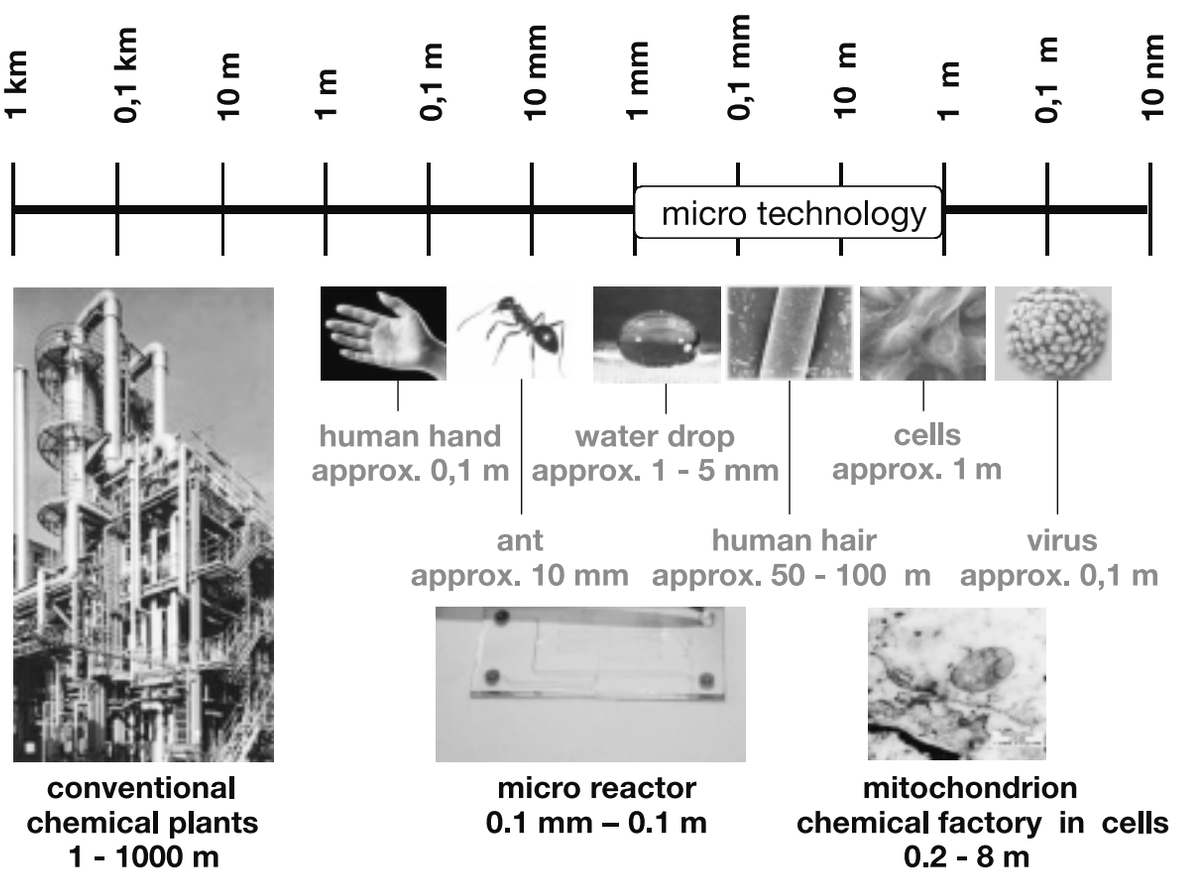

Figure 1: Comparison of geometrical dimension of chemical reactors

about the geometrical dimension of microreactors in comparison to conventional chemical plants. Microreactors may contain micromixers, micro heat exchanger and/or micro separation system. Catalysts may also be coated on the surface of the reaction channels.

Microreactors have many advantages when compared to traditional production procedures:

1) By performing reactions in micrometer channels, very efficient mass and heat exchange processes will take place, due to miniaturisation. Reactions can be performed in a fraction of the traditional reaction times. Side reactions will be suppressed, which will result in an increase in selectivity.

2) The high levels of control, as well as the application of small reaction volumes will result in a much safer use of inherently toxic or explosive compounds.

3) Because a multitude of reaction channels and connections can be assembled on an integrated circuit, a change in reaction conditions can be applied very quickly. This results in a very flexible production process.

4) Besides the flexibility in reaction conditions, microreactors are also very well suited for performing combinatorial chemistry, via parallel synthetic procedures.

5) An increase in production volume from synthesis in a research environment to production scale can be carried out with microreactors by a scaling out procedure. Using an array of parallel operating chips, there is no need for extensive pilot plant studies. An increase in production volume is easily achieved by an increase in number of microreactors.

6) The high level of dimensional control on (sub) micron scale allows very well defined production of micrometer-sized morphologies, as applied in e.g. food textures.

Sensors and Actuators for Process Controlling in Microreactors

In chemical reaction technology process controlling is a key technology enabling chemical processes to run under controlled and regulated conditions. Sensors are needed for the acquisition of process parameters like temperature, pressure, flow or pH value. Also, detection of conductivity or concentration of the chemical species are necessary to determined the reaction yield. Controllers process the acquired data and

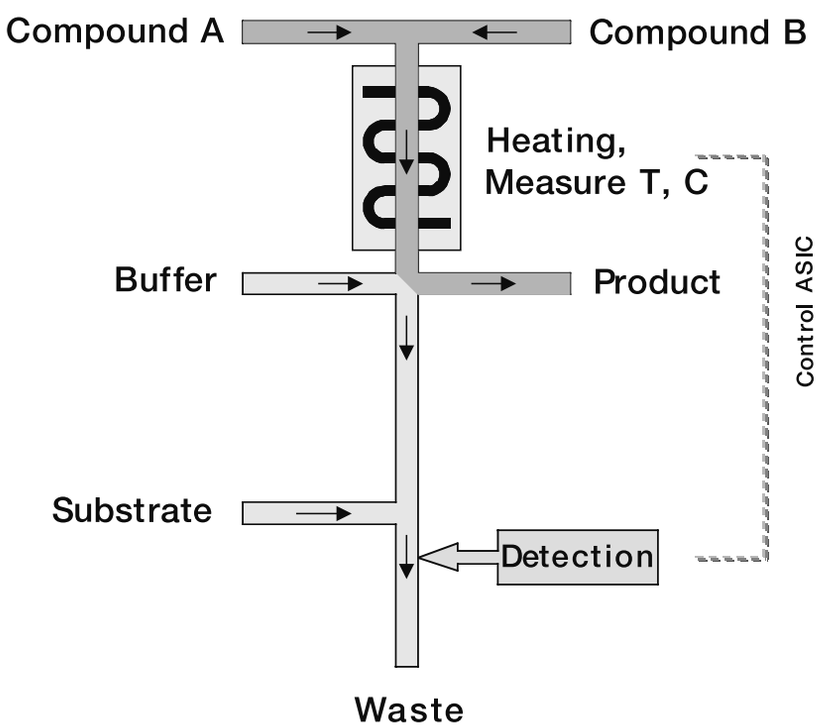

Figure 2: Principle of a closed loop controlled microreactor

regulate the process parameters by actuators like heater (e.g. resistor), cooler (e.g. peltier element), pumps and valves in a closed loop as depicted schematically in figure 2.

For microreactors with typical feature size of the microchannels in the sub-millimeter regime dedicated miniaturized sensors and actuators are needed. Such devices can be realized with microsystem technology. IMS has developed a portfolio of such micro devices in the two decades since its foundation. Integrated pressure sensors fabricated in surface micromachining cover a broad pressure range from ambient pressure up to 300 bar. Temperature sensors in CMOS are integrated on-chip. Thermal flow sensor has been developed. Gas sensors for hydrogen detection has been realized. PH sensor and amperometric devices for detection of dissolved oxygen in liquid or other redox species have been fabricated. Image sensors are also available. IMS has a strong expertise on mixed signal ASIC development. Figure 3 shows some examples of the devices. For their application in the microreactor environment the devices have to be adapted in the layout in order to fit into the dedicated packages and assembly technology. Redesign also might be necessary to meet the dedicated specification of the applications.

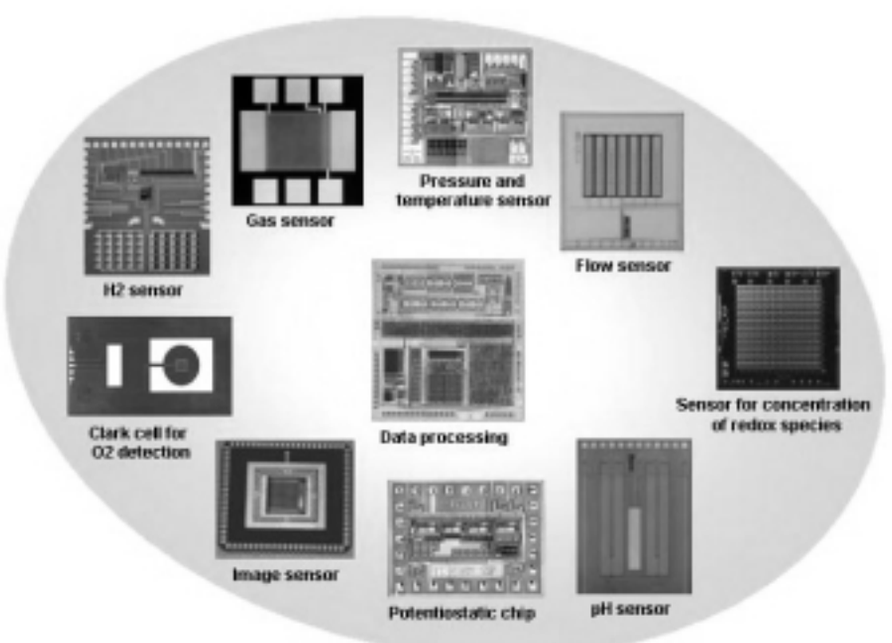

Figure 3: Examples of micro devices suitable for process control

The Euregio Microreactor Project

Ministerie van Economische Zaken

euregio

NRW.

The Euregio Microreactor Consortium is tackling the above described challenge to integrate microsensors and actuators into a microreactor environment. The Euregio Microreactor Project is a collaboration between the universities of Wageningen and Radboud University Nijmegen and the Fraunhofer Institut in Duisburg, which are located within close proximity of each other and have ample expertise in the field of food technology, molecular synthesis and microelectronics, respectively. The Euregio initiative is combining existing technology and expertise within these three partners to develop a versatile, miniaturised processing device prototype, which will be of great value to stimulate the commercialisation of integrated microreactor systems, resulting in a strong economic impulse to the area. The financial support of the project by the Euregio Rhine-Waal is strongly acknowledged by the consortium. The project is started in July 2003 and has a duration of 4 years. The project is cofinanced by the EU-program INTERREG IIIA of the Euregio Rhine-Waal and the ministeries of economic affairs of the Netherlands and NRW.

CMOS Sensor for 3D Imaging

O.Schrey, O. Elkhalili, W. Brockherde

Keywords: 3D, Image Sensor, CMOS Photo Sensor, Multiple Double Short Time Integration (MDSI), Pixel Array

Introduction

Machine vision represents one of the most important imaging applications. Three-dimensional (3D) imaging is essential for highly reliable object recognition and indispensable for measuring distance, shape, and volume of objects. Classical 3D imaging is based on time-of-flight (TOF) method but it is slow, bulky, and expensive because it requires rotating mechanical mirrors for 3D-scanning. Other methods, like model-based object recognition and stereoscopic vision are troublesome and unsatisfactory. Our TOF method is based on a pulsed laser source operating in the near-infrared (NIR) range which is widespread to illuminate the entire scene and thus avoids any mechanical scanning. In this way the TOF systems become smaller, cheaper, simpler to realize, and yield 3D images in real time.

In this communication we present a 3D TOF sensor chip realized in 0.5 µm n-well standard CMOS process with on-chip signal processing. First of all the TOF method will be briefly explained. Then, the 3D pixel circuit will be presented. After that, the realized chip will be described, and finally, some experimental results will be demonstrated.

Distance Measurement with TOF Principle

Figure 1 shows the measurement principle of the TOF method employed. A few nanoseconds long light pulse generated by an NIR laser diode and defocused by diffractive optics illuminates the entire field of view. The image depth is determined by measuring the time delay elapsed between the emitted light pulse and its reflection by a distant object in the scene [1]. There is also a possibility to employ a continuous-wave modulation instead of the pulse modulation [2,3]. The phase shift between the emitted and reflected waves then yields the distance measure.

The fundamental problem of all optical TOF approaches is the effect of background illumination, because in practice it imposes heavy demands on the input irradiance range of the TOF detector. Here the pulse modulation is superior to the continuous-wave modulation because it can use very short pulses exhibiting high optical power. Then the pulse irradiance is much higher than the background irradiance (thus making the pulse detection easier), while the amount of the emitted laser energy remains low (thus ensuring eye safety). Also, the pulse modulation does not suffer from any ambiguity problems. Nevertheless it requires broadband photdetectors and electronics, which makes their design to be quite a challenging task.

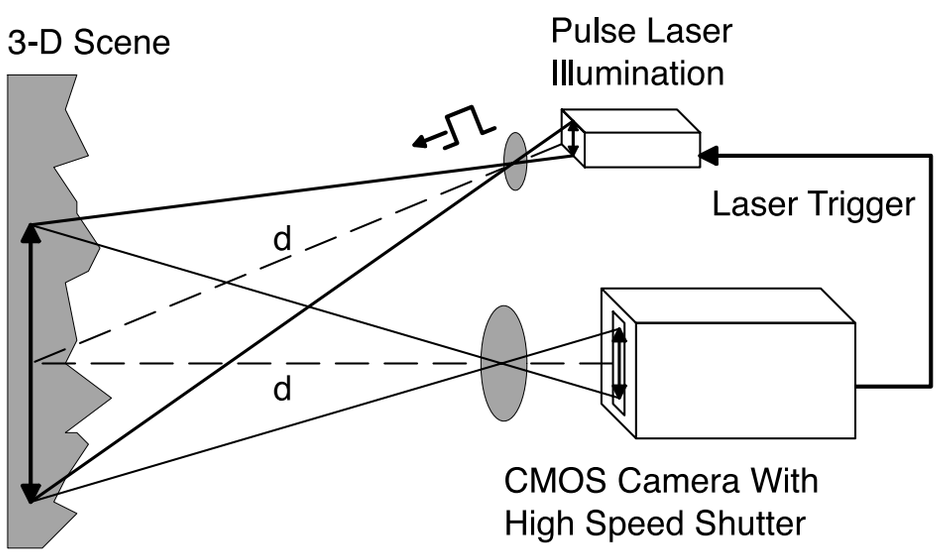

Figure 1: 3D measurement principle

So far we have described just a one-dimensional TOF measurement. This can be, however, easily extended to two- or three-dimensional measurements simply by using array detectors. Thus, to realize such arrays all we have to do is to design extremely fast array imagers.

Pixel Circuit description

Figure 2 shows the pixel circuit schematic of the fast 3D image sensor. The pixel contains a photodiode PD operating in the reverse-bias mode. The operation can be described as follows: the photodiode capacitance C_D and the storage capacitor C_{Sx} are periodically charged to the reference voltage V_{REF1} by activating the reset switch M_1 and the shutter switch M_4. After opening the reset switch M_1 the discharge of capacitances C_D and C_{Sx} starts due to the photocurrent of the photodiode PD generated by the incident light. Deactivating the shutter switch M_4 stops the discharge process at C_{Sx} and thus enables the integration time control. The remaining voltage stored at C_{Sx} is read out and stored at a second capacitor C_{Hx} which acts as a hold capacitor. The voltage values being stored at C_{Hx} are read out using the correlated double sampling (CDS) stage by activating the select switch M_3. Meanwhile, the acquisition of the next value at C_{Sx} is performed, so that this architecture yields zero-dead-time. The switch M_3 also enables multiplex operation of the CDS stage that is shared between two pixel circuits. Note that in order to save power dissipation the bias currents I_{bias1} and I_{bias2} of the source followers SF1 and SF2, respectively, are controlled (they are increased for image acquisition and reduced in the stand-by mode).

In the actual implementation of the pixel circuit we have added switches and extra logic to enable binning (see Figure 2).

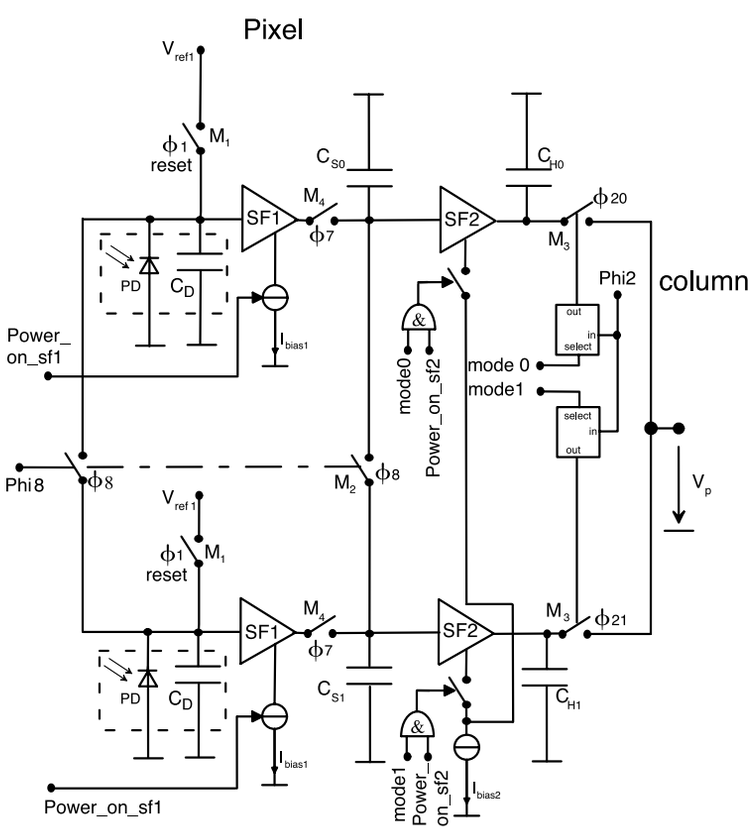

Figure 2: Double 3D pixel circuit with synchronous shutter

CDS Readout

The CDS stage (see Figure 3) serves to amplify the useful signal, to cancel all offset and 1/f-noise voltages, and suppress the effect of background illumination. Because each CDS stage is multiplexed, an analog memory has been added to store the signals. The operation can be described as follows: according to the selected row of the pixel matrix, the sampling capacitance C_{Cl} is charged to the output pixel voltage V_p of the selected pixel available at C_{Hx} plus all offset and noise voltages (ϕ_3 and ϕ_5 are ON, ϕ_{4x} is OFF): this is the "signal sampling" cycle. In the reset phase, V_p containing the reset voltage of the pixel plus all offset and noise

voltages is sampled at C_{CI}, which is the "reset sampling" cycle. The charge difference between the two cycles is now transferred to the corresponding storage capacitor C_{Fx} of the analog memory (Φ_3 and Φ_5 are OFF, one-of-N Φ_{4x} is ON). The result is available as an output voltage V_F free of all offsets, independent of the reset voltage, and with suppressed 1/f-noise.

The suppression of the background illumination requires two measurements: one with a light pulse being fired by the laser source and one measurement without a light pulse, but with identical timing. For a slowly varying background illumination the subtraction of both measurements cancels its effect.

Unfortunately, besides the dependence on pulse travel time the voltage V_F is also dependent on the laser power and the object reflectance. This can be again eliminated using two measurements. Consider the timing diagram in Figure 4 for two light pulses at two different shutter times (T_1 and T_2) but an identical pulse arrival time T_0 and the same pulse width T_{pulse}. The first measurement is performed by using $T_1 = T_{pulse}$, with T_1 the active time of M_4 and T_{pulse} the duration of the laser pulse. As an example, the output voltage of the CDS stage at the time T_1 is V_{F1} (see Figure 4). In a second cycle this measurement is repeated at a different integration time T_2, with T_2 now greatly exceeding Tpulse. This time we obtain V_{F2} at T_2. This means that the complete reflected laser energy is located within the shutter window. Finally, the quotient between V_{F1} , V_{F2} is being computed off-chip in the camera system thus yielding a responsivity- and reflectance-free magnitude. The time T_{travel} elapsed between the emission and reception of the pulse at pixel no. x (i.e. $T_{travel,\,x}$) depends on the travel distance as $T_{travel,\,x} = 2\,v_c/d_x$, where v_c is the velocity of light. The quotient in Eq. (1) now represents the distance of the object point d_x [5, 6]:

$$d_x = \frac{v_C}{2} \cdot T_{pulse} \cdot \left(1 - \frac{V_{F1,x}}{V_{F2,x}}\right) \qquad (1)$$

From Eq. (1) follows that when T_{pulse} = 30 ns the maximum range to be measured is 4.5 m. However, if there is a variable delay between the firing of the laser and the opening of the shutter then the range can be extended. Optionally, each of the two measurement cycles may be repeated n times using laser pulse bursts. The resulting voltages are accumulated in the analog memory of the CDS stage when operating in accumulation mode: this is called multiple double short time integration (MDSI). This increases the signal-to-noise ratio by sqrt (n) and extends the sensor dynamic range by increasing the range resolution also by sqrt (n). All control signals are synchronized using on-chip flip-flops.

Chip Architecture

Figure 5 shows the architecture of the realized 3D CMOS imager. The CMOS image sensor contains 2 x 64 photo detector lines containing the double pixel structure shown in Figure 2. The design is mirrored at the horizontal symmetry axis of the pixel array. Both sides of the pixel have an H-tree clock synchronization circuit in order to minimize clock skew for the shutter and reset signals in the horizontal direction.

The CDS stages are located at the bottom of each column and on both sides of the pixel array. The readout of the analog CDS memory is carried out by a column parallel shift register operating at 5 MHz pixel clock. A line multiplexer performs the selection between the four 64 pixel lines, i.e. 2 double pixel

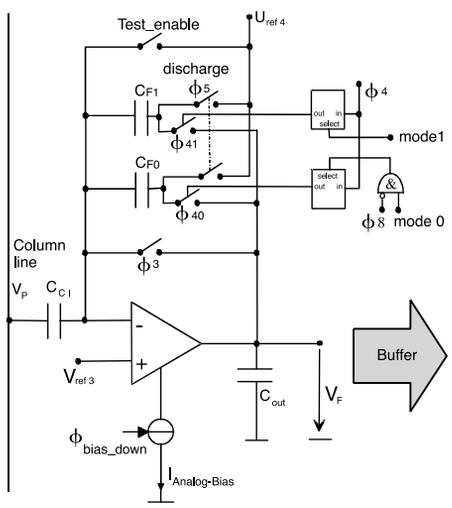

Figure 3: CDS stage and analog memory

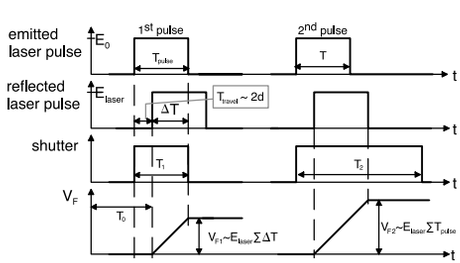

Figure 4: Timing diagram

Figure 6: Chip microphotograph

lines. The sensor can be operated in two modes: the binning mode (mode 0 and mode 1 are activated), where the twin pixels (see Figure 2) are short-circuited, and the high-resolution mode (either mode0 or mode1 is activated). The switching sequence of mode [1] and mode[0] determines the row that is read out. Signal mode [0] selects pixel no. 0....64 and mode [1] selects number 64....127. Since the photodiodes of 2 adjacent lines are shifted by half a pixel pitch, the lateral resolution in horizontal direction can be increased by alternate readout of two lines. In this case, mode [1] and mode [0] permanently change between addressing the lower and upper pixels (see also Figure 3), thus yielding the sequence: PD00, PD64, PD01, PD65... (see Figure 5).

In normal resolution mode, the sequence is: PD00, PD01, PD02,...., PD127.

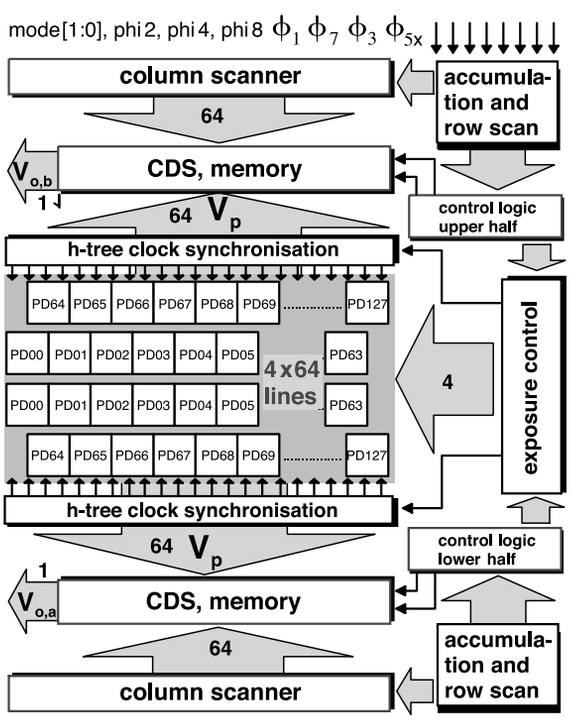

Figure 5: Chip architecture

Moreover, the sensor is capable of binning two lines of either sensor half by applying mode 0, mode 1 and phi8 = "HIGH". All multiplexers are designed as shift registers in order to save chip area and keep their design as regular as possible, which minimizes run time effects, such as the critical clock skew.

Experimental Results

Figure 6 shows the microphotograph of the realized CMOS image sensor. The sensor has been fabricated in a standard 0.5 µm CMOS process and it occupies an area of 58.3 mm^2. Technical data of the imager are summarized in Table 1.

Figure 7 shows the measurement of the responsivity and the Noise Equivalent Power (NEP) which represents the input-referred noise-equivalent irradiance and is about 4.1 W/m^2 at 30 nsec shutter speed. NEP is essential in determining the depth resolution.

The sensor presented has been developed for automatic door control but it can serve in numerous other applications, such as person counting, automotive etc.

Conclusion

A 4 x 64 pixel 3D CMOS imager based on time-of-flight (TOF) has been developed and successfully tested. The measurement range is up to 8 m with resolution of 1 cm. The scene depth is determined by measurement of the travel time of reflected laser pulses by employing a fast on-chip synchronous shutter (max. shutter speed 30 ns). "Multiple Double Short Time Integration" (MDSI) algorithm enables suppres-

sion of the background illumination and correction for reflectance variations in the scene objects. The pixel size is 130 x 300 µm². The sensor chip has been realized in the 0.5 µm n-well standard CMOS process of Fraunhofer IMS. A brief discussion of existing technologies and different approaches to 3D imaging clearly shows the advantages of our approach.

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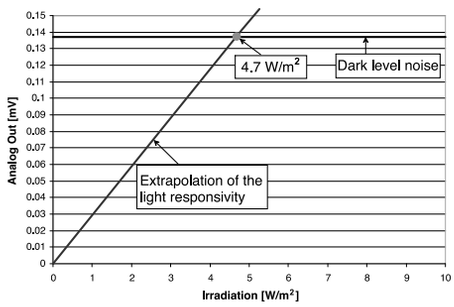

Figure 7: Responsivity and NEP Measurement

Parameter	Data
Pixel count	4 x 64
Pixel geometry	130 x 300 µm²
Pixel principle	linear
Power dissipation @ 3.3 V	350 mW
Max. shutter speed	30 ns
Laser Power*	200 W
Laser wavelength	850–910 nm
Measurement range **	≤ 8 m
Range resolution (1 pulse)	< 5 cm
Range res. in burst mode (100 pulses)	< 1 cm
Max. clock skew	< 200 psec
NEP @ 30 nsec shutter speed	4.1 W/m²
Dynamic range	80 dB
Linearity	< 5 %
Max. frame rate (sync clock 66 MHz)	19500 fps
Frame rate @ 100 pulses	195 fps
Pixel clock	5 MHz

* f = 4 mm; f# = 1; Object reflectance = 0.1; Fill factor = 100 %
** with delayed pulse

Table 1: Electrical parameters of the image sensor

CMOS X-Ray Image Sensor for C.T. Application

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Introduction

Currently computer tomography (C.T.) detectors are built of discrete electronics and 2D photodiode arrays with external readout electronics [1, 2]. To reduce the board module complexity, to increase the SNR, and to enhance the functionality of C.T. detectors, an integration of electronics and photosensor array in a single device is required. A CMOS integration has been proven in several imaging applications to be the most cost effective way for the integration of such active pixel sensors (APS). Nonetheless, the photodiodes in standard CMOS cannot be particularly optimized with respect to their sensitivity due to fixed processing step sequence. However, CMOS circuits offer a wide variety of noise reduction techniques. Low noise is extremely important, because it defines minimum detectable irradiance.

1 X-Ray Detector Module

The x-ray detector presented here is based on an indirect conversion principle, which means that the incident x-ray photons are converted by a scintillator crystal to photons of visible light. These photons are detected by a CMOS active pixel image sensor and converted into an electrical charge. The sensor readout electronics converts this charge into an analogue output voltage. As can be seen in Figure 1 the scintillator crystal grid is glued on top of the CMOS image sensor chip in a way that its lead frame, which is intrinsically used to prevent optical cross talk in the scintillator crystal, also protects the readout electronics from x-ray radiation damage. This leads to heavy demands on the available chip area of the readout electronics, since the ratio of scintillator area to the lead and the spacer determines the fill factor of the detector which determines the radiation dose. Hence, the fill factor should be as large as possible. For the first prototype a fill factor of > 60 % was targeted.

Low Noise Redout Electronics

Low noise readout electronics is essential for artifact-free C.T. image capture. So far this is currently done by dedicated ASICs or current-mode ADCs which are designed for modular electronic approaches resulting in separate detector and readout chips. These ASICs are mostly serving for single channel only. The pixel readout electronics of the detector described in this communication is designed for multichannel low noise detection cointegrated with an on-chip photosensor array with significantly reduced cost per channel.

1.1 Pixel Readout Electronics

Due to the heavy requirements on linearity the use of OTA-based feedback integrators is mandatory. In standard integrator circuits the dynamic range of 17 bit is extremely difficult to be fulfilled unless an extremely large chip area is used.

In order to relax the requirements on the operational transconductance amplifier (OTA) the dynamic range is divided into two gain regions. Implementing a gain ratio of 32 the OTA dynamic range could be reduced by 5 bit down to 12 bit, which could be integrated on the chip area available in the area protected from the x-ray radiation underneath the lead frame. The analog signal is sampled by a sample and hold stage and read out in parallel with digital signal of the subsequent frame using the row and column multiplexer circuitry.

1.2 Low Dark Current, Low Capacitance Photodiode

To ensure maximum signal resolution and to maintain maximum dynamic range it is essential to reduce both, the capacitance and the dark current of the photodiode. As can be seen from a detailed noise analysis, the capacitance of the detector determines the reset and the OTA thermal noise which are the most dominating noise sources after the shot noise of the photodiode. It must be recalled however, that the photon noise and the dark current noise exhibit characteristics of a shot noise. Therefore, the goal was to design a low dark current and low capacitance photodiode. Both requirements can be achieved with a dot diode approach, where the pn-junction is formed by multiple dotsize pn-junctions connected in parallel. Here, the diode capacitance and the dark current are proportional to the area and the perimeter ratio of a dot diode. They are low when compared with a corresponding large area diode, if a large dot distance can be used, taken into account that the perimeter and area parameters of these diodes are different. For large area diodes the dominating charge transport mechanism is drift current because the photocurrent generated in the space charge region dominates. In dot diodes the pn-junctions are separated and the photocurrent is generated mainly off the space charge region. Hence, minority charge carrier diffusion is the dominating charge transport mechanism in this type of diode. With a loss of 1/3 in sensitivity a dot diode with a dot distance of 100 µm could be chosen. To reach the optimum sensitivity with a minimum detector capacitance, a hexagonal dot structure was chosen (see Figure 2).

A significant reduction in detector capacitance is the only way to fulfil the very restrict C.T. detector noise specifications. Therefore a photon noise limited photodetector has to exhibit a detector capacitance below 8.25 pF. In the case of a standard CMOS process this can only be achieved by the use of the dot type photodiode described above.

In comparison to standard CMOS large area photodiodes the dark current is significantly reduced by factor of 6 down to below 150 fA. This is due to the separation of diode junctions and the substrate contacts which reduces the electrical field nearly to zero.

1.3 X-ray Detector Module Design

As already stated above, the readout electronics has been designed for array operation. Each pixel consists of the integrator unit, the automatic gain control unit, a sample and hold unit and the row select switches for the multiplexer operation. All pixel circuits are connected columnwise to the combined digital and analog column multiplexer unit.

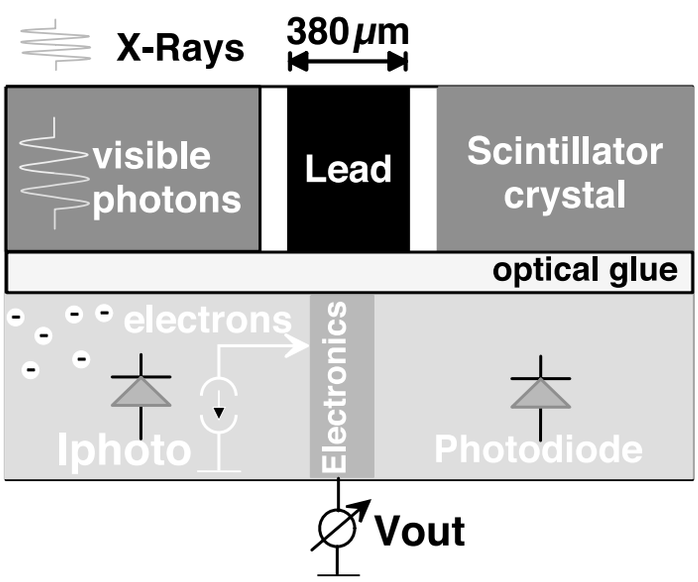

Figure 1: Cross section of x-ray detector module

In order to provide easy calibration procedures and to achieve individual temperature calibration capability, each x-ray detector chip contains a temperature sensor with a voltage output signal proportional to the absolute temperature (PTAT). In combination with a sample & hold stage with an amplification of 3 the output sensitivity is 3 mV/Kelvin. The temperature sensor sample & hold output signal can be read out with the same multiplexer schemes as the x-ray signal addressed as an additional row.

For the x-ray C.T. detector module prototype, the pixel circuit is arranged in a 20 columns and 10 row arrays with 1000 µm pixel pitch in x-direction and 1800 µm pixel pitch y-direction. Together with the central electronic unit consisting of the control unit, the multiplexing unit, the temperature sensor, and the readout buffers the pixel array has been integrated on single chip. The analog-to-digital signal conversion of all 200 channels is done externally with a standard 14 bit, 800 kS/s ADC. Compared with the single channel 20 bit current-mode analog to digital conversion used in competing designs, the use of a standard ADC significantly reduces the module price per channel. The latched digital gain setting signal is read out by the external digital interface with one frame delay together with digitized analog signal from the ADC, resulting in 17 bit dynamic range output signal.

2 Realization

The 20 x 10 pixel image sensor was physically designed with a 1000 µm horizontal and 1800 µm vertical pixel pitch. All signals are distributed column wise from the bottom of the chip to ensure a 3 side buttable detector concept. Together with the central electronic unit and ESD protection structures, this results in 20 mm x 20 mm CMOS image sensor.

The prototype, which can be seen in the photomicrograph in Figure 3, was manufactured using the FhG-IMS 1.2 µm CMOS process. Due to the very low metal layer density, special care was taken during metal processing to increase the metal processing reliability. Hence, significant improvement in yield figures could be achieved. Two of the CMOS image sensor chips are mounted with very high precision on a multilayer ceramic board together with the external circuitry which contains the two ADCs and the digital interface. As it can be seen from Figure 3 (b) the scintillator grid is glued on top of the image sensor chips, normally covering both sensor chips. For the complete C.T. scanner 48 modules are assembled on a high precision carrier, paying attention on constant pixel pitch to ensure an artifact free x-ray image sensing. All together this results in a three side seamless, low noise CMOS x-ray image detector with 96 cm x 4 cm of size.

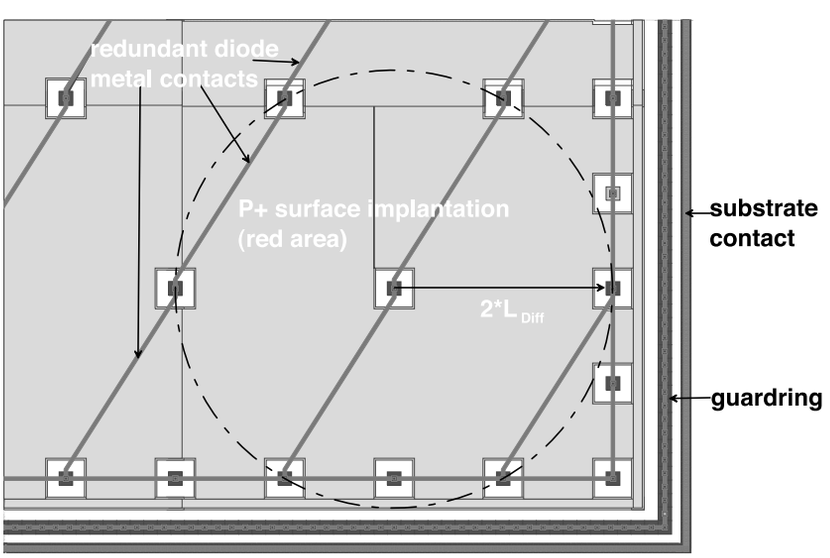

Figure 2: Hexagonal dot structure for low capacitance photodiode

3 Summary and Conclusion

The principle of an indirect CMOS x-ray image sensor has been demonstrated. The resulting specifications on the image sensor performance are very strict and an array integration of the readout electronics seems to be impossible with standard circuit concepts. A gain switching scheme has been developed, to ease the demands on the OTA design. The SNR and dynamic requirements are quite stringent and, therefore, intensive noise analysis has to be performed. Beside the fact that the OTA design could be improved, the most important outcome was that a very low capacitance photosensor element is required to achieve a photon noise limited system at low signal levels. By investigating the semiconductor physics of minority carrier lifetime and by experiential determination of diffusion length a hexagonal dot diode with a dot distance 100 µm have been developed. With a reduction of the capacitance value by a factor of 9 the sensitivity was reduced only by 30 % which ensures a photon noise limited operation. With this detector an array of 20 x 10 pixel and a pixel pitch of 1 mm by 1.8 mm respectively was designed and manufactured in the FhG-IMS 1.2 µm CMOS technology line. Measurements show that the photon noise limited operation could be fulfilled. A prototype based on the CMOS imager approach has been built by Philips Research Labs and will be extended to a full C.T. scanner with multislice operation.

This prototype of a large area, low noise CMOS photodetector for x-ray imaging in C.T. systems yields significant improvement in system integration and performance, compared to standard system designs. Further complex system integration with further improvements may be possible and seems to be feasible in CMOS technology. But the key issue of all concepts will be the noise performance. Hence, in our opinion the low capacitance photodetector based on dot diodes is the key to low noise large area photo sensing applications.

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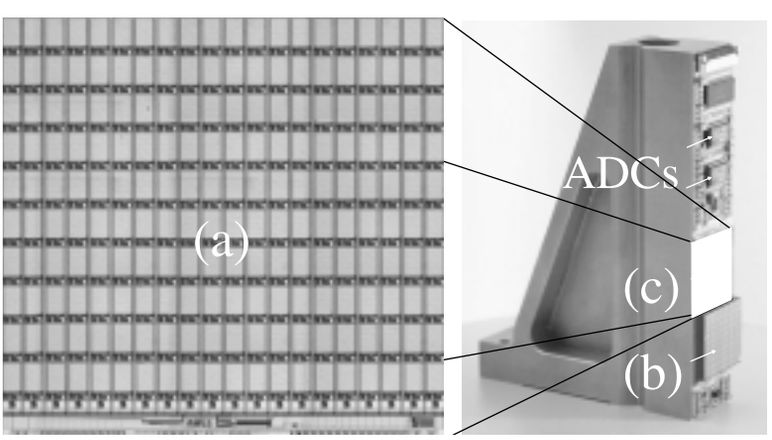

Figure 3: Chip and pixel micrograph of the 10 x 20 pixel array, 2 cm x 2 cm, 3 side buttable X-ray CMOS imager (a), prototype of CMOS-imager bases x-ray detector module with (b) and without scintillator crystal grid (c)

A/D-Conversion for Integrated Passive "Tire Pressure Monitor Systems" (TPMS)

D. Weiler, P. Fürst, J. Michael, T. van den Boom

Introduction

The main part of a "Tire Pressure Monitor System (TPMS)" besides the RF-interface and sensory part is the Analog/Digital converter (ADC). For passive transponder systems the overall power consumption is the main design criteria for the choice of ADC parameters like type, resolution, and sampling frequency. In domain of low power applications cyclic ADCs are commonly used.

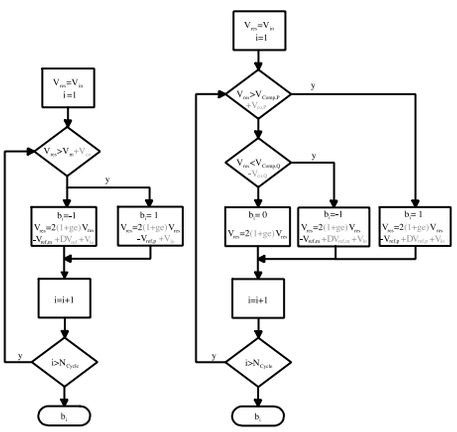

Figure 1: Algorithmic description of cyclic ADCs including error sources (a: cyclic CR ADC, b: cyclic RSD ADC)

Principle of Cyclic ADCs

Two main approaches of cyclic ADCs are known: First, a conventional restoring (CR), and second a redundant signed digit (RSD) ADC. The conversion results and the influence of possible errors sources can compared using two behavior models based on MATLAB simulations.

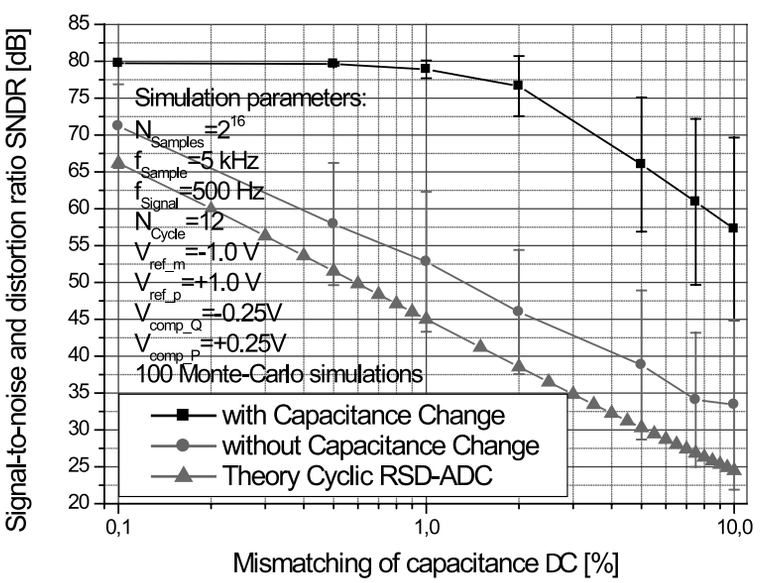

Figure 2: Influence of mismatching

The conversion principle of the cyclic CR ADC is based on a loop, which includes a comparison with a comparator voltage, V_m, followed by a multiplication by two. If the residual voltage V_{res} is larger than the comparator voltage V_m, the residual voltage V_{resN} will be the residual voltage V_{resN-1} multiplied by two and reduced by the positive reference voltage $V_{ref,\,p}$ and the digital output bit will be set to $b_i = 1$. If the residual voltage V_{resN} is smaller than the comparator voltage V_m, the residual voltage V_{resN} will be V_{resN-1} multiplied by two and reduced by the negative reference voltage $V_{ref,m}$. In this case the digital output will be set to $b_i = -1$. This loop will be repeated for the number of conversion steps N_{cycle}. This algorithm will start by first calculating the MSB and then the least significant bits of the digital word. The algorithmic description of a cyclic CR ADC is shown in Figure 1a.

The cyclic RSD ADC uses for each bit two comparators instead of one in the CR principle. If the residual voltage V_{resN} is larger than the positive comparator voltage $V_{Comp,P}$ then the output is set to $b_i = 1$ and the residual voltage V_{resN} is calculated by $V_{resN} = 2*V_{resN-1}-V_{ref,\,p}$. For residual voltages V_{resN} smaller than the negative comparator voltage $V_{Comp,Q}$ the output is set to $b_i = -1$ and the residual voltage VresN is calculated by $V_{resN} = 2*V_{resN-1}-V_{ref,\,m}$. If the residual voltage V_{resN} is between both comparator voltages $V_{Comp,Q}<V_{resN}<V_{Comp,P}$ the output is set to $b_i = 0$ and the residual voltage is calculated by $V_{resN} = 2*V_{resN-1}$. The algorithmic description of a cyclic RSD ADC is shown in Figure 1b.

Due to the two comparators used in the RSD-principle and the 1.5 bit output signal of each conversion cycle, the RSD-ADC achieves a 1 bit better resolution for the same number of conversion cycles compared to a CR-ADC.

Impact of Non-Idealities

To compare the performance of both cyclic ADC types the effect of several non-idealities on the SNDR of the output signal must be taken into account. The most important effects could be modeled by adding factors into the algorithmic description representing the non-idealities [1].

A detailed analysis of the impact on the signal-to-noise and distortion ratio SNDR shows a better performance for the cyclic RSD ADC in terms of reduced comparator accuracy requirements, relaxed reference voltage stabilization, and smaller loop offset influence. Both types of cyclic ADCs are sensitive to gain errors which represent the deviation of the factor 2 used for the multiplication in each step. The insensitivity to gain errors will achieved using a periodic change of the sample and feedback capacitor decribed below [2]. The impact of mismatching on the SNDR has been simulated using MatLab. Figure 2 shows the simulation result which compared a cyclic ADC with and without periodic permuting capacitances. The result represent the enormous advantage of the periodic change.

Circuit Realization

The circuit is a switched-capacitor circuit with two OTAs, feedback and sample capacitances and some switches [3]. The OTA on the left side works as a sample-and-hold stage. The other one realizes the multiplication by the factor of two. C3 and C4 are the input capacitances where the input signal will be sampled. To get an exact multiplication factor of two, the sampling capacitors (C5, C6) and the feedback capacitors (C1, C2) will be switched after every cycle. This new signal will be stored on the capacitors (C7 – C10) at the left OTA for the next cycle. The comparators at the right side of Figure 3 have low demand. This is possible regarding the RSD principle. They are responsible for comparing the input signal with P and Q.

OTAs of the ADC

The used OTA is an concept with adaptive bias [4] (Figure 4). The OTA regulates its own bias current. If no signal is applied the amplifiers operate at very

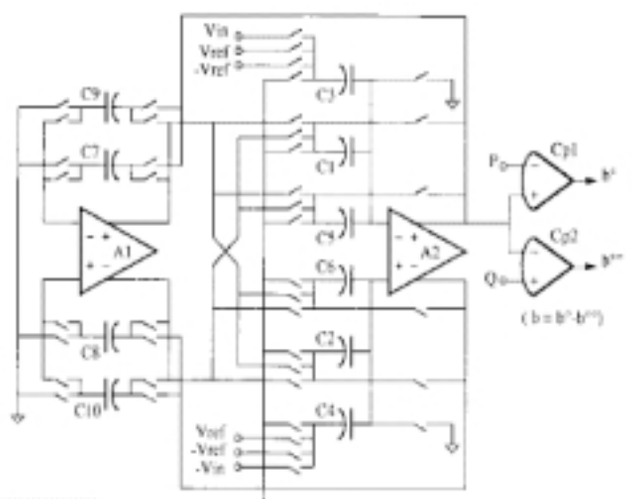

Figure 3: Cyclic RSD ADC (SC-realization) [3]

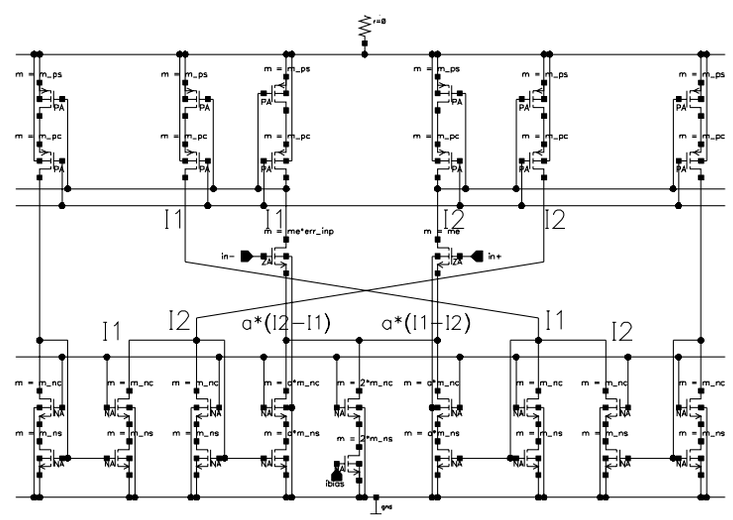

Figure 4: OTA with adaptive biasing

low current. Only when a signal is applied the current of the OTAs increases so that they have a high driving capability. The advantage is a lower current consumption than with fixed bias. The base structure of the OTA is a standard single-stage differential OTA with common mode feedback regulation. The advantage of the single-stage structure is the high speed, the low current consumption, and the easy common-mode regulation.

Comparators of the ADC

One advantage of the RSD-ADC concept are the low performance requirements on the comparators. Their threshold accuracy has to be only a quarter of a reference voltage. The used structure is a hysteresis comparator (Figure 5). The advantage of this structure is the well defined behavior and a stable and simple design [5]. Some "sleep-transistors" shut down the comparators when they are not in use. This reduce the current consumption of a whole signal conversion.

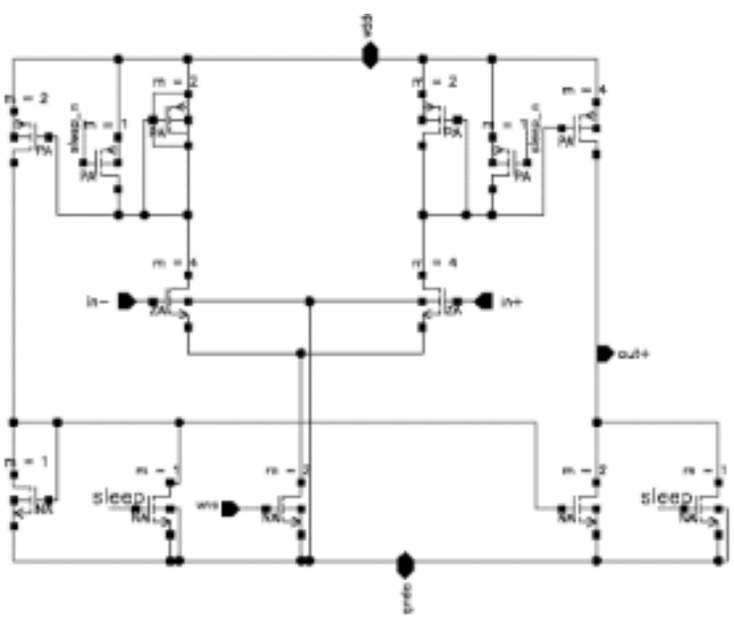

Figure 5: Comparator of the Cyclic RSD ADC

Conclusion

A passive transponder system for tire pressure monitoring has been designed which includes a cyclic RSD ADC as the main part. The measured resolution for the pressure and temperature mode is 50 mbar and 1 °C. The average current consumption of the total sensor readout including a C/V-converter and a cyclic RSD ADC is about 25 µA during the measurement period.

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Design of CMOS-∑Δ-Fractional-N-Synthesizers for Low Noise and Settling Time

N. Christoffers

Introduction

CMOS-∑Δ-Delta-Fractional-N-Frequency-Synthesizers [1] play an important role in the design of low power wireless transceivers. As an example, consider the direct-upconversion FSK transmitter using a modulatable ∑Δ-Fractional-*N*-synthesizer in Fig. 1. The modulation technique shown is denoted two-point-modulation [2]. The synthesizer is formed by VCO, frequency divider, ∑Δ-Modulator, charge pump and loop filter. The modulated signal is the output of the VCO and fed directly into the class-D-power amplifier. The output frequency f_{LO} depends on strongly varying component values. Additionally, it is sensitive to injection pulling [3, 4]. To adjust it as accurately as required by the communication standard the VCO must be stabilized in a control loop (phase-locked-loop, PLL): by means of a frequency divider, the output frequency is divided by a known number denoted the modulus and then compared with a reference frequency f_{ref} stemming from an accurate crystal oscillator. The comparison is carried out by means of the phase-frequency-detector (PFD), charge pump and loop filter. The output of the loop filter controls the VCO frequency in such a way that it is a known multiple of the accurate reference frequency.

The modulus of the frequency divider is always an integer number. However, frequency modulation at low modulation indexes normally forbids that the output frequency is an integer multiple of the considerably high reference frequency. This problem is solved by a time varying modulus. Due to inertness the PLL cannot follow the intense modulus switching and settles toward some average frequency. The sequence of moduli is supplied by the all digital ∑Δ-Modulator and the modulation is carried out varying its input word (control word) *K*. To compensate eventually occuring low-pass filtering of the modulation (due to the inertness of the PLL) a high-pass filtered version of the modulation is added using an adder at the VCO-input and a DAC.

Such synthesizers, however, entail one design difficulty. Even if the control word *K* is constant the output signal of the synthesizer is still deteriorated by residual frequency variations. To reduce them the inertness of the PLL must be increased, i.e. a trade-off between settling time and spectral purity of the output frequency exists. The IMS has developed a novel design methodology that relaxes this issue and allows both extraordinary low settling time in spite of an excellently pure output frequency.

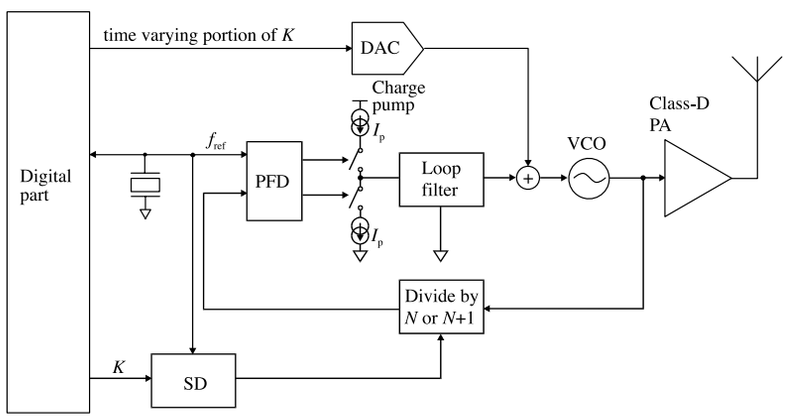

Figure 1: FSK transmitter using two-point modulated Synthesizer

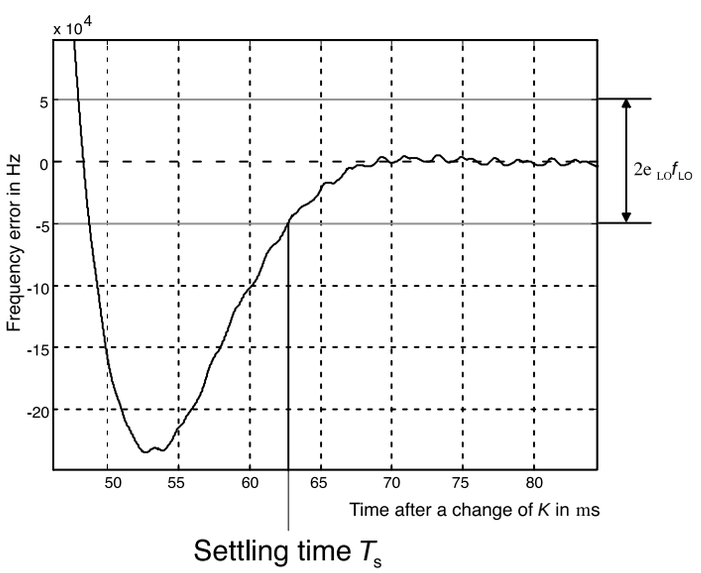

Figure 2: Illustration of Settling

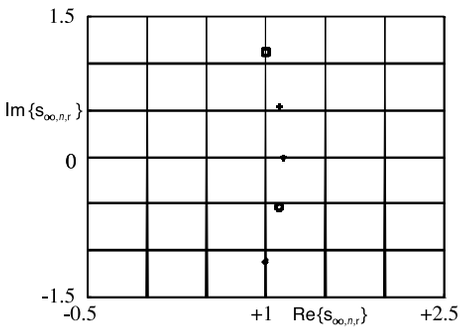

Figure 4: Optimum relative poles of a fifth order PLL

Since the synthesizer is basically a control loop the most important influence on its properties is provided via its loop-transfer function. This is generally expressed in terms of poles and zeros. The impact of good pole placement in case of PLLs is described in Section 2.

To realize a certain loop transfer function the loop filter must be designed properly. It was found that best properties can be obtained if the loop filter comprises biquadratic cells (biquads). A technique to design them allowing low noise, low power consumption and low chip area is introduced in Section 3. Additionally the properties of the resulting synthesizer are found using circuit simulations.

In Section 4 the contribution is summarized.

The influence of the PLL transfer function

Since the frequency synthesizer, as a PLL, is a control loop it can be described in terms of its closed-loop transfer function (phase transfer function) $H_{PLL}(s)$ and its open-loop transfer function $H_{OL}(s)$. Both functions relate the phase at the reference input to the phase at the output of the frequency divider in case the loop is closed or cut between divider and PFD, respectively. It is

$$H_{PLL}(s) = \frac{H_{OL}(s)}{1+H_{OL}(s)}. \qquad (1)$$

Both functions can be expressed in terms of poles and zeros. PLLs are distinguished into type-I ore type-II-PLLs depending on whether the open-loop transfer function has a single or a double pole at the origin. Type-II-PLLs are capable to start-up from any intitial condition and are hence preferred in microelectronic synthesizers. The closed-loop transfer function of a type-II-PLL is

$$H_{PLL}(s) = \frac{1+ s/s_{0,PLL}}{\prod_{n=1}^{N} 1+ s/s_{\infty,PLL,n}} \qquad (2)$$

where $S_{0, PLL}$ is the zero and $S_{\infty, PLL, n}$ are the poles of the PLL. Their number N is denoted also the order of the PLL. Since S_0 is also the zero of the open-loop transfer function it has an important meaning to closed-loop stability and, hence, cannot be chosen independently from the poles. Note that $H_{PLL}(s)$ is a low-pass transfer function.

A change of the carrier frequency is sometimes required and triggered by a step in the control word K of the SD-Modulator which in turn causes the frequency divider to divide by another average modulus. The response of the output frequency of the synthesizer to the required frequency change follows thus the step response associated with $H_{PLL}(s)$. Note that the synthesizer is not considered settled before the output frequency is adjusted as accurate as

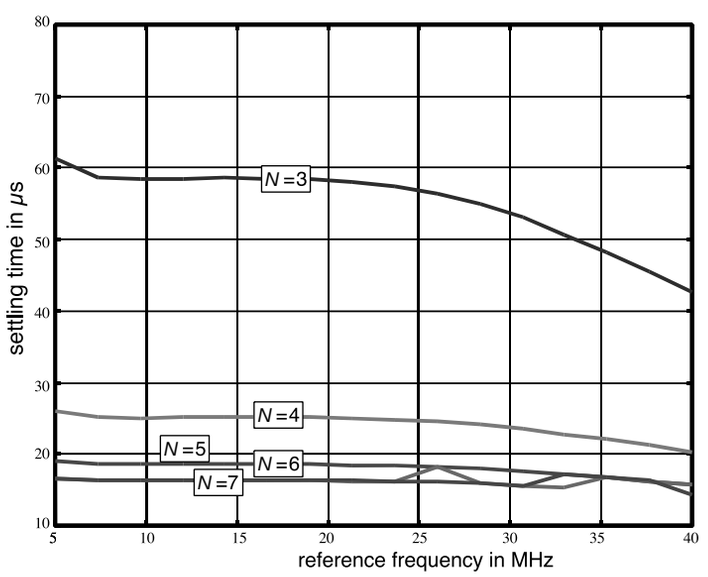

Figure 3: Minimum settling time versus reference frequency for fractional spurs lower than -125 dBc/Hz@2,5 Mhz and $M_V = 2$

required by standard. A graphical explanation of the term settling time is given in Figure 2.

Even if K remains constant modulus switching still occurs. The instantaneous modulus then follows the quantization error of the ΣΔ-Modulator. The response of the PLL to this is also determined by the closed-loop transfer function. The residual frequency variations are reflected by emissions of the synthesizer apart from the desired output frequency. Such emissions can disturb the communication in neighboring frequency bands and are denoted spurious emissions. Their power spectral density can be computed using a formula available from the literature [5]:

$$L_{\Sigma D}(\Delta f) = \left|H_{PLL}(j2\pi\Delta f)\right|^2 \frac{M^2{}_V \pi^2 \left|H_q(z)\right|^2}{3 f_{ref} \left|1\text{-}z^{-1}\right|^2} \quad (3)$$

where $L_{\Sigma\Delta}(\Delta f)$is the power spectral density of the output signal of the VCO at a frequency offset Δf with respect to the output power of the VCO, $H_Q(z)$ the noise shaping function of the SD-Modulator and $z = \exp(j2\pi\Delta f/f_{ref})$. The integer number M_V is the modulus of a fixed frequency divider eventually preceding the adjustable divider controlled by the ΣΔ-Modulator.

Since the quantization error has the most spectral energy at high frequencies it can be rejected the better the lower the bandwidth of $H_{PLL}(s)$. However low-bandwidth systems tend to settle slowlier than high-bandwidth system.

To escape this dilemma it is proposed to set the poles in an optimum fashion employing numerical optimization. Several of these optimizations have been carried out at the IMS. Figure 3 displays a result. Shown there is the minimum achievable settling time if an upper bound for the spurious emissions at some frequency offset is given.

The results were obtained for $M_V = 2$, a particular ΣΔ-Modulator and different orders of the PLL. The spectral density of the spurious emissions had to be lower than -125dBc/Hz (deciBels below carrier into one Hertz bandwidth) at 2.5 MHz frequency offset. Thereby it is maintained that the total power leaking into the frequency band 2.5 MHz < Δf < 3.5 MHz due to the spurious emissions is 5dB lower than specified in the Bluetooth-Standard. Note that the settling time can be reduced in two ways. Firstly, the reference frequency can be increased from 5 MHz to 40 MHz. However multiplying it by eight entails only a reduction by less than 30 %. It is more effective to increase the order of the PLL: The settling time drops from around 60 µs at

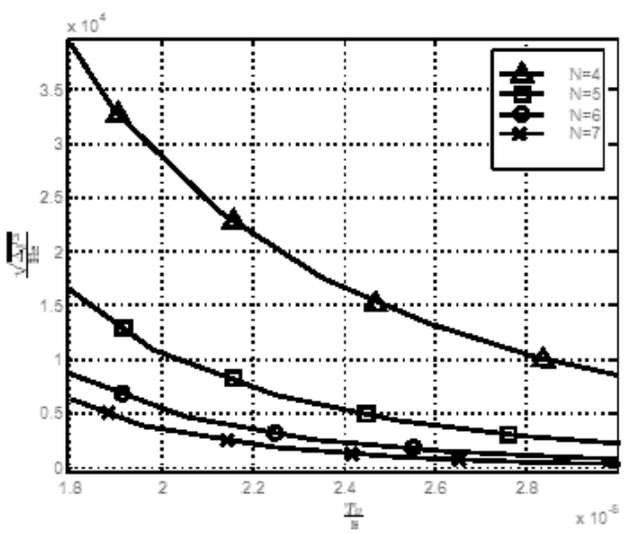

Figure 5: Residual frequency modulation versus settling time if relative poles of Figure 4 are used

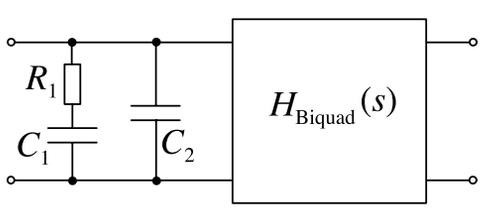

Figure 6: Structure of the fourth order optimum loop filter

8 MHz reference frequency to less then 20 µs if the order rises from three to four. Increasing the order to five yields another 50 % settling time reduction.

Another important insight of the optimization was that the poles have always been multiples of an order-specific configuration in spite of a varying specification (in this case reference frequency). The configuration for fifth order PLLs is shown in Figure 4. Therefore for an optimum PLL it is

$$S_{\infty,\,PLL,\,n} = S_N S_{\infty,\,PLL,\,n,\,r} \quad (4)$$

where s_N is a reference location on the negative real axis in units of rad s^{-1} and the $S_{\infty,\,PLL,\,n,\,r}$ are the relative pole locations found for the particular order.

The mean value of the absolute frequency deviations from the desired output frequency due to the modulus switch is denoted the residual frequency modulation. It was found that the relative pole locations found in the optimizations yield a good performance in terms of residual frequency modulation, too. Figure 5 shows the residual frequency modulation as a function of settling time. Note that a higher PLL order allows lower residual frequency modulation at a certain settling time, too.

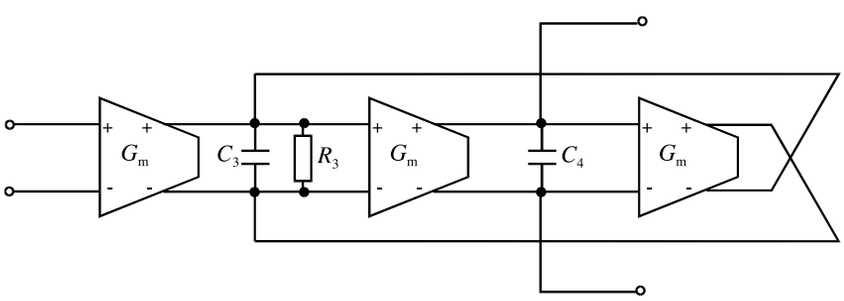

Figure 7: Circuit realization of the biquad

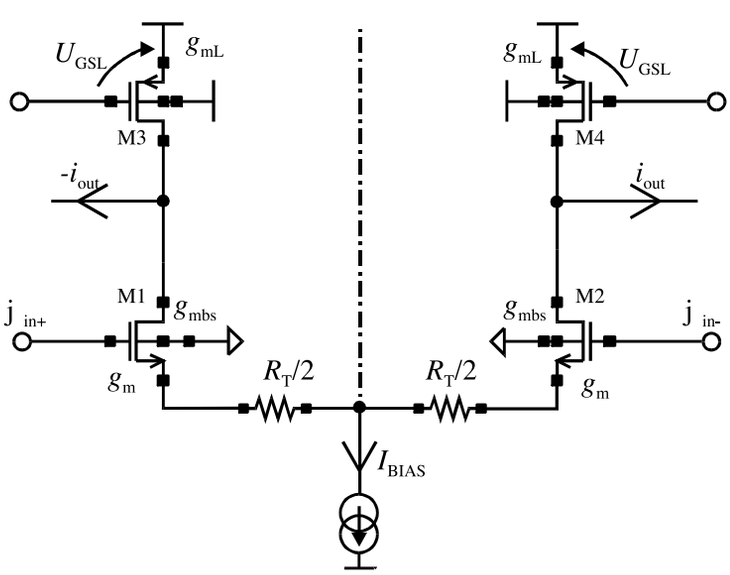

Figure 8: Circuit realization of the transconductor

Circuit design

After having established an optimum closed-loop transfer function the open-loop transfer function associated with it must be found. Using the Equation (2) reveals that the optimum open-loop transfer function exhibits complex pole pairs. To obtain them the loop filter has to have the structure given in Figure 6. It comprises a passive *RC*-loop filter realizing the real poles followed by a biquad for the pole-pair.

As a circuit realization of the biquad the G_m-C-biquad of Figure 7 is proposed. To build it capacitors, resistors and transconductors are required. Transconductors are voltage controlled current sources and can be realized easily as differential amplifiers as depicted in Figure 8. The linearity was improved using resistive feedback (degeneration). Although very simple the circuit can provide low noise and low current consumption.

The phase noise (some sort of spurious emissions) contributed by the loop filter

is depicted in Figure 9. Note that the phase noise is lower than -145 dBc/Hz at 2.5 MHz offset. The noise contribution was obtained using a Spectre (Cadence) simulation of the synthesizer. The current consumption of each transconductor was 170 µA.

The control voltage of the VCO as a function of time and the spurious emissions found by Spectre and Simulink simulations are compared in the Figures 10 and 11. In both cases the settling time was below 25 µs and the spurious emissions lower than -145 dBc/Hz at 2,5 MHz offset. Note that the prediction by Simulink is quite accurate even though transistor level model of the PFD, charge pump, and loop filter have been employed in Spectre. The prediction of Equation (3) was correct, too.

Summary

In the preceding a new design technique for ΣΔ-Fractional-N-synthesizers was proposed. It allows a good suppression of the quantization error of the ΣΔ-modulator in spite of a low settling time. The loop filter had to comprise biquadratic cells. It was shown that their realization is possible at an only moderate power consumption.

Several investigations have not been shown but were carried out already. For example, the behaviour of the synthesizer in the presence of component value variations is very good, too.

Such fast settling ∑Δ-Fractional-N-Synthesizers with low spurious emissions can be used in other applications than FSK transmitters, too. For instance an 802.15.4 (ZigBee) radio operating at both frequency bands 868 MHz and 915 MHz must start-up very quickly and hence requires low settling time of the frequency synthesizer. Additionally frequencies in both bands have to be derived from only one crystal reference oscillator. Both, however, is difficult to achieve without Fractional-N-Synthesis. Especially here the design approach is very helpful.

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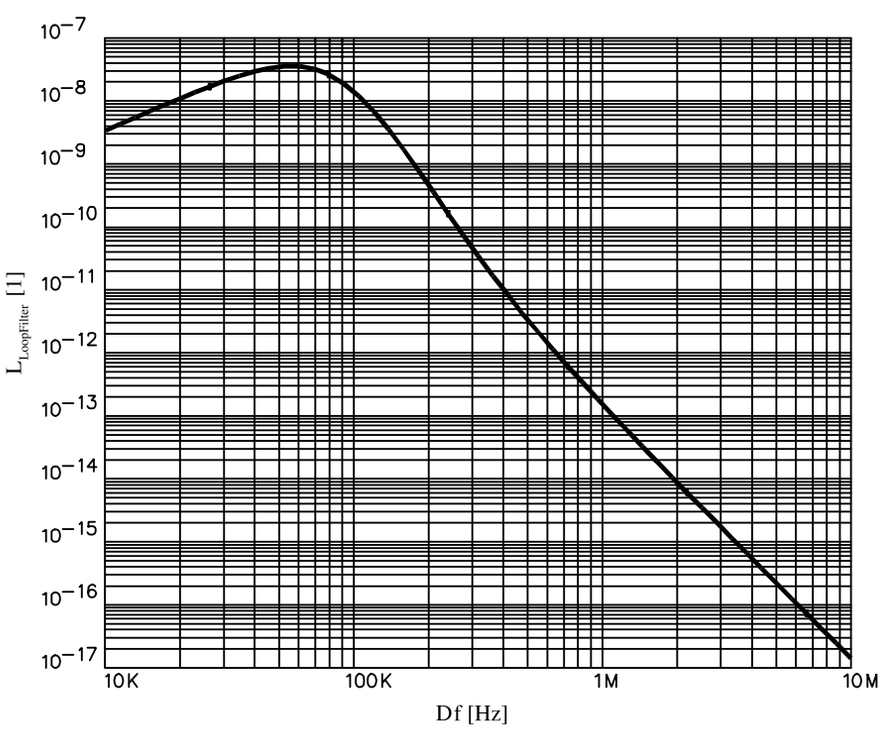

Figure 9: Phase noise contribution of the loop filter

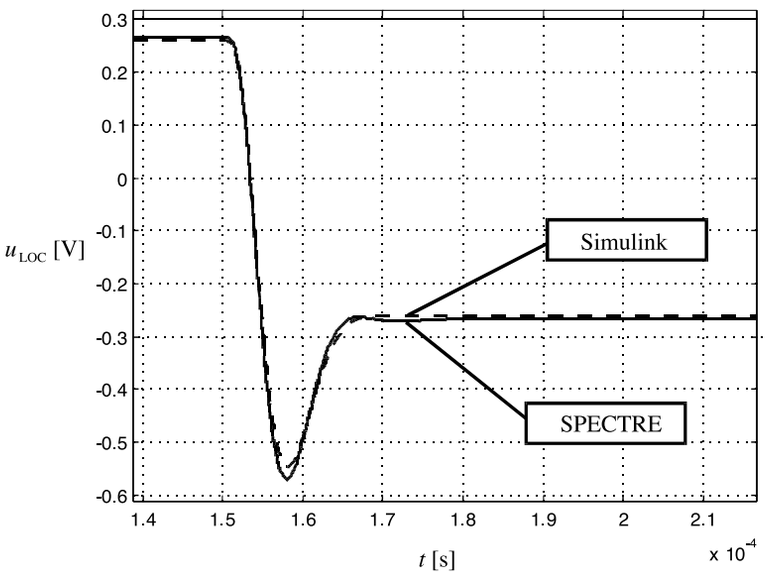

Figure 10: Settling of an optimized fifth order synthesizer

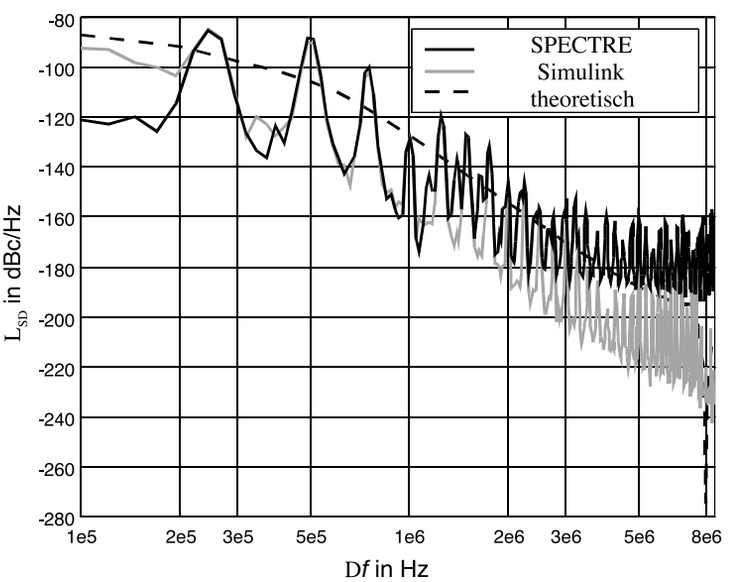

Figure 11: Spurious emissions of an optimized fifth order synthesizer

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A Tire Pressure Measurement System for Passenger Cars based on a passive Transponder

M. Bresch, G. vom Bögel

Introduction

Underinflation is the most dominant reason for traffic accidents.
Since legislation tends to require an automatic tire pressure measurement system (TPMS), IMS has designed a sensor system for passenger cars based on a passive transponder system for all four tires as shown in Figure 1. Since tire pressure is temperature dependent, the TPMS also provides a temperature measurement. A manual tire pressure measurement has two disadvantages. First of all, the manual measurement is not executed sufficiently frequently so that the risk to cause accidents rises with wrong inflation. Moreover, the tire pressure is specified for cold tires. However, on the way to the pressure measurement at the filling station the tires heat up. Measurements at the filling station are not temperature compensated.

Requirements

Since a heavy dynamic load in the tire will effect the driving conditions, the transponder inside the car must be very light. Only less than 5 g weight is acceptable. At a car velocity of 200 km/h, the acceleration is no less than 4000 g. Therefore, a passive transponder has to be prefered. The tire pressure is measured continuously when the car is driving. Since the tire pressure even can be measured in turns, the reading range of the passive transponder system is from 5 cm to 40 cm to adapt itself to the varying distance between wheel and reader antenna depending on the curvature. For this reading range, the transponder does fulfill the severe requirement, that it consumes only 20 µA current at 3 V power supply. The transponder operates at temperatures from -40 °C up to +125 °C. The transponder tag is coated in order to be protected against humidity and chemical influences. However, the coating is pressure sensitive. The communication link between reader and transponder copes with the vast attenuation caused by metal of the car body.

Transponder Modul

The transponder PCB (printed circuit board) carries a 133 kHz resonator with a ferrite coil for inductive coupling. This antenna has to reach a quality factor of 70 to provide enough power at 40 cm distance. The PCB carries clamp diodes to protect the ASIC at small distances between wheel and transponder, capacitors, that maintain the supply voltage, when the transponder is outside the

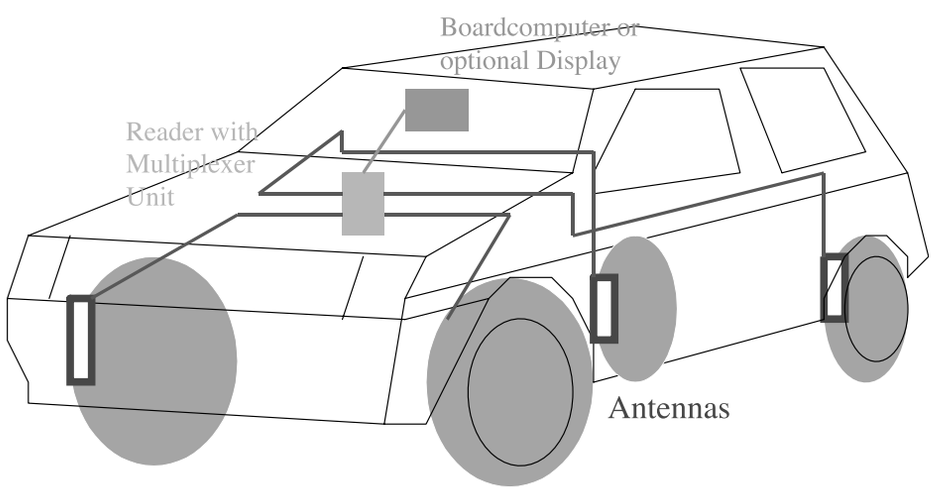

Figure 1: Transponder system

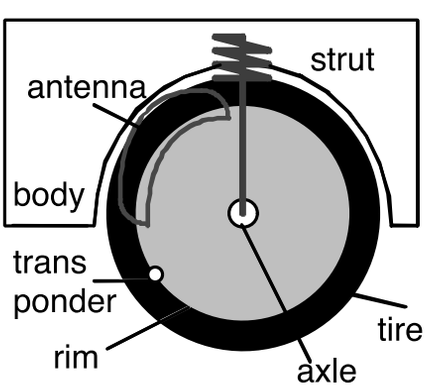

Figure 2: Positions of transponder ASIC on the rim and of reader antenna

interrogation field of the reader. The PCB carries the ASIC. The tag size is 5 cm^3. Only ISM frequencies are admissible. The low carrier frequency leads to an inductive coupling, which is less effected by metal attenuation than electro-magnetic RF coupling. At 133 kHz transmission frequency, the transponder system operates in the near field. A coil antenna in the near field leads to an attenuation of 60 dB/decade outside the size of the transmitting antenna, which allows higher transmission power as in the case of lower attenuation rates, since the permitted radiation is restricted. The enlarged transmission power is necessary to meet the range requirements. External Zener-Diodes of 12 V break-through voltage enhance the load modulation, so that the tag signal can be detected by the reader.

Transponder ASIC

The transponder ASIC consists of a micromachined pressure sensor, a temperature sensor, the sensor readout, EEPROMs, the RF front-end, and a micro controller.

The RF front-end rectifies the induced AC voltage supplied by the resonator to generate the DC voltage supply. It contains an excess voltage protection for small reading ranges. This enables the tag operation at supplies between 3 V and 12 V. The clock is extracted from the induced AC voltage. The RF front-end comprises a load modulator, since only load modulation is acceptable due to power restriction. The RF Front-end provides a clock fail indication as well as a power fail indication for micro controller and sensor readout. Furthermore, the RF Front-end provides a regulated voltage for the analog part as well as reference voltages for the sensor readout.

The pressure sensor is a micromachined capacitance, in which a membrane covers a vacuum chamber. If a pressure is applied, than the membrane is deflected accordingly. For accurate measurement, calibration data must be provided, since the membrane deflection is a highly non-linear three-dimensional process. The TPMS ASIC is therefore a combination of micro mechanic and micro electronic components and thus fabricated in a special CMOS process. Only CMOS enables the very low power consumption.

The sensor readout calibrates the obtained sensor signal by using the sensor and a reference structure. The sensor signal is digitized by an 8 bit RSD-cyclic ADC, which receives its reference voltages from the RF front-end. It is in power-down when not measuring. The non-linearity of the pressure measurement forces the ADC to provide a higher resolution than the accuracy. For an accuracy of 5 Bit (100 mbar in the range 0 to 3 bar relative pressure range) at least 8 bit resolution is necessary. The RSD-cyclic ADC operates at 133/16 kHz and needs one clock cycle per bit. The benefit of a cyclic ADC for the application of a passive transponder is its very low current consumption. A special RSD-cyclic ADC features high precision. Therefore, the digitization of the measurement data takes 8 clock cycles, i.e. 1 ms. A second millisecond is necessary to transmit the data to the reader. The RSD-cyclic ADC employs reference voltages obtained from the RF font-end. In order to ensure a meaningful sensor signal digitization, these reference voltages have to be stable. Therefore, the ADC must not operate "soon" after a power-up. Only after a recovery time of about 2 ms, the sensor readout operates, when the reference voltages have settled and become stable.

The EEPROMS have to carry the 96 bit calibration data for the pressure and

the temperature sensor, and has to carry a specific 64 bit ID. This specific ID can be used e.g. to ensure the traceability of the chip and uniquely identify producer and charge, since 64 bit are sufficient to make the ID unique world-wide. The EEPROMs are field programmable.

The micro controller is responsible for the protocol for steering the load modulation, steering the sensor readout and reading and transmitting the EEPROM data. The measurement conditions at high car velocity impose severe requirements to the protocol, since only 3 Bytes can be sent within one wheel revolution. The TPMS is designed for measurement at car velocities up to 250 km/h, where one wheel revolution takes about 22 ms. As to be seen from Figure 2, about 290° of one wheel revolution cover the dark phase, in which there is no communication link between transponder and reader. Only about 70° mark the retention phase. At low velocities, a complete protocol set can be sent to the reader. It has to contain 8 bit pressure data, 8 bit temperature data, 96 bit calibration data, 64 bit specific ID, headers, CRC data, and stop bits. A complete protocol set contains 256 bytes and can be transmitted within one wheel revolution up to car velocities of about 30–40 km/h. The measurement accuracy of the design is proposed to be 100 mbar in a pressure measurement range of 0 bar to 4 bar absolute pressure and it is designed for a measurement accuracy of 5 °C in a measurement range of -40 °C to 125 °C. Since calibration data and specific ID have to be transmitted only scattered while measurement data shall be transmitted continuously at high priority, the protocol adapts to the car velocity, which is measured employing the clock fail indication.

The protocol at low velocities to transmit a complete data set in a row: pressure measurement, temperature measurement, calibration data, specific ID. All transmission bytes are interleaved by recovery cycles to ensure stable measurement conditions.

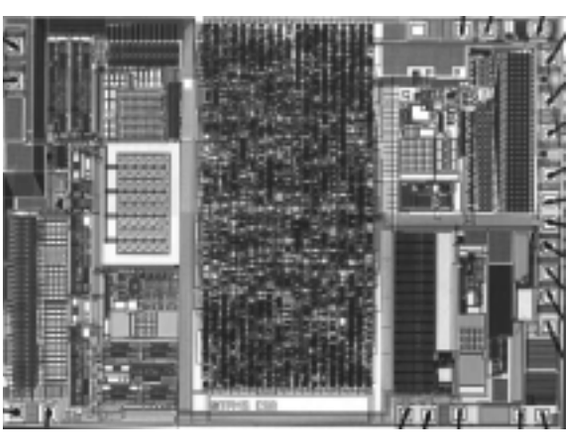

Figure 3: Chip Photo of the transponder ASIC

Reader

The TPMS comprises one reader for four transponder ASICs and one reader antenna for each wheel. The reader generates the 133 kHz RF transmission carrier and thus provides the RF supply energy by inductive coupling. The reader contains a modulator to analyze the data acquired from the tags. The reader communicates with the transponders of four wheels by means of time multiplexing and provides the car interface. Reader antenna and transponder positions are depicted in Figure 2. The reader antenna is a square coil of 30 cm length and 12 cm width. Figure 3 shows the Microphotograph of the transponder ASIC. The reader operates typically at a DC power supply of 12 V, as usual for automotive applications. The size of the reader antenna is designed considering the limited space in the wheel house, the reading range requirement: The reading range increases with the antenna size. Moreover, the antenna is designed considering the requirements by ETSI, which restricts the radiated power in a way, that the magnetic field strength 3 meters apart from the antenna shall not exceed 4.7 mA/m. Since ETSI imposes almost the hardest limitations of the world, the transmission power design enables licensing the TPMS systems in all major countries.

A Bluetooth based medical Transponder System for Intraocular Pressure Monitoring

R. Ochsenbrücher, S. Kolnsberg, B. Klein, R. Kokozinski

Introduction

For a better treatment and analysis of the eye disease *Glaucoma*, a continuous measurement and knowledge of the eye's internal (intraocular) pressure is of particular importance. The Bluetooth based medical transponder system presented in this article offers a measurement of the intraocular pressure using a passive transponder ASIC with a fully integrated pressure sensor. It processes the data via a portable reader, which also stores the measurement data and transmits it to a PC or laptop nearby using an integrated Bluetooth module.

Figure 1 gives an overview of the complete system, while the following subsections present the working principle and the technical details.

The second most frequent cause of blindness in industrialized countries is the eye disease Glaucoma. In Germany, about 800,000 people suffer from this disease. Due to a high pressure within the eye (> 20 to 22 mmHg), caused by an accumulation of intraocular fluid, the optic nerve is damaged. Partial loss of vision, and – if not treated – total blindness of the patient is the consequence [1].

Various medication methods are used by attending physicians to lower the high intraocular pressure (IOP) of their patients, but the main drawbacks of these medication methods are inaccuracy and unreliability due to great variations of the IOP within one day [1, 2]. Thus, with the help of a continuous measurement of the IOP the treatment of Glaucoma will be optimized and the therapy can be adjusted to each patient's needs. Furthermore, the monitoring of the IOP can take place in familiar surroundings of the patient.

Description

The presented transponder system for IOP monitoring comprises an artificial ocular lens, special eyeglasses and a portable reader attached with a Bluetooth module (as seen in Figure 2).

Artificial ocular lens: Figure 3 shows the lens which consists of an encapsulated passive transponder ASIC with an micromachined capacitive pressure sensor as well as a circular antenna coil (diameter: 10.8 mm) for power supply of the single-chip ASIC and wireless data transmission. The ASIC and the coil are placed in the non-optical part of the lens. In combination they are called a *transponder tag.*

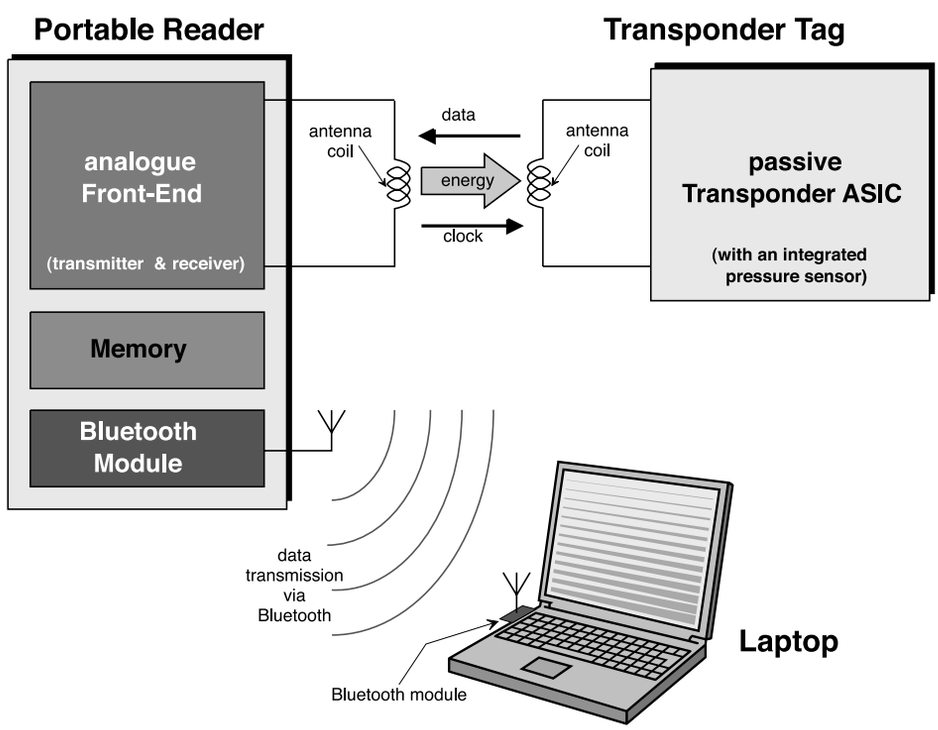

Figure 1: Overview of the Transponder System for IOP Monitoring

Figure 3: Artificial ocular lens with an encapsulated passive transponder ASIC and a circular antenna coil

Special eyeglasses: After the artificial ocular lens has been implanted in the patient's eye, he or she has to wear special eyeglasses. Depicted in Figure 4, an attached antenna is integrated into these eyeglasses. This antenna coil is connected via a wire with the portable reader, the patient has to wear, too. The antenna coil is used to transmit energy to and to receive measurement data from the transponder tag. For this purpose the antenna coil is coupled inductively with the antenna of the transponder ASIC.

Portable reader: On the one hand, the portable reader provides a high-frequency electromagnetic field (f = 13.56 MHz) by which the passive transponder ASIC is supplied with power. Additionally, the transponder ASIC extracts a clock signal from that field to operate its digital signal processing unit. On the other hand, the portable reader receives and processes the transmitted measurement data of the transponder ASIC. Furthermore, it stores the incoming pressure values into its memory.

Bluetooth module: A 2.4-GHz Bluetooth module attached to the portable reader is used to transfer the measured and stored pressure values to a PC wirelessly – provided that the PC is also equipped with a Bluetooth module (see Figure 1). Note, that if a Class-1 Bluetooth modules with a transmitter power of 100 mW is used, a wireless data exchange across a distance between reader and PC of up to 100 meters in open space and of several ten meters in buildings is feasible.

Using Bluetooth, the attending physician can analyze and monitor the continuously measured IOP of his or her patients centrally, if several patients are equipped with the presented transponder system. Additionally, the usage of Bluetooth makes it possible to have online access to the measurement data of patients which are located in different rooms of the doctor's practice or at home (i.e. assuming the patients have access to the internet).

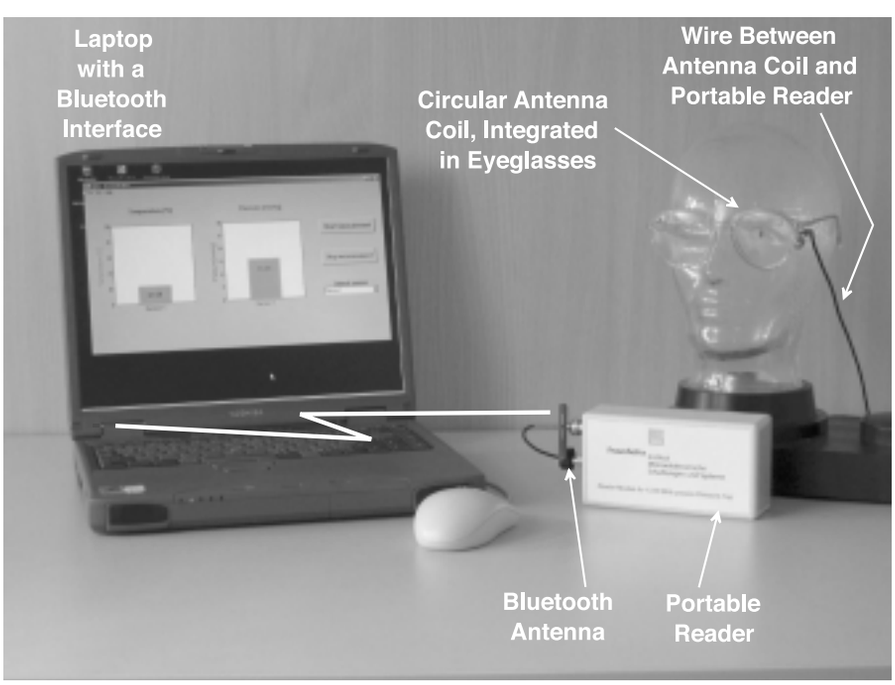

Figure 2: Photograph of the prototype of the Transponder System for IOP Monitoring

As another application example, the system could be combined with an alarm function. Thus, it can inform the doctor if a particular limit was exceeded, and when other pieces of information about the patients as well as additional out-patiently recorded data are regarded, a more reliable and more efficient monitoring of patients is possible.

Working principle: After the activation of the transponder ASIC the IOP is measured. Additionally, the ASIC performs a temperature measurement. Thereby, the thermal dependence of the pressure can be taken into account, while processing the measured pressure values and calibrating the transponder system. The calibration data in combination with an individual identification

number of each transponder ASIC is stored into the portable reader's memory.

Having finished the measurements, the pressure and temperature values are transmitted at a data rate of 26.5 kBit/s from the transponder ASIC to the portable reader via load modulation of the electromagnetic field of the reader's antenna.

Subsequently, the received signal is demodulated, the temperature and the pressure values are processed and stored into the memory of the portable reader.

Circuit Design

The single-chip transponder ASIC consists of the following main building blocks (see Figure 5): RF-Front-End (used for clock extraction, modulation, half-wave rectifying, excess voltage protection, voltage regulation and generation of a power-on-reset signal), digital processing unit (protocol and measurement control), EEPROM (storage of an identification number and a CRC checksum for error detection), sensor readout (A/D-Converter), pressure and temperature sensors, and an on-chip tunable capacitance, which forms a resonant circuit together with the off-chip antenna coil.

The transponder ASIC takes up a chip area of 6.5 mm^2 and is fabricated in a 1.2 µm n-well CMOS process. Its current consumption at a supply voltage of 3 V is lower than 250 µA. Therefore, a reading range of maximal 5 cm between the reader's antenna and that of the ASIC is possible.

Pressure Sensor: The CMOS process mentioned above is extended by additional processing steps providing capacitive pressure sensors. The sensor element (Figure 6), used in the presented system, comprises an array of surface micromachined vacuum gap capacitors. While the top plate of such a capacitor is a membrane made of polysilicon, the bottom electrode is formed by a highly doped n-well. Both electrodes are separated by a sealed vacuum cavity [2, 3].

Within the given measurement range of 600 to 863 mmHg the pressure can be measured with a total accuracy of +/- 2.25 mmHg.

Temperature Sensor: The basis for the temperature sensor is the temperature dependency of MOSFET characteristics in the weak inversion region.

For the presented system a measurement range from 34 to 40 °C is sufficient, because it is implanted in human beings.

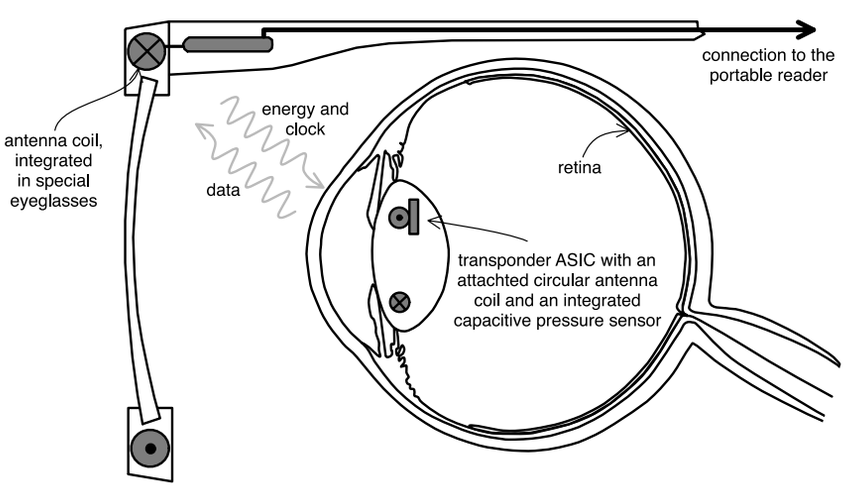

Figure 4: Architecture of the intraocular pressure sensor system

Conclusion

With the presented Bluetooth based medical transponder system it is possible

1 to measure the IOP continuously in familiar surroundings of a patient suffering from Glaucoma,

2 to achieve a better analysis of the eye disease Glaucoma,

3 to find a more reliable and optimized medication method,

4 to monitor the IOP of several patients centrally,

5 to administer the treatment of their disease more efficiently, and

6 to form e.g. an alarm function, which indicates an exceeding of a particular IOP limit.

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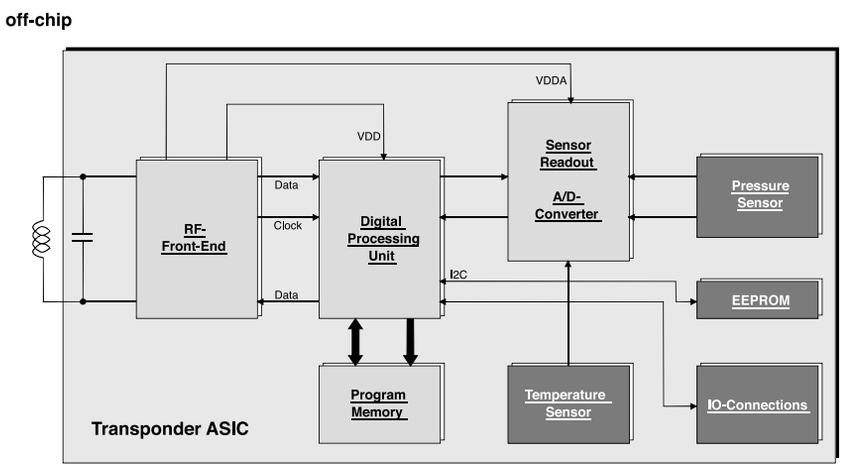

Figure 5: Block diagram ot the transponder ASIC

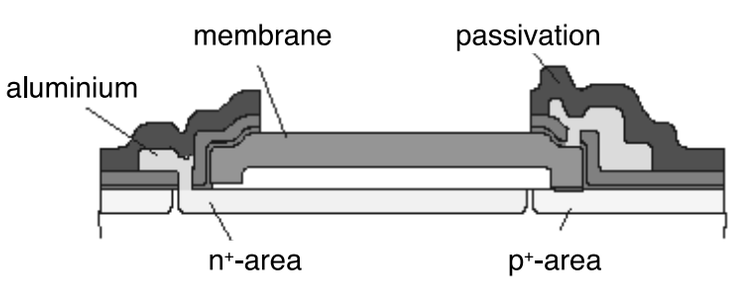

Figure 6: Cross-section of the integrated pressure sensor element

An IEEE 802.15.4 Wireless Sensor Network Node

M. Holzapfel

Introduction

Using transceiver chips for the IEEE 802.15.4 standard, the Fraunhofer IMS has implemented wireless sensor network nodes, which can be used to establish a Wireless Personal Area Network (WPAN). These networks form the basis for a multiplicity of applications such as plant automation, goods monitoring, home and building automation, medical technology, computer periphery and entertainment electronics. These application fields are particularly characterized by their small amount of data, which must be rarely transmitted and thus requires only a very small data transmission rate. The network topologies can be star network, mesh network or a combination of the two topologies. A coordinator communicating with all other network end nodes in his proximity characterizes the star network. In a mesh network, however, each end node is allowed to exchange data with its direct neighbour nodes (see Figure 1).

Wireless Sensor Network Nodes

It is an important demand on a network node to be used as long as possible without any manual interaction like changing the battery. The active phase of the node, in particular the transmitting and receiving activity, must be kept as short as possible. Limited energy resources must be likewise considered with the selection of the hardware for a network node. Preferably an 8 or 16-bit microcontroller is used, which has to manage only a small data memory.

The networking of the individual sensor network nodes must be simple and if possible without any manual interaction. Furthermore the loss of an individual node should not lead to the breakdown of the complete network. The network nodes must be able to find independently an alternative path within a meshed network over which the data can be transported to the destination. Due to the up mentioned demands, the underlying protocol must be as compact and durable as possible.

Realisation of the hardware

Two different kinds of radio modules have been developed at Fraunhofer IMS, which can be used to build up wireless sensor networks: a development board and a sensor board. Both modules include a 2.4 GHz transceiver chip, which is controlled by an 8-bit microcontroller. While an antenna is integrated on the printed circuit board (PCB), alternatively an external antenna can be attached to an SMA connector.

The sensor board with a size of 33 mm x 55 mm provides an SPI interface, an I^2C interface, five analog inputs, two external interrupt inputs, and depending on the circuit up to 26 general purpose digital inputs/outputs for the access of sensors or actuators.

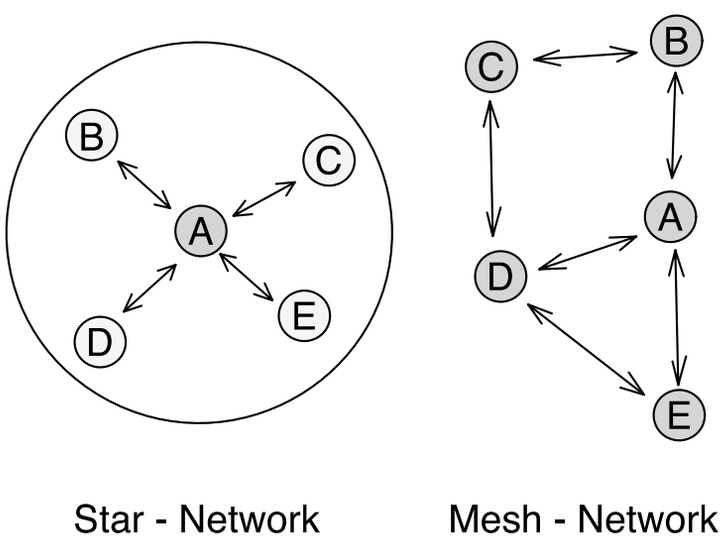

Figure 1: Topologies: Star Network and Mesh Network

The development board has a size of 60 mm x 90 mm and provides an RS232 interface for connecting this board to a PC in addition to the SPI and I^2C interfaces. Eight analog inputs, two external interrupt inputs and up to 18 general-purpose digital input/output to access sensors or actuators. In order to be able to fulfil the necessary routing tasks in a larger network, this network node is equipped with 64 kByte external RAM memory. The memory can be used to store the dynamically established network paths within routing tables.

Realisation of the software

Both radio modules have been developed to support the ZigBee/IEEE 802.15.4 standard. This standard is based on two independent standards: the IEEE 802.15.4 [2] and the ZigBee standard from the ZigBee alliance [3], an industry consortium of leading semiconductor manufacturers, technology providers, OEMs and end-users worldwide. The IEEE 802.15.4 protocol defines the lower protocol layers, i.e. the Physical (PHY) Layer and the Media Access Control (MAC) Layer and has been officially released in October 2003. The ZigBee protocol provides upper layers of the protocol stack on top of the IEEE 802.15.4 standard, which includes the Network (NWK) Layer and the Application (APL) Layer. Figure 2 shows an overview of all layers used for a ZigBee application.

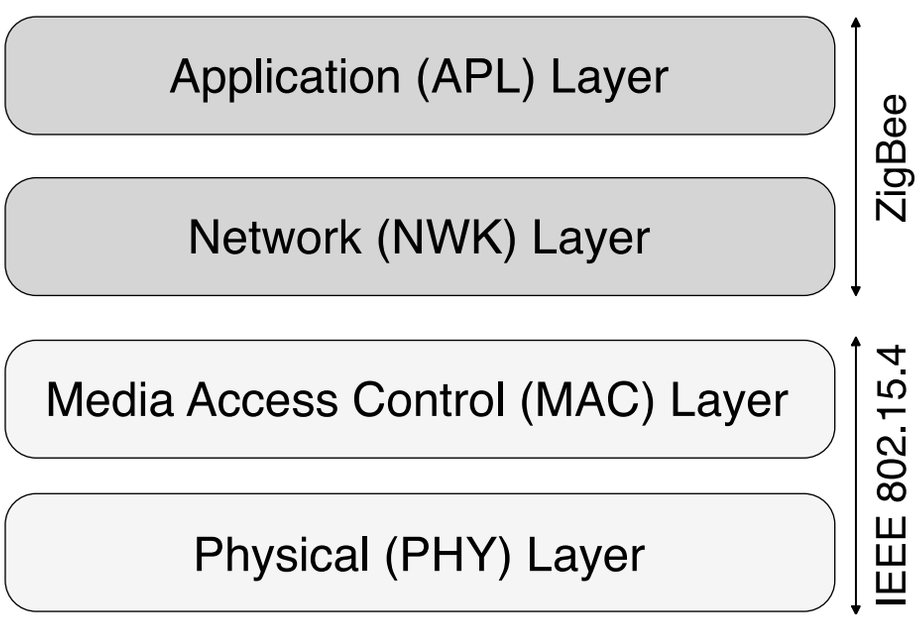

Figure 2: IEEE 802.15.4/ZigBee Protocol Stack

TinyOS

Not only ZigBee but also TinyOS [1] has successfully been ported on the IMS's radio modules. TinyOS is an "Open Source" operating system, which was developed with regards to hardware with small power consumption. Originally it has been developed and verified by the University of California, Berkley. It provides the basic functionality to address input and output operations as well as a hardware abstraction layer (HAL), which "hides" the particular hardware. This makes the operating system and the application software highly portable. TinyOS provides the user with functions for analog and digital measurements, for the communication with external hardware and for the transmission and reception of data packets from the connected IEEE 802.15.4 transceiver. By its modular structure and event-oriented mode of operation, the applications make use of a current savings management so that the life span of the sensor nodes increases.

Fraunhofer IMS ZigBee solution

While the IEEE 802.15.4 PHY layer has been realised completely in hardware,

the MAC functionalities have been partitioned into a hardware part and a software part. Fraunhofer IMS makes use of a software solution, which has been developed with respect to the transceiver chip on the radio module. The complete ZigBee protocol stack, i.e. NWK layer and APL layer have been developed by the worldwide leading ZigBee protocol developer Figure 8 Wireless [4].

Being an institute of the Fraunhofer Gesellschaft, Fraunhofer IMS is as member of the ZigBee Alliance and is thus able to offer both the necessary software and the hardware needed for a ZigBee network. Beyond that the Fraunhofer IMS can provide costumers with applications adapted to the individual customer's needs.

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Moving Images via UMTS

D. Greifendorf, R. Kokozinski

Introduction

There are only very few commercial UMTS handhelds available yet. Providers are offering a very limited number of services which really expand the benefits of mobiles beyond conventional telephony. Thus, the UMTS market is currently not growing with the desired speed. A major technical obstruction results from the very distinct evolutionary speeds of microelectronics on the one hand and of the battery technology on the other. Highly advanced services need large signal processing power and in consequence, large battery capacities. Today, there are no batteries on the market, which give small size and enough capacity simultaneously. Consequently, a potential user must decide between a small sized UMTS handheld with limited operation periods between battery charging cycles, and a rather large mobile with extended operation periods. Thus, on the microelectronics side, there is still a need for powerful signal processing algorithms supporting highly advanced services but requiring minimised processing power. With our focus on the transmission of moving images via UMTS, we have built up a development platform for the efficient implementation and testing of signal processing algorithms. This platform is based on the hardware of conventional PCs and on Digital-Signal-Processors (DSPs).

State-of-the-Art and Objectives

A popular software tool for the fast prototyping of digital signal processing algorithms is the program Matlab from 'The MathWorks, Inc' [1]. This software is based on an easy-to-use programming language which is especially suited for the calculation with vectors and matrices. Because Matlab programs are interpreted (and not compiled), complex algorithms may need very long simulation periods. Thus, real time simulations are not possible. Furthermore, the necessary final manual code conversion for the target-DSPs forms a rather large step in the development process. By this, a lot of uncertainty is postponed to the end of the development sequence.

Our basic idea was to combine the benefits of the Matlab program with the real time facilities of current digital signal processors. The platform should support the development of digital signal processing algorithms in 'fine steps', i.e., a developer should have access to all Matlab interpreter benefits in early stages of the development process. DSP code should be created not only in the final step but as early as possible. In summary, we pursued the following objectives:

1 The program Matlab as the 'frame' for the development platform,

2 DSP executable code as early as possible in the development process,

3 Final real time facility for algorithm simulation,

4 Conventional personal computers as frame hardware.

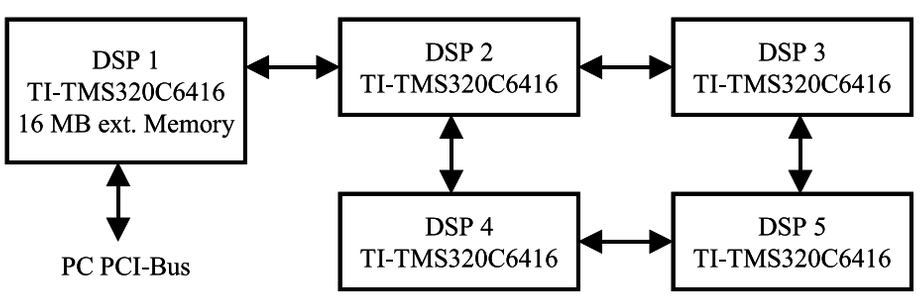

Figure 1: DSP Network in the Development Platform

Implementation of the Development Platform

The hardware of the development platform consists of a conventional personal computer. A PCI carrier board is installed inside on which five digital signal processors from Texas Instruments (TI) are located. The type of all DSPs is 'TMS320C6416'. The reason for this large number of processors is caused by the philosophy of a 'fine step' development process, already mentioned above: The developer can start to run his algorithm on the DSPs in an early non optimised status when still large processing power is needed. Then, he can improve his code, thus reducing the necessary hardware resources step by step.

One of the five processors is suitably connected to the PCI bus, thus having access to PC resources like harddisk, screen, etc. This processor is equipped with 16 MB external memory and thus can run algorithms which large memory demand. The other four DSPs can only use 1 MB internal memory. Tasks running on the different processors can communicate via so called comports [2] for data exchange. This enables the developer to run parts of his algorithm concurrently for faster operation. Figure 1 shows the DSP network in the development platform.

On the software side, a four layer structure has been implemented. This is shown in Table 1.

The program Matlab comes along with a so called Matlab-Exchange interface (MEX interface). This allows to call compiled code located within dynamic link libraries (DLLs) directly out of Matlab scripts. Matlab offers only full functionality for double float variables while the DSPs only perform fixed point (integer) operations. In the wrap layer all necessary forward and backward conversions are implemented so that Matlab can run DSP sourcecode in early stages of the development sequence after the compilation with an compatible PC compiler. The wrap layer is one of the core elements of the platform.

After a successful Matlab simulation, the DSP source code can be compiled for the DSP hardware. We use the TI CL6XC-compiler. Because the hardware forms a multi DSP network, this has to be done in a suitable framework. Our preference is the multi DSP OS system '3L-Diamond' from Sundance [2]. 3L-Diamond uses the TI CL6X-compiler as well, however to the procedure of compilation and linking an additional step is added in which the DSP code is partitioned for the DSP network. This is controlled by a simple ASCII file. The DSP source code must not be changed for a different partitioning if the code is written in a foresighted manner. Again, this supports the philosophy of the 'fine step' development process.

Layer 4	Compiled DSP Sourcecode
Layer 3	'Wrap' Layer
Layer 2	MEX Interface
Layer 1	Matlab Main Program

Table 1: Layer Structure of the Development Platform

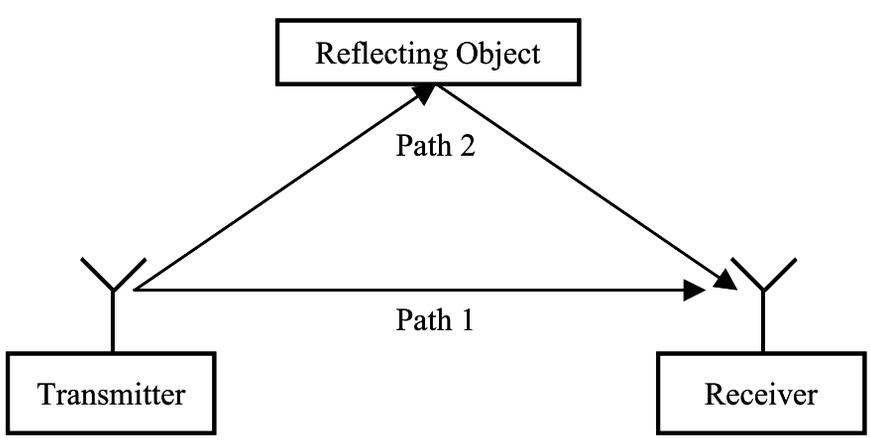

Figure 2: Scenario for a Multipath Reception

Transmission of Moving Images

Simulation of algorithms for the digital baseband of UMTS mobiles need a suitable testbench. We have implemented for both – for Matlab and for the DSP – a UMTS transmitter and a channel model. These two modules form the other core elements of the development platform. The transmitter module under Matlab can be adapted to several UMTS services. For the DSP network, we have only implemented the DL reference measure channel with 384 kbps, yet. This is the most suitable service for the transmission of moving images specified in 3GPP [3].

The channel model can simulate time variant multipath transmission. Figure 3 shows an appropriate scenario: The electromagnetic waves may be reflected by obstacles, and thus, can arrive the receiver on different ways with different path lengths. In this situation, the receiver sees the signal more than once. From analog TV reception this is well known as 'ghost images'. One of the tasks of the digital baseband in an UMTS mobile is to compensate these artefacts. If the mobile is used in a car, the scenario will become even more complex because the multipath transmission will vary with time. The realized channel model can simulate this scenario as well. Figure 4 shows an example of an implemented time variant impulse response function.

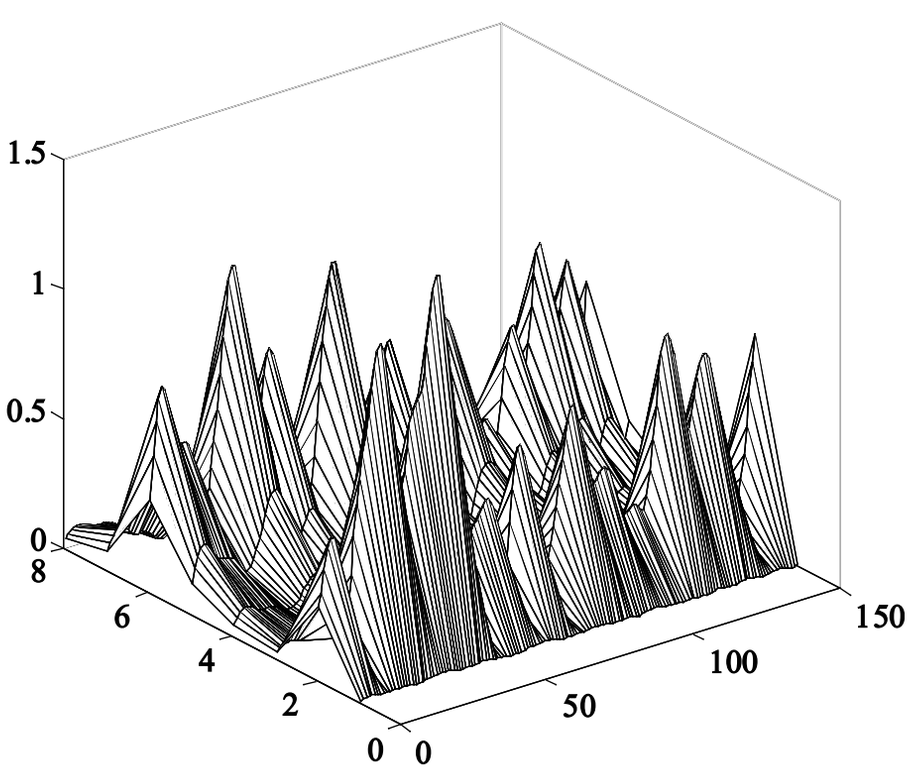

Figure 3: Example for a time variant impulse Response Function

Summary

A platform for the development of algorithms for the digital baseband of UMTS mobiles has been introduced. In contrast to other solutions, this platform follows the philosophy of 'fine steps' during the development process. Source code can already be tested in a very early stage on the target DSP platform. By this is avoided that a lot of uncertainty is postponed to the end of the development sequence.

References

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[2] 3L-Diamond User Guide Version 2.4, May 2004.

[3] 3GPP TS25.101, V4.2.0, Ch. A.3.4, p. 50.

Measurement and Modelling of Electronic Devices for RFID Circuit Simulation

N. Christoffers

Introduction

Accurate device models are crucial to the design as well as to the debugging of RF-CMOS circuits. Transistor, coil, and capacitor geometries and materials are chosen based on circuit simulations which employ models known or estimated before fabrication. Only sufficient model accuracy allows a good agreement of predicted and measured circuit performance and hence chips meeting their specifications.

To maintain model accuracy as well as to analyse circuit behaviour post-fabrication measurement based modelling techniques must be used additionally. Hence, circuits can be resimulated after fabrication using updated models. Potential sources of errors can be revealed and eliminated such that the circuit performance rises at each technology run.

In this communication modelling techniques are described. Microelectronic coils are chosen as an example. Matlab is used as an interface between different modelling approaches. Mathematical algorithms for anticipation of coil parameters are combined with measurements and fed back into circuit simulations.

In Section 2 microelectronic coils are described in more detail a reasonable circuit model for them is proposed. In Section 3 the procedure of model extraction and simulation is outlined in more detail. It is based on numerical methods, on-wafer measurements and curve fitting in Matlab. Modelling results are presented.

In Section 4 the paper is summarized and an outlook given.

Spiral Inductors

A microelectronic coil is a spiral shaped conductor made of metal (e.g. aluminium) over a substrate. In CMOS the substrate material is typically p-doped and grounded conductive silicon. The difficulties associated with microelectronic coils are the parasitic capacitance of the spiral conductor to the substrate, the energy losses caused by currents flowing in the substrate due to induc-

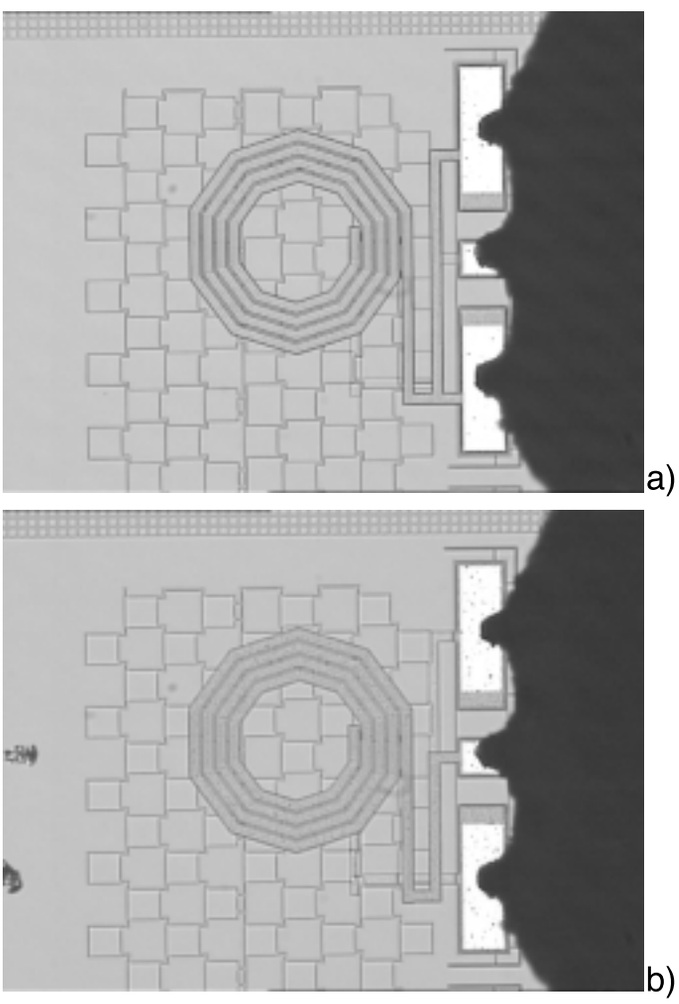

Figure 1: Chip-Foto of a coil with attached measurement-probe-tips
a) wound from the inside to the outside b) wound from the outside to the inside

tive and capacitive coupling, and the low sheet resistance of the thin metal layers in CMOS processes.

A circuit model taking into account all the effects mentioned above is depicted in Fig.1. In addition to the series inductance L_S and the series resistance R_S, it comprises a fringing capacitance C_0 between terminal A and terminal B to model the inter-winding capacitances. Also, the coil terminals are attached with a lossy capacitive connection to the ground potential including oxide and bulk capacitance. Note that this model implies that the coil is inductive only for frequencies below a self-resonant frequency. At these the quality factor of the coil is already degraded through the reactive currents flowing through C_{sia}, C_{oxa}, C_{sib} and C_{sia}. To increase the quality factor it is worth trying to increase the self resonant-frequency narrowing the conductor. But thereby the series resistance R_s is increased, and the subsequent quality factor degradation may reverse the advantage achieved by the increased resonance.

The parasitic components in the model reflect deviations of the coil behaviour from the desired behaviour. Its exact model must be known. Otherwise characteristics of RF circuits like resonances, reactive currents, gains, transfer functions or noise are not predicted correctly.

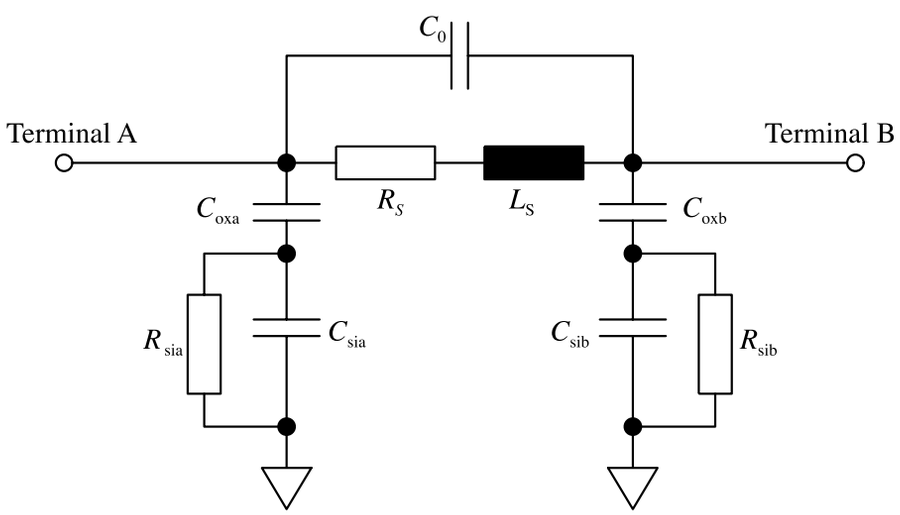

Figure 2: Schematic of coil model

Modelling method

A Matlab-Program to generate a coil model of the type depicted in Fig. 1 [1] forms the basis for a contiguous design flow with emphasis on accurate coil models. Each time it is called it reads s-parameter data from a text file and transforms them into y-parameters. Using a least square fitting algorithm it finds the component values of the model in Fig. 1. in such a way that the mean square deviation between measured y-parameters and those of the model is minimized. The component values can be automatically entered into a Spectre-netlist and appended to a Spectre-model-library. Using a suitable symbol-view it can be represented in a Cadence-Virtuoso schematic and simulated using Cadence-Analog-Design-Environment.

The text file can contain measurement data obtained using a Wafer-Prober and an s-Parameter-Network-Analyzer suitable for GHz-Measurements (both available at the IMS). Alternatively, the s-parameter data can stem from simulation programs specialized on coil analysis as ASITIC or FastHenry as well as

from FEM-Simulations. The text file can contain real and imaginary parts of s-parameters arranged in columns. But also measurement-equipment specific formats could be read. The CITI-file format used in our Agilent-Network-Analyzer is already implemented as an example.

Figure 2 shows chip-fotos of an accurate measurement of coils. Two identical coils are measured in two ways. In the first experiment the outermost winding of the coil is connected to the signal source of the Network-Analyser via the middle probe-tip of a ground-signal-ground RF-Probe. The innermost winding was grounded. In the second experiment the RF-current is flowing in the opposite direction. The VNA measures the reflection factor s_{11} for both experiments and stores it too disk. Chip-area could be saved at the expense of accuracy if a single coil would be measured using a full two-port measurement. The reduced accuracy in the catter case stems from the high sensitivity of y-parameters to s-parameter errors.

Figure 3 shows the measured and simulated inductance and quality factor of the coil excited at the innermost winding and grounded at the outermost. The simulation has been carried out using Matlab and the model-extraction tool. The deviation of measured inductance to the simulated is low in a frequency range from 1 GHz to 6 GHz. Figure 4 shows the simulated impedance of a coil model found using Matlab in comparison with the admittance of an AHDL coil model generated by Cadence in terms of real and imaginary part. The Matlab model was extracted using s-Parameters measured at the terminals of the AHDL model. Even though the Matlab-model is very simple it is possible to compute currents and voltages flowing into the coil very accurate.

Summary

Device modelling is crucial for the Design of RF-CMOS circuits. To obtain the highest possible confidence it has to be assisted by measurements. Such measurement-based simulation methods are most attractive if they are seamlessly integrated in the design and simulation flow. In this communication it was shown how an on-wafer measurement of a microelectronic coils was carried out using a wafer prober and a network analyzer. Simply by feeding the measurement results to Matlab a Spectre-Netlist readable by Cadence was generated automatically. In such a

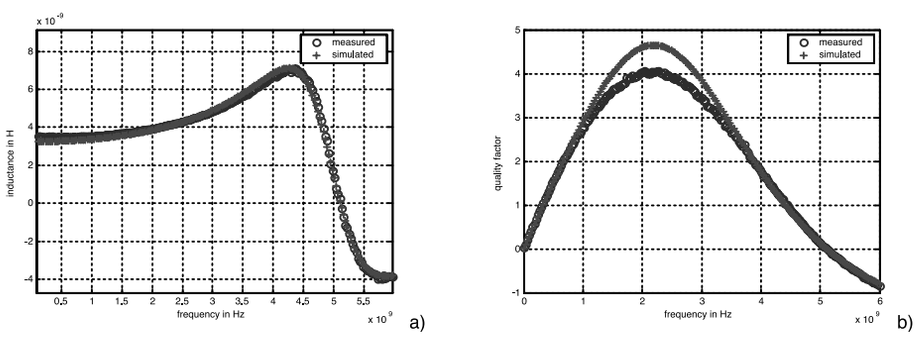

Figure 3: Simulated and measured a) inductance, b) quality factor (Matlab)

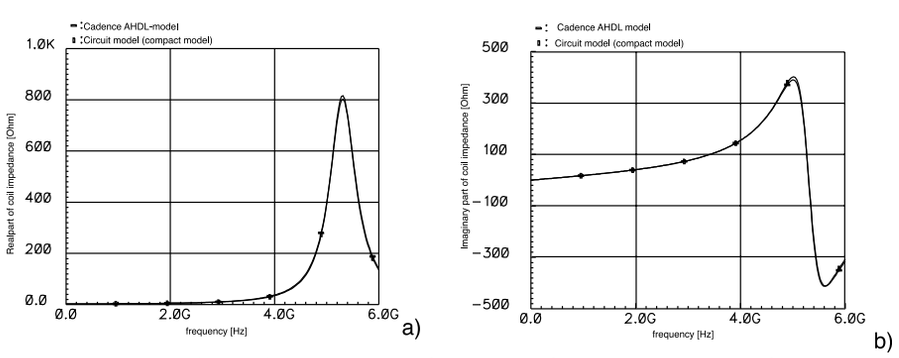

Figure 4: Simulated a) real, b) imaginary part of an inductor from the circuit model of Figure 2 and from an AHDL-model generated using FastHenry

way a model can be employed in circuit simulations that describes the coils as they are after fabrication. The simulation results, therefore, do not rely on theoretical predictions based on parameters known only inaccurately before fabrication. Such simulations complement those obtained using models found using specialized programs for coil analysis.

Note that the current accuracy of the model was obtained using a very simple equivalent circuit. By adding more components to the circuit model it's accuracy will even rise.

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System Simulation of Wireless LAN and Sensor Networks

T. Stücke, N. Christoffers

Introduction

There are a variety of wireless communication systems, which are located in the private ambience of the human beings and also at a industrial environment. To design successfully such a complex wireless system it is necessary, that an appropriate system level design is performed during an early design phase. To fulfill this important duty, several parasitic effects of a practical system must be considered.

A practical receiver must cope e.g. with noise, non-linearity of the stages and depending on the used architecture with DC offsets and I/Q mismatch or with image rejection. There are different origins for non-linearity in circuits, which will cause problems as harmonics, gain compression, desensitization and blocking, cross modulation and intermodulation. The noise sources are e.g. thermal noise, 1/f noise and phase noise.

In case of sinusoidal input signals it is possible to calculate the system performance simply using an EXCEL sheet (level diagram). However, practical signals exhibit a larger bandwidth, and can not be approximated by sinusoids. Hence, various problems will occur. For example, the actual influence of filters is unpredictable by level diagram, only crude estimation is possible. It is also important to deal with the aliasing components, which arise from sampling of the ADC or the algorithms from the digital part, which have also a great impact on the system performance. Therefore, a system simulation is indispensible to evaluate the resulting performance of the whole system.

The system simulation must consist of a model of the analog front-end and the digital part, which can be integrated in a flexible system simulator to determine and to verify specifications of the whole front-end or of its single stages. The whole system performance is finally determined by the bit error rate (BER), where the upper allowed boundary is specified by the corresponding wireless standard. But the simulation must deal with the problem, that the RF-signal bandwidth is several decades lower than the carrier frequency. An adequate baseband model is absolutely crucial, to avoid a nearly infinite simulation time when time consuming BER curves shall be computed.

The system simulation allows to evaluate the resulting BER for the considered system architecture and accompanies the design during all phases. Thereby wrong decisions will be prevented on system level, the time to market can be reduced and this reduces costs efficiently

In the following Sections, by means of the two system examples WLAN and ZigBee, will be shown how the system simulation can evaluate the resulting system performance and reveal effects which can not be predicted by pure analytical methods.

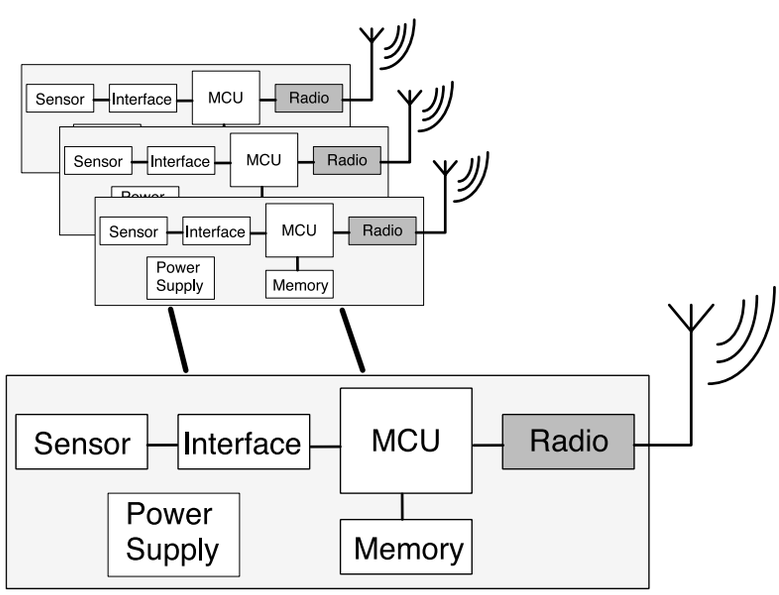

Figure 1: Wireless Sensor Networks

System Example – ZigBee

According to the previous Section, a successful radio level transceiver design should be assisted by a proper system simulation. This will be shown by means of the system example ZigBee. Due to the high abstraction level it was chosen perform simulations with Matlab. Matlabs allows to have the simulation algorithms and hence the simulation speed completely under control of the system designer.

ZigBee is defined by the IEEE 802.15.4 standard and is intended for communication systems with low data rates, allowing reduced protocols and short duty cycles. By this, a battery durability of several years becomes feasible. A growing market for ZigBee is expected, since there is a large a diversity of applications: Light switches in great halls, alert sensors such as smoke detectors or housebreaking sensor etc. Often, sensors and actuators are far away from other electric installations, making expensive cable installation necessary. This can be avoided by wireless systems. An additional field of applications is the monolithic integration of sensors – i.e. for temperature, light or pressure sensors Wireless sensors can form a self organized sensor network which can be sold for an favorable price. Such networks can be installed in offices, private houses or in industrial environments.

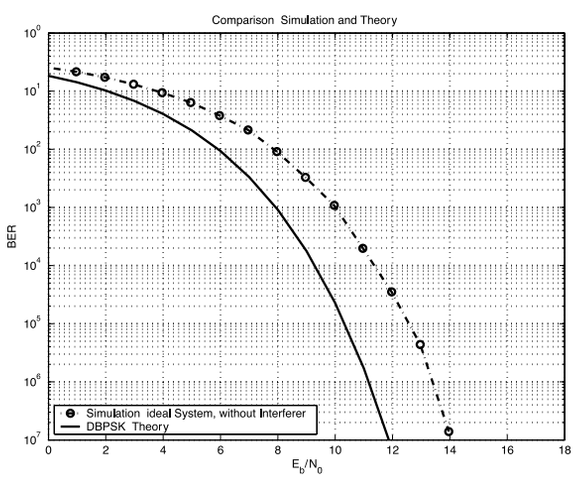

Figure 2: Comparison of theory and simulation with practical realistic filter

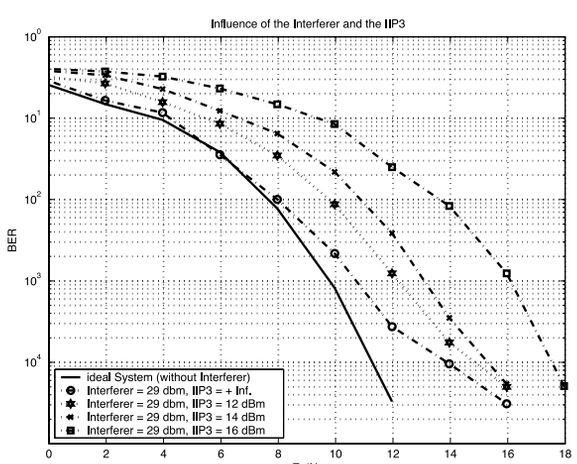

Figure 3: Influence of the interferer and the IIP3

As an example, a wireless sensor network can comprise of several ZigBee transceivers units with integrated sensors. As depicted in Figure 1, a transceiver unit consists of a sensor and its interface, a micro controller with memory, the power supply and the radio itself. The BER performance of a practical receiver is degraded by the radio front end. According to the first Section a model for such a receiver frond-end can be derived and integrated in the flexible system simulation to evaluate the resulting BER performance.

At first simulation result, Figure 2 show the comparison of the theoretical curve of DBPSK with the model of the receiver chain. The deviation from the theoretical curve can be traced back to the fact, that bandwidth of the practical antialiasing filter is higher than the bandwidth of the matched filter which was assumed for the derivation of the theoretical DBPSK curve.

A very strong interferer of -29 dBm is assumed to determine its influence. This simulation result is depicted in Figure 3.

In spite of an assumed linear receiver the curve starts to deviate at low BER value. Since the antialiasing filter is not a brig wall filter which have infinite attenuation in the cut-off region, this yields a aliasing effect and thereby to a degradation of the BER performance. If a nonlinear behavior of the receiver chain is supposed, the BER curve will be shifted toward higher Eb/N0 values which can be seen also in Figure 3. This yields for example to a severer specification for the receiver NF.

It is also important to deal with a proper choice of the filter bandwidth. On the one hand, a smaller filter bandwidth leads to a lower noise power and to a stronger attenuation of the interferer. On the other hand, if the corner frequency is to close to the desired signal, the performance will decreased as well. This is especially the case, if the receiver should be realized in CMOS technology with typical large process tolerances. Figure 4 shows the simulation results with different 3-dB corner frequencies of the antialiasing filter. The BER curve for the 150 kHz antialiasing filter is almost identical to the theoretical BER curve of DBPSK. However, this choice results in an unpractical receiver design.

This results could never been obtained by pure analytical methods, which could be implemented in a level diagram. This inside can only be obtained by a proper model of the analog part which can be integrated in the system simulation.

System Example – Wireless LAN 802.11a/g

System simulations carried out using Matlab have to be complemented by Cadence-Simulations. The Cadence-software allows to simulate models at different abstraction levels in the same testbench. For instance, a filter at the output of an analog receiver can be modelled at circuit level using transistors, capacitors and resistors whereas the preceding stages are described using AHDL as equivalent baseband models. Also, it is possible to create interfaces from Cadence to other simulators as Matlab or Simulink, e.g. using Aptivia. Investigations of such a type allow a seamless and careful descend from a high abstraction level to the circuit realization.

It is not indispensably necessary to have a digital front-end designed to carry out a proper post-processing of analog output signals. The Cadence Design Systems GmbH in Munich has designed a Skill post-processing tool for WLAN-Signals as an example. During this task the IMS Duisburg has consulted them in terms of digital signal-processing. The post-processing is linked into the Cadence Analog-Design-Environment and can be accessed via the calculator function in the Waveform-Window. It can process equivalent baseband signals obeying the 802.11a/g standard for OFDM and QAM16 modulated carriers.

A screenshot of the post-processing control dialog is given in Figure 5. The user is allowed to set the circuit nodes where the equivalent baseband signal can be measured at. He can also specify a reference signal the received signal is compared with to compute bit-error-rate (BER) or error-vector-magnitur (EVM). The tool is also capable of carrying out a pilot-based delay calculation (time synchronization). To carry out trade-offs from the viewpoint of analog/digital codesign it is also possible to specify an oversampling of the analog signal. Thereby the influence of an increased or reduced ADC-sampling rate can be simulated.

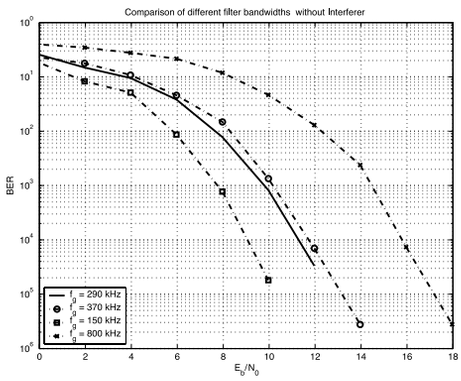

Figure 4: Comparison of different filter bandwidth

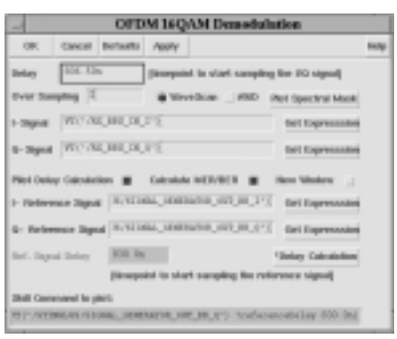

Figure 5: Dialog of the OFDM-post-processing tool

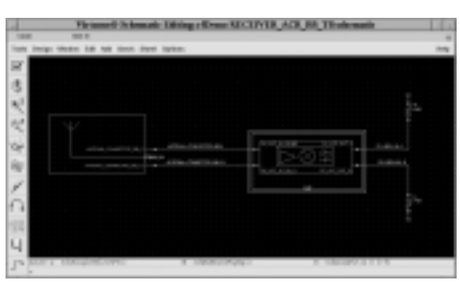

Figure 6: Adjacent channel rejection testbench in Virtuoso

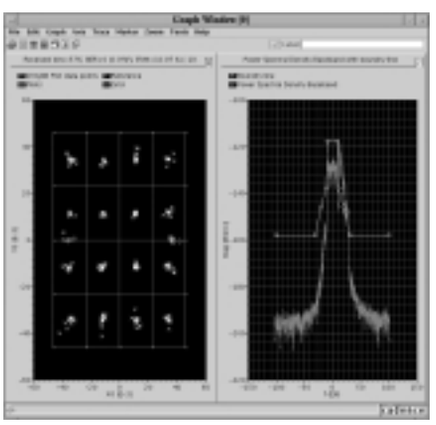

Figure 7: Constellation diagram and spectrum of received signal for OSR = 1 in Wavescan

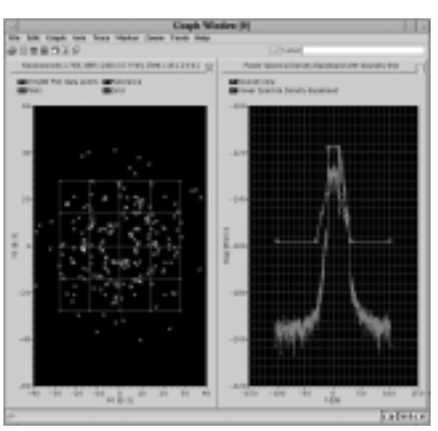

Figure 8: Constellation diagram and spectrum of received signal for OSR = 2 in Wavescan

A WLAN receiver testbench drawn in Virtuoso is shown in Figure 6. The aim of the testbench is to check the receivers capability of adjacent channel rejection. The receiver itself comprises AHDL models of LNA, mixers and baseband filters. A simulation result obtained using the testbench and the post-processing tool is shown in Figure 7. The left half of the screenshot shows the constellation diagram at the receiver output which is apparently undeteriorated by an adjacent channel signal. The right half shows the power spectrum at the output of the receiver and makes the interfering signal visible. It can be seen that the baseband filters are not capable of suppressing it completely. A complete suppression would require more expensive or narrower filters. The latter, however, would cause significant phase distortion within the signal band and thereby reduce the receiver performance.

The reason why the receiver worked well in spite of a strong interferer was the filtering of the signal in the digital part simulated by the post-processing tool. Note that the Nyquist-criterion requires sufficiently high sampling rate to process the interferer digitally. The over-sampling ratio is the ratio between actual sampling rate and rate required for the desired signal. To obtain the results of Figure 7 it was chosen as two. A lower over-sampling ratio would allow a lower power consumption of the digital part. However, the constellation diagram looks like depicted in Figure 8. There is no reception of signals possible since the interferer falls into the signal band due to aliasing.

Conclusion and Outlook

The system simulation shows precisely the influence of the different factors on the whole system performance on high abstraction level. Therefore, it becomes possible to evaluate directly the resulting BER curve based on the considered receiver system. For example the presence of an interferer at the input of a nonlinear front end can be simulated and also the influence of a practical antialiasing filter. Assisted by high level simulations it is possible to derive and verify specifications for the single receiver stages. The system simulator (Matlab or Cadence) can also be used to develop algorithms for the digital part like carrier frequency-, chip- and frame-synchronization or to test their performance. Therefore it supports an analog and digital co-design. It is also possible to use the system simulator for debugging if a problem is encountered in the receiver chain.

The model itself will be extended by phase noise and 1/f noise. Furthermore, the desired signal and the interferer can be implemented with varying signal power and an algorithms to simulate the function of an AGC. With respect to the used frequency band, it could be useful to model an interferer as a ZigBee, GSM, UMTS, Bluetooth, RFID or a WLAN signal. If for example the target application is a sensor network in an industrial environment, some special interferers have to be considered. The current model assumes a simple AWGN channel. Therefore, it could be advantageous to implement a more realistic channel model, e.g. a special indoor channel model.

In summary the level diagram provides just a helpful short overview while the system simulation considers the influence of many effects in the analog and digital part and thus forms a good basis for successful radio level transceiver design.

A System-on-Chip Emulator for new Bluetooth Baseband Concepts

M. Marx, M. Holzapfel, H.-C. Müller, R. Kokozinski

Introduction

Bluetooth technology (BT) is a standard for shot range communication in the scientific and medical (ISM) band at 2.4 GHz with the aim to eliminate cables between both stationary and mobile devices.

At the department of WCS a digital base band prototype for this standard has been developed that is suitable for use as an IP core on system-on-chip ASICs. The IP includes a hardware-software co-design. Time critical functionalities have been hard coded whereas more complex upper layer protocol functions are realised in software, running on the included IM3311 micro controller (µC), compatible with the well known industrial standard M68HC11 [1], [2].

The prototype is implemented on an FPGA, enabling together with a debugger software for the µC an efficient evaluation and verification of different base band concepts and protocol implementations.

Prototype architecture

Functional, the entire base band system can be separated into a digital physical layer system (PLS), responsible for the transmission of the rough bits and an upper layer protocol system (ULS), implementing medium access controlling and data link management. Figure 1 shows the architecture of implementation. The ULS is partly hard coded (coding unit) and soft coded (in firmware running on the µC Core).

Physical layer system

In the PLS, primary modulation and demodulation functionalities are implemented. By doing that completely in the digital domain, performance degradations due to inaccuracies inherent the manufacturing for analogue implementations have been prevented.

For demodulation, a new zero crossing (ZC) approach together with a low intermediate frequency (IF) architecture has been deployed, requiring only a limiter to convert the IF Signal to the digital domain instead of a more elaborate implementation for an analogue to digital converter (ADC).

In the zero crossing demodulator, the periods between consecutive zero crossings of the limited IF Gaussian Frequency Shift Keying (GFSK) signal are measured by means of a fast clocked counter. In Rx mode the output signal is switched to a digital filter, which is designed for optimal suppression of

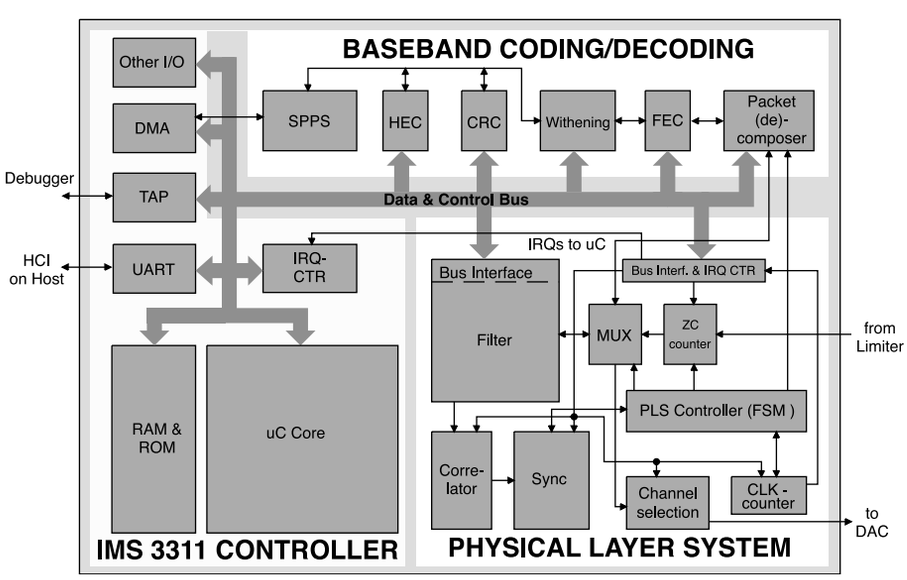

Figure 1: Architecture of Implementation for Bluetooth base band SoC

inter symbol interferences (ISI) within the received data bursts [3]. Since bluetooth uses a time division duplex (TDD) scheme, the filter architecture is shared for both Tx – and Rx mode and operates at higher clock frequency, enabling additional sharing of multiplier – and adder (MAC) units.

The equalized data bursts at the filter output in Rx mode are correlated with a local a priori known "Access Code" (AC), which marks the start of a packet. If the AC of an incoming packet correlates "well enough" with this AC, the internal clock will be re-synchronised and the synchronisation unit tracks onto the optimal samples within the over sampled received data burst.

In Tx mode, the data bursts from the upper layer system are pulse formed and delivered to a synthesiser in an analogue front end. Figure 2 shows a BER curve of the PLS.

Upper layer System

The ULS is responsible for data link functions of the bluetooth system like medium access control, framing of bits, error handling and link management.

For all required framing and error handling functions a dedicated logic implementation (coding unit called) is used to provide a low power solution whilst providing the required data throughput. The error handling functions implemented in hardware include forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), and data whitening.

The packet composer and decomposer units gather the data segments of AC, packet header, payload and CRC bits into frames and exchange them with the PLS.

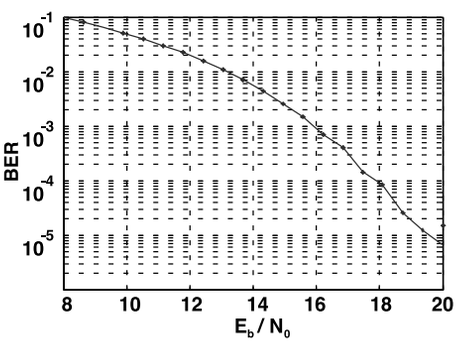

Figure 2: BER curve of BT path

Medium access control has been implemented as hardware software co-design. The firmware corresponds closely with a hard coded state machine within the PLS, which controls time critical functions like switching between Tx and Rx modes, handshaking with coding unit and controlling of counters.

Link managing has been implemented within firmware running onto the µC core.

A direct memory access unit enables autonomous access to ready packets within memory, thus saving resources of the µC.

The firmware interprets host controller commands (HCI) conforming with bluetooth standard. It can be controlled via an external host computer e.g. by RS232.

Designflow

First, the concept for the PLS has been verified by means of a system simulation. In reality the signal at the output of the PLS passes through the analogue radio frequency front ends (AFE) in both devices and the physical channel of the air link until it stimulates again the input of the PLS in Rx. For simulation, this real environment must be emulated. Limitations in afford allow here generally only a rough modelling of this real environment. This rough model describes only some basically issues of the reality.

A more accurate verification of the concept is possible by using a prototype of the PLS, embedded in the real environment. This enables a real time interaction of the PLS with the real environment. Thus the developing of a prototype has been placed very early into the design flow. The hardware

architecture of the PLS has been described by a hardware description language (HDL) and automatically implemented into an FPGA.

Parallel to the development of the PLS the development of the concept for the ULS had been started. The ULS implementation is a hardware software co-design und contributes interactions between the hard coded and soft coded partitions of the implementation. Thus, for efficient verifying an rapid prototype of the entire SoC, consisting of the PLS, the hard coded parts of the ULS and the micro controller core, where the ULS software parts are running on, has been implemented on an FPGA. This system emulates the later SoC for an ASIC and accelarates the development and verifying of the base band concept. The emulation is supported by a debugger software for the µC core, running onto a PC. The software communicates via an IEEE1149 protocol with the µC core and provides usual debugger functions like trace, breakpoints and so on. Figure 3 shows the emulator assembly. Since the prototype emulates the whole SoC Design, it responses to all interactions with the real environment in real time. Besides evaluating the performance with real AFEs, this approach enables also real time interactions with higher layer protocol systems, thus facilitating developing and testing of software, communicating with such higher protocol layers running onto an host PC.

Summary

A SoC emulator system has been developed, which enables efficient and realistic design verification of different base band concepts. The interaction with real environment in real time enables more accurate verification and no afford for emulating this interactions. Base band functionalities implemented in software are tested significantly faster as in simulations.

The design deploys a new zero crossing demodulator yielding area and power economic ASIC designs.

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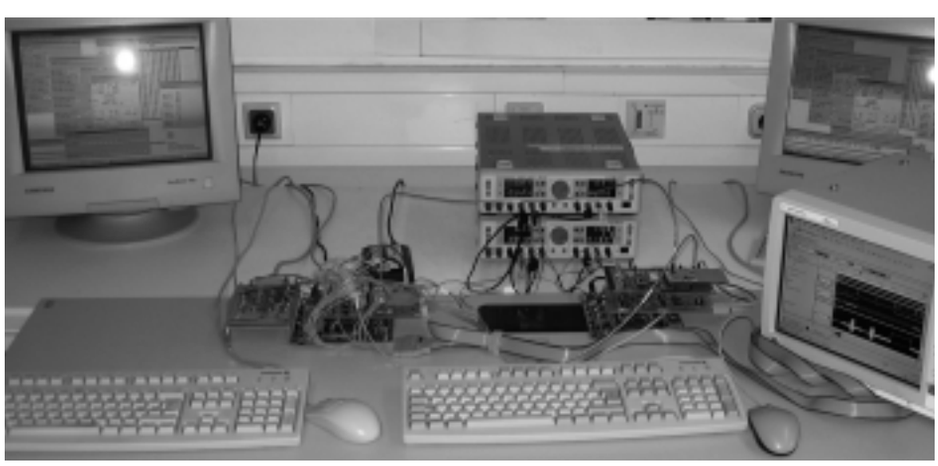

Figure 3: Assembly of Emulatorsystem with two bluetooth SoC's. Internal registers are visible via debugger software

Open Service Integration for Ambient Intelligence Systems

K. Scherer, V. Grinewitschus

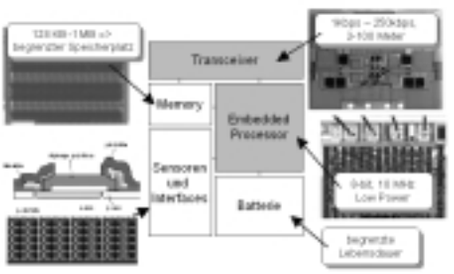

Figure 1: Typical embedded microelectronics with computing power and connectivity

Abstract

Ambient Intelligence (AmI) is the information-technology intelligence surrounding us in everyday life and is used as a helpful assistant to human being.

With automobile industry, this vision has to a great extent already become reality; in the house and in the household, however, this holds true for fragments only. Many research centres, demonstration facilities and pilot projects keep investigating, implementing, testing and demonstrating information-technology in networked intelligent systems embedded in diverse application environments.

The present article attempts to discuss technology aspects and applications using selected AmI examples in smart houses and households. These examples are R&D results from the inHaus innovation centre for intelligent house systems of the IMS (www.inhaus-duisburg.de). The main technology focus will focus on open system integration technologies for ambient intelligence systems.

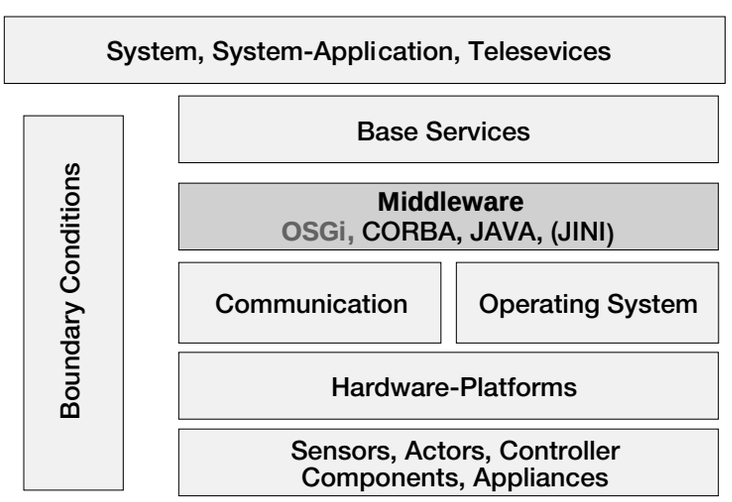

Figure 2: Layer model of open integrated house systems using middleware

1. Introduction

1.1 Devices and components capable of system-integration

Microelectronics allows for the integration of affordable computing power in almost any user-defined devices and components.

Needless to say, washing programs of today's washing machines and control systems of heating facilities run on the basis of microprocessors. Also for sensor signal processing in smoke detectors a microprocessor is used. However, the interesting question is whether these single intelligent or smart components are capable of exchanging relevant data with other smart components (inter-connectivity) or whether they are even able to co-operate with each other to ensure profitable system functioning (inter-operability).

If these components have neither interconnectivity nor interoperability, we will be facing a smart black box which forms a functional island. Such functional islands could also be subsystems with proprietary cross-linking. Examples of these are heating systems, master key systems and alarm systems of certain manufacturers.

Image 1 shows a typical embedded ambient intelligence component, as for instance for a wireless networked smoke detector with separate energy source, voltage sensors, memory, processor and a RF-transceiver (e.g. ZigBee to come). Such electronics can also be found e.g. in washing machines, cars and heating systems.

1.2 Feasibility of internal and external networking

The range of networking technologies for the internal and external inter-

linkage of AmI systems is enormously manifold. Concerning its profitableness and utility for certain applications, it is comparably complex for laymen and experts to make implementation decisions.

Examples of networking standards for the house and household are:

1. Internal networking: KNX, LON, LAN/Ethernet, WLAN, BlueTooth, (ZigBee)

2. External networking: ISDN, DSL, broadband cable, GSM/GPRS, UMTS

Many of the standards mentioned are itemized along several layers of the OSI/ISO-model, while concrete implementations of data interfaces contain only parts of it. For the most part, these standards are specified for multiple transmission media such as twisted pair (TP), power-line (PL), radio frequency (RF) or coax cable (CX).

Since all of these methods serve for the transmission of manifold information with manifold different transfer rates and network typologies, our aim is not to answer the question which one single networking standard is the only one to chose for AmI systems solutions. Adding economic aspects and other boundary conditions such as data security to your considerations it will thus make it easier to retrace the complexity of the networking decisions subject mentioned above.

A further aspect of consideration is the inter-linkage of the network standards with certain fields of application and the market. For instance, Ethernet including the TCP/IP protocols represents the classic standard for the networking of personal computers, while ISDN is the standard worldwide recognized for networking of telephone applications. Last but not least, WLAN takes a position as the standard traditionally used for wireless networking of diverse applications. We may therefore note that all the remaining other standards represent useful supplementary standards at the low end of the hierarchical scale (e.g. BlueTooth).

2. Open Integration Technology for AmI Systems

2.1 Integration servers as key components

In order to manage the difficulties brought about by heterogeneous networking technologies of today and the future [4], [5], three server types are to be considered as possible central AmI system integration components:

1. webservice integration platforms which serves to bundle external webservices, e.g. senior care, video-on-demand, housekeeper services, television and radio if required; this server can also be operated as a campus server by a service provider; the webservice platform is interconnected with the service gateways and the multi-media servers in local AmI networks;

2. multi-media personal computer servers which are interconnected with the internal intranet of e.g. a household for television, radio, video, visual data, sound, internet, personal computer functions, data storage of all kinds,

3. embedded control servers which are responsible for automation of e.g. house subsystems (light, heating and alarm system, security); this component which is inter-linked with the external webservice platform and the internal AmI network is also called Residential-Gateway or Service Gateway.

2.2 Open system integration by middleware

Middleware stands for a software layer between the hardware components and the software itself. Even an operating system belongs to middleware already. Middleware in a narrow perspective of the word involves the provision of abstraction features for data and functions. It leads to greater transparency towards the application programmer concerning the enormous heterogeneity and complexity of lower system layers which include various hardware components, operating systems, computer languages and networks.

For example, in a heterogeneous and distributed system, remote event messages become detectable, distributed transactional processes become programmable and methods of an object on a remote station become available to the application programmer.

The implementation of a middleware system layer conceals the fact that messages, function requests and results have to be transmitted via networks and data busses within a distributed system.

Image 2 shows the positioning of the middleware within a layer model for a complete system: it is located between the operation system layer and the basic services, which are the fundament for any functions of an open integrated AmI system.

With this, a middleware layer provides the programmer with a universal platform, which is as consistent as a computer operating system.

Additionally, continuous programming of system functions by means of the portable JAVA-code offers greater flexibility in operating the system and reasonable protection of investment as regards the software solutions of the application layer.

Meanwhile, the Open Service Gateway Initiative (OSGi, for short) counts several hundred members worldwide including important producers of all market segments.

The Residential Gateway mentioned above represents a suitable implementation platform for an OSGi-middleware layer. However, by adding an OSGi-framework including JAVA-communication and application programmes (cp. Image 3) it resembles more and more a system-integration- and service-management-module [4].

On principle, it is feasible to implement an OSGi-service-manager inclusive of network-integration functions on a

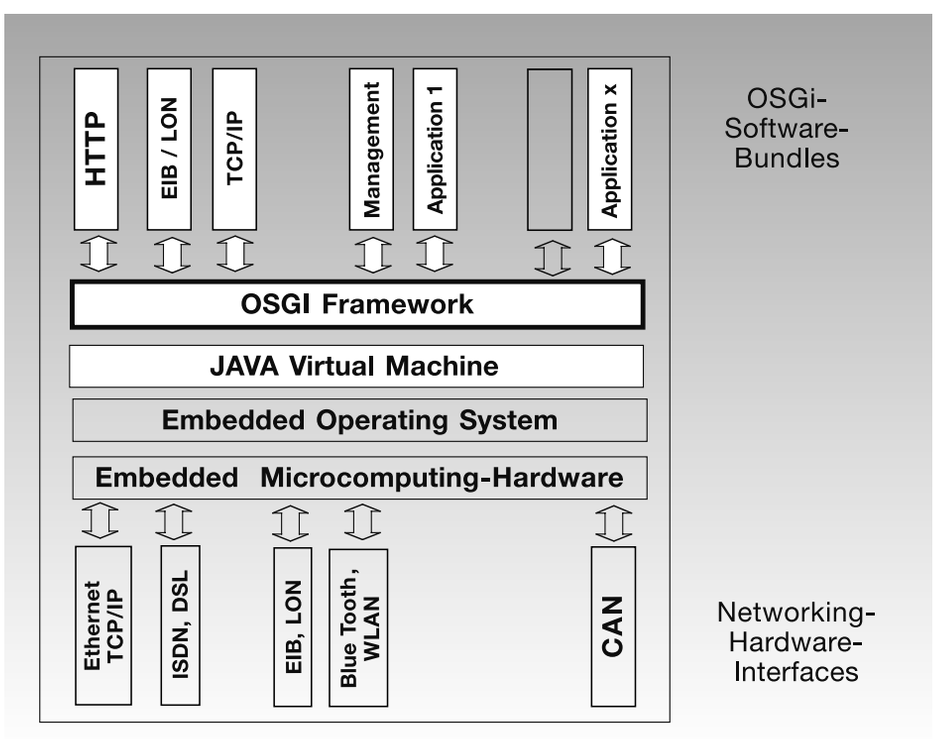

Figure 3: Architecture of an Open-Service-Gateway

personal computer, as for instance the Home-Multimedia-Server-Computer. In this case the operating system, e.g. Windows-XP, is supplemented with the OSGi-framework using a JAVA-virtual-machine.

This way, diverse bus- and network segments in the AmI system can be operated by the communication-, service- and application-software-modules (OSGi-software-bundles, cp. Image 3) via interface cards, which are inserted into the personal computer.

Since this personal computer is also used for various applications as well as for entertainment functions such as Internet, CD, DVD, there is the risk of facing negative effects on system automation caused by these applications with lower reliability requirements of the software.

It is therefore reasonable to outsource the local automation functions and services with their necessary network integration functions into a highly stable, energy saving system manager module (which is also called residential gateway).

This module can be attached to the port terminal point of e.g. a house AmI system in the form of a top hat rail component. It is permanently active and always connected with the services of the internet for instance via a DSL-flatrate [3].

way can be seen in the multitude of operating units and concepts of manifold types

In order to solve this problem a solution based on the embedded Server-Gateway with WLAN-networked PDA has been developed for the intranet of the inHaus Centre at IMS. This solution has been tested with applicants and proven to be a success (cp. Image 4).

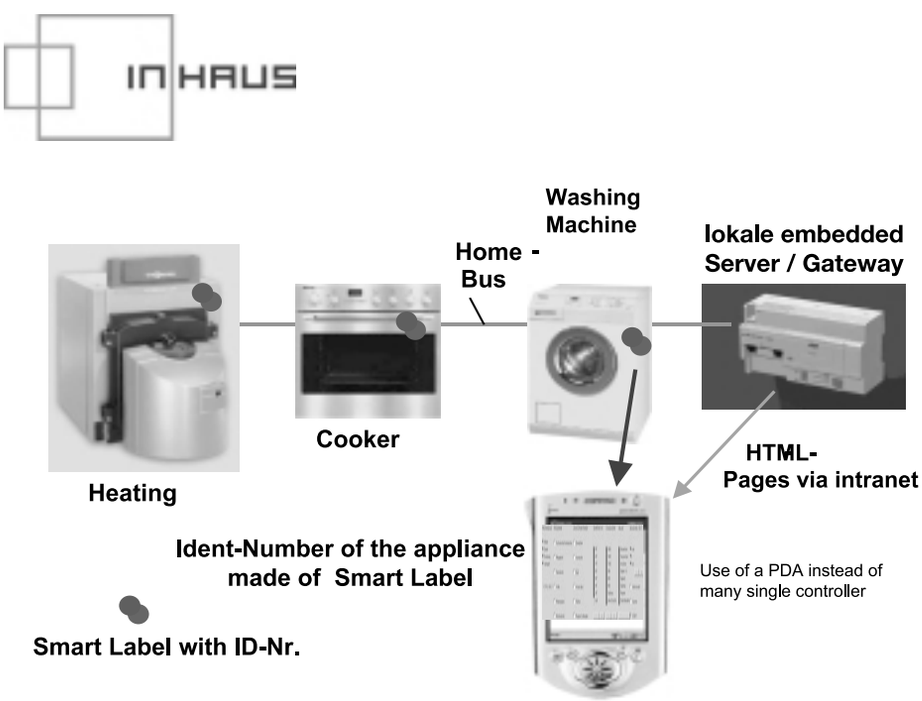

Figure 4: AmI based integrated system operation

3. AmI Application examples in Smart Houses

3.1 Integrated system operation

One of the most outstanding inconveniencies of modern households, which are crammed with electronic devices in an extremely non-systematic

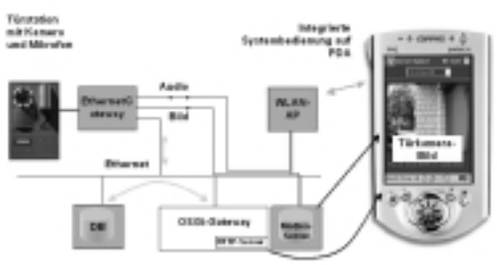

Figure 5: Integrated sound-and-vision via PDA and door station

Devices, which are connected with the house-intranet are identified by a smart-tag reader in the PDA. The corresponding operation interface is automatically loaded onto the web-browser of the PDA via WLAN. Thus, whenever the user approaches a certain device in the household the corresponding operation control interface (MMI, man-machine-interface) appears automatically on the PDA as from ghost hand. From the user's perspective, the PDA thus represents the only remote control of the complete household.

3.2 Integration of data in sound and vision

The integrated system operation unit cannot only be used on the PDA to control narrow-band signals via the internal intranet of the house. In the same way, multimedia function networks for attractive applications are feasible.

When a visitor appears at the entrance door, this is recognized by the motion detector device. This way, a communicative process with exchange of visual data, voice-recognition data and control data between the PDA-system operation unit, the door-station and the house-information and communication network-infrastructure including the OSGi-Gateway-Server is established (cp. Image 5).

3.3 Integrated surplus value services

The most complex and therefore probably the most efficient kind of novel embedded system functions is certainly represented by those process flows, which integrate the internal and external information and communication infrastructures of the house [3].

In the external area, these are services bundled via web-service platforms, as for example the delivery of pharmaceuticals permanently required by the elderly or by ill people. For this scenario, the physician, the chemist, the delivery service as well as the household have to be made interoperable within an open networked information-and-communication infrastructure. The components of this scenario include an electronic prescription, an electronic order, a networked delivery box near the house and a networked intelligent medicine cupboard in the household (cp. Image 6).

If the health-care-management-software identifies a shortage of pharmaceuticals on prescription in the medicine cupboard via the Service-Gateway, the pharmaceuticals required will automatically be reordered from the internet-pharmacy via email. The delivery service of the pharmacy will then deliver the products into the home-box of the household (access permitted, for example, by means of smart-cards). In turn, the networked home-box recognizes the delivery and reports it to the occupant, either to his mobile phone or to his office computer.

The system is also capable of supporting the occupant concerning correct

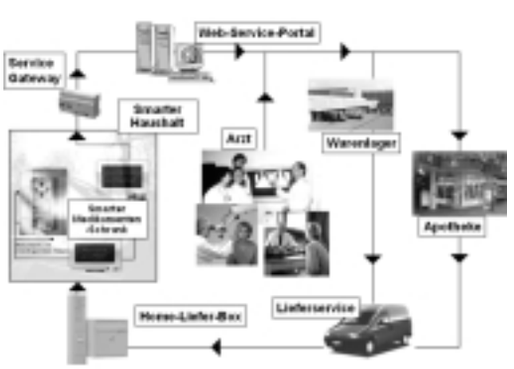

Figure 6: Integrated delivery service of pharmaceuticals

consumption advice of the pharmaceuticals, if this is desired.

This system is currently being developed and tested as a prototype at the inHaus Centre in Duisburg [2].

4 Summary and future developments

So far, digitalisation of life and development of software and intellectual property (short: IP) has already lead to significant advances in convergence which stands for the coalescence of devices, functions and services. We expect this tendency to keep growing.

Latest software technologies, which will be expedient for the intranet in AmI systems have already come into sight. Just to give an example, mobile software agents will soon be executing certain specific tasks within a networked environment [1].

But if technological development of complex AmI systems does not correspond to the appropriate development of cooperative and systemized marketing, installation and maintenance, the problem of non-profitable fragmentation of the solutions will last.

The end user desires an embedded system, which adapts itself to the requirements including easy and consistent operations.

Therefore, we need novel cooperation networks combining partners of all kinds. All of the technologies and applications described are part of an overall integrated system with an open standardized reference architecture.

These components, devices and services in e.g. AmI households and houses will be openly integrated by Service-Gateways, Multimedia-PC-Servers and Web-Server-Platforms. As regards the external world, they will be more and more connected to various surplus web-services via the internet.

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Active transponder systems for wireless measurement of forces in tensioning devices with optimised power-management

G. vom Bögel

Introduction

When it comes to increasing the efficiency, safety and endurance of machines in production, the gathering and processing of operation conditions like tension devices becomes more and more important. The use of manifold sensors is state of the art in modern automation processes. The collection of sensor data from moving and rotating parts by means of wireless technologies makes great demands on microelectronic systems. Values of interest are tool carriers in rotating spindles and work-holding devices in machine tools. Further applications include measurement of contact pressure in clutches and screw joints.

Wireless transmission lines should meet two major requirements. In spite of massive metallic parts and interference from drives the transmission has to operate safely. Furthermore, additional expenditure for maintenance work, such as frequent battery changes on sensor modules, is not acceptable.

Approach

The progress of integrating complex circuits has lead to improvements concerning the functionality and performance of systems, even in the area of RF front-ends. For instance, the development of bluetooth provides evidence that it the realization of low cost and single chip radios is feasible. This step of innovation can yet be assigned to further applications, such as automation. In order to introduce a system on a wide base, a common concept covering a wide range of requirements is necessary. Therefore, the approach selected here combines two transmission methods which can be used alternatively or in parallel.

Figure 1 shows a block diagram of the system. It consists of a mobile sensor module called sensor transponder and the respective reader.

The sensor transponder can be operated in passive as well as in active mode. The short range transmission channel runs on the 2.45 GHz ISM frequency band and uses a bi-directional (symmetric) data transmission scheme.

An RF-front-end which provides 100 channels in the used band was chosen here in order to execute the operation in disturbed environments and to allow a parallel transmission of various transponders. As a consequence, "hopping" to any free channel becomes feasible.

The second transmission line operates on a low frequency (LF) band at 125 kHz and uses the modulation principle of passive transponder systems called absorption modulation. The LF transceiver within the transponder provides an energy-saving feature. In this case the transponder can be activated from stand-by mode via a wake-up command. In addition, the LF front-end

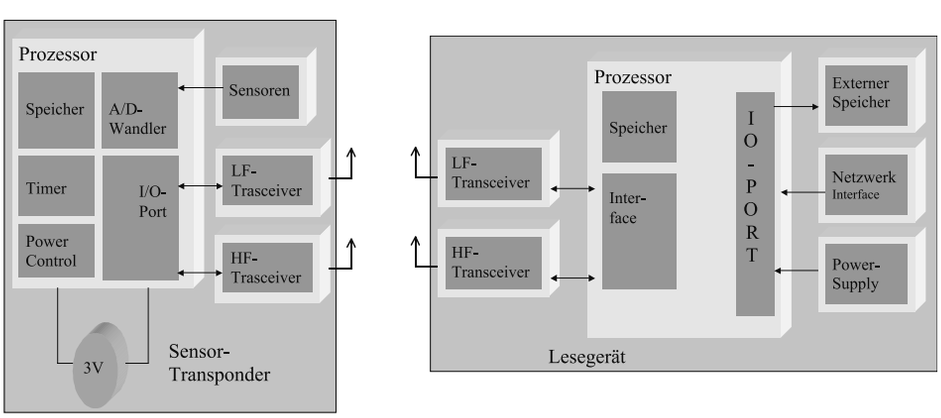

Figure 1: block diagram of a transponder system with dual transfer matrix method

comprises a carrier-detect function which can activate the processor at power-down mode by means of a transmitted code word. During phases of low-activation the transponder can be launched to an energy-saving mode. With this, only the front-end consumes energy at very low stand-by power.

In addition to the energy saving front-ends, also the residual circuit has been designed for the least possible power demand. As a processor, we chose a low-power risc controller with an operational current of less than 200 µA. The controller contains an A/D-converter with a multiplexer for the activation of multiple sensors. The system presented here in its current realisation is designed for the measurement of forces. For this, a novel sensor has been integrated which is well suited for telemetric systems due to its high resistance. The sensor is made up of a hard material layer which measures only a few micrometers. It is based on adamantine carbon and it is extremely wear-resistant and resistant to corrosion.

Unlike commonly used force and pressure sensors which function on the principles of bending and elongation, this system remains almost fixed. The measurement of force results from a change in electric resistance in which the layer receives only a marginal deformation in the range of nanometers, even with high charges. Thus, the application can immediately be effected at the frictional connection of the components. The mounting of additional joints is not necessary.

Results

The telemetric system has been developed for the following fields of application:

- The measurement of tension forces of work-holding devices. The aim of this application is the continuous surveillance of the tension force during the working process. The clamping jaws comprise force sensors. Here, the transponder is battery-operated and works in the active mode. The LF-line provides for the activation of the transponder; sensor data are transmitted via the HF-line at high data rates.

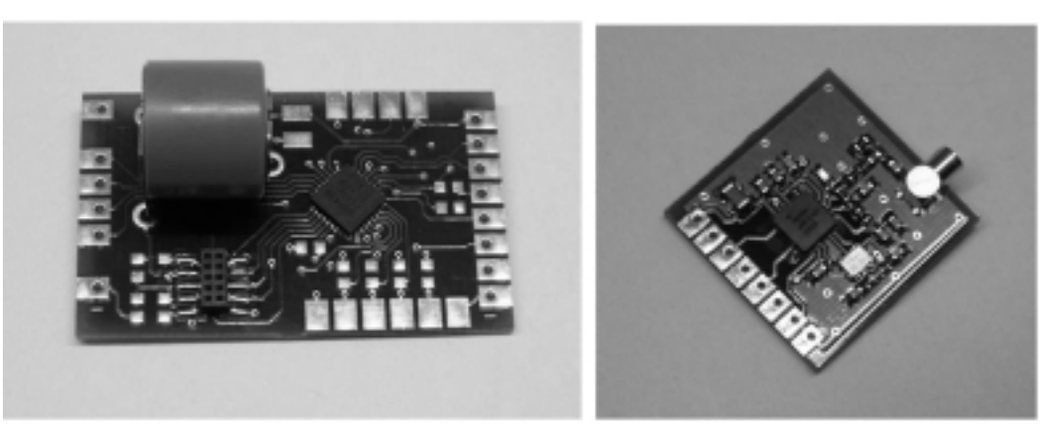

Figure 2: transponder processor and HF-circuit

- The measurement of tension forces of tool fitting in spindles. With this, the correct fitting of tools is monitored. Energy is transmitted via the LF-line, the transponder is thus working in passive mode. Again, sensor data are transmitted via the HF-line at high data rates.

- The measurement of contact pressure of segments in clutches. The sensor is here coated on a pressing spring. The transponder works as a passive transponder, the transmission of data and energy are both effected via the LF-line. The HF front-end is not activated in this case.

- The monitoring of forces in bolted assemblies (for instance, at the pin wheel blade). The sensor is put into practise by means of a coated washer. The transponder functions as shown in the first example.

Modular DSP and Cryptographic Units for Area Efficient Microcontroller Systems

M. Jung, R. Lerch

Introduction

The processing of signals and data usually accompanies with exceeding throughput demands, which were predominantly satisfied by digital signal processors (DSPs). As the areas of application for signal and data processing algorithms more and more expand into fields, that are traditionally dominated by small microcontrollers, the advantages of both architectures can be merged to a powerful combination.

There are diverse application areas for such enhanced microcontrollers like automotive systems, smart cards, wireless communication or medical technology systems. Many of those applications are very cost sensitive. Since the production of such chips is often associated with high volumes, it is essential to reduce the unit cost. Especially the reduction of silicon and chip area, respectively, results in a reasonable price per unit. Thus it is important to analyze which architecture results in a high signal processing performance at a minimal area effort.

High-end general purpose microcontrollers satisfy the demands of the signal processing task, but they are often oversized for the remaining jobs, which leads to wasted chip area and as a consequence to high silicon cost.

The idea is to extend an area efficient standard microcontroller core with modular acceleration units, which enhance the performance of the controller just in dedicated areas. These extension units are on-chip with the core, its peripherals and the internal memory.

The concept of modularity is important in order to avoid high development costs. For different applications different acceleration units can be plugged to the microcontroller system.

Hence, a slim interface is required, which supports a large range of different coprocessor concepts. The interface concepts should also be applicable for two or more parallel coprocessors.

The acceleration units are tailored for the 8-bit microcontroller IMS3311C. This small and efficient architecture is instruction set compatible with the Motorola M68HC11 and is well suited for embedded systems. In addition it provides a coprocessor interface, which supports the development of internal on-chip acceleration units.

Two microcontroller extensions were developed, which systematically accelerate the 3311C in different fields: A cryptographic unit that encrypts and decrypts data blocks with the Advanced Encryption Standard (AES) and a Multiply-Accumulate (MAC) unit that speeds up digital filtering with FIR or IIR filters. Figure 1 represents the architecture of the extended controller.

Interface

The IMS3311C reserves two opcodes for coprocessor instructions. Both op-

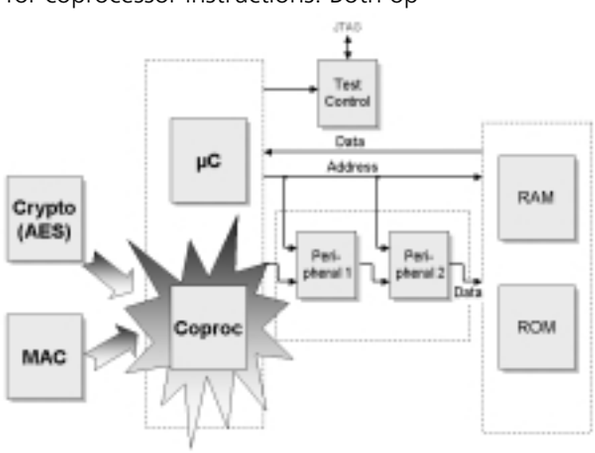

Figure 1: Digital signal processing with the IMS3311C µC

codes span new opcode map tables. As a result, more than 60,000 different coprocessor instructions can be defined. Those instructions are subdivided into the following classes:

1. Branches,

2. Memory Accesses and

3. Internal instructions.

Branch instructions allow the coprocessor to initiate conditional jumps within assembler programs. So the program is able to react to the coprocessor's internal status.

Possible memory accesses are Load/Store and Push/Pull instructions. The core provides its addressing modes for Load/Store instructions to the coprocessors. The Push/Pull instructions allow access to the processor stack.

In addition, burst memory access is supported by the controller, so an arbitrary number of subsequent data bytes can be read from or written to memory by a single coprocessor instruction.

Internal instructions do not require any support from the processor core, since they exclusively execute operations within the selected coprocessor (e.g. data encryption for the AES unit).

More than one parallel acceleration unit can be connected to the controller core, so that a high flexibility of the controller system is achieved.

Figure 2: Encryption with the AES cryptographic core

AES Coprocessor

The AES is a symmetric block cipher, which was announced as a standard by the NIST (US National Institute of Standard and Technology) in the year 2000. Symmetric ciphers are characterized by an identical key for sender and receiver (see Figure 2).
Block ciphers in contrast to stream ciphers process blocks of a constant size.

The AES is used in systems that have high security claims as they deal with personal or secret data like smart cards, networks or mobile communication systems.

128 bit data blocks are encrypted within 10 to 14 almost identical rounds, using a secret key K with a size of 128, 192 or 256 bits. The key K is expanded by a further algorithm, so that each of the rounds works with a different derivation K_e or K_d of the key.

Figure 2 depicts the encryption operation with $E(M, K_e)$, where M is the plain message. The reverse AES algorithm $D(C, K_d)$ decrypts the ciphertext C and retrieves the message.

Within each of the rounds input data are modified by sequential operations like byte transpositions, the addition of the round key or arithmetic operations. These mathematical operations are based on the theory of Galois fields.

As illustrated in Figure 2, the AES coprocessor provides instructions for the encryption and decryption of the 128 bit data blocks. Furthermore it supports the expansion of a secret key using a single instruction. Hence, the chip secures bi-directional data transmissions over an insecure channel with few instructions.

Message, ciphertext and key can be stored at an arbitrary position in memory. The unit just needs information about the start address of these data blocks. The results of the coprocessor operations are stored at a desired memory address.

Furthermore, special instructions support fast ciphering of large data blocks, which exceed the standard AES block size of 16 Byte.

It is possible to run the cryptographic unit in parallel to the microcontroller, so the core can proceed with processing of the program during coprocessor activity. The unit's activity status can be checked by special branch instructions.

MAC Unit

The MAC unit supports technical applications like vector multiplications, FIR or IIR filters.

Since filter operations often require a high accuracy, the calculation with an 8-bit microcontroller is usually very slow and seizes a large program memory. For those operations, a 16 or 32 bit microcontroller would be more adequate.

Hence, the developed MAC unit enhances the 8-bit controller IMS3311C with several 2- and 4-byte operations, which are frequently used in digital signal processing. These instructions comprise

1. the multiplication of two 16 bit numbers,

2. the multiplication of two 16 bit numbers with subsequent addition to an accumulated 32 bit value (MAC),

3. the addition or subtraction of two 32 bit values and

4. arithmetic left or right shifts of a 32 bit value.

The first operations accelerate the multiplication of the filter coefficients with input values, while the shift instructions are used for the normalization of the results. These operations allow arithmetic left and right shifts within the range of 0 to 14 positions. They are implemented by a combinatorial barrel shifter. All of these operations are processed in at most two execute cycles.

In addition to the arithmetic and logical instructions, the MAC unit supports several load and store operations, which provide memory access for operands or calculated results.

Conclusions

A modular and fast coprocessor interface for the IMS3311C was developed, which allows to extend the core with dedicated DSP or cryptographic units.

Two acceleration units were designed: an AES coprocessor and a MAC unit. Controller core and coprocessor together require less than 6000 NAND2 gate equivalents for the digital part plus the core's microcode ROM, which is the smallest known combination. Though the developed systems have a smaller gate count than 32-bit microcontrollers, they can compete with 32-bit solutions concerning AES encryption and digital filtering, respectively.

Furthermore, the modularity of the system provides a convenient opportunity to expand the core with several different coprocessor units at low development cost, since the coprocessor units can easily be plugged to the controller core.

Especially at high volumes, the low gate count and small silicon area of the microcontroller with on-chip coprocessor results in an efficient solution.

List of Projects
IMS Duisburg

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IMS Duisburg

Project Title	Partner	Project Period
Pulse Generator	Industry	07/1996-12/2004
Triangulation Sensor	Industry	05/2003-05/2004
Redesign Triangulation Sensor	Industry	07/2004-12/2004
Delivery Triangulation Sensor	Industry	07/2004-09/2004
MISSY	Funding Authority: EC	08/2001-07/2004
Service Measurement	Industry	07/2004-12/2004
Process Transfer	Industry	06/2004-12/2004
Foundry Jamex 2000	Industry	04/2004-09/2004
Bluetooth-Transceiver	Funding Authority: Local Government NRW	01/2001-12/2004
MIMOS-Smart Pressure Sensor 2	Industry	11/1999-10/2004
Delivery of Pressure Transponder 3	Industry	08/2002-03/2004
Video ADC	Industry	09/2002-11/2004
Smart Control Inhaus	Industry	04/2004-07/2004
Distributed Information Network	Funding Authority: BMBF/Industry	07/2001-04/2004
Mixed ASIC 1	Industry	07/2001-10/2004
VAMOS -Sensor	Industry	12/2001-07/2004
Delivery of Memory Tag II	Industry	01/2004-12/2004
Smart Living NRW	Funding Authority: Projektträger Jülich	10/2004-09/2007
Demonstrator VIP Transponder	Funding Authority: Projektträger Jülich	05/2004-04/2006
Fabrication of 100 K Temperature Transponder	Industry	10/2001-07/2004
EADS Plus	Industry	12/2001-03/2005
Fabrication IODS	Industry	04/2003-08/2004

Foundry IODS M	Industry	10/2003-12/2004
Foundry IODS C	Industry	10/2003-12/2004
Minpro	FhG defined Project	01/2004-12/2008
Office 21	FhG defined Project	07/1998-04/2004
Micro Camera	FhG defined Project	01/2004-12/2006
Tungsten Plugs	Industry	08/2003-07/2004
Delivery of Memory Tag	Industry	01/2004-12/2004
Pressure Transponder 3	Industry	08/2002-03/2004
SOLION	Forschungszentrum Karlsruhe	01/2003-06/2004
VW Connection Inhaus	Industry	07/2004-09/2004
ITO Processing	IMS defined Project	01/2004-07/2004
Study PL-Controller	Industry	08/2004-12/2004
Process Development	Industry	08/2004-12/2005
Development Pressure Sensor	Industry	08/2004-03/2006
Thin Film Resistor	Industry	09/2004-04/2005
IMEX Pressure Sensor	Technische Hochschule RWTH Aachen	06/2002-11/2004
Characterisation HDR	Industry	11/2003-05/2004
Telemetric System DiaKra	Funding Authority: BMWI	08/2003-03/2005
High Voltage SOI-CMOS	Industry	01/2004-12/2004
Foundry IVTMX	Industry	04/2004-03/2005
Micro Reactors	Funding Authority: EU, Local Government NRW, Province Gelderland	07/2003-06/2007
X-Ray Detectors I	Industry	08/2003-11/2004
X-Ray Detectors II	Industry	08/2003-11/2004

Inhaus	Forschungszentrum Karlsruhe	09/2003-11/2004
Delivery Tire Pressure Sensor	Forschungszentrum Karlsruhe	03/2004-09/2004
REOS-Digital II	Industry	10/2003-01/2004
Development Memory Tag III	Industry	10/2004-08/2005
Development 0,25 µm Process	IMS defined Project	01/2004-12/2004
Design Kit 0,25 µm Process	IMS defined Project	07/2004-12/2004
200mm Technology	IMS defined Project	01/2004-12/2004
Delivery REOS	Industry	10/2004-03/2005
Delivery of Handheld Reader	Industry	08/2003-01/2004
Delivery OA32	Industry	01/2004-10/2004
High Temperature Electronics	Funding Authority: Local Government NRW	01/2004-12/2006
Service Handheld Reader	Industry	01/2004-12/2004
Delivery High Pressure Sensor	Industry	4/2004-06/2005
IP Controller	Industry	06/2004-12/2006
RF-based VRU Detection	Funding Authority: EC	02/2004-07/2005
CIF-Sensor Fabrication	Industry	05/2004-04/2006
Relative Pressure Sensor	Industry	04/2004-06/2005
Workshop CMOS Imaging	Industry	01/2003-12/2004
Amigo	Funding Authority: EC	09/2004-02/2008
WLAN 802.11b Design Concept	Industry	02/2004-05/2004
Foundry Pressure Sensor	Industry	10/2003-08/2004
Logistic Demonstrator	Industry	01/2004-09/2004
Modernisation Metal Layer	Industry	07/2004-12/2004

High Temperature Image Sensor	Industry	02/2004-06/2006
Generic Ambient Intelligent Network	IMS defined Project	10/2004-12/2004
Tire Pressure Measurement System	Industry	02/2004-11/2004
Installation Packaging Line	IMS defined Project	01/2004-04/2004
High Temperature Pressure Demonstrator	Industry	03/2004-07/2004
UseRCams	Funding Authority: EC	02/2004-01/2007
Home Demonstrator/Inhaus	Industry	4/2004-08/2004
ASIC Design – Tire Pressure Transponder	Industry	03/2004-06/2004
Layout – Tire Pressure Transponder	Industry	03/2004-06/2004
Through Wafer Interconnect	Industry	03/2004-11/2004
Fabrication Full Bridge	Industry	04/2004-09/2004

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3. Patents

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Board Memberships for Associations and Authorities, 2004

Dr.-Ing. G. vom Bögel

– AIM-Deutschland e. V. Industrieverband für Auto ID und BDE/MDE Systeme

– E-Logistik Plattform Duisburg/Logistik Initiative Duisburg – Niederrhein

Dipl.-Ing. W. Brockherde

– Member of the Technical Program Committee: "European Solid State Circuits Conference"

– Member of "Wissenschaftlich-Technischer Rat (WTR) der Fraunhofer-Gesellschaft"

Dr.-Ing. V. Grinewitschus

– VDI/VDE Gesellschaft für Mess- und Automatisierungstechnik (GMA)
Fachausschuss 1.8:
Methoden der Steuerungstechnik-
Initiative "intelligentes Wohnen" des ZVEI

– Fachbeirat der Messe e/home

Prof. B. J. Hosticka, Ph. D.

– VDE Informationstechnische Gesellschaft (ITG)
Fachausschuss 5.4:
System- und Schaltungstechnik
Fachausschuss 5.5:
Integrierte Elektronik

– Senior Member of IEEE

Dr.-Ing. S. Kolnsberg

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM)

– Deutsche Gesellschaft für Biomedizinische Technik (DGBMT) im VDE

– Member of IEEE

Prof. Dr. rer. nat. W. Mokwa

– Member of "Wissenschaftlicher Beirat des Instituts für Schichten und Grenzflächen des Forschungszentrums Jülich"

– Member of the "Kuratorium des Fraunhofer Instituts Photonische Mikrosysteme Dresden"

– Member of the Program Committee: "Eurosensors"

– Member of the Progam Committee "IEEE Sensors"

– Head of "Gutachtergruppe 6 Mess- und Informationstechnik der AIF"

Dipl.-Ing. H.-C. Müller

– Member of "Wissenschaftlich-Technischer Rat (WTR) der Fraunhofer-Gesellschaft"

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM)

– Informationstechnische Gesellschaft im VDE (ITG)

Dipl.-Phys.-Ing. J. Peter-Weidemann

– Benutzergruppe Ionenimplantation

Dipl.-Ing. J. Pieczynski

– Arbeitskreis MOS-Modelle und Parameterextraktion

Dipl.-Ing. K. Scherer

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM) Fachausschuss 8.4: Beschreibungssprachen und Modellierung von Schaltungen und Systemen

– Beirat VDE Rhein-Ruhr und Leitung Fachgruppe Mikroelektronik und Systeme

– Arbeitskreis Intelligentes Wohnen des ZVEI

Prof. Dr.-Ing. H. Vogt

– VDE/VDI Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM) Fachausschuss 6.3: Gesamtprozess/Devices

Dipl.-Ing. P. Wiebe

– Universitätszentrum Medizintechnik (UZMT) an der Ruhr Universität Bochum

– Deutsche Gesellschaft für Biomedizinische Technik (DGBMT) im VDE

– Studiengemeinschaft "WORT UND WISSEN e. V."

Chronicle 2004

IMS wins futurist house technology contest in the Ruhr Valley with the project "SmarterWohnenNRW"

(business partners: Hattinger Wohnstätten, Centre for Telematics in Health Care Northrhine Westphalia and FhG-ISST Dortmund).

Within this project, electronic and information technological system solutions which have been developed and tested at the inHaus Innovation Centre in Duisburg will be implemented and tested with occupants, first in 200 model apartments and subsequently in 1100 additional housing units within the Southern City of Hattingen from October 2004 until January 2007.

The information technologically based house- and apartment equipment is combined with tele services which are being developed and optimised by the Fraunhofer Society ISST department.

Our aim is a broad implementation of housing services for more security, comfort and assisted living for senior citizens. As a result, a substantial increase in new jobs especially as regards the segment of service providers is expected.

www.smarterwohnennrw.de
www.inhaus-duisburg.de

Membership ZigBeeTM alliance

The Fraunhofer Society now takes an active part in the ZigBeeTM alliance, a union of enterprises and companies promoting the open and global ZigBeeTM standard. The objective of this union is to establish low-cost and low-power solutions for wireless network communication. Fields of applications are remote control and monitoring for domestic and industrial automation as well as monitoring of transport, logistics, infrastructure, and environment.

The Fraunhofer Institute of Microelectronic Circuits and Systems in Duisburg offers design services as well as complete hardware, software, and systems for the ZigBeeTM standard. A protocol stack is available and can be tailored to the customer's demands. The institute can provide the linkage to sensors as well as a CMOS chip-integration. A ZigBeeTM compliant evaluation kit with radio interface, processor, and connectivity to a PC is available as well.

For the setup of wireless sensor networks so called µNodes (micro-nodes) and µGates (micro-gateways) have been designed which provide a complete hardware and software implementation on a few square centimetres, including a radio interface, a processor, a protocol, a sensor interface, and connectivity to an application. A flexible architecture allows the implementation of the ZigBeeTM protocol and operating systems for embedded solutions and sensor networks.

Contact

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ZigBee™ Alliance
Wireless Control That Simply Works

2004-2005 Certificate of Membership

Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V.

is a member in good standing with the ZigBee™ Alliance, an association of companies working together to enable reliable, cost-effective, low-power, wirelessly networked, monitoring and control products based on an open global standard.

Bob Heile
Chair, ZigBee Alliance

Deepak Kamlani
Executive Director, ZigBee Alliance

ZigBee Alliance

Press Review

Forschung zwischen Existenz und Energie

JAHR DER TECHNIK / In Duisburg vom 18. bis 21. November

Das Jahr der Technik, organisiert vom Bundesforschungsministerium, dem Verband technisch-wissenschaftlicher Vereine und der Initiative Wissenschaft im Dialog, geht zu Ende. Zum Abschluss finden vom 18. bis 21. November zahlreiche Veranstaltungen in Duisburg statt.

Die letzte Großveranstaltung zum Jahr der Technik steht ganz im Zeichen des Leitthemas: „Vitalitätsimpuls - Existenz und Energie". Wie sieht das Haus der Zukunft aus? Bestellt der Kühlschrank die Milch selbstständig neu, wenn sie abgelaufen ist, und hält der Rasenmäher von allein das Gras kurz?

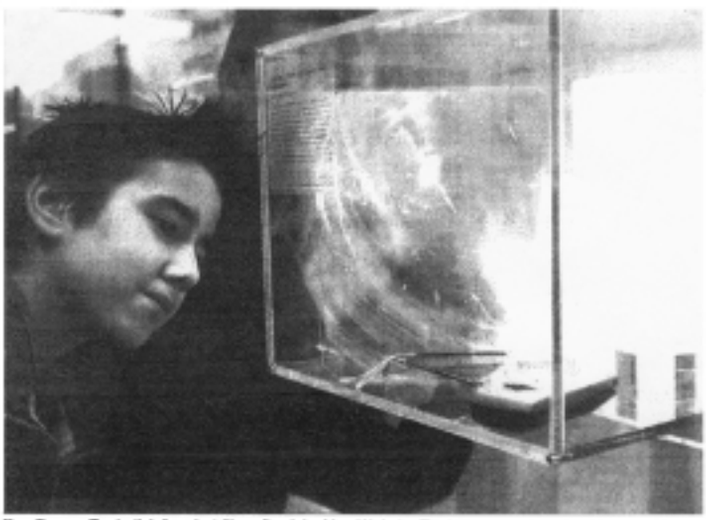
Bestes Beispiel ist das Duisburger „inHaus", ein intelligentes Gebäude. Da wird beispielsweise die Bewässerungsanlage des Gartens über eine drahtlose Tastatur gesteuert und der Inhalt des Kühlschranks elektronisch per Computer überwacht. Das Fraunhofer-Institut für mikroelektronische Schaltungen und Systeme (IMS) erprobt dort Haustechnik der Zukunft und arbeitet an der Vernetzung von neuen Entwicklungen. In Zukunft sollen Bewohner ihr Haus per Internet und Computer steuern können.

Weiteres Thema rund um Existenz und Energie: Die natürlichen Ressourcen wie Kohle, Öl und Erdgas sind begrenzt. Wie helfen innovative Techniken Energie zu sparen? Ingenieure und Ingenieurinnen arbeiten schon heute an Lösungen für die langfristige Energieversorgung und entwickeln Technologien, die das Leben - nicht nur zuhause - angenehm gestalten.

Doch es muss ja nicht immer Hochtechnik sein. Auch andere Fragen sind spannend. Warum können manche die Zunge rollen und andere nicht? Welche Temperatur herrscht in einem Vakuum? Könnte ein Mensch übers Wasser laufen wie Jesus? Antworten dazu gibt das WDR-5-Wissenschaftsmagazin „Leonardo" in der „Kleinen Anfrage". Vom 18. bis 20. November können die Besucher des Atlantis Kindermuseums die „Kleine Anfrage" live erleben. Zwei Leonardo-Autoren präsentieren die spannendsten Fragen, lassen Tomatensoße spritzen und Zitronenhaare schweben und laden natürlich zum Mitmachen ein. Für die besten Antworten gibt es - mit etwas Glück - auch einen Preis.

Organisiert wird das Jahr der Technik in Duisburg in Kooperation mit der Universität Duisburg-Essen. Die Veranstalter verfolgen vor allem das Ziel, junge Menschen für eine technische Ausbildung oder einen technischen Studiengang zu begeistern. Zu den Höhepunkten gehört dabei zweifelsohne das Technik-Vor-Ort-Programm.

Informationen über alle Veranstaltungen gibt es am Tor zur Technik, das vom 16. bis 21. November, 10 bis 20 Uhr, in Duisburg am Portsmouthplatz geöffnet ist, oder im Internet unter www.jahr-der-technik.de. Eine gebührenfreie Hotline steht montags bis freitags von 8 bis 20 Uhr zur Verfügung unter der 0800-TEC2004 (fax 0800 / 832 2004). tw



Das Tor zur Technik informiert über die vielseitige Welt der Technik. Nach seiner Tour, die u.a. über Berlin, Dresden und Darmstadt führte, ist es nun in Duisburg zu bewundern. Bild: Markus Schmidt

WAZ 15.11.2004

CMOS-KAMERA

Für „Night Vision"

Im Auftrag der BMW AG entwickelte das Fraunhofer Institut für Mikroelektronische Schaltungen und Systeme, Duisburg, eine neuartige hochdynamische CMOS-Kamera mit PAL-Auflösung. Das Kamerasystem verwendet für die Bildaufnahme ein patentiertes Verfahren, beruhend auf dem Prinzip der Mehrfachbelichtung. Herzstück der Kamera ist ein neuer CMOS-Bildsensor mit 768 x 576 Pixeln, der im 0,5 µm-CMOS-Prozess des Fraunhofer IMS gefertigt wird. Mit Mehrfachbelichtung erreicht der Sensor laut Hersteller mit seiner linearen Charakteristik eine Helligkeitsdynamik von 118 dB. Gleichzeitig weist er dennoch eine hohe Nachweisempfindlichkeit von 33 µW/qm (entsprechend 4,9 Millilux) bei 50 Vollbildern pro Sekunde auf, womit er ideal für „Night Vision" geeignet sein soll.

Damit ins Kamerasystem werden die bei verschiedenen Belichtungszeiten aufgenommenen Bilder mit relativ einfachen und schnellen Algorithmen zu einem linearen hochdynamischen Gesamtbild verrechnet. Die Algorithmen stabilisieren das Kamerasystem gleichzeitig gegen Temperatur- und Langzeitdrift-effekte, wodurch nachfolgende Signalverarbeitungsalgorithmen unempfindlich gegen Störeinflüsse werden sollen.

▶ **Fraunhofer IMS**
T 0203/3783-138
martin.sanacherer@ims.fhg.de, www.ims.fhg.de
Stand 2.0.111

Focus 18.10.2004

• BLENDFREIE KAMERA
Eine Digitalkamera für **extreme Helligkeitsdifferenzen** hat das Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme entwickelt. Sie nimmt ein Motiv mehrfach mit unterschiedlichen Belichtungszeiten auf – die jeweils passend belichteten Partien kombiniert sie dann zum kompletten Foto.

Mikrochip-Produktion im Duisburger Fraunhofer-Institut THOMAS EICKHOFF

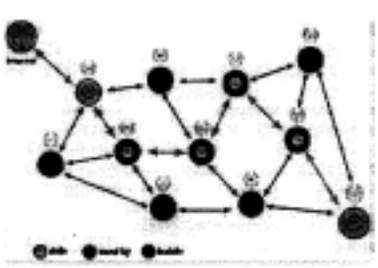
Hoffnungsträger im neuen Revier

Welt am Sonntag 24.10.2004

Qualität und Zuverlässigkeit
01.10.2004

Funkstandard "ZigBee" für Datenzwerge

Daten schwirren wie Bienen zu Blumen



Duisburg (pte, 10. Mär 2004 13:05) - Am Fraunhofer Institut für Mikroelektronische Schaltungen & Systeme (IMS) http://www.ims.fhg.de werden derzeit Schaltungslayouts mit Sensorik für den neuen Funkstandard "ZigBee" entwickelt. Die neue Lösung soll die Lücke schließen, die Bluetooth hinterlassen hat. Mit 250 Kilobit pro Sekunde erreicht ZigBee zwar nur eine Datenrate von rund 10 bis 15 Prozent im Vergleich zu Bluetooth, verbraucht aber deutlich weniger Energie. Beim neuen Network halten Batterien deshalb um ein Vielfaches länger.

Breitbandige Standards sind für Datenzwerge wie Sensoren, Alarmanlagen, Lichtschalter oder kabellose Computermäuse überdimensioniert. Für einfache Schaltungen soll deshalb der neue, für jeden Hersteller frei zugängliche Funkstandard eingesetzt werden. Im drahtlosen "ZigBee-Multi-Hop-Netzwerk" mit bis zu 250 Knoten und 70 Metern Reichweite suchen sich die Daten den schnellsten und günstigen Weg selbst. Dabei habe der Zickzackflug von Bienen über eine Blumenwiese Pate gestanden.

Für Schaltungen mit dem sparsamen Funk sieht in Duisburg bereits eine CMOS-Fertigungslinie bereit. "Bisher existieren zwar erst wenige Unternehmen, die Chips oder Systeme mit dem neuen Standard bauen oder anbieten, wir verzeichnen aber bereits eine wachsende Zahl von Interessenten", weiß Rainer Kokozinski vom IMS. Mitglieder des Institute of Electrical and Electronic Engineers, die dem neuen Standard ihren Namen gegeben haben, sind Big Player wie Honeywell, Invensys, Mitsubishi, Motorola und Philips. (Ende)

Pressetext Deutschland 10.03.2004

Cleveres Energiemanagement macht häufige Batteriewechsel überflüssig

Funktechnik Zigbee schlägt Bluetooth bei Sensordaten

Die Drahtlostechnik Zigbee bietet nur einen Bruchteil der Bluetooth-Bandbreite – das reicht aber völlig aus für Sensordaten mit wenigen Bytes. Dafür leben die Senderbatterien dank des knauserigen Stromverbrauchs bis zu mehreren Jahren.

Der Machine-to-Machine-Kommunikation (M2M) wird seit Jahren der baldige Durchbruch im Massenmarkt prophezeit. Doch bislang ist der drahtlose Informationsaustausch zwischen Maschinen, Fahrzeugen, Containern, Automaten oder anderen Objekten mit einer zentralen Leitstelle noch eher die Ausnahme als die Regel. Das könnte sich bald ändern, denn Experten erwarten noch in diesem Jahr den Einsatz des neuen Funksystems Zigbee und glauben an dessen Erfolg im Markt.

Dabei handelt es sich um eine abgespeckte Bluetooth-Variante für Sensornetzwerke, die lizenzfrei zur Verfügung stehen soll, wie Thomas Luckenbach, Abteilungsleiter für neue Netzwerktechnologien beim Fraunhofer-Institut für Offene Kommunikationssysteme (Fokus), erklärt. „Das wird deutlich billiger als Bluetooth." Der Kurzstreckenfunk auf Basis der IEEE-Spezifikation 802.15.4 sucht automatisch nach freien funkkanälen und soll sich mit anderen Drahtlosnetzen vertragen. Außer dem lizenzfreien 2,4-Gigahertz-Band stehen in Europa Frequenzen bei 868 Megahertz für Zigbee zur Verfügung. Bei 2,4 Gigahertz soll die Funktechnik Übertragungsraten von bis zu 250 Kilobit pro Sekunde erreichen, was je nach Frequenz rund 10 bis 25 Prozent von Bluetooth beträgt. Das Netzwerkprotokoll baut auf sichere Übertragung durch hohe Redundanz. Die Reichweite wird je nach Sendeleistung zwischen 10 und 75 Metern liegen.

Der große Vorteil von Zigbee gegenüber Bluetooth besteht darin, dass die in der Regel batteriebetriebenen Geräte durch Power-Management und kurze Aktivitätszeiten viel weniger Strom verbrauchen. Hat das Gerät nichts zu tun, verfällt es in einen energetischen Tiefschlaf. Bei Zigbee halten Batterien je nach Datenaufkommen und Funkreichweite mehrere Monate bis Jahre. Bluetooth ist dagegen mit seiner Bandbreite für Datenzwerge wie Sensoren in Wetterstationen und medizinischen Geräten, Alarmanlagen, Lichtschalter, PC-Mäusen oder in industriellen Überwachungssystemen schlicht überdimensioniert.

„Die Anwendungen schreien geradezu nach Zigbee", sagt Stephan Kolnsberg, Gruppenleiter für Chipentwicklung im Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) in Duisburg. Dort werden zurzeit Schaltungskomponenten für den Funkstandard entwickelt. Auch Nigel Deighton, Experte für drahtlose Kommunikation bei Gartner, sieht für Zigbee großes Potenzial. Mögliche Anwendungen gebe es etwa bei Energieversorgern, in der Überwachung der Körperfunktionen bei Kranken und Pflegebedürftigen sowie im Sicherheitsbereich mit Alarmanlagen und Ortungssystemen für gestohlene Autos.

Vorangetrieben wird die Entwicklung von der Zigbee-Allianz (www.zigbee.org), einem Konsortium aus Halbleiter- und Technologieanbietern sowie Anwendern. Dazu zählen Branchengrößen wie Motorola, Philips, Honeywell und Samsung. Noch hat die Organisation den Standard allerdings nicht frei zugänglich gemacht. Kolnsberg rechnet aber noch für Ende dieses Jahres damit. Ulrich Hottelet/dpa

Computerzeitung 10.05.2004

Die drahtlose Übermittlung von Maschinendaten an die Zentrale ist eine der Anwendungen der Funktechnik Zigbee. Foto: Motorola

Airbag beschleunigt

Ein neuer „Beschleuniger-Chip" bläst Airbags ebenmal schneller auf als bisher. Entwickelt hat den Beschleunigungssensor des Fraunhofer Zentrum für Mikrotechnologien.

Auto Bild 09.07.2004

Empfindlichkeits-Weltrekord für CMOS-Kameras

Belichtungssystem schafft 118 dB Helligkeitsdynamik

Duisburg (pte, 12. Okt 2004 12:04) - Wissenschaftler des Fraunhofer Instituts für Mikroelektronische Schaltungen und Systeme (IMS) http://www.ims.fhg.de haben eine hochempfindliche Kamera für extreme Lichtbedingungen entwickelt. Während übliche Digitalkameras etwa 60 dB verkraften, kann die neu entwickelte CMOS-Kamera ein SW-Bild mit einer maximalen Helligkeitsdynamik von 118 dB darstellen. Für CMOS-Kameras mit linearen Kennlinien ist das laut IMS Weltrekord.

Um diese hohe Helligkeitsdynamik zu erreichen, nutzt die Kamera den gleichen Trick wie das menschliche Auge. Je nachdem, wohin das Auge blickt, stellt sich die Pupille blitzschnell auf hell oder dunkel ein. Im Gehirn verschmelzen die Bilder und suggerieren einen höheren Tonwertumfang als die Netzhaut wahrnehmen kann. Bei 50 Vollbildern pro Sekunde wählt die integrierte Elektronik der Kamera bis zu vier zeitlich benachbarte Aufnahmen mit unterschiedlicher Belichtungszeit. Anschließend kombinieren Algorithmen gut belichtete Partien in Echtzeit. Bisherige Kamerasysteme standen vor dem Dilemma, dass helle Partien oft "ausgefressen" wirkten, während in dunkle Bereiche "absoffen". Je nach gewählter Belichtung gingen so viele Nuancen unwiederbringlich verloren.

"Ein weiterer wichtiger Wert kommt zum tragen, wenn konventionelle Kameras bei 1/50 Sekunden Belichtungszeit nur noch 'schwarz sehen'", erklärt Gruppenleiter Werner Brockherde vom IMS. "Unsere Kamera erreicht hingegen bei 1/50-Sekunden eine Nachweisempfindlichkeit von nur 33 Mikrowatt pro Quadratmeter, dies entspricht weniger als fünf Millilux und ist extrem hoch", so Brockherde. Entwickelt wurde die Technik ursprünglich für ein optisches Fahrspurerkennungssystem von BMW. Nun suchen die IMS-Forscher nach weiteren Anwendungsmöglichkeiten. Vorstellbar wären etwa Überwachungsaufgaben, die sich durch hohe Kontraste oder starke Tag-Nach-Lichtwechsel in der Verkehrsüberwachung auszeichnen. (Ende)

Pressetext Deutschland 12.10.2004

EDITORIAL

Gute Zeiten in Sicht

Die Sensorik wird vielfach als Schlüsseltechnologie für alle Bereiche angesehen, wo elektronisch gemessen, geprüft, überwacht oder automatisiert wird. Das reicht von der produzierenden Industrie über Handwerksbetriebe bis hin zum Privathaushalt. Wir alle kennen Sensorsysteme in Maschinen, Werkzeugen, Automobilen, Raumstationen, Haushaltgeräten, Informationstechnologien, usw.

Betrachten wir das Automobil aus Sicht der Sensorwelt: Es gibt schon eine Vielzahl von Sicherheitssensoren, Komfortsensoren sowie Antriebsteuerungssensoren und ein Ende an Neuentwicklungen in dieser Branche ist bei weitem noch nicht absehbar. So hat beispielsweise Continental einen Reifen als Sensor entwickelt. Hergestellt wurde der Sensor, um Informationen über die zwischen Fahrbahn und Fahrzeug wirkenden Kräfte zu erhalten. Das Messprinzip basiert auf einer magnetisierten Seitenwand als Bindeglied zwischen Fahrzeug und Straße. Die auf diesem Wege ermittelten Messdaten werden unter anderem für das Antiblockiersystem (ABS) benötigt.

Ein anderes Beispiel an innovativer Technik findet man beim Fraunhofer-Institut für Mikroelektronische Schaltungen. Die Wissenschaftler beschäftigen sich seit längerem mit der Thematik Ölsensor. Wann muss das Motoröl gewechselt werden? Bislang konnte die Antwort nur über Maßgaben wie Zeitdauer oder Laufleistung gegeben werden. Der neue Ölsensor erkennt den genauen Zeitpunkt. Er ermittelt Messwerte wie beispielsweise die elektrische Leitfähigkeit und die Viskosität des Öls. Dadurch wird der Schmierzustand der Maschine einschätzbar.

Aber Sensoren sind nicht nur eine Schlüsseltechnologie, sondern sie spielen auch eine zentrale Rolle in der Wirtschaft. Hochrechnungen gehen davon aus, dass es in Deutschland ca. 600 bis 700 Hersteller von industriellen Messsystemen gibt. In einer Umfrage hat der AMA Fachverband für Sensorik e.V. festgestellt, dass in den letzten Jahren ca. 4000-5000 neue Arbeitsplätze geschaffen wurden. Für die Sensorik-Branche in Deutschland ergab die AMA-Umfrage einen jährlichen Zuwachs von ca. 8 bis 12 % pro Jahr. Dabei sollten allerdings die einzelnen Anwendungen differenziert werden. In Anwendungen wie beispielsweise im Bereich der Chemie- oder Biosensorik stehen die Sensorsysteme erst am Anfang ihrer Karriere und weisen daher zweistellige Zuwachse auf – also: Gute Zeiten in Sicht!

Die MSR-Redaktion wird Sie auch in diesem Jahr wieder über die neuesten Entwicklungen der Branche informieren.

Christin Fiores

Christin Fiores

MSR Magazin 01.02.2004

Mit implantiertem Chip läßt sich ganz einfach der Blutdruck messen

Die gemessenen Werte können mit einem Gerät am Gürtel abgefragt werden

WIESBADEN (gwa). Ein Chip mit Antenne, die in einer 2,3 mm dünnen Silikonkapsel mit drei Ankerfüßen eingegossen sind, könnte möglicherweise in Zukunft eine Dauerkontrolle des Blutdrucks bei Hypertonie-Patienten ganz einfach machen. Die Aachener Kapsel soll etwa in einer Beckenarterie verankert werden. Die gemessenen Werte würden an einen Empfänger, der subkutan sitzt, übermittelt. Die Blutdruck- und Pulswerte könnten dann über etwa Handy-große Geräte, die die Patienten am Gürtel tragen würden, abgefragt werden.

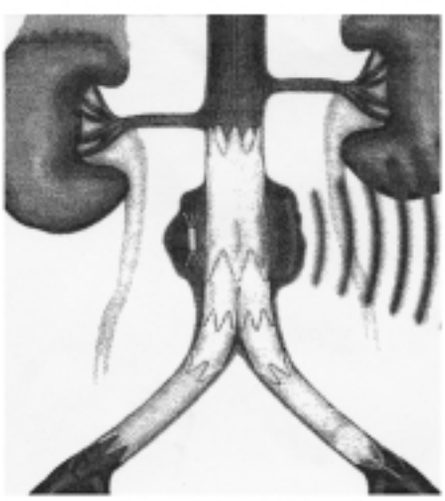
Diese Neuheit, die sich noch in der Entwicklung befindet, wurde auf dem Erfinderforum des Deutschen Röntgenkongresses in Wiesbaden vorgestellt. Vorab erläuterte Professor Thomas Schmitz-Rode von der RWTH Aachen das Prinzip und weitere Optionen: Über einen Katheter in der Leiste kann der „dreibeinige Blutdruck-Wächter" in eine Arterie eingesetzt werden. „Zielgefäß ist eine Aufzweigung der inneren Beckenarterie", so Schmitz-Rode zur „Ärzte Zeitung". Dort können sich die Ankerfüßchen verhaken. Die Kapsel könnte dann ständig und über lange Zeit den Blutdruck messen. Das sei wichtig bei der Medikamenten-Einstellung, aber auch zur Therapie-Kontrolle.

Im Tierversuch mit acht Schweinen, denen insgesamt 18 Kapseln eingesetzt wurden, konnte jedenfalls belegt werden, daß die Kapseln funktionierten und sicher verankert blieben. Allerdings entwickelten sich bei einigen Tieren Thromben. „Dieses Problem müssen wir noch lösen", sagte Schmitz-Rode.

Eine weitere Option für die Aachener Kapsel, die von der RWTH in Kooperation mit der Universitätsklinik Aachen und dem Duisburger Fraunhofer Institut IMS entwickelt wurde, könnte die eines Warnmeldens etwa bei Bauchaorten-Aneurysmen sein. Bei solchen Aneurysmen werden etwa Y-Prothesen in die Aorta eingesetzt, die von oberhalb des Aneurysmas bis in die Beckenarterien reichen. Dabei kann es zu einer Leckage mit einem Blutstrom in das Aneurysma kommen. Das könnte dann reißen. „Hier könnten wir eine solche Kapsel, die dann größer sein kann, in das Aneurysma zwischen Prothese und Wand legen. Bei Zunahme des Drucks wird die Kapsel dann einen Ton als Warnsignal aussenden."

Die Weiterentwicklung der Aachener Kapsel kann zu intelligenten Implantaten führen, die etwa den Blutzucker kontinuierlich messen. „Solche Chips könnten zum Beispiel eine integrierte Mini-Insulinpumpe steuern", sagte Schmitz-Rode.

Ärzte-Zeitung
09.09.2004



Bauchaorten-Aneurysma. Y-Prothese wurde eingesetzt. Der Blutdruck-Wächter (Aachener Kapsel) sitzt links im Aneurysmasack. Foto: Schmitz-Rode, RWTH Aachen

„Smarte" Häuser vom Land gefördert:

In Hattingen startet Zukunft des Wohnens

Von Christoph Meinerz

Hattingen. Ein Knopfdruck, und nach Verlassen der Wohnung sind sämtliche Elektrogeräte abgeschaltet, alle Türen und Fenster verriegelt: Ein Beispiel für die Zukunft des Wohnens, die in Hattingen beginnen soll, modellhaft gefördert vom Land NRW.

Rund 185 Einfamilienhäuser und Wohnungen will die Hattinger Wohnstättengenossenschaft (HWG) bis 2007 mit so genannter „intelligenter Technik" ausgestattet haben, die das Leben daheim komfortabler und sicherer macht. Für das Land ein Testlauf, der zeigen soll, ob solch neue Wohnformen im großen Stil durchsetzbar und damit auch neue Arbeitsplätze in der Region zu schaffen sind. Im Rahmen des „Zukunftswettbewerb Ruhrgebiet" fördert das Wirtschaftsministerium das Projekt über drei Jahre mit 2,3 Millionen Euro, wenn die HWG selbst mindestens 4,6 Mio € investiert. Für den finanzstarken Wohnungsbauer kein Thema. Er plant ohnehin gerade mehrere neue Einfamilienhaussiedlungen und eine Modernisierung von rund 1000 Mietwohnungen aus den 50er Jahren im Süden der Stadt.

Die HWG erhielt den Zuschlag gemeinsam mit den Fraunhofer-Instituten in Dortmund und Duisburg sowie dem Zentrum für Telematik im Gesundheitswesen (ZTG, Krefeld) - die Bildung eines Netzwerks wurde vom Land ausdrücklich gewünscht. Unter dem Titel „Smarter Wohnen NRW" läuft die nun preisgekrönte Innovation.

Die Palette der Möglichkeiten ist groß. Wer will, kann von außerhalb via Laptop sein Haus fernüberwachen, aus dem Urlaub heraus den heimischen Garten bewässern oder die verlassene Wohnung mit Licht- und Musikszenarien beleben.

Firmen mit neuer Technik stehen bereits Schlange

Angeboten werden soll aber auch praktische Überlebenshilfe für Menschen, die gebrechlich sind. Wer krank ist, kann sich über ein Notrufsystem mit einem Arzt oder einer Klinik vernetzen lassen. Sinkt etwa die Herzfrequenz, wird automatisch ein Notruf abgesetzt.

Firmen, die entsprechende Techniken anbieten, stehen bei der Hattinger Wohnstättengenossenschaft bereits Schlange, bei der Wohnung der Zukunft wollen auch sie ihren Fuß in der Tür haben. Selbst Microsoft war schon da. HWG-Vorstandsvorsitzender Burkhard Sibbe freut sich über den Vertrauensvorschuss vom Land. Er sagt: „Was an technischen Gesamtlösungen in Autos längst eine Selbstverständlichkeit ist, sollte doch auch in Wohnungen möglich sein."

Westfälische Rundschau
01.10.2004

Auf dem Weg ins All

Als am 30. Januar das Sojus Transportraumschiff in Kasachstan zur Internationalen Raumstation ISS startete, war auch Hight Tech aus Berlin mit an Bord. Die Firma Chronos Vision hat gemeinsam mit Forschern des Klinikums Benjamin Franklin ein neuartiges Meßsystem entwickelt, dass die präzise Erforschung des menschlichen Gleichgewichtssystems in der Schwerelosigkeit erlaubt. Unter Verwendung von CMOS Bildsensoren des Fraunhofer Instituts in Duisburg wurden besonders schnelle Kameras entwickelt, die bis zu 400 mal in der Sekunde die Position der Augen registrieren und damit Aufschluss über verschiedene Funktionen des Gehirns geben. Das System wird auch im April benutzt werden, wenn Astronaut André Kuipers im Rahmen des holländischen Taxiflüges zur ISS fliegen wird. Anschließend verbleibt es an Bord und steht als Bestandteil der ISS Human Research Facility internationalen Forschern zur Verfügung.

Berliner Wirtschaft, Die
01.02.2004

Den Meistern auf der Spur

Digitalkamera sieht fast so scharf wie Katzen

Die Augen der Katze sind besonders lichtempfindlich. (Foto: BASF)

Technik. - Katzenaugen sind immer noch wesentlich empfindlicher als die meisten Kameras. Fraunhofer-Forscher haben jetzt allerdings ein System entwickelt, das es soll dem Gesichtssinn der Tiere aufnehmen kann. Auf der Stuttgarter Messe "Vision" präsentierten sie ihre Entwicklung.

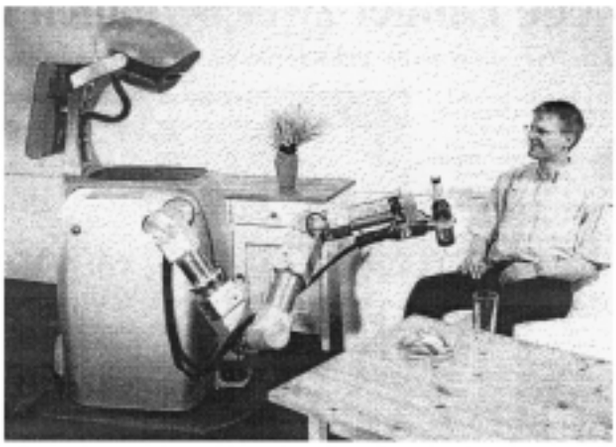
Duisburger Forscher vom Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) haben eine ungewöhnlich scharfsichtige Digitalkamera entwickelt, die bei Nacht fast so gut wie eine Katze sieht. "Das Sensordesign besitzt eine Empfindlichkeit von weniger als fünf Millilux", erklärt Olaf Schrey, der zuständige Ingenieur im IMS, "das ist für den Bereich des ortshochaufgelösten Nachtsehens von extremer Wichtigkeit." Wie ein Katzenauge sieht die Kamera nur Grautstufen, deren allerdings rund eine Million verschiedene. Herkömmliche Amateurkameras geben bereits bei 1000 auf.

Kann die Kamera in puncto Empfindlichkeit mit einer Katze mithalten, so hat sie größere Hürden bei der Verarbeitungsgeschwindigkeit zu überwinden. Das Katzenauge befreit sich mit einer rigorosen Auswahl aus der gewaltigen Datenflut. Nur das wichtigste wird überhaupt wahrgenommen. "Leider passiert das Gasse jedoch in einer für bestimmte Applikationen und Problemstellungen nicht ausreichenden Geschwindigkeit", erklärt Schrey. Will sagen, für moderne Geschwindigkeiten reichen die Verarbeitungskapazitäten eines Katzenhirns nicht mehr aus. Schließlich sollen Digitalkameras etwa im Bereich der Fahrerassistenz und der Fahrzeugsteuerung eingesetzt werden, und dürfen dann nicht wegen Überlastung schlapp machen. Die Fraunhofer verwenden hierfür energiesparende CMOS-Chips, bei denen jeder Bildpunkt bereits einen Teil der Informationsverarbeitung übernimmt. Dadurch erreicht die Kamera extrem kurze Reaktionszeiten. Schrey: "Unsere Kamera macht im Prinzip nichts anderes als Bilder gestaffelt bei verschiedenen Belichtungszeiten in sehr schneller Folge hintereinander aufzunehmen. Und für jedes Bild hinterher den optimalen Signalwert, Pixelwert zu bestimmen und das Ergebnisbild aus den Optimalpunkten zusammenzusetzen." Aus diesem Bild kann das Kamerasystem dann die Informationen für ein eventuelles Fahrassistenzsystem ableiten.

"Ursprünglich sollten wir für BMW ein Fahrerassistenzsystem entwickeln, das die Fahrspuren bei jeden Lichtverhältnissen sehr genau detektiert.", erinnert sich Martin van Ackeren, "und dabei ist die Helligkeitsdynamik sehr, sehr wichtig." Inzwischen haben sich auch andere Einsatzgebiete ergeben, etwa die Überwachung von Anlagen, die nicht in Rotondos Scheinwerferlicht getaucht sind. Trotz Dunkelheit kann durch den Vergleich zweier Bilder jede Bewegung erkannt und gemeldet werden. Auch bei der Qualitätskontrolle etwa bei Schweißnähten ist das Verfahren einsetzbar

[Quelle: Caja Kutzbach]

Deutschlandradio 01.10.2004



Ein Haushaltsroboter, der den Apfelsaft aus dem Kühlschrank holt

Duisburg/Stuttgart – (lsw) Der Haushaltsroboter Care-O-bot II aus Stuttgart ist in das „Intelligente Haus" in Duisburg eingezogen. In dieser vernetzten Welt ist alles ferngesteuert. Nach zwei Jahren im Labor wird das Gerät des Stuttgarter Fraunhofer-Instituts jetzt erprobt. Der Gehilfe kann Kaffee servieren, Apfelsaft aus dem Kühlschrank holen und dem Besitzer im Sessel erklären, dass der gewünschte Orangensaft leider ausgegangen ist und ihm die Alternative anbieten. Serienreif soll „Care-O-bot" in fünf bis zehn Jahren sein. Noch sieht er ein wenig unförmig aus, weil er viele Batterien beherbergt. Zielgruppe für die spätere Serienfertigung sind ältere, behinderte Menschen. Mit Hilfe des Roboters könnten sie ohne menschliche Hilfe länger als heute möglich in den eigenen vier Wänden wohnen bleiben. Als Marktpreis peilen die Stuttgarter Forscher etwa 20 000 Euro an. Bild: Privat

Ludwigsburger Kreiszeitung 21.02.2004

Handy als Lichtschalter

Im **intelligenten Haus** ist alles vernetzt und vieles möglich

Mit dem Handy, Notebook oder über das Internet die Fenster des Hauses öffnen oder schließen, den Eingangsbereich überwachen, das Kinderzimmer kontrollieren, den Herd in der Küche ein- und ausschalten. Das alles ist keine Zukunftsmusik mehr.

Die Grundidee des „intelligenten Hauses" ist relativ einfach: Unterschiedlichste Geräte und Anlagen wie Heizung, Licht, Alarmanlage oder Personal Computer werden durch ein elektronisches Netzwerk verkabelt oder drahtlos – miteinander verbunden. Sie können mit Hilfe intelligenter Computertechnik sinnvoll zusammen wirken und auch von außen einfach bedient und gesteuert werden. Wissenschaftler des Duisburger Fraunhofer Instituts Mikroelektronische Schaltungen und Systeme (IMS) arbeiten in dem Modellprojekt „Inhaus" zusammen mit 17 Unternehmen an der optimalen Integration von moderner Informationstechnik und Elektronik in den privaten Haushalt.

Das Projekt ist ein reales, vollständig vernetztes Haus, das eine Art wissenschaftliches Forschungslabor darstellt. Über das Internet haben die fiktiven Bewohner Zugang zu allen Funktionen des Hauses. Über den Bildschirm kann so beispielsweise das Haus bewacht, zu einer bestimmten Uhrzeit die Heizung an und wieder abgeschaltet oder auch die Heizung gewartet werden.

Ganzheitlichkeit, Vernetzung und Kommunikation sind die Schlüsselbegriffe des Hauses der Zukunft. Werden heute weitgehend Licht-, Heizungs- oder Stromanlagen durch separate Steuerungssysteme gelenkt und kontrolliert, sollen im „intelligenten Haus" Kontrolle, Leitung und Wartung auch unterschiedlichster Gewerke, Infrastrukturen und Anlagen im Haus technisch so vereinheitlicht werden, dass sie zentral von jedem Ort der Welt über Datenleitung gesteuert werden können.

Erhöhter Wohnkomfort und vereinfachte Bedienung, aber auch ökologische und langfristig finanzielle Gründe sprechen für das „Intelligente Haus". Es kann beispielsweise beim Energiesparen helfen, indem es Heizkörper in den Räumen abstellt, in denen Fenster geöffnet sind, oder das Licht in Räumen ausschaltet, in denen sich niemand aufhält. Außerdem können die Komponenten eines intelligenten Hauses die Sicherheit seiner Bewohner erhöhen.

Einzelne Komponenten eines elektronischen Steuerungssystems sind auf dem Markt bereits verfügbar. So montiert eine Berliner Firma bereits intelligente Haustechnik, die über einen firmeneigenen elektronischen Weltzeitgreifer die Lichtanlage über das Handy steuert. Befindet sich der Bewohner in fernen Gefilden im Urlaub, kann er von dort telefonisch das Licht in der Wohnung nach Belieben ein- oder ausstellen. Mit 1200 bis 1500 Euro sind die Kosten für den Einbau eines solchen Systems auch noch überschaubar. (tan)

Südkurier 14.04.2004

Unsichtbare Technik: Die Steuerung von Jalousien oder Raumtemperatur im Duisburger InHaus wirkt im Hintergrund. Fotos: dpa

Die intelligente Wohnung

Leben im vernetzten Haus / Technik teilweise schon im Handel

Duisburg (dpa) • Wenn die Gewitterwolken vor dem Fenster dichter und dunkler werden, sagt bei vielen die Unsicherheit: Sind zu Hause die Fenster zu, die Jalousien heruntergelassen? Geht es nach dem Willen einiger Forscher, müssen sich die Rollläden schon bald automatisch – und auch sonst wird daheim mit Hilfe der Technik einiges komfortabler und sicherer. „Ambient Intelligence" heißt die Technik, die dahinter steht. Sie wird derzeit in verschiedenen Stilen in Prototypen der Zukunftshäuser erprobt.

Box nimmt Lebensmittel in Empfang

Die erste Partie, die dauerhaft in einem solchen vernetzten Haus lebt, heißt Steiner und wohnt im Schweizer Kanton Zug. Das Positive überlegen „Es ist angenehm, sich unabhängig zu fühlen, da wir unser Haus nicht bedienen, abfragen und steuern können."

Um dies Wochenendeinkauf müssen sie sich keine Sorgen machen: Die so genannte Skybox kann Pakete und Lebensmittel in Empfang nehmen, auch wenn niemand da ist.

TV-Kühlschrank mit Alarm für abgelaufene Speisen

Was in der Schweiz das Projekt PeinerLife ist, sind in Duisburg das InHaus und in Eindhoven das HomeLab. In diesen Häusern wird jedoch nur zur Probe gewohnt. Diplomingenieur Klaus Scherer vom Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) in Duisburg macht darauf aufmerksam, dass ein Teil dieser Zukunftsmusik bereits heute in normalen Häusern gespielt werden kann. „Die Geräte sind bereits am Markt." Energieeinsparung ist damit genauso möglich wie die Telebedienung von Hausfunktionen über das Internet.

Unterhaltungselektronik bereits vernetzt

Das InHaus wird nicht mehr über viele Fernbedienungen für die verschiedenen Geräte, sondern nur noch über eine „integrierte Systembedienung" gesteuert.

Serienreif und im Handel erhältlich ist bereits der Multimedia-Kühlschrank von LG Electronics mit eingebautem Fernseher. Er schlägt Alarm, wenn Verfalldaten erreicht sind und meldet ausgehende Lebensmittel. Damit beschäftigt sich das smarte Wohnen in der Praxis oft auf die Vernetzung von Unterhaltungselektronik. In diesem Bereich können viele Geräte dank des drahtlosen Funkstandards WLAN bereits miteinander kommunizieren. „Im Wohnzimmer führen wir die IT- und die AV-Welt immer stärker zusammen", so Pressesprecher Nils Seib bei Sony in Köln. Dabei kommt das Herzstück meist aus der Informationstechnologie: „Der Computer ist der Server und das Archiv des Heimnetzwerks", so Seib.

Bei Philips können die Geräte auch ohne Hilfe eines Computers miteinander agieren. Mit einem digitalen drahtlosen Medienempfänger werden die „Medienbrüche" überwunden. Philips setzt wie Sony nach Angaben von Pressesprecher Jean-Philippe Roman auf offene Lösungen. „Man muss mit den Geräten miteinander reden, ohne Computerexperte zu sein."

Schweriner Volkszeitung

05.08.2004

PC statt Pflegepersonal

Innovationszentrum Inhaus in Duisburg erprobt intelligente Techniken für altengerechtes Wohnen

In den eigenen vier Wänden wohnen, so lang es eben geht: Diesen Wunsch kann intelligente Technik unterstützen. Seit März 2003 tuten rund 15 Ingenieure im „Inhaus – Innovationszentrum Intelligentes Haus" an der Lotharstraße 55 in Duisburg, was mit Computertechnik heute schon machbar ist.

Türen, die sich auf Zuruf öffnen, Kühlschränke, die fehlende Ware selbst nachbestellen, oder Badezimmer, die automatisch erkennen, wer sie betritt, zählen in diesem Haus eher zu den simplen Projekten. Namhafte nationale und internationale Unternehmen erproben hier unter Leitung des Fraunhofer IMS weitaus ausgefeiltere Konzepte, die insbesondere ältere oder betreuungsbedürftigen Menschen den Alltag erleichtern.

Vergesslichkeit allein wäre beispielsweise kein Grund, den eigenen Haushalt aufzugeben, wenn verlegte Schlüssel sich durch Fingerabdrücke ersetzen ließen und intelligente Herde, Wasserkähne und Waschmaschinen sich rechtzeitig vor Brandkatastrophen oder Überschwemmungen selber abstellen.

Auch Menschen mit psychischen Handicaps könnten weiterhin selbstständig leben, wenn mit einer Art Pennüberwachung über Sensoren in den Räumen bestimmte normale Verhaltensweisen wie zum Beispiel „ist aufgestanden", „zur Toilette gegangen", „bewegt sich" oder „wechselt Zimmer regelmäßig" registriert und nur bei Auffälligkeiten entsprechende Alarme an Betreuungsstellen gegeben würden.

Fünf Jahre lang soll in Duisburg erprobt werden, was sinnvoll, wünschenswert, bedienbar und letztlich auch bezahlbar ist. Für die ersten 1 000 Haushalte im Rhein-Ruhr-Raum beginnt dabei das „Leben im Smart-Hause" bereits in diesem Jahr. Dann sollen die ersten Technologien in Feldversuch getestet werden. Vorab kann das „Inhaus" in Duisburg von Fachleuten nach Voranmeldung besichtigt werden. ■

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