ReliaVision: In-circuit transistor reliability investigation using XML-based technology reliability information in PDKs

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***Abstract*—To verify the reliability of integrated circuits before manufacturing and testing, aging simulations can assess the impact of transistor degradation mechanisms on circuit performance. Although available in design environments, they still appear uncommon in circuit design projects. One major problem, from our experience, is the simulation effort that aggravates the problem of mastering verification. We present ReliaVision, an approach to overcome this issue by enabling an in-circuit investigation of transistor reliability based on transient stress simulations of mission profiles and demonstrate it based on an example. We particularly address the task of providing transistor reliability information in process design kits in a machine readable form by using XML syntax.**

Keywords—transistor reliability, HCI, BTI, design support, reliability simulation, PDK

I. Introduction

Physical mechanisms that degrade integrated transistors, such as hot carrier injection (HCI) and bias temperature instability (BTI), have been known for decades [1]. The continued shrinking of semiconductor technology nodes has amplified their impact on the long-term behavior of integrated circuits (ICs). This is especially critical for automotive and industrial applications, where ICs have to operate for 10+ years under particularly harsh conditions, but also gains importance for consumer electronics [1].

To verify the reliability of an IC before entering manufacturing, circuit-level aging simulations can be performed. They are available in different environments for electronic design automation (EDA) [3]-[5]. Basically, as indicated in the orange box in Fig. 1, they complement standard verification in IC design projects. Stress simulations, that is transient simulations of typical use scenarios, are performed. The scenarios are often referred to as mission profiles. For each transistor, the individual stress on terms of gate-source voltage V_{gs}, drain-source voltage V_{ds}, and/or drain current I_d is extracted from the waveforms of the stress simulations. Degradation models transform this information into virtually aged individual device representations to mimic the impacts of HCI and BTI. During this transformation, an extrapolation has to take place: while mission profiles in aging simulations last only up to milliseconds due to simulation effort, lifetimes in the range of years have to be addressed. For the extrapolation, it is assumed that the mission profile is periodically repeated until the target lifetime is reached. Writing the results of the transformation and extrapolation back into the circuit netlist results in a representation of the virtually aged circuit after a certain time of operation. This representation can then be investigated based on the testbenches that are available from the standard verification runs.

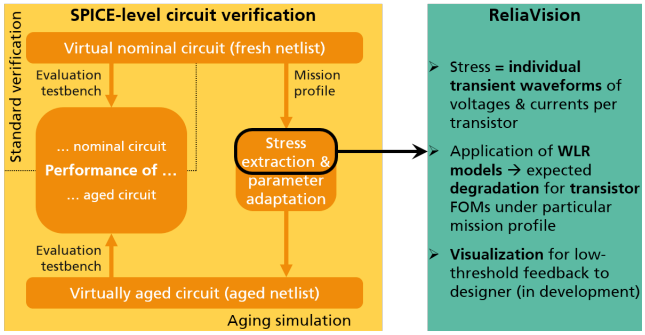

Fig. 1: Aging simulation flow (orange), extended from [2] to illustrate ReliaVision methodology for fast reliability assessment (green).

Although necessary to investigate the impact of transistor degradation on circuit performance, aging simulations take a significant effort. From our experience, this effort is typically dominated by stress simulations and investigating the aged circuit, but not by evaluating the degradation models. This effort is one reason for the only occasional use of aging simulations in practice [6].

We address the issue of the verification effort by a methodology for fast reliability assessment, which is illustrated in the green box in Fig. 1 and referred to as ReliaVision. The basic idea is to determine the individual degradations of device characteristics from stress simulations and visualize these results accordingly. This will provide designers a convenient assessment of device degradation in their circuits without having to simulate any virtually aged circuit.

In this paper, we introduce the methodology before focusing on one important aspect: a flexible way to provide information on device reliability in process design kits (PDKs). We propose an XML representation of reliability information as a solution approach. We discuss the file content and outline a simple application scenario for our fast reliability assessment.

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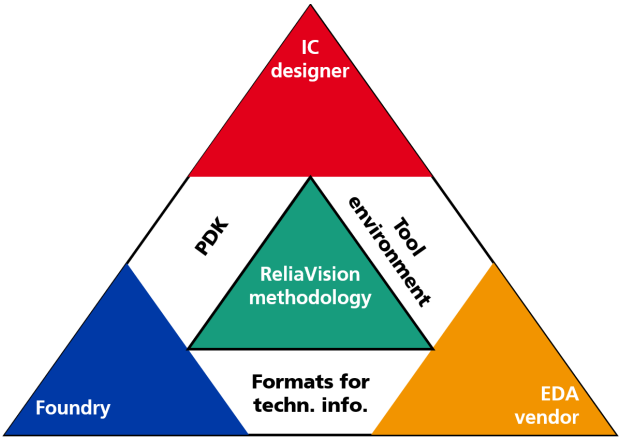

Fig. 2: Interfaces required for ReliaVision methology

II. ReliaVision methodology

The ReliaVision methodology is intended to provide a fast reliability assessment in IC verification. Based on waveforms form stress simulations, the individual degradations of the characteristics of the transistors in a circuit are determined. These can include shifts in device threshold voltages or saturation currents, for instance. The convenient visualization of the results is under development. For example, feedback to designers on transistors with significantly different degradation than surrounding devices or mismatch induced by un-balanced loads outlines potential reliability risks to designers. ReliaVision is intended to support an efficient identification of these risks but leaves the evaluation on criticality up to the designer's expertise. Analyzing the impact of HCI and BTI degradation on circuit performance remains a task for aging simulations.

We are aware of the fact that similar approaches are occasionally used in the industry. For instance, checkers for safe operating areas (SOAs) investigate whether device bias conditions exceed critical limits. Device reliability can also be analyzed based on wrappers around the compact models, similar to the approach proposed in [7]. With their interfaces and flows, these custom solutions are tailored to the particular design styles and environments.

We target a unified methodology that is more flexible and easier to transfer. For this purpose, we have to establish different interfaces in the interplay between foundries, IC designers, and EDA vendors. As visualized in Fig. 2, it is state of the art that IC designers use the tool environment provided by the EDA vendor and technology information provided by the foundry in the PDK. Foundries and EDA vendors have to align on which technology information needs to be available in which formats to enable an efficient application of the EDA tools. For the ReliaVision methodology, we need

- a reasonable and efficient way to exchange device reliability information, preferably as part of PKDs;
- a corresponding approach to preferably support multiple simulation tools and design data, such as schematic and layout;
- as well as feasible and convenient visualizations of the analysis results

to make our approach more flexible than existing custom solutions.

In particular, the reliability investigation in ReliaVision is based on wafer level reliability (WLR) models. Reliability teams in foundries investigate the impact of transistor degradation mechanisms, such as HCI or BTI, as part of the process qualification. WLR measurements are performed according to applicable standards, such as JEDEC standards in [8]-[10]. In stress-measure-stress procedures, the degradation of selected figures of merit (FOM) is recorded, for instance depending on time t, temperature T, gate-source voltage V_{gs}, drain-source voltage V_{ds}, drain current I_{d}, or device geometry. The selection of the figures of merit (FOMs) differs between foundries as well as technology nodes and their target applications.. Examples include the maximum linear current I_{dlin}, saturation current I_{dsat}, maximum transconductance G_{mmax}, threshold voltage V_{th}, etc. Corresponding WLR models are chosen and calibrated to fit the measured data. For instance, the equation

$$\Delta = A \cdot \exp\left(\frac{B}{V_{\mathrm{ds}}}\right) \cdot \exp\left(\frac{E_{\mathrm{aa}}}{k_{\mathrm{B}} \cdot T}\right) \cdot t^{n} \qquad (1)$$

is a simple HCI model for the degradation of an arbitrary FOM Δ depending on drain-source voltage V_{ds}, temperature T, and time t with constant A, fit parameter B, apparent activation energy E_{aa}, Boltzmann constant k_{B}, and time exponent n [11]. The extrapolated time to achieve a (usually) 10 % degradation at a typical stress of 10 % above operating voltage is documented as device lifetime in the device specification.

As introduced in Fig. 1, ReliaVision is based on simulations of mission profiles, which are transient stress simulations. Device-specific stress is extracted in terms of transient voltages and currents. WLR models, such as in Eq. (1), are used to determine the expected degradation of the device FOMs and provide an overview feedback to the designer for assessing potential reliability issues and deciding on the necessity of detailed aging simulations. The details of the feedback to the designers are under development. Potential solutions include

- log-file information and, e.g.; bar charts to outline devices with the highest degradation;
- back-annotations of information on device degradation into the schematic;
- and color-coded overlays of expected transistor degradation on top of the circuit layout.

From the perspective of a foundry, such a method has to be enabled by providing device reliability information in terms of parametrized WLR models. To solve this task, we propose to use XML syntax. Details of this representation of the reliability information are discussed in the subsequent section.

III. XML representation of WLR models

To demonstrate how WLR information can be represented in XML, we use an artificial example of technology qualification results. We assume an HCI degradation of the linear current IDLIN and the saturation current IDSAT of an NMOS to be described by the WLR models

$$\mathrm{d\_IDLIN} = \frac{\mathrm{IDLIN}(t)}{\mathrm{IDLIN}(t=0)} = -0.71 \cdot \exp\left(\frac{-5}{V_{\mathrm{ds}}}\right) \cdot t^{0.25} \qquad (2)$$

$$\mathrm{d\_IDSAT} = \frac{\mathrm{IDSAT}(t)}{\mathrm{IDSAT}(t=0)} = -1.56 \cdot \exp\left(\frac{-7}{V_{\mathrm{ds}}}\right) \cdot t^{0.25}. \qquad (3)$$

```xml
<?xml version="1.0" encoding="UTF-8"?>
<technology>
    <!-- definition of aging equations -->
    <degradationmodels>
        <!-- simple HCI model -->
        <model name="HCI_simple">
            <equation  expr="A * exp(B/VDS) * t^n">
            <parameter name="A"       unit=""/>
            <parameter name="B"       unit="V"/>
            <parameter name="n"       unit=""/>
            <variable  name="VDS"/>
            <variable  name="t"/>
        </model>
    <!-- other models -->
    </degradationmodels>

    <!-- degradation of device "nmos" -->
    <device name="nmos">
        <!--"HCI section"-->
        <mechanism name="HCI">
            <!-- degradation of figure of merit "IDLIN" -->
            <FOM name="d_IDLIN" model="HCI_simple">
                <parameter name="A"   value="-0.71" />
                <parameter name="B"   value="-5"    />
                <parameter name="n"   value="0.25"  />
            </FOM>
            <!-- degradation of figure of merit "IDSAT" -->
            <FOM name="d_IDSAT" model="HCI_simple">
                <parameter name="A"   value="-1.56" />
                <parameter name="B"   value="-7"    />
                <parameter name="n"   value="0.25"  />
            </FOM>
        </mechanism>
    </device>
</technology>
```

Fig. 3: XML representation of transistor reliability information.

These models, which are simplified from Eq. (1), are very basic for demonstration purposes only.

With our work, we want to establish a flexible interface to provide reliability information. At the foundry side, WLR information shall be provided in terms of parametrized models. Considering the fact that the formulations of WLR models may change when considering different FOMs of a transistor, different transistors in one technology, or different technologies in a foundry, the interface should allow the specification of custom WLR models and parameters. The given equations are automatically parsed and evaluated by ReliaVision. To use a file format that can be easily processed by software and that can be read by humans for maintainability, we chose XML. Fig. 3 shows the resulting XML representation of the NMOS reliability information defined in Eqs. (2) and (3).

In the element tagged "degradationmodels", WLR models are defined in terms of equations. In addition, parameters (A, B, n) and variables (V_{ds}, t) are identified. This distinction is required when automatically evaluating the WLR models and apply them to simulation waveforms. In Fig. 3, the model "HCI_simple" implements the general model behind Eqs. (2) and (3). Additional impact factors can easily be added to a WLR model by adding the corresponding term, for instance an Arrhenius term for the temperature dependency. With unique names, further WLR models can be defined. In our implementation, we have to ensure that ReliaVision is able to apply models, which are defined for DC stress conditions, such as in Eqs. (1)-(3), to arbitrary transient stress waveforms. To allow models beyond t^n, we work on implementing the findings of [8]: model formulations of the form $g(f(V) \cdot t)$ can be efficiently applied to transient stress. WLR models beyond this rule can be addressed with numerical methods. Further investigations are required to support models that are based on subsequent phases in the stress waveforms. An example is the NBTI model in [13], which is based on subsequent phases of stress and recovery.

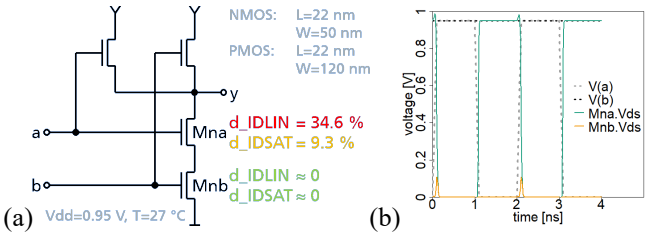

Fig. 4: (a) NAND2 schematic with degradations of IDLIN & IDSAT after 5 years of operation with input a pulsed (2 ns period, 100 ps rise and fall time, 900 ps at logic "1") and input b at logic "1"; (b) input waveforms and resulting V_{ds} of both NMOS instances.

The "device" element applies the WLR models, which were defined in the "degradationmodels" section, and sets their parameters for the FOMs of the devices. In Fig. 3, the model parameters A, B and n are set for the IDLIN and IDSAT degradations of the NMOS under HCI according to Eqs. (2) and (3). When data is available for other FOMs, further degradation mechanisms (e.g. BTI), or additional devices, they can be added correspondingly. This approach allows foundries to efficiently maintain and add reliability information when required. From our perspective, this is beneficial for foundries that typically provide the reliability information.

We work on extending the XML representation toward degradation models for aging simulations. An idea to generically transfer WLR information to subcircuit models or adapted model card parameters to mimic transistor aging is to use interpolation schemes. To enable this, we implemented our approach to dynamically evaluate the reliability information in the XML file and transient stress simulation results into the common SPICE simulator APIs for degradation models, for instance OMI [1]. This approach also allows to combine different use conditions by defining different consecutive mission profiles.

IV. Application Example

To demonstrate the results of ReliaVision with back-annotations of the results to the schematic, we apply it to the characterization of a NAND2 gate with the schematic in Fig. 4(a). The circuit is based on the 22 nm low-power predictive technology model (PTM) [14],[15]. Furthermore, we use the artificial reliability information in Eqs. (2) and (3), which describe the NMOS HCI degradation of the linear current IDLIN and the saturation current IDSAT.

In our simulations in a commercial SPICE simulator, we keep the NAND2 input "b" at "logic 1" and stress the input "a" with a pulse signal for 5 years. The corresponding simulation waveforms are shown in Fig. 4(b). ReliaVision extracts the V_{ds} waveforms of both NMOS instances and computes the individual degradations of IDLIN and IDSAT by applying Eqs. (2) and (3). For visualization purposes, we manually added these information to the schematic in Fig. 4(a) and work on an automated solution. Due to the switching activity at input "a", the NMOS instance "Mna" significantly degrades (34.6 % IDLIN degradation and 9.3 % IDSAT degradation) while instance "Mnb" is nearly unaffected. The degradation can easily be transferred into a lifetime

information if required, e.g. into the time required to achieve a 10 % degradation.

This information is provided to the designer to support in assessing potential reliability issues. How the individual degradations of the different transistor instances impact the circuit behavior, can only be investigated by further simulations of the aged circuit. This step will be available in the future when the WLR information determined in ReliaVision can be transformed into degradation models for aging simulations will be closed automatically. For this, we need to extend the XML representation as outlined at the end of Section III.

V. Summary

In this paper, we introduced the idea of ReliaVision to enable an efficient in-circuit assessment of transistor degradation and lifetime. Based on transient SPICE simulations of mission profiles and WLR information, the degradations of transistor FOMs are computed individually. We found that providing transistor reliability information, preferably as part of the PDK, is a major sub-task on the way to enabling the methodology. We propose a generic XML representation of reliability data to address this task. Since the file is evaluated and processed automatically, the XML format provides users an immense flexibility in terms of setting up and maintaining aging equations, impact factors, captured devices, and FOMs depending on available data and designer's needs.

Nevertheless, multiple tasks remain for future work. They include the interface of ReliaVision to designers, especially for visualizing the results; an extensions to efficiently allow aging simulations of circuits when required remain; as well as approaches to include statistical information on variability of manufacturing processes and aging mechanisms.

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