COMPARISON OF DIFFERENT DIELECTRIC PASSIVATION LAYERS FOR APPLICATION IN INDUSTRIALLY FEASIBLE HIGH-EFFICIENCY CRYSTALLINE SILICON SOLAR CELLS

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ABSTRACT: Due to the trend towards thinner and higher efficient crystalline silicon solar cells, it is substantial to decrease the surface recombination velocity and to increase the internal optical reflection at the rear surface. Therefore, dielectric passivation of the rear surface is a key technology for the next generation of industrial solar cells. This paper presents a study on the applicability of different dielectric layers and stack systems ranging from high-temperature thermal oxides via silicon nitrides to low-temperature amorphous silicon. It is pointed out that a low surface recombination velocity in lifetime measurements is only one necessary condition for a high-quality rear structure. Due to its high thermal stability and good surface passivation quality, silicon carbide layers have been used as rear surface passivation in high-efficiency cell structures and efficiencies of more than 20% are reported for the first time.

Keywords: High Efficiency- 1: Passivation - 2: c-Si - 3.

1. INTRODUCTION

In order to reduce the costs of solar cells from mono- and multicrystalline silicon wafers, efficiencies have to be increased and wafer thickness has to be decreased. A crucial component of the cell for the realisation of such goals is the rear surface due to the increasing demands for optical (internal reflection) and electrical quality (surface passivation). The standard structure for state-of-the-art industrial cells is an aluminium back surface field (Al-BSF) created by firing a screen-printed Al paste. Although this process is well suited in terms of industrial feasibility, it can not be used for future generation cells with efficiency levels above 18% and wafer thicknesses below 150 µm. This is due to the relatively poor electrical and optical properties which will reduce the cell performance on thin substrates. Additionally, the wafer bow caused by the Al firing process is a crucial problem. Thus, it is quite obvious that future generation industrial cells will use the same rear surface structure as the one introduced for high-efficiency lab cells a couple of decades ago: the dielectric passivation. As the related local contact formation is industrially feasible using the laser-fired contact (LFC) process, one question is still open: "What is the optimal dielectric passivation layer?"

This paper tries to give an answer to this important question not only in terms of electrical and optical quality of the different layer systems, but also in terms of their application in cell structures, required surface preparation and topography, thermal budget and thermal stability.

2. DIELECTRIC PASSIVATION VS. BACK SURFACE FIELD

As already mentioned the present state-of-the-art rear surface structure of industrial silicon solar cells, the screen-printed and thermally fired Al-BSF, has two major restrictions: the wafer bow due to the firing process and the lower electrical and optical properties. Especially for the crucial parameter S_{back}, a great variety of values can be found in literature which makes it difficult to evaluate the potential of Al-BSFs vs. dielectric passivation.

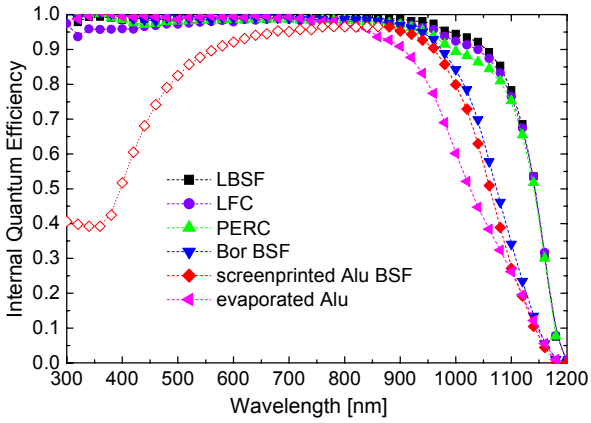

Figure 1: Internal quantum efficiency of different rear surface structures on 1 Ω cm 250 µm thick FZ-Si with a high-efficiency front structure. Note: The low internal quantum efficiency for short wavelengths (open symbols) of the Al-BSF cell is due to a degradation of front surface passivation during firing. Nevertheless, the IQE starting at 900 nm is identical to the performance of industrial cells.

Thus, at Fraunhofer ISE we have performed an experimental study of different rear surface structures combined with a high-efficiency front structure which is not limiting the cell performance [1]. This makes it possible to determine the surface recombination velocity S_{back} and the internal reflectivity R_{back} quite accurately. Figure 1 shows the measured internal quantum efficiencies of different rear structures starting from a low-quality ohmic Al-contact up to a PERL[2]/LBSF[3] rear surface. The effective S_{back} and R_{back} have been extracted from the IQE and reflection measurement.

Table I: Internal reflectivities (R_{back}) and rear surface recombination velocities (S_{back}) as extracted from the data in Figure 1.

Structure	R_{back} [%][1]	S_{back} [cm/s]
LBSF (105 nm oxide)	94.5	60
LFC (105 nm oxide)	95.5	110
PERC (105 nm oxide)	95.0	200
Diffused Bor-BSF	71	430
Screen-printed Al-BSF	65	750
Evaporated ohmic Al contact	83	10^7

Using these parameters, it is possible to determine the influence of different rear surface structures on the performance of industrial cells (see Figure 2). With the introduction of higher-quality emitter structures, the benefit of a dielectric passivation will be even higher.

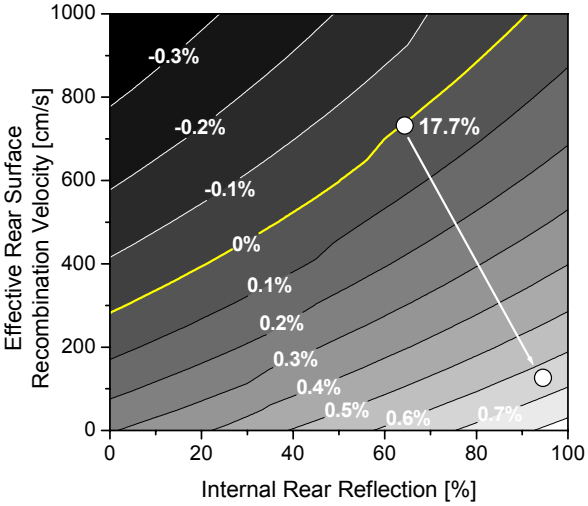

Figure 2: Change in efficiency gain due to variation of S_{back} and R_{back}. The 0% isoline refers to a 220 µm thick industrial solar cell with 60 Ω/sq emitter and Al-BSF on 1 Ωcm monocrystalline silicon with a diffusion length of 400 µm. The second point relates to the LFC parameters.

3. PASSIVATION MECHANISMS OF DIELECTRIC LAYERS

There are two different mechanisms leading to good surface passivation: (a) the reduction of interface states D_{it} and (b) field effect passivation, i.e. the strong reduction of one carrier type by incorporation of fixed charges Q_f in the passivation layer. Although these mechanisms or the combination of both lead to low surface recombination velocities, the resulting $S_{eff}(\Delta n)$ curve shows different characteristics (see Figure 3). It seems that the reduction of interface states is more effectively reached for thermally grown SiO_2 layers while the field effect passivation together with a moderate reduction of D_{it} is more typical for deposited layers like SiN_x. Typical values for SiO_2 are $D_{it} = 10^{10}$ cm^{-2}eV^{-1} and $Q_f = 10^{10}$ cm^{-2} while for SiN_x values $D_{it} = 10^{11}$ cm^{-2}eV^{-1} and $Q_f = 10^{11}$ cm^{-2} are found.

[1] Note that for a proper description, it is necessary to introduce a Phong-like characteristic.

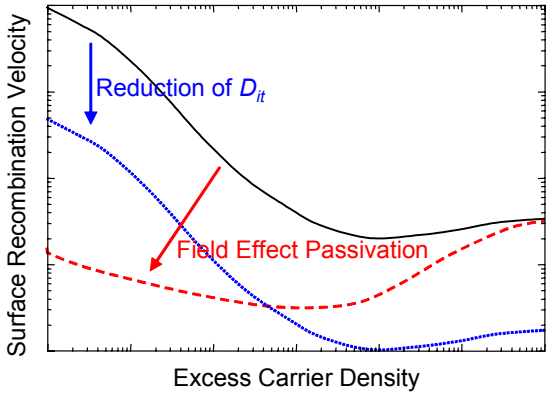

Figure 3: Sketch of the impact of the two passivation schemes, reduction of interface state density, D_{it} (dotted) and field effect passivation (dashed).

4. DEPOSITION TEMPERATURE

A critical issue for the fabrication of a dielectric passivation layer is the deposition temperature. The best solar cells so far have been passivated with thermally grown oxides [4,5]. Thermal oxides have been optimized in MOS-technology for decades and supported by the well-known "Alneal"-effect [6] extremely low interface state densities and surface recombination velocities have been achieved. Unfortunately, the typical temperature of thermal oxidation is around 1050°C. This temperature range is no problem for high-quality FZ-Si and can even increase the minority carrier lifetime in Czochralski-grown silicon [7] but it is extremely detrimental for block-cast multicrystalline silicon [8,9]. The minority carrier lifetime can be reduced by a factor of about 10 [10]. Thus, it is substantial to find passivation layers deposited at lower temperatures. One possibility quite close to the thermal oxide is a wet oxidation at temperatures of around 850°C [11]. The wet atmosphere increases the oxidation rate drastically which makes it possible to obtain the typical oxide thickness of 105 nm in a reasonable time. This strategy was applied to multicrystalline silicon and has lead to the actual record for multicrystalline silicon of 20.3% [10]. The average efficiencies of these cells were in the range of more than 18% showing that also low-quality regions do not degrade due to this treatment. A very interesting alternative to wet oxidation is the creation of a thin oxide layer at temperatures around 850°C in dry atmosphere. This thin layer has to be combined with a second deposited layer on top and will be discussed later on.

The second choice are deposited layers such as PECVD SiN_x. The typical deposition temperatures are in the range of 350° to 400°C and excellent surface recombination velocities of less than 10 cm/s have been reached (see e.g. [12]). An additional advantage of SiN_x is the incorporation of hydrogen in this layer which could act as a bulk passivation source for multicrystalline silicon. A very fast alternative to PECVD reactors are sputter systems for which excellent surface recombination velocities below 30 cm/s have also been achieved [13].

The lowest deposition temperatures between 200°C and 250°C are needed if amorphous silicon is used as the rear passivation layer. This passivation scheme is successfully applied in the HIT structure [14] for which efficiencies of

21% have been obtained. Recently, it was shown that amorphous silicon works also pretty fine with standard cell structures with diffused emitters [15] and efficiencies of 20.1% have been reported.

5. PRECONDITIONING

Besides the deposition temperature, another technological issue is the preparation of the surface before the fabrication of the dielectric layer. A clean surface is substantial for oxidation processes since otherwise surface contaminants will diffuse into the bulk. This problem is less severe for deposited passivation layers due to the lower process temperatures. However, a very shallow layer of crystal damage which could be left over after a prior etching step will decrease the passivation quality significantly. This problem is less pronounced for oxidised surfaces since a part of the upper silicon layer is taken by the oxidation process (approximately half of the final oxide layer).

Another topic is the surface geometry. In contrast to microelectronics, surfaces in industrial solar cells are generally not smooth due to the anisotropic damage etch or a wet-chemical texturization process.

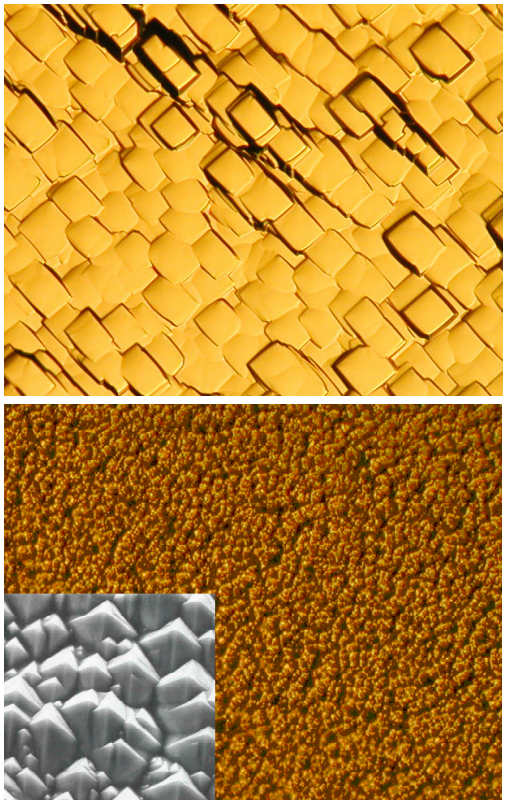

Figure 4: Surface topography after alkaline damage etch (top) and random pyramid texture (bottom). Both photos are taken with a light microscope; the inset in the lower figure is a scanning microscope picture to show the pyramid geometry more clearly.

It is an important question whether a rough surface structure results in lower optical and electrical performance if compared to a smooth shiny etched surface. Thus, we have prepared different topographies on a set of solar cells with the same material (FZ-Si) and cell structure (front: random pyramids, 105 nm thermal oxide, rear: 105 nm thermal oxide, 2 µm aluminium and LFC contacts).

Table II. Results of oxide-passivated cells on 0.5 Ω cm FZ-Si with different rear surface topographies (average of 7 cells).

Rear surface topography	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF*	η [%]
Shiny etched	677.1 +/-0.6	38.14 +/-0.15	80.4 +/-0.2	20.8 +/-0.1
Damage etched	678.9 +/-0.3	38.21 +/-0.06	80.9 +/-0.1	21.0 +/-0.04
Random pyramids	673.2 +/-2.2	37.25 0.28	80.1 +/-0.4	20.1 +/-0.2

While the cells with the damage-etched and shiny-etched rear surface nearly show the same performance (see Tab. II), the cells with the textured rear exhibit lower efficiencies mainly due to a loss in current which can be clearly attributed to the lower performance of the textured rear surface (see Figure 5).

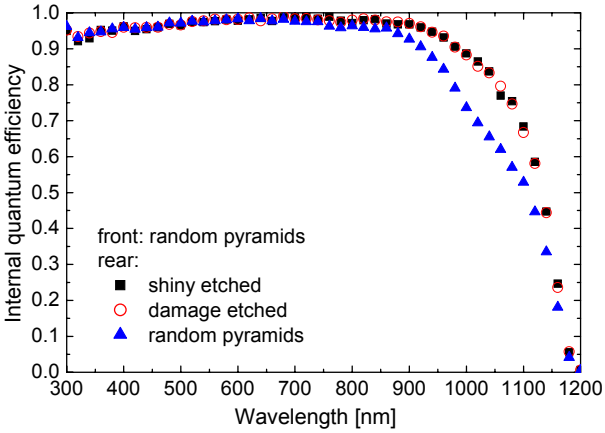

Figure 5: Internal quantum efficiencies of cells with oxide-passivated rear surface on 0.5 Ω cm FZ silicon.

De Woolf *et al.* [16] showed a similar reduction of passivation quality with increasing surface roughness for PECVD-SiN_x-layers. This reduction was less significant after a subsequent thermal treatment.

6. INTERNAL REFLECTION

Next to the passivation quality it is important to analyse the optical properties of a rear surface passivation layer. The "traditional" Si/SiO_2/Al system has very high internal reflectivity due to the low refractive index of SiO_2 (n=1.46) [17]. A pyramid texture on the front surface results in an oblique light path (angle 41.4° from perpendicular) and total reflection occurs at the rear surface. Thus, R_{back} values of 95% to 89% can be obtained. However, since most of the deposited layers with good passivation quality as Si-rich SiN_x have quite high refractive index, R_{back} is strongly decreased.

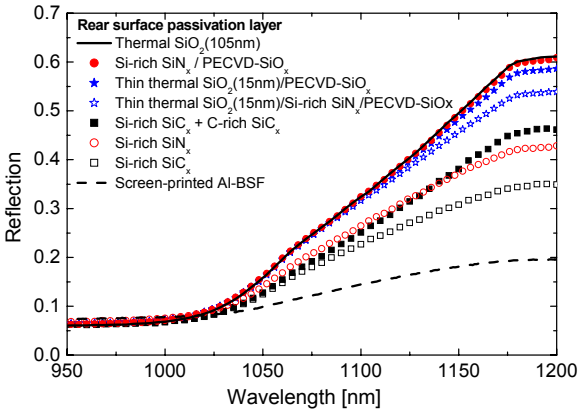

Figure 6: Reflectivity measurements of solar cells with front texture and different rear surface passivation layers. The upper margin is a 105 nm thermal oxide (solid line), the lower margin is screen-printed Al-BSF (dashed line).

Figure 6 shows the reflectivity measurements of solar cells with textured front side and different rear surface passivation layers. If silicon-rich layers with high refractive indexes (SiN_x = 2.9, SiC_x > 3) are applied, the R_{back} values are still better than the industrial standard but much lower than the thick thermal SiO_2 layer. Since these layers usually show very low surface recombination velocities, it is favourable to keep them as the first layers close to silicon. In order to improve the optical properties it is a good idea to apply a second layer with a lower refractive index [18]. In fact, a quite strong increase is observed if a PECVD SiO_2 (n = 1.46) is deposited on top of the Si-rich SiN_x-layer or a C-rich SiC-layer on top of the Si-rich SiC_x layer ($n \approx 2$), respectively. Also the optical performance of a thin thermal oxide (15 nm) can be increased by the deposition of additional low-temperature PECVD-SiO_2. Thus, stack systems allow to assign the two important tasks "passivation" and "reflection" to different layers.

Recently, dielectric rear passivation concepts have been introduced where the rear surface metallization is performed by grid-shaped screen-printed contacts, thus, leaving nearly the whole surface with only the dielectric passivation layer. A great disadvantage of such systems is much lower internal reflection as compared to the Si/dielectric layer/Al system.

7. APPLICATION TO SOLAR CELLS

Although it seems possible to design the perfect layer or layer system just by lifetime and optical measurements, the final decision has to be made by applying these layers to solar cells. A good example that a good surface passivation quality is only a necessary but not a sufficient condition is given by the SiN_x passivation. Although SiN_x layers show the very best surface passivation quality on lifetime test wafers - even better than thermal oxidation - nobody has managed to fabricate a cell with efficiencies as high as the ones featuring the "classical" thermal oxidation. Especially, the short-circuit current is significantly lower. This reduction was explained by Dauwe *et al.* [19] by the short-circuiting of the inversion layer induced by the fixed charges in the SiN_x layer at the rear contact points. Since the inversion layer is a crucial part of surface passivation mechanism of SiN_x layers, the apparent quality of SiN_x layers on lifetime test wafers "vanishes" when applied to real cells. The best values reported so far for silicon nitride rear surface passivation were 21.5% [20] and 20.6% [21]. In the first case a very sensitive plasma etch was used to open the contact holes in the SiN_x layer so that the inversion layer was not shunted. In the second case a local boron BSF reduced the shunting of the inversion layer. However, if used with a "rough" process like laser-fired contacts or mechanical sawing generally efficiencies below 20% were reached.

This problem can be solved in two ways: (i) the development of SiN_x layer which are passivating more due to a reduction of interface states than to field effect passivation (i.e. reduction of D_{it} and Q_f) [18] or (ii) by the application of thin thermal oxide (10-15 nm) below the SiN_x layer. This oxide layer can be grown very fast (e.g. RTO) and at relatively low temperatures (850°C). Excellent surface passivation quality has been reported [22,23]. Additionally, the thin oxide layer will also serve as a front passivation for lower doped emitter on the front[2].

Using such a stack system on the rear efficiencies of 20.5% have been reported [24]. By the addition of the thin oxide layer, a clear improvement of the internal quantum efficiency if compared to a pure SiN_x layer was observed (see Figure 7) although both layers showed the same excellent passivation quality (around 1000 µs effective lifetime on 1 Ω cm silicon).

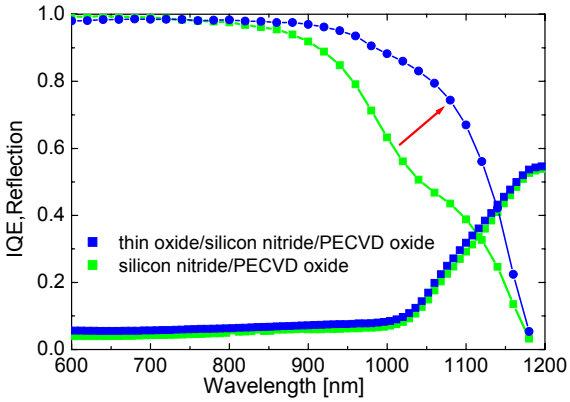

Figure 7: Improvement in red response due to the addition of a thin thermal oxide layer below the Si-rich SiN_x layer. Note the different x-axis scaling which amplifies the effect.

8. THERMAL STABILITY

Another crucial issue is the thermal stability of a passivation layer. Only if the dielectric layer is deposited after the complete fabrication of the front surface (including emitter diffusion, contact deposition and fire step) or if the rest of the cell is also fabricated at very low temperatures (as in the case of the HIT cell), no attention has to be paid to this property. Since it will be quite difficult to obtain a clean surface after the metallization on the front, it would be ideal to deposit the passivation layer before the front contact formation (including firing) or

[2] Since the oxide layer is very thin it is possible to apply a second front layer with higher refractive index (i.e. SiN_x), resulting in very good optical performance.

even better before emitter diffusion. In fact the latter case would be ideal since an unfavourable emitter diffusion on the rear would be avoided by using the passivation layer as a masking layer. Since the very low-temperature passivation schemes as amorphous silicon show a very low thermal stability, they have therefore to be combined with special new cell structures (as it was done in the HIT cell).

The high-temperature passivation schemes as thermal oxidation show a very high thermal stability. They can be grown before emitter diffusion and have still a very high passivation quality after diffusion and firing step. Thus, for the first application of laser-fired contacts to industrial cell structures, thermal oxides were used and efficiencies of 18% have been achieved [25].

But even if using thermal oxide, it is not possible to deposit the rear metal (aluminium) before a high-temperature step of moderate duration and to keep the full high passivation quality. We have performed Suns-Voc-measurements [26] on test structures with emitter and front passivation but without front contacts and full rear contact scheme (105 nm thermal oxide, thermal evaporation 2 µm aluminium and LFC contacts). By leaving out the front contacts it is guaranteed that no J_{02} or R_p problems arise due to the diffusion of the front metallization. The open-circuit voltage measured before the following thermal treatment was 670 mV. After thermal treatment for 10 min at different temperatures in forming gas the voltage first increases up to 700 mV at a temperature of 450°C and then drops down to less than 620 mV at 700°C (see Figure 8). The increase is due to the beneficial "Alneal" effect, while at higher temperatures Al spikes through the oxide layer and destroys the passivation quality. Note that this temperature treatment for 10 min is a much harder stress for the dielectric layer compared to the firing step which lasts only for seconds.

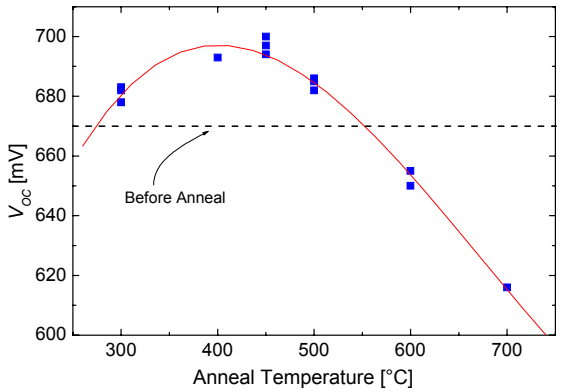

Figure 8: Open-circuit voltage of a test structure measured using Suns-Voc. At temperatures below 450° the voltage is increased due to "Alneal" effect, at higher temperatures Al spikes through the rear oxide layer.

Using PECVD SiN_x layers deposited at temperatures of 350°C up to 400°C the thermal stability has to be analysed carefully. De Woolf *et al.* performed a study on PECVD-SiN_x layers with different compositions [16]. They confirmed the trend already observed by Lauinger *et al.* [27] that Si-rich layers show the best surface passivation quality. However, after a thermal treatment comparable to a firing step (without metal coverage on top) they found a strong decrease of passivation quality for these Si-rich layers while more moderate composed layers show quite a good thermal stability. Using these thermally stable nitrides for a PERC-like structure, efficiencies of 17.1% have been reported [28]. Thus, SiN_x layers could be in principle applicable before the firing step.

To enhance the thermal stability of a SiN_x layer and also to increase the optical properties (see section above), it is beneficial to apply a PECVD SiO_2 layer on top of the SiN_x layer [18]. Since this deposition can be performed in the same system, such a stack system is not too complicated for industrial production. In fact a stack system of thin thermal oxide/PECVD nitride/PECVD oxide showed reasonable surface passivation quality after a 795°C firing step [24].

Nevertheless, there are other materials which seem to have physical advantages in terms of thermal stability. SiC_x is well-known to be quite hard against thermal treatments. In fact it is used at Fraunhofer ISE as a diffusion barrier layer for recrystallization of silicon thin-film layers on low-cost substrates [29]. Recently, Martín *et al.* [30] reported that SiC_x also shows good passivation quality (S < 30 cm/s). After a firing step at 730°C, the passivation quality was not decreased. Needless to say that an application of this new material type to a high efficient cell structure is quite interesting.

9. A NEW SYSTEM: SiC_x

In a first experiment high-efficiency solar cells with oxide-passivated emitter (120 Ω/sq), random pyramids and evaporated contacts were fabricated on 0.5 Ω cm 250 µm thick FZ-silicon at Fraunhofer ISE. After removing the oxide on the rear surface, different SiC_x layers and layer systems were deposited at UPC, Barcelona. The contact regions were opened using plasma etching and aluminium was locally evaporated in this holes. After a short forming gas anneal, the structures were measured using QSSPC [31].

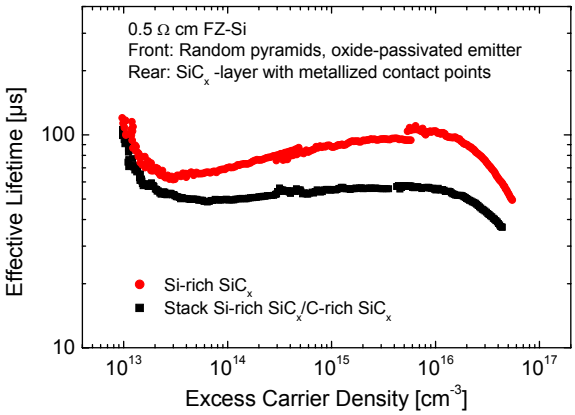

Figure 9: QSSPC lifetime measurements of solar cell precursors with SiC_x rear passivation.

From these measurements an open-circuit voltage of 674 mV and 664 mV for a Si-rich SiC_x layer and a stack system of Si-rich SiC_x layer plus a C-rich SiC_x layer can be predicted, respectively. Actually, the finished cells show a different trend. While the cells with the stack system exhibit a very good performance, the parameters of the cells with the Si-rich layer are quite below the expected values. This effect is probably not due to a

chemical degradation of the layer (see [32]). As discussed before the stack system with the combination of a high and low refractive index system also resulted in much better optical properties. Although, this was the very first batch, already conversion efficiency higher than 20% was achieved, a very encouraging result.

Table III: Solar cell results with SiC_x rear passivation

SiC_x rear surface layer system	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]
UPC stack Si-rich/C-rich, PERC structure	665.3	38.26	79.4	20.2[3]
UPC layer Si-rich, PERC structure	624.8	36.03	80.3	18.1
ISE layer type 2l Si-rich LFC structure	664.8	37.51	80.3	20.2[3]

Thus, an optimization study was performed on the Roth&Rau plasma reactor at Fraunhofer ISE. Two different single layer system based on different composition were deposited on 1 Ω cm FZ-Si and the lifetime was measured (see Figure 10). Not only the deposition but also the surface conditioning was performed in the PECVD reactor. These layers were used for the rear passivation of cells with the identical front structure as described before. However, this time e-gun evaporation was used for the deposition of the 2 µm thick Al layer and the laser-fired contacts process was applied. Although, the cells have not been annealed after e-gun evaporation and LFC formation efficiencies of more than 20% have been achieved.

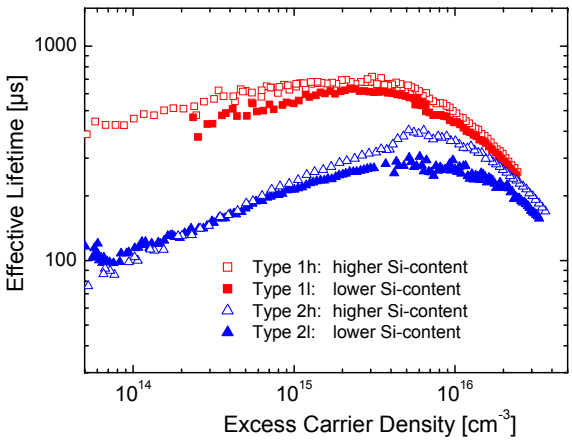

Figure 10: Lifetime test structures passivated with different SiC_x-layer on 1 Ω cm FZ-Si.

Surprisingly, the best results were achieved on layer type 2, while for layer type 1 which shows a much higher effective lifetime, the cell efficiency was about 1% absolute lower. This emphasizes again the fact that a good surface passivation is only one prerequisite for a good solar cell.

[3] Independently confirmed at Fraunhofer ISE CalLab.

10. CONCLUSION

The decision for the "best" dielectric passivation layer can not be only based of lifetime measurements on test structures. Other criteria as e.g. thermal budget and stability, optical performance, surface topography and preconditioning are also very important to look at.

In our study we found that a very good performance can be obtained by stack systems consisting of a thin thermal oxide plus PECVD nitride and oxide layers resulting in efficiencies higher than 20%. The thin thermal oxide (15 nm) avoids the detrimental shunting effect of silicon nitride and can serve as surface passivation for high-quality front structures (lowly doped emitter) at the same time.

For a direct application to standard screen-printed cells, a less complex system with a single passivation layer would be more interesting. SiC_x was introduced as an alternative to the well-known SiN_x and efficiencies of more than 20% have been achieved.

Acknowledgements

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