
Current Control for an Interleaved 3-phase, 3-level Power Converter with the Balancing of Multiple Parallel-Connected Phase Legs

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Abstract

As alternatives to traditional energy sources, renewable energy sources like solar and wind energy are being employed more frequently. Due to numerous circumstances including weather, irradiance level, wind speed, etc., the main energy of these sources varies greatly in its nature. To connect these sources to the grid, high-efficiency power electronic converters are needed. The operation of grid-connected converters depends heavily on control algorithms. Therefore, this thesis aims to examine a PI control technique with different tuning methods to tune a PI controller for a 3-phase, 3-level ANPC inverter with an LC+EMI output filter.

Develop a control system for a 3-level 4-wire active neutral point clamped (ANPC) inverter utilizing two interleaved output stages. The control should assure stable grid operation as well as a balanced current distribution between the two interleaved output stages. The implementation of current control for a 3L ANPC inverter. At first, the plant needs to be analyzed and modeled as a state-space model. Investigate and implement different tuning methods to tune a PI controller and analyze the performance of the system by varying the grid impedance and the system parameters. Determine which tuning method is most effective based on the performance of the system. Modeling and simulation of power electronic converters using averaged model and switched model. The stability of the system is analyzed in different scenarios.

Statement

The work in this thesis is based on the research carried out at the Department of Stormrichter Regelung & Embedded Systems, Fraunhofer-Institut für Energiewirtschaft und Energiesystemtechnik IEE, Kassel and the Technische Hochschule Rosenheim. No sections of this thesis were submitted or used to gain another academic degree. Hereby I state, that this thesis was written alone by myself.

Rosenheim, July 7, 2022

Ravi Chandra Reddy Yenuga Krishnareddy Gari

Acknowledgment

This Master's thesis is based on the research carried out at the Department of Stormrichter Regelung & Embedded Systems, Fraunhofer-Institut für Energiewirtschaft und Energiesystemtechnik IEE, Kassel and the Technische Hochschule Rosenheim. I would like to express my deepest gratitude to my supervisor Mr. Matthias Klee and first Examiner Prof. Dr. Ing Franz Stubenrauch for their constant guidance, helpful comments, advice, and support. Their guidance has been the backbone of progress during my thesis and their guidance helped me throughout the whole period of the thesis. Furthermore, I would like to express my sincere gratitude to Mr. Jonas Steffen for giving me this wonderful opportunity to write my thesis at Fraunhofer IEE and for all the help, support, and guidance. I thank him for his faith in me to work on this topic. Besides, I deeply thank the second supervisor Prof. Dr. Ing Frank King.

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Words are inadequate to express my heartfelt gratitude to my parents, girlfriend, and my friends for the moral support and the trust they have in me. Without them, I could hardly finish this work.

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Ravi Chandra Reddy Yenuga Krishnareddy Gari

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1 Introduction

1.1 Background

Due to the uncertainty about the future supply of crude oil and the related problems of environmental pollution, the renewable energy sector has experienced an increasing trend in the last decade, especially solar and wind energy. The continued growth of the renewable energy market is driven by its low carbon footprint, as carbon emissions are the main cause of global climate change. Global renewable energy consumption is projected to grow by an average of 2.6% (per year) through 2040 [1]. The integration of renewable energy sources into the power grid requires an interface converter. Power electronic converters are considered the backbone of energy conversion. For example, in solar power generation, they convert direct current (DC) from a photovoltaic (PV) array to alternating current (AC), which is then fed into the grid [2]. Remarkable advances in semiconductor technology have enabled better and more efficient power conversion. To increase the power quality and utilization of the PV system, new inverter topologies with better control algorithms must be proposed. This work aims to investigate some of these control techniques for a recently proposed 3-phase, 3-level Active Neutral Point Clamped Inverter (ANPC).

In recent years, grid-connected inverters for PV systems have experienced rapid growth, both for utility-scale applications and distributed generation, because of government incentives, declining PV panel prices, and advances in power electronics [3, 4]. The expansion of photovoltaics has been exponential between 1992 and 2017. During this era, photovoltaics has evolved from a distinct segment marketplace for small applications to a widely used power source. There has been tremendous growth from about 1.2 GW in 1992 to 401.5 GW in 2017. For instance, see Figure 1.1, which shows the annual installed solar capacity for various regions of the globe. Although European countries collectively have the best number of solar installations, China appears to be leading the way in solar installation growth. The European Photovoltaic Industry Association claims that alternative energy is the biggest source of electricity in the world by 2050 [5]. In Germany, it is now common for PV systems to be installed on rooftops or PV farms of varying capacity next to rural roads.

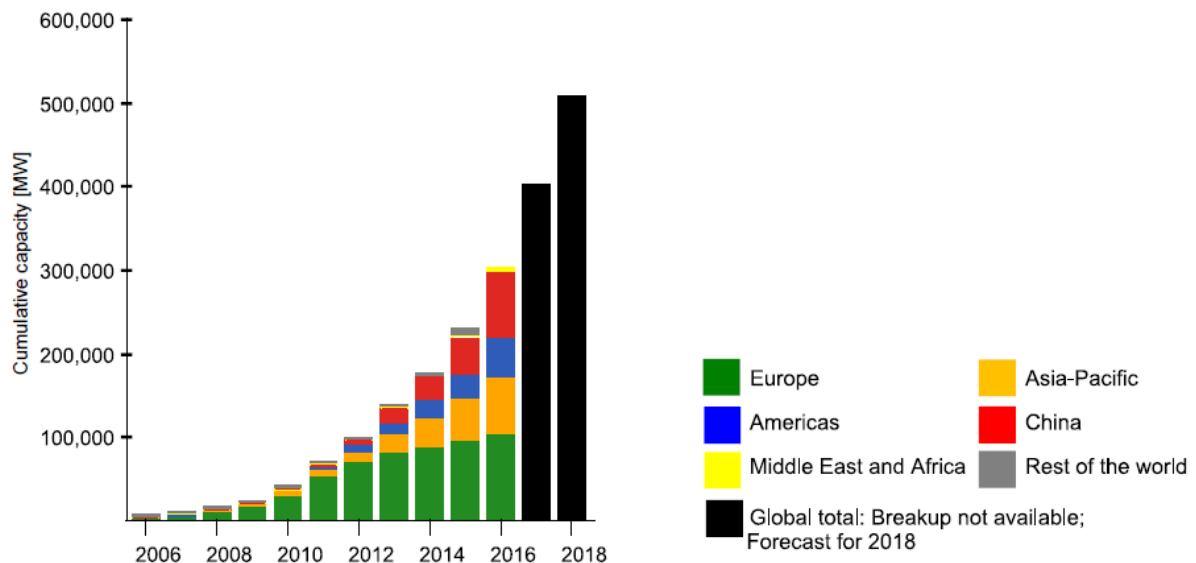


Figure 1.1: Yearly installed solar capacity [5]

A typical configuration of a grid-connected PV system is shown in Figure 1.2. The PV modules generate a DC, which varies according to solar irradiance, temperature, and terminal voltage [4]. The DC generated must be converted and fed into the grid as AC. Additional components used include a grid connection filter, a transformer, and a typical grid angle tracking system, like a phase-locked loop (PLL). An optional DC-DC converter stage is used between the PV modules and also the inverter. A DC/DC converter is often used to decouple the operating point of the PV system from the inverter and provide maximum power point tracking (MPPT) control. Additionally, the DC/DC stage is widely used to increase the PV output voltage [4].

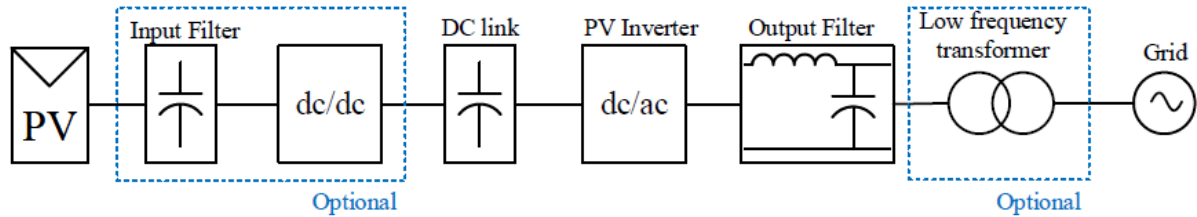


Figure 1.2: A generic structure of a grid-connected PV system [4]

In PV applications, a transformer is often used for galvanic isolation and voltage conversion [3]. However, transformers are quite bulky and so increase the size/weight of the inverter while decreasing efficiency and power density. Because of the large development of grid-connected PV systems, there's an increasing trend to avoid the use of interface transformers and replace them with transformerless inverter topologies. Although transformerless topologies offer better efficiencies, lower weight-to-volume ratio, and thus lower cost, the elimination of the transformer leads to common mode currents or leakage currents due to the parasitic capacitance between the PV panel and its frame [3]. Therefore, additional measures must be taken to eliminate leakage currents and avoid safety hazards. Consequently, grid-connected transformerless PV inverters must meet stringent safety standards [3]. Several research papers have proposed various techniques to mitigate the common mode currents, such as decoupling the dc side from the ac side and/or limiting the common-mode voltage (CMV) during the freewheeling phase or using common ground configurations [3]. Shared-ground PV inverters have attracted much interest from both industry and academia because they will effectively reduce the leakage current of the PV system. Many transformerless common ground inverters have been proposed, e.g., in [6, 7, 8, 9, 10, 11], but they either use more switches or more passive components.

1.2 Motivation

Although Germany features a highly available, high-quality electrical power grid, there's a requirement for grid supporting and regulating generation units or stabilizing grid resources. On the one hand, these systems are used to support a locally weak infrastructure. On the other hand, they're used to build up a grid infrastructure in areas where a corresponding expansion of the present grid infrastructure isn't profitable from an economic point of view. Additionally, these systems are deployed in areas where the grid infrastructure has not yet been expanded, isn't yet maintained, is partially defective, or has been destroyed.

Commonly diesel-based generation units are used today. These units are not energy efficient and also produce CO₂. To be able to offer an efficient, environmentally friendly, and modular alternative with functional expansion, a new type of battery inverter with a high mass power

density is to be researched and demonstrated, which makes it possible to form a highly available and self-sufficient AC network as well as a power supply system.

Regardless of the precise application of a high-performance battery inverter, the associated markets are increasingly developing into a cost-driven environment. While this trend has already been noticeable for a long time for traditional PV systems within the commercial, industrial, and particularly the utility-scale area. This cost pressure necessitates massive reductions in material and weight while at the same time ensuring high functionality.

These technical and economic challenges are to be solved with the aid of advanced circuit topologies supported by innovative SiC MOSFET power modules, magnetic components, and control strategies. The targeted operation at a switching frequency of up to 200 kHz in the power range of 200 kW should cause massive material, weight, and price savings compared to today's conventional inverter solutions. New control strategies are to supply higher performance and provide grid-supporting functions. This can lead to new solutions for this area of application, which don't seem to be yet commercially available within the market.

Power electronic converters are enabling technologies for the control and conversion of electric power by a certain pattern of switching operations applied to semiconductor switches. In grid-connected power electronic systems quality of the current injected into the grid is a priority. Grid forming controls focus on voltage quality as well. The use of grid-connected converters allows independent control of active and reactive power exchanged with the grid. However, grid-connected converters generate harmonics that might be harmful to other devices connected to the same grid. To meet the grid-code requirement of injecting a clean current, with less total harmonic distortion (THD), it is crucial to use a filter (L or LCL filter) between the converter bridge and the grid. Compared to the L filter, the LCL filter, LC+EMI filter provides much higher attenuation of switching harmonics and uses smaller components that reduce the volume and weight while increasing power density [12].

Conventionally, the control of grid-connected inverters is carried out by employing voltage-oriented control (VOC) [13, 14]. VOC uses linear controllers supported by a simple proportional-integral (PI) controller, designed within the synchronous reference frame. Although these controllers are simple and may ensure a moderate quality of the injected grid current, the design of controller gains is often based on the linear model and hence does not include any non-linearity present in the system. Additionally, this controller suffers from the problem of integral windup which necessitates the use of anti-windup methods; hence the dynamic response of this scheme is slow.

Among other approaches, a proportional-resonant (PR) controller [15], a design based on the linear quadratic regulator (LQR) presents in [16]. The PR controllers are widely used for the control of grid-connected inverters because of their property to introduce infinite gain at selected frequencies, thereby mitigating the resonant behavior of LCL filters. In [17, 18, 19] a pole-placement-based control strategy has been proposed that has inherent resonance damping and doesn't require any additional damping solutions. While [17] deals with the control design in continuous-time, [18, 19] have proposed a controller in the discrete-time domain. Since pole placement is usually not supported by a systematic design procedure, [16] presents a controller design based on the linear quadratic regulator (LQR), where a cost function is minimized to place the poles optimally.

Motivated by the increasing trend in the use of transformerless topologies for grid-connected inverters, the main target of this thesis is deriving the state-space model of the output filter,

design, and implementation of various control strategies for a 3-phase, 3-level ANPC with an LC+EMI output filter.

1.3 Thesis objectives

This thesis aims to model the state-space representation of LC+EMI filter operation in differential mode operation, investigate and implement a PI control strategy with different tuning methods to tune a PI controller that assures stable grid operation as well as a balanced current distribution between two interleaved output stages. This thesis aims to fulfill the following objectives:

- Derive the state-space model of the output filter in differential mode operation.
- Implement a PI control strategy with different tuning methods to tune a PI controller for differential mode operation.
- Investigation of stability of the system with varying grid impedance.
- Investigation of stability of the system with varying system parameters.
- Implementation of current control for 3P, 3L 4 wire ANPC inverter.
- Implementation of current control for parallel interleaved 3P, 3L ANPC with the balancing of multiple parallel-connected phase legs.

1.4 Thesis organization

The upcoming chapters of this thesis are organized as follows:

Chapter 2 presents a theoretical background of this thesis topic. Introduction to power converters and the 3-phase, 3-legs, 4 wire ANPCs operation. A quick review of common mode and differential mode, EMI filters. Effect of grid impedance on the system. Introduction to control schemes.

Chapter 3 presents the implementation of the symmetrical optimum and root locus tuning methods to find PI control parameters. Investigation of system stability with varying grid impedance of the system with two PI parameters. Investigation of system stability with varying system parameters.

Chapter 4 presents the comparison of the two tuning methods with the performance specifications of the system. Verification of state-space model with a single-phase Simulink model. Investigation of the first-order filter with two different cut-off frequencies 35 kHz and 6 kHz of the system with the third-order measurement filter (voltage).

Chapter 5 presents the simulation of power electronic converters with averaged model and switched model. Current control of 3L ANPC inverter with dq control and the results. Current control of parallel interleaved 3L ANPC inverter with the distribution of the total current and balancing of multiple parallel-connected phase legs.

2 Theoretical Background

This chapter covers all of the necessary foundations for this thesis. Three-level inverter as an alternative to the conventional two-level voltage source inverter (VSI). Differential and common mode operation operating principles. The EMI filter and grid impedance are briefly discussed. An overview of different control techniques and state feedback. The state-space representation and Monte Carlo simulation objectives.

2.1 Power Electronics Converters

A switching converter is an important component of power electronics. According to the sort of power conversion accomplished, power electronic converters can be classified into four groups [20]. A DC-DC converter processes a DC input voltage of a certain amplitude to produce an output voltage of lesser or greater amplitude. An AC-DC converter, commonly known as a rectifier, converts an AC input voltage to a DC output voltage. The current waveform input and the amplitude of the DC output can both be modified. A DC-AC converter or inverter adjusts the output current amplitude and frequency to conduct the inverse conversion. Controlling an input voltage to a specified magnitude and frequency at the output is the goal of AC-AC cycle conversion [21]. Real devices are typically constructed by combining a few fundamental switching converter kinds. A three-phase frequency inverter for motor control, for example, is made up of AC-DC and DC-AC converters as shown in Figure 2.1.

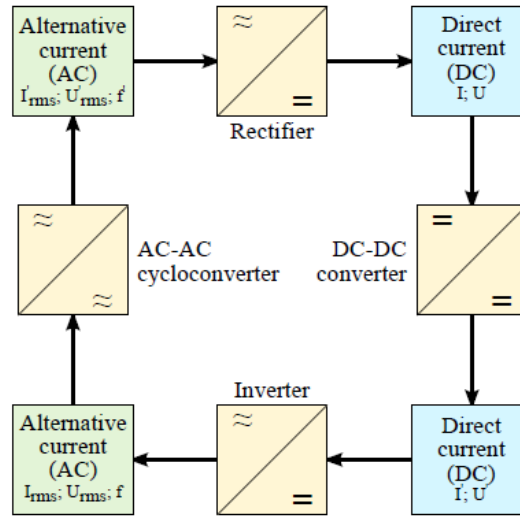


Figure 2.1: Classification of power converters

Semiconductor devices are at the heart of all power electronic converters [22]. Power semiconductors are typically used in an on-off or switching mode (in contrast to signal processing). A power semiconductor should, in ideal power, have zero current in the off-state and zero voltage drop in the on-state. Vertically structured power semiconductors include the insulated gate bipolar transistor (IGBT) and the metal-oxide-semiconductor field-effect transistor (MOSFET). The advancement of semiconductors is driving the development of power electronics applications. Nonetheless, passive components, particularly power magnetics, are critical in power electronics systems and can account for up to 80% of the volume of a power electronic system. Higher switching frequencies of semiconductors allow for the reduction of passive component size and, as a result, an increase in power density, but they also cause more disturbances in the higher frequency range.

2.1.1 Multilevel Inverter

Multilevel inverters (MLIs) have recently emerged as the most powerful power transformation technology for a variety of applications, including renewable energy resources (RERs), flexible AC transmission systems (FACTS), and electric motor drives, among others. MLI has gained appeal in medium- to high-power operations due to several advantages, including low harmonic content, lower power consumption from power electronic switches, and lower EMI at the receiving end. In comparison to a traditional two-level inverter, the MLI offers many important benefits, including voltage profile enhancement, increased overall system efficiency, the ability to generate high-quality output with a lower switching frequency, lower total harmonic distortions (THD) without reducing inverter power, and the use of very low device ratings.

Properties	Two-Level Inverter	MLI
Structure	Complicated	Modular
Operating at high voltage and current	Can operate (for parallelized structures)	Can operate
Stress on power electronic switches	More	Less
Application	Low voltage	High voltage
Power quality performance	Low	High
Harmonic content	Low	High
Electromagnetic interference (EMI)	Less	More
Immunity/susceptibility	Less	More
Production of common-mode voltage	Higher	Lower
The ability of transformer-less operation	No	Yes
Efficiency	Low	High
Switching losses	High	Low
Operation at the fundamental frequency	Fails	Can operate
Input current distortions	High	Low
Fault-tolerant operation	Impossible	Possible
Rate of change of voltage	High	Low
Production of multiple voltage level	Not possible	Possible
Electromagnetic interference generation	High	Low

Table 2.1: Comparison between traditional two-level inverter and MLI [23]

2.1.2 3-Phase, 3-Level ANPC:

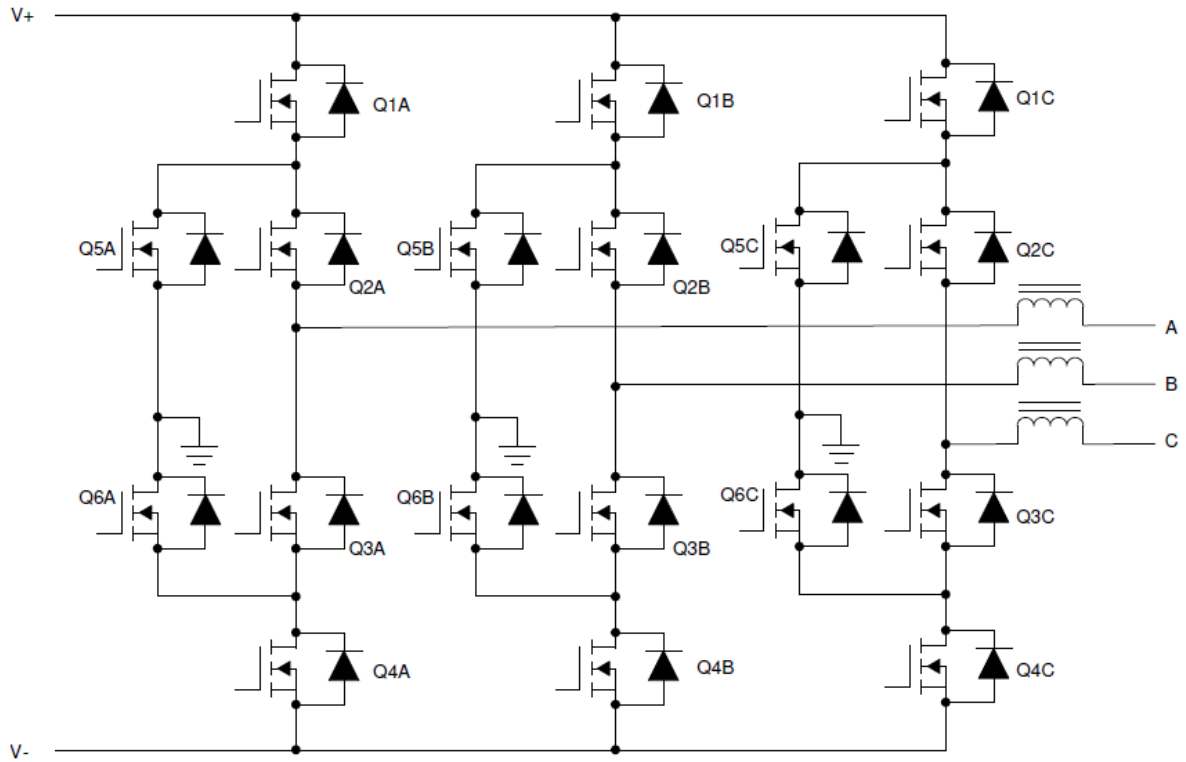


Figure 2.2: Three-phase 3L ANPC inverter topology

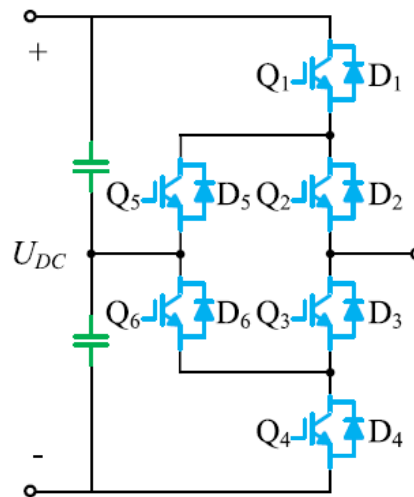


Figure 2.3: A single-phase leg of the ANPC converter with SiC MOSFETs

Figure 2.3 depicts a single-phase circuit, there are six active switches. Q2 and Q3 use SiC MOSFETs, whereas the rest make use of Si-IGBTs. Except for the addition of SiC and Si devices, the circuit layout is identical to that of a conventional Si-based ANPC converter.

Furthermore, because SiC MOSFETs have lower switching losses than IGBTs, overall switching losses can be greatly reduced. Balance of losses (push them on the MOSFETs), the IGBT should feature lower losses when conducting, the drawback is less flexible in PWM

patterns. Also, this particular structure is cheaper. The ANPC converter will have substantially higher efficiency and switching frequency as a result of these changes.

The gating signals for Si device pairings Q1 Q6 and Q5 Q4 are always the same. Furthermore, these two Si device pairs switch in a complementary manner. SiC MOSFET Q2 and Q3 on the other hand, are complementary pairs. Only one "0" level state is employed in each half cycle of the modulation wave. Only the "O+" state is employed in the positive cycle, while the "O-" state is used only in the negative cycle. Q1 and Q6 are always in the ON state during the positive half cycle, according to these selected switching patterns. The only two complementarily switching devices are Q2 and Q3.

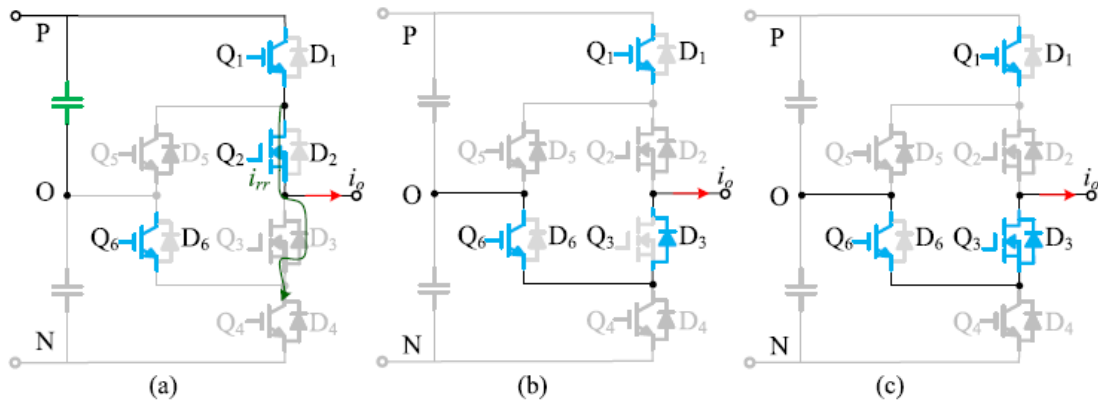


Figure 2.4: Demonstration of commutation under the inverter mode. (a) Equivalent circuit of state "P". (b) Equivalent circuit during the deadtime. (c) Equivalent circuit of state "O+"

The main current will flow via Q1 and Q2 when the circuit outputs the state "P," as indicated in Fig. 2. 4. (a). As seen in Fig. 2.4(b), shutting off Q2 causes the main current to commute to Q6 and D3 (b). When Q3 is turned on, it will work in the synchronous rectifier mode, as shown in Fig. 2.4. (c). Changing from state "P" to the deadtime state in this mode will result in Q2 turn-off loss. The changing from the deadtime state to state "P" will create turn-on loss in Q2 and reverse recovery loss on D3.

According to the results of the above analysis, switching losses on SiC MOSFETs Q2 and Q3 or their body diodes D2 and D3 are only caused by commutation between the "P" and "O+" states. As a result, employing these two SiC MOSFETs can greatly reduce switching losses. Similarly, Q4 and Q5 are always in the ON state during the negative half cycle. The only two complementarily switching devices are Q2 and Q3. By implementing the proposed strategy, all switching events are shifted to the two SiC MOSFETs. As a result, when compared to all-SiC MOSFET-based ANPC converters, the proposed hybrid ANPC converter may attain the same switching loss performance. But due to the forward voltage drop of bipolar devices the light load conduction losses should be higher.

Switch state	Voltage level	Q1	Q2	Q3	Q4	Q5	Q6
N	1	0	0	1	1	1	0
O-	0	0	1	0	1	1	0
O+	0	1	0	1	0	0	1
P	-1	1	1	0	0	0	1

Table 2.2 Switching states of 3L ANPC

2.2 Common mode and Differential mode

For conductive EMI investigations, the division of interferences into two types based on formation nature is commonly used. Symmetric or differential mode (DM) and asymmetrical or common-mode (CM) interferences are both possible [24, 25]. The mechanisms by which various interference kinds emerge differ greatly. Currents flowing in the same direction in all conductors and a return path passing via the ground generate common-mode EMI (2.2.1). According to (2.2.2), differential mode interferences are caused by current flowing in opposing directions in phase wires.

$$i_{cm} = i_a + i_b + i_c + i_N \quad (2.2.1)$$

$$i_{a,dm} = i_a - i_{cm} = (i_b + i_c + i_N) - 2i_{cm} \quad (2.2.2)$$

A three-phase power electronics setup is used to demonstrate common and differential currents in Figure 2.5. When a power electronics converter switches, both DM and CM interferences are produced, which are represented by voltage sources V_{DM} and V_{CM} . Common mode currents are illustrated with red arrows, while differential mode currents are indicated with blue arrows. It is clear from this analogous circuit that phase current measurements are the total of DM and CM currents.

The line choke and DC-link capacitor of Ampere Interrupting Capacity (AIC) [26, 27] partially absorb DM currents since their path is identical to that of phase currents. Meanwhile, the fundamental components of AIC do not affect a CM path; it is only influenced by the additional EMI filter impedance introduced in this way. As a result, the majority of research [28, 29, 30] concentrates on the prediction and analysis of CM current pathways. At least one stray capacitor in the entire drive system must participate in the CM current channel to produce a closed-loop for the CM current flow.

To eliminate EMI produced by AIC, EMI filters can be put between the power grid and the power electronics converter. A low impedance CM current channel is produced by routing CM current through filter capacitors to the ground. It prevents disruptions caused by a PE converter from being transmitted to the electrical grid. Choke functions as an EMI filter's supplementary Y-capacitor. The power electronic converter (PEC) is decoupled from the grid by an EMI filter, but the load is still influenced by produced EMI. Surely, to eliminate EMI on the motor side, some additional filtering components (common mode chokes or EMI filters) can be included.

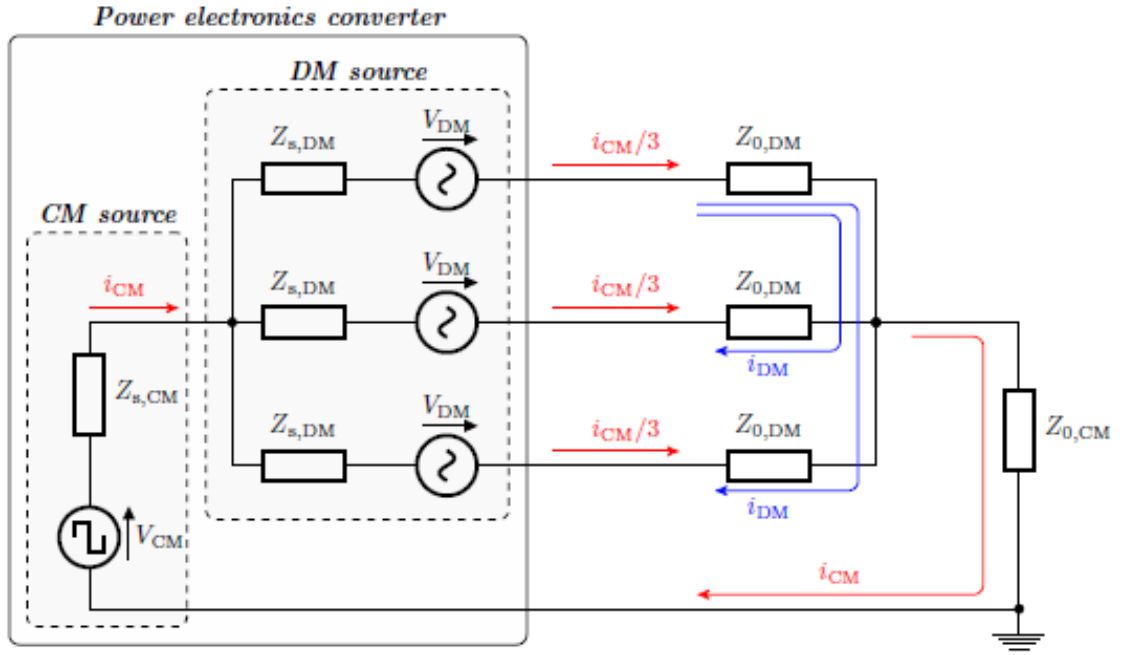


Figure 2.5: Common and differential mode interferences in a three-phase system

2.3 EMI filter

The primary goal of EMI filters is to improve the level of electromagnetic emission produced by a PE system. In this case, the phrase "electromagnetic compatibility (EMC) filters" can be used instead [31]. When used in conjunction with a power electronic converter, a more dependable system with improved electromagnetic compatibility and susceptibility is created. Motors, electronic controls, power supplies, inverters, clock circuits, microprocessors, appliances, electronic gadgets, and other electrical and electronic devices all produce a high-frequency noise. This noise is often in the 9KHz to 10GHz frequency range, and it can damage or limit signal transmissions and/or electrical/electronic equipment's intended functionality. The EM noise's lower frequency components can also affect power quality.

However, unlike the use of EMI filters, these procedures do not guarantee that the created electromagnetic interferences will be reduced to an acceptable level, particularly in the MHz range. As a result, in the vast majority of real applications, EMI filters remain the most trustworthy solution [32]. EMI filter design tasks are typically fairly complicated, requiring knowledge of two fields: electromagnetic compatibility and power electronics as shown in Figure 2.6. The production of faulty mathematical models is caused by a lack of skill in any of these two domains. It causes numerous issues during prototyping since the dampening of EMI filters predicted in simulations differs from reality.

As a result, precise behavioral models reflecting all significant aspects impacting EMI filter properties must be established. Furthermore, the load and source impedances have a significant impact on the Insertion loss (IL) of EMI filters. In an ideal world, a specific EMI filter would be investigated alongside a PE converter under realistic operating conditions. An EMI filter constructed independently of a PE system can have even worse IL than the theoretical worst-case scenario indicated [33, 34].

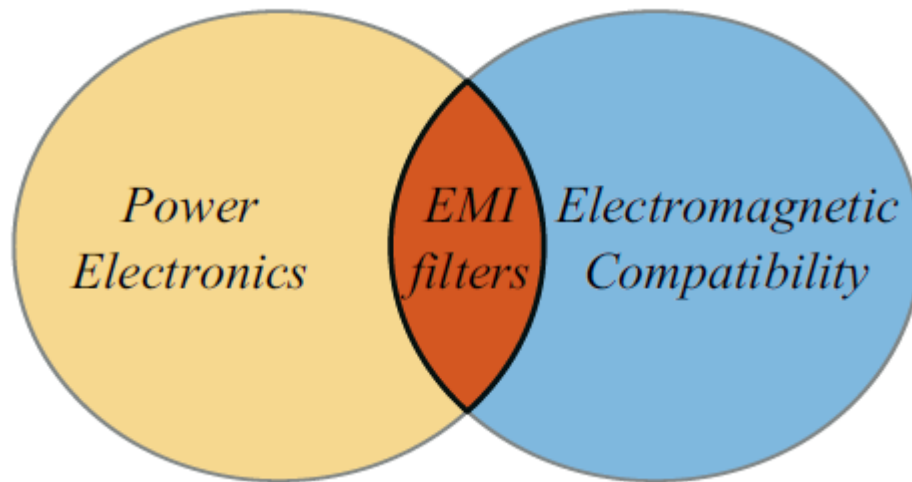


Figure 2.6: Interdisciplinary allocation of EMI filters

The separation of interference types into common and differential classes is a standard EMI filter analysis [35, 36]. Different noise propagation channels are individually analyzed in this technique, and the associated stages of an EMI filter are developed following the interference types that they are meant to handle [26].

Common mode and differential mode Insertion loss (IL) exhibited by the single EMI filter installed in the power electronic converter systems are not equal and should be adjusted separately according to CM and DM disturbance levels. Therefore, different filter topologies, as well as component values, have to be used for DM and CM damping. Typically for a power electronic converter CM impedance on the converter side is bigger than CM impedance on the grid side. For this particular case, an LC configuration of a CM filter is suitable. DM signals see a PEC as a capacitive load (DC-link capacitor in series with semiconductors) exhibiting low impedance. Hence DM filters should have a C L configuration. Since a single EMI filter must provide attenuation of both CM and DM disturbance, components responsible for attenuation of both disturbance types have to be included in the device. Figure 2.7 shows the topology of the conventional industrial three-phase EMI filter [37], where L1 is a three-phase common mode choke. As seen from the name CMC is responsible for the CM interference attenuation. The windings of the CMC are coupled so that fluxes generated by DM currents are canceled inside of the choke core and do not see its impedance while CM currents see the whole impedance of the CMC. Typical values of the CMC inductance are 1mH – 10mH. Characteristics of a CMC directly depend on the utilized core material.

Y-capacitor refers to the CY1 capacitor. By definition, this type of capacitor is connected between conductive components and the ground. It is positioned between the start point and the ground in this scenario. This is a common configuration for three-phase EMI filters. The capacitor CY1 is connected in series with the capacitors CXY1, CXY2, and CXY3 in CM noise. A Y-capacitor does not affect DM interferences in this form of connection (it is true for ideally balanced phases). The maximum leakage current limits the values of Y-capacitors, which normally do not exceed 3 μ F. X-capacitors include capacitors CXY1, CXY2, CXY3, CX1, CX2, and CX3. CXY functions as both X and Y capacitors. Because of safety concerns, the values of these capacitors are not limited (there is the effect on leakage current). Alternatively, X-capacitors can be used to connect phases directly. The nominal voltage of capacitors must be increased in this circumstance. X-capacitors, on the other hand, may alter a power electronic converter's transfer function and cause resonance effects with grid inductance or other power

electronic devices connected to the same grid. These capacitors typically have values ranging from $1\mu\text{F}$ up to $10\mu\text{F}$. They introduce additional resonant frequencies. The Insertion loss (IL) of the filter is unaffected by resistors R_1 , R_2 , R_3 , and R_4 . When the voltage is removed, they discharge the filter capacitors.

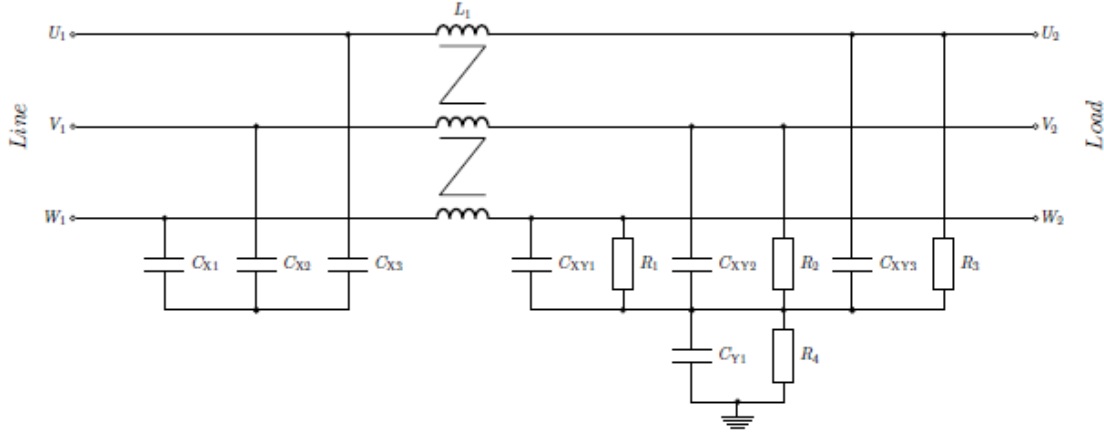


Figure 2.7: Topology of a typical three-phase EMI filter

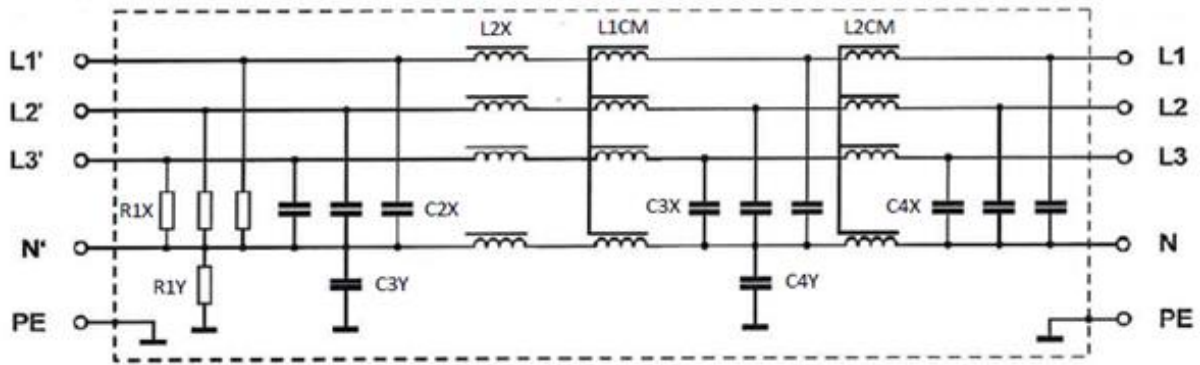


Figure 2.8: EMI topology used for this thesis

Figure 2.8 depicts the topology of an EMI filter that is used in this thesis.

2.4 Grid impedance

The growing number of photovoltaic and wind power installations has resulted in a grid configuration in which many inverters are connected in parallel to a point of common coupling (PCC). Inappropriate behavior or even instability might occur from this connection [38, 39]. Furthermore, the connected distributed energy systems must meet the requirements imposed by the grid operators.

The grid impedance couples parallel functioning inverters of distributed energy resources. The grid impedance affects the inverter's performance. Grid impedance can change quickly if a transmission line fails or is disconnected. It's also known to make current control slower. Grid-connected inverters have been proven to become unstable due to fast grid synchronization when grid impedance is high. Control or filter design can be used to eliminate harmonics [40]. Grid impedance connected at the inverter's output terminals resembles a resistive-inductive circuit in most scenarios.

In this thesis, the grid resistance (R_g) is considered as $300\text{ m}\Omega$ and grid inductance (L_g) as $150\text{ }\mu\text{H}$. In Chapter 3, the selection of grid impedance values is investigated. The grid resistance and grid inductance values are chosen from [71]. In this paper, grid impedance varies on conditions for example grid condition in Laboratory, Emulated grid condition 1, and emulated grid condition 2. The value of grid impedance in laboratory conditions is $R_g = 325\text{ m}\Omega$, and $L_g = 150\text{ }\mu\text{H}$. In this thesis, the grid inductance value is varied in the range of $100\text{ }\mu\text{H}$ to $500\text{ }\mu\text{H}$ to observe the stability of the system by increasing the value in a big range.

2.5 Control schemes

The control techniques employed in grid-connected power electronic systems are classified in Figure 2.9. As can be seen, converter control can be divided into two categories: conventional and advanced strategies.

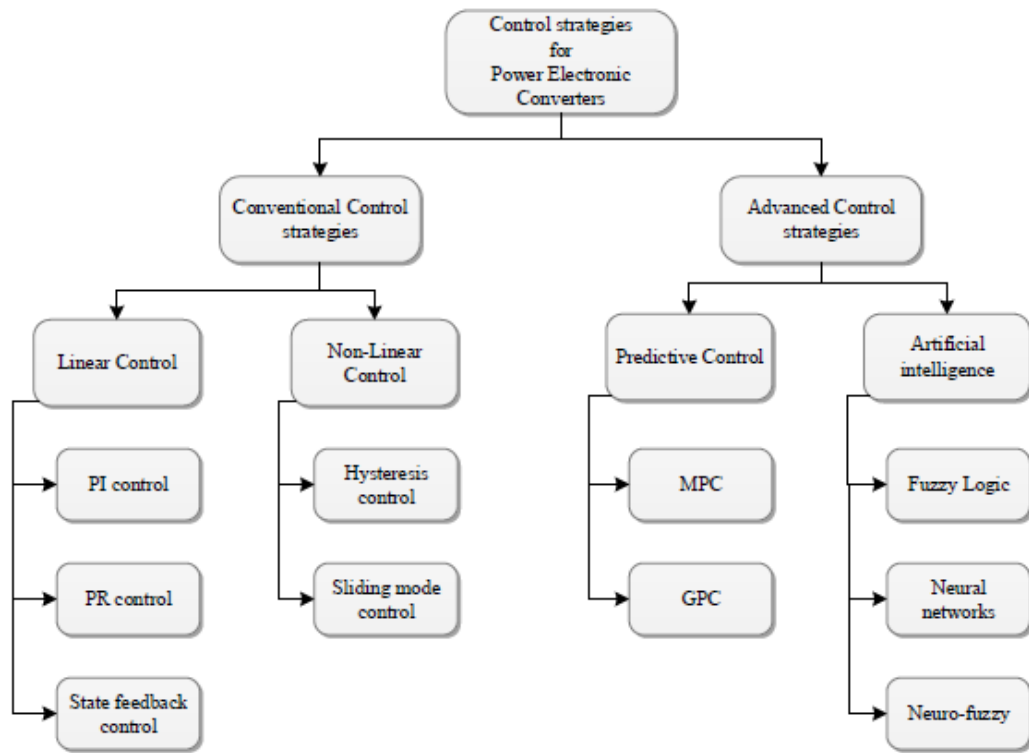


Figure 2.9: Control methods for grid-connected converters [41]

PI-based Voltage Oriented Control (VOC) is a popular linear control technique because it is simple to implement and provides good steady-state performance. For small-time instants, the power converter's non-linear behavior is approximated as linear, and a modulator can be used to generate Pulse Width Modulation (PWM) [42]. A PWM modulator generates a pulsed waveform for switching devices by comparing a sinusoidal reference signal to a triangular carrier signal. In this way, the inverter can switch between different states and generate different voltages.

The VOC is not chosen in practical systems because of its sluggish dynamic performance. State feedback control (SFC), on the other hand, has received a lot of attention and has a lot of applications in grid-connected systems [19, 43, 44, 45]. It outperforms PI control in terms of dynamic performance and steady-state performance. However, using linear techniques to

regulate non-linear systems has the disadvantage of producing unequal performance across the dynamic range. The numerous system limits and needs (such as maximum current and switching frequency or total harmonic distortion) cannot be readily accommodated with linear controller design [42].

Nonlinear approaches have many advantages over linear techniques. In particular, Model Predictive Control is a technique that can control multiple conflicting objectives and allows to incorporate of system constraints as well. With predictive control, the cascaded structure, found in linear schemes, can be avoided to produce very fast transient responses [42].

2.6 State feedback control

Grid-connected converters provide unidirectional or bidirectional power transfer with minimal current distortion. Grid regulations impose strict constraints on the present THD of the grid, which is separated into two portions. The first problem is caused by grid voltage background distortion, which causes low-frequency harmonics. This is linked to the existing controller's disturbance rejection capacity [19]. Harmonic rejection requires a large control bandwidth. The second source of grid current harmonic distortion is harmonics at the converter's switching frequency. Because of its excellent filtering feature above their resonant frequency, LC+EMI filters are increasingly being utilized to mitigate switching harmonics [19].

Active damping is frequently preferred over passive damping for damping the resonant behavior of the LC+EMI filter because it is more flexible and efficient. However, as the LC+EMI resonance dynamics approach the desired control bandwidth, achieving resonance damping and high bandwidth with adequate robustness becomes more difficult [44]. State Feedback Control (SFC) [19, 43, 44, 45]. allows a converter connected to the grid via an LC+EMI filter to have a high dynamic performance. The dominant and resonant dynamics can be controlled simultaneously according to desired specifications with SFC, making resonance damping simple [43].

The closed-loop poles in -State Feedback Control can be positioned in many different ways: 1) PI control, 2) dead-beat control; 3) Bessel Functions; 4) cost function optimization as in linear-quadratic (LQ) control; 5) direct selection of preferred pole sites [43]. Because it provides an indirect way for optimal pole placement, LQ control is extremely appealing for the design of a controller when working with very complicated systems. The solution of the Riccati equation and the determination of the cost-function weights, on the other hand, is a time-consuming operation [21]. Direct pole placement (see [43, 44]) is a simpler alternative to LQ control in which the controller gains are defined using system parameters and dynamic performance specifications [43].

Pole placement is a technique for describing closed-loop performance in terms of the pole and zero locations. The control parameters can be adjusted to get the desired results. Despite the ease of parameter calculation, correct specification of closed-loop poles and zeros is required [18].

One drawback is that not always all states can or will be observed, this might interfere with controllability and observability, one might need to add an observer to estimate states.

2.7 State-space system

The dynamics of a linear time-invariant (LTI) system can be represented using ordinary differential equations (ODE). A general LTI system in state space can be written as

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \quad (2.7.1a)$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \quad (2.7.1b)$$

For the given LTI system, the state vector $\mathbf{x} \in \mathbb{R}^n$ has dimension n , the input vector $\mathbf{u} \in \mathbb{R}^p$ has dimension p and the output vector $\mathbf{y} \in \mathbb{R}^q$ has dimension q . Therefore, the state-space matrices have dimensions: $\mathbf{A} \in \mathbb{R}^{n \times n}$, $\mathbf{B} \in \mathbb{R}^{n \times p}$, $\mathbf{C} \in \mathbb{R}^{q \times n}$ and $\mathbf{D} \in \mathbb{R}^{q \times p}$. This set of equations including the dimensions of vectors and matrices is drawn in the following block diagram [46].

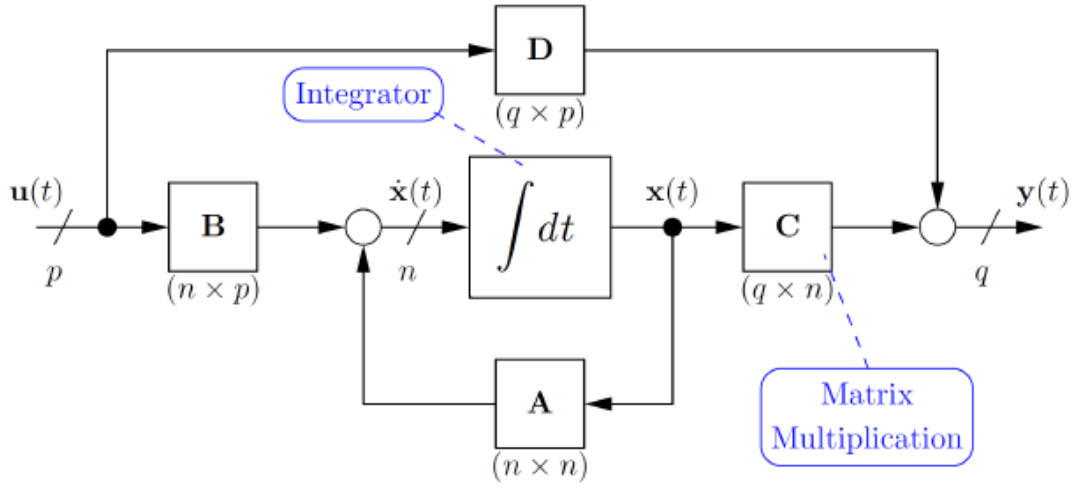


Figure 2.10: State feedback of the system

Let us consider the complete response of a linear system of first-order to an input $u(t)$. The state equation $\dot{\mathbf{x}} = \mathbf{a}\mathbf{x} + \mathbf{b}u$ can be written in the form

$$\dot{\mathbf{x}}(t) - \mathbf{a}\mathbf{x}(t) = \mathbf{b}u(t) \quad (2.7.2)$$

If both sides are multiplied by an exponential time function e^{-at} , the left-hand side becomes a perfect differential

$$e^{-at} \dot{\mathbf{x}} - e^{-at} \mathbf{a}\mathbf{x} = \frac{d}{dt} (e^{-at} \mathbf{x}(t)) = e^{-at} \mathbf{b}u \quad (2.7.3)$$

Which can be integrated directly to give

$$\int_0^t \frac{d}{d\tau} (e^{-a\tau} \mathbf{x}(\tau)) d\tau = e^{-at} \mathbf{x}(t) - \mathbf{x}(0) = \int_0^t e^{-a\tau} \mathbf{b}u(\tau) d\tau \quad (2.7.4)$$

and rearranged to give the state variable response explicitly:

$$\mathbf{x}(t) = e^{at}\mathbf{x}(0) + \int_0^t e^{-a(t-\tau)} bu(\tau) d\tau \quad (2.7.5)$$

The development of the expression for the response of higher-order systems may be performed in a similar manner using the matrix exponential e^{-At} as an integrating factor [47]. Matrix differentiation and integration are defined to be element operations, therefore if the state equation $\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t)$ is rearranged, and all terms are pre-multiplied by the same matrix e^{-At} , we get:

$$e^{-At}\dot{\mathbf{x}}(t) - e^{-At}\mathbf{A}\mathbf{x}(t) = \frac{d}{dt} \left(e^{-At}\mathbf{x}(t) \right) = e^{-At}\mathbf{B}\mathbf{u}(t) \quad (2.7.6)$$

Integration of (2.7.6) gives

$$\int_0^t \frac{d}{d\tau} \left(e^{-A\tau}\mathbf{x}(\tau) \right) d\tau = e^{-At}\mathbf{x}(t) - e^{-A0}\mathbf{x}(0) = \int_0^t e^{-A\tau}\mathbf{B}\mathbf{u}(\tau) d\tau, \quad (2.7.7)$$

and because $e^{-A0} = \mathbf{I}$ and $[e^{-At}]^{-1} = e^{At}$ the complete state space response may be written as

$$\mathbf{x}(t) = e^{-At}\mathbf{x}(0) + \int_0^t e^{-A(t-\tau)}\mathbf{B}\mathbf{u}(\tau) d\tau \quad (2.7.8)$$

To design a controller for the LTI system, linearization of the ODE is carried out to consider the behavior of the system around a reference or steady-state point. Additionally, the controllability of the system has to be checked to verify that a controller can be designed.

2.7.1 Kirchhoff's Current (KCL) and Voltage (VCL) Law

The equivalent resistance of a complex network and flowing currents in different conductors. Both AC and DC circuits can be solved and simplified by using these simple laws which are known as Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL).

In any electrical network, the algebraic sum of incoming currents to a point and outgoing currents from that point is Zero. Or the entering currents to a point are equal to the leaving currents of that point.

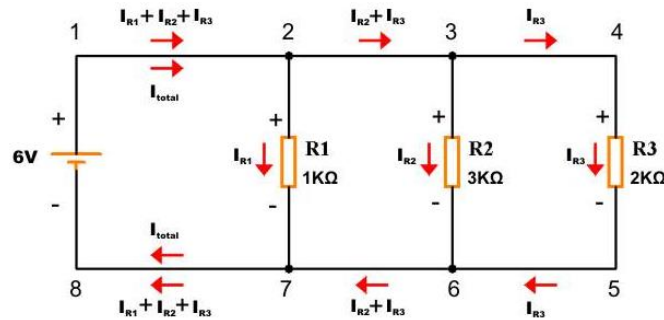


Figure 2.11: Demonstrating Kirchhoff's Current Law (KCL)

$$I_{\text{existing}} = I_{\text{entering}}$$

$$I_{\text{entering}} + (-I_{\text{existing}}) = 0$$

Kirchhoff's Voltage Law (KVL)

In any closed-loop network, the total voltage around the loop is equal to the sum of all the voltage drops within the same loop which is also equal to zero.

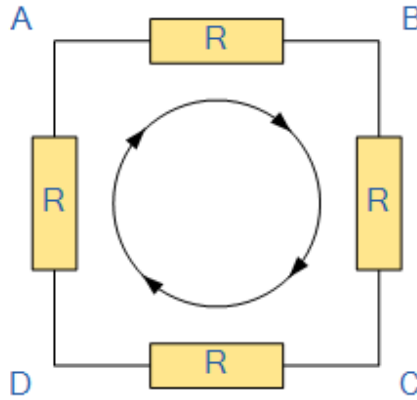


Figure 2.12: Demonstration of Kirchhoff's Voltage Law (KVL)

The sum of all the voltage drops around the loop is equal to zero.

$$V_{AB} + V_{BC} + V_{CD} + V_{DA} = 0$$

2.7.2 State feedback

Once it is determined that the system is controllable, assuming $D = 0$, feedback can be added to the system as shown below,

The State feedback controller is defined by

$$u(t) = -Kx(t) \quad (2.7.9)$$

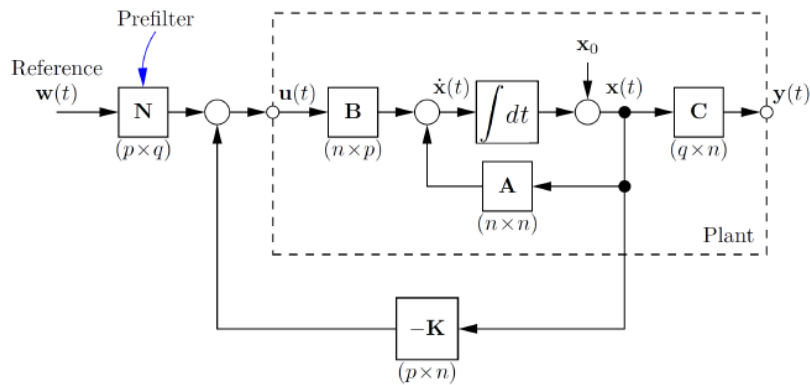


Figure 2.13: State feedback controller

Substituting (2.7.9) into the state ODE $\dot{x}(t) = Ax(t) + Bu(t)$ yields the feedback system

$$\dot{x}(t) = (A - BK)x(t) \quad (2.7.10)$$

The control design has two objectives:

- Design **K** such that the state space control loop is stable.
(**A - BK**) is stable, i.e., all its eigenvalues have negative real parts.
- Design a prefilter **N** such that for a reference input ω , the output vector $y(t) \rightarrow \omega$, for $t \rightarrow \infty$.
The control law becomes $u(t) = -Kx(t) + N\omega$

2.8 Monte-Carlo simulation

Computer simulations now account for a large portion of the research. Probabilistic simulation methods can be used to investigate the impact of random variability on machine attributes, chemical or biological processes, a structure's load-carrying capacity or reliability, and many other applications. The Monte Carlo technique is a strong tool for studying random occurrences or processes.

Monte Carlo simulation method

The Monte Carlo method [48, 49] is a simple computer methodology that involves doing a series of simulated experiments with random numbers. Its application is ubiquitous and requires no prior understanding of probability theory. Only the relationship between the output and input quantities,

$$y = f(x), \text{ or } y = f(x_1, x_2, x_3, \dots) \quad (2.8.1)$$

as well as knowledge of the probability distributions of the input variables, are required. The method repeats trials using computer-generated random numbers that have been subjected to the appropriate mathematical processes. The input variables $x_1, x_2, \dots, x_n$ are given random values in each "trial," but their distributions match the probability distribution of each variable. Equation (2.8.1) is used to calculate the output quantity y using these data.

The generated values can be used to calculate the average value, the likelihood that y will be lower or greater than a given value y^* , or the values that will be exceeded (or not achieved) with a certain probability (e.g., the time to failure, maximum expectable load or deformation).

Monte Carlo simulations can be performed using a variety of commercial computer programs, but they can also be constructed from scratch. A random number generator is the foundation of such programs. These numbers were generated using an appropriate algorithm rather than being truly random. These generators work on a basic premise. The so-called congruential generator, for example, generates random integers with uniform distribution in the interval (0; 1) as shown below. For the sequence of random numbers u , one number is chosen as the base (e.g., $u_0 = 0.5284163$). This number is now multiplied by some suitable number Q , such as 997, in the first step. $997 * 0.5284163 = 526.8310511$ is the product. The first random number, u_1 , is then generated as part of the result, just after the decimal point; in our case, $u_1 = 0.8310511$. In the

second phase, u_1 is multiplied by the same number Q , $997 \times 0.8310511 = 828.5579467$, and the second random number ($u_2 = 0.5579467$) is generated as the decimal component of the result. The reader is advised to make additional pauses in this manner; $u_3 = 0.2728599$ is a good check. The distribution of a lengthy series of these numbers is roughly uniform. There are many additional techniques; one for normal distribution, for example, is based on the central limit theorem. Random number generators are also included in universal computer applications like Matlab. Commercial generators are strongly recommended because they have undergone extensive statistical testing to demonstrate that they act almost as randomly as true randomness. Excel, too, includes a generator, albeit with restricted capabilities.

Conclusion:

Extreme values are chosen for simulation in this example, based on temporal complexity. For speedy simulations, +20 % and -20 % variations are evaluated for the inductor and capacitor, respectively, and the results are compared to the nominal values. The stability of the system is analyzed with varying parameters of the system.

3 Differential mode modeling and control

3.1 LC+EMI filter resonance damping

The LC+EMI filter's resonant behavior must be suitably dampened using either passive damping components or an active damping method. If the resonant frequency is not appropriately damped, an LCL+EMI filter may degrade the system's performance due to increased grid current distortion [50].

3.1.1 Passive Damping

Passive damping is performed by connecting resistance to the filter's capacitance C_1 , C_2 , and C_3 or inductance L_1 , L_2 , and L_3 in series or parallel. Figure 3.1 depicts two possible solutions in which a series resistance is applied.

Adding a series resistance for the inductor R_{L1} , R_{L2} , and R_{L3} and adding series resistance in series with the filter capacitor R_{C1} , R_{C2} , and R_{C3} , aren't damping resistances but approximations of our series resistances due to in-perfect components give good damping with fewer losses.

3.1.2 Active Damping

Although passive damping is a simple approach, it reduces the efficiency of the system. Other resonance damping methods include 1) the virtual resistance method, 2) the use of a lag-lead compensator, and 3) the use of a Notch-filter. Because it provides a workaround for the resistance damping approach, the virtual resistance method has been widely employed in the literature [51, 52, 53]. Instead of employing an actual resistor, the controller emulates the behavior of the resistance using feedback signals and proportional terms. When appropriately tuned, the virtual resistance approach performs similarly to passive damping without incurring additional power losses.

3.2 Differential mode topology

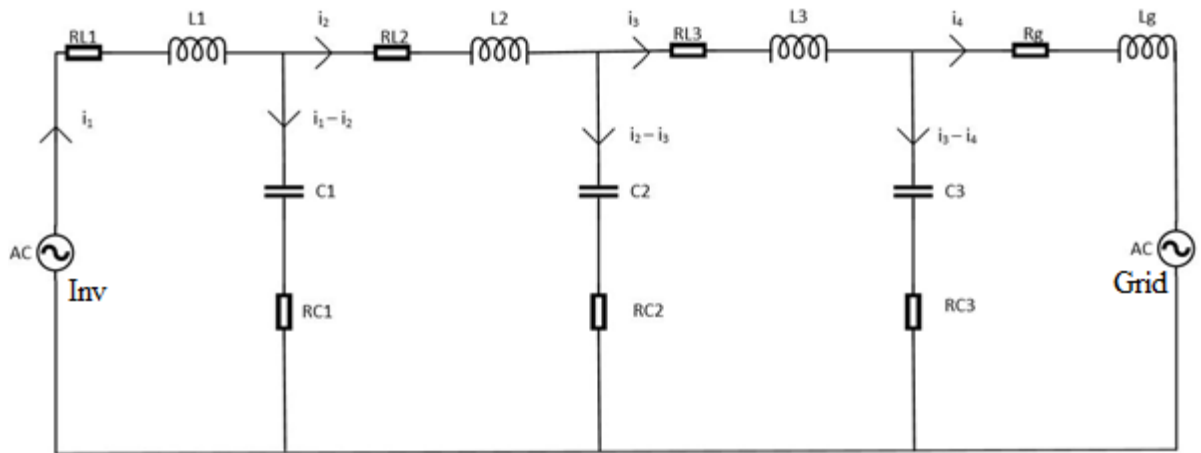


Figure 3.1: LC+EMI filter differential mode

3.2.1 System Parameters

Parameter	Symbol	Value
Series resistance with L1	R_{L1}	1 m Ω
Inductance 1	L1	32.5 μH
Capacitance 1	C1	64.7 μF
Series resistance with C1	R_{C1}	10 m Ω
Series resistance with L2	R_{L2}	0.6 m Ω
Inductance 2	L2	26.8 μH
Capacitance 2	C2	4.7 μF
Series resistance with C2	R_{C2}	5 m Ω
Series resistance with L3	R_{L3}	0.1 m Ω
Inductance 3	L3	6.3 μH
Capacitance 3	C3	4.7 μF
Series resistance with C3	R_{C3}	0.1 m Ω

Table 3.1: System parameters

Parameter	Symbol	Value
Switching frequency	f_{sw}	70 kHz
Sampling time	T_a	1/70000
Nominal grid voltage	u_g	230 V(RMS)
Current filter cut-off frequency	Fil_IL1_c1	35 kHz
Voltage filter cut-off frequency	Fil_UC3_v1	6 kHz
Grid Resistance	R_g	300 m Ω
Grid Inductance	L_g	150 μH

Table 3.2: Additional parameters for simulation

3.2.2 State-space modeling of the LC + EMI filter

3.2.2.1 Deriving the state-space equations

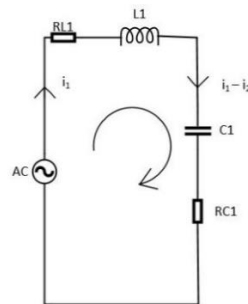


Figure 3.2: First loop

Applying KVL and KCL for loop 1 in Figure 3.2, we get:

$$V_i - i_1 R_{L1} - L_1 \frac{d}{dt} i_1 - V_{C1} - R_{C1} (i_1 - i_2) = 0 \quad (3.21a)$$

$$L_1 \frac{d}{dt} i_1 = V_i - i_1 R_{L1} - V_{C1} - R_{C1} i_1 + R_{C1} i_2 \quad (3.21b)$$

$$i_1 = \frac{1}{L_1} V_i - \frac{(R_{L1} + R_{C1})}{L_1} i_1 - \frac{1}{L_1} V_{C1} + \frac{R_{C1}}{L_1} i_2 \quad (3.21)$$

$$i_1 - i_2 = C_1 \frac{d}{dt} V_{C1} \quad (3.22a)$$

$$\dot{V}_{C1} = \frac{1}{C_1} i_1 - \frac{1}{C_1} i_2 \quad (3.22)$$

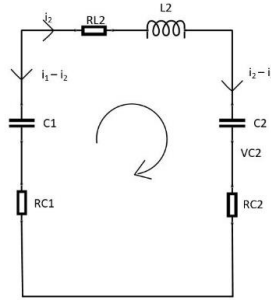


Figure 3.3: Second loop

Applying KVL and KCL for loop 2 in Figure 3.3, we get:

$$V_{C1} + R_{C1} (i_1 - i_2) - i_2 R_{L2} - L_2 \frac{d}{dt} i_2 - V_{C2} - R_{C2} (i_2 - i_3) = 0 \quad (3.23a)$$

$$L_2 \frac{d}{dt} i_2 = V_{C1} + R_{C1} i_1 - R_{C1} i_2 - i_2 R_{L2} - V_{C2} - R_{C2} i_2 + R_{C2} i_3 \quad (3.23b)$$

$$i_2 = \frac{R_{C1}}{L_2} i_1 + \frac{1}{L_2} V_{C1} - \frac{(R_{C1} + R_{L1} + R_{C2})}{L_2} - \frac{1}{L_2} V_{C2} + \frac{R_{C2}}{L_2} i_3 \quad (3.23)$$

$$i_2 - i_3 = C_2 \frac{d}{dt} V_{C2} \quad (3.24a)$$

$$\dot{V}_{C2} = \frac{1}{C_2} i_2 - \frac{1}{C_2} i_3 \quad (3.24)$$

Applying KVL and KCL for loop 3 in Figure 3.4, we get:

$$V_{C2} + R_{C2}(i_2 - i_3) - i_3 R_{L3} - L_3 \frac{d}{dt} i_3 - V_{C3} - R_{C3}(i_3 - i_4) = 0 \quad (3.25a)$$

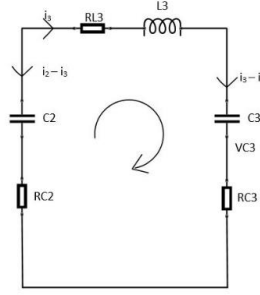


Figure 3.4: Third loop

$$L_3 \frac{d}{dt} i_3 = V_{C2} + R_{C2} i_2 - R_{C2} i_3 - i_3 R_{L3} - V_{C3} - R_{C3} i_3 + R_{C3} i_4 \quad (3.25b)$$

$$i_3 = \frac{R_{C2}}{L_3} i_2 + \frac{1}{L_3} V_{C1} - \frac{(R_{C2} + R_{L3} + R_{C3})}{L_3} - \frac{1}{L_3} V_{C3} + \frac{R_{C3}}{L_3} i_4 \quad (3.25)$$

$$i_3 - i_4 = C_3 \frac{d}{dt} V_{C3} \quad (3.26a)$$

$$\dot{V}_{C3} = \frac{1}{C_3} i_3 - \frac{1}{C_3} i_4 \quad (3.26)$$

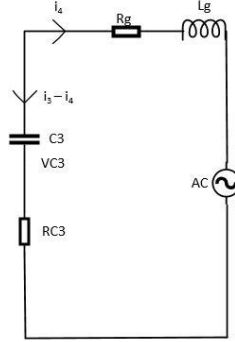


Figure 3.5: Fourth loop

Applying KVL and KCL for loop 4 in Figure 3.5, we get:

$$V_{C3} + R_{C3}(i_3 - i_4) - i_4 R_g - L_g \frac{d}{dt} i_4 - V_g = 0 \quad (3.27a)$$

$$L_g \frac{d}{dt} i_4 = V_{C3} + R_{C3} i_3 - R_{C3} i_4 - R_g i_4 - L_g \frac{d}{dt} i_4 - V_g \quad (3.27b)$$

$$i_4 = -\frac{1}{L_g} V_{C3} + \frac{R_{C3}}{L_g} i_3 - \frac{(R_{L3} + R_g)}{L_g} i_4 - \frac{1}{L_g} V_g \quad (3.27)$$

3.2.3 State-space representation

The state space is one of the ways of describing a dynamic model of the system, and it can be used to represent not only linear systems but also nonlinear systems. The state-space representation of a system is always referred to as the internal model description because the internal variables, such as the states, are fully described in such a model representation.

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \quad \text{state equation}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \quad \text{output equation}$$

$\mathbf{x}$ = state vector

$\dot{\mathbf{x}}$ = derivative of the state vector with respect to time

$\mathbf{y}$ = output vector

$\mathbf{u}$ = input or control vector

$\mathbf{A}$ = system matrix dimension of $\mathbf{A}$ is $n * n$

B = input matrix dimension of B is $n * p$

C = output matrix dimension of C is $q * n$

D = Feed forward matrix (in the case where the system model doesn't have direct feedthrough, D is the zero matrix), dimension of D is $q * p$

Writing down the state-space model from the above-derived equations 3.21, 3.22, 3.23, 3.24, 3.25, 3.26, and 3.27,

We get,

$$\dot{x} = \begin{bmatrix} i_1 \\ V_{C1} \\ i_2 \\ V_{C2} \\ i_3 \\ V_{C3} \\ i_4 \end{bmatrix} = \begin{bmatrix} \frac{-(R_{L1} + R_{C1})}{L_1} & \frac{-1}{L_1} & \frac{R_{C1}}{L_1} & 0 & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ \frac{R_{C1}}{L_2} & \frac{1}{L_2} & \frac{-(R_{C1} + R_{L2} + R_{C2})}{L_2} & \frac{-1}{L_2} & \frac{R_{C2}}{L_2} & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & \frac{-1}{C_2} & 0 & 0 \\ 0 & 0 & \frac{R_{C3}}{L_3} & \frac{1}{L_3} & \frac{-(R_{C2} + R_{L3} + R_{C3})}{L_3} & \frac{-1}{L_3} & \frac{R_{C3}}{L_3} \\ 0 & 0 & 0 & 0 & \frac{1}{C_3} & 0 & \frac{-1}{C_3} \\ 0 & 0 & 0 & 0 & \frac{R_{C3}}{L_g} & \frac{1}{L_g} & \frac{-(R_{C3} + R_g)}{L_g} \end{bmatrix} \begin{bmatrix} i_1 \\ V_{C1} \\ i_2 \\ V_{C2} \\ i_3 \\ V_{C3} \\ i_4 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & \frac{-1}{L_g} \end{bmatrix} \begin{bmatrix} V_i \\ V_g \end{bmatrix} \quad (3.2.8)$$

$$y = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ V_{C1} \\ i_2 \\ V_{C2} \\ i_3 \\ V_{C3} \\ i_4 \end{bmatrix} + 0.u$$

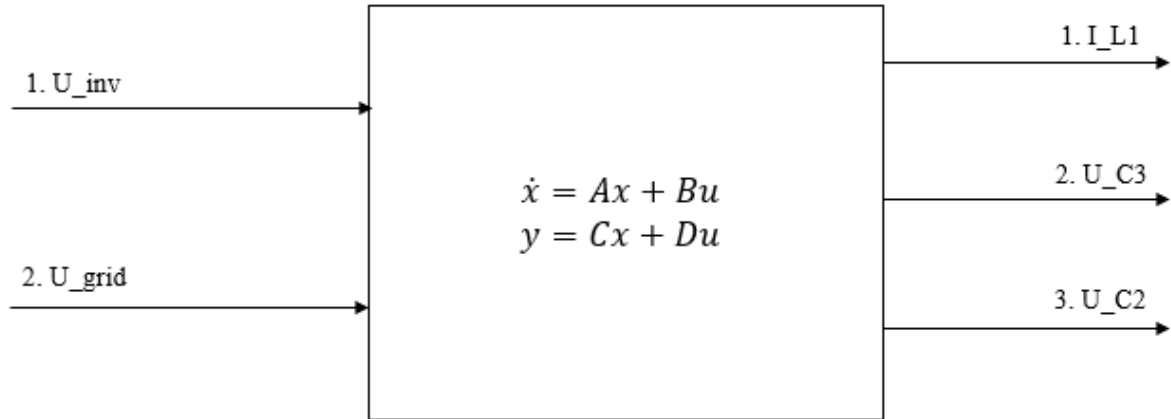


Figure 3.6: Block diagram representation of the state-space model

The output filter with two inputs and three outputs looks like in Figure 3.7. The block diagram represents an LC+EMI filter system. The Open-loop step response of the system is shown in Figure 3.7, and the open-loop step response of the output current is shown in Figure 3.8. In this,

the output current on the inverter side is to be controlled. Adding a current measurement filter to the first output of the system and a voltage measurement filter to outputs two and three of the system. Develop a stable controller which operates with a wide range of grid impedances and varying in system parameters. This is discussed in the following sections.

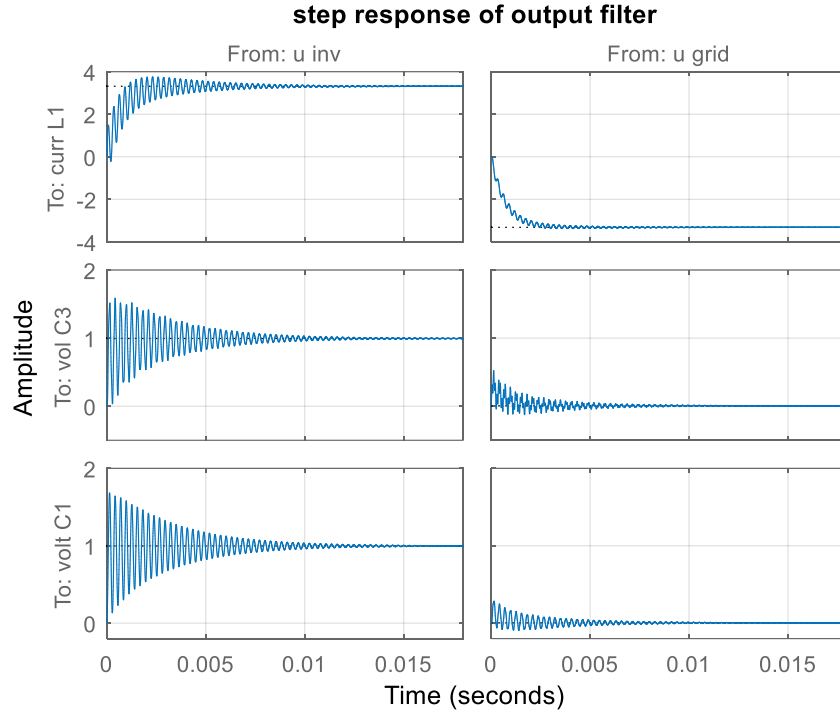


Figure 3.7: Step response of LC+EMI filter

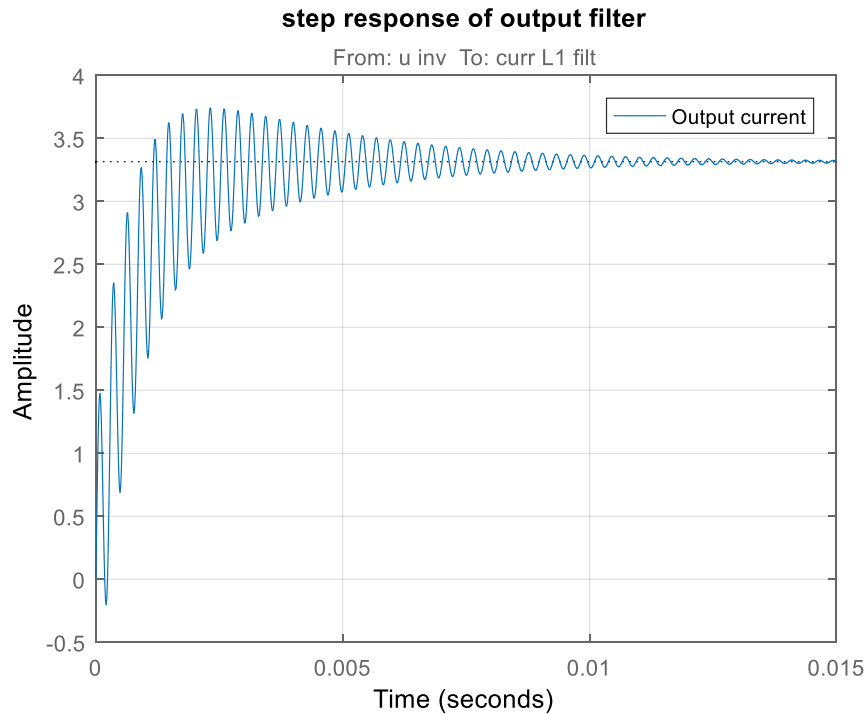


Figure 3.8: Step response of output current

3.3 Measurement filters

Filters are useful in a variety of situations. A single-pole low-pass filter is frequently used to stabilize amplifiers by rolling off the gain at higher frequencies where excessive phase shift can induce oscillations.

In high gain amplifiers or single supply circuits, a simple single-pole high-pass filter can be utilized to block dc offset. Filters can be used to segregate signals, pass the ones that are of interest, and suppress the ones that aren't.

The signal one wants to process is passed through with gain while the rest of the signals are attenuated. Filters are also employed in data conversion to eliminate the impact of aliases in AC/DC systems. They're also used to smooth the waveform at the output of a DC/AC by removing higher-frequency components like the sampling frequency and its harmonics.

The amplitude response of an ideal filter will be unity at the frequencies of interest and zero everywhere else. The cut-off frequency is the frequency at which the response transitions from passband to stopband.

Typically, one or more of the above parameters will be variable. For an antialiasing filter for a power electronic converter, you will know the cut-off frequency, the stop band frequency, (which will generally be the Nyquist frequency ($= \frac{1}{2}$ the sample rate)) and the minimum attenuation required (which will be set by the resolution or dynamic range of the system).

3.3.1 A third-order voltage measurement system

Different filters are investigated for voltage measurement. Bessel filter, Butter filter, and Chebyshev filter. The order of the filter is 3 with a cut-off frequency of 6000 Hz. The step response and bode plots of the different filters are shown below.

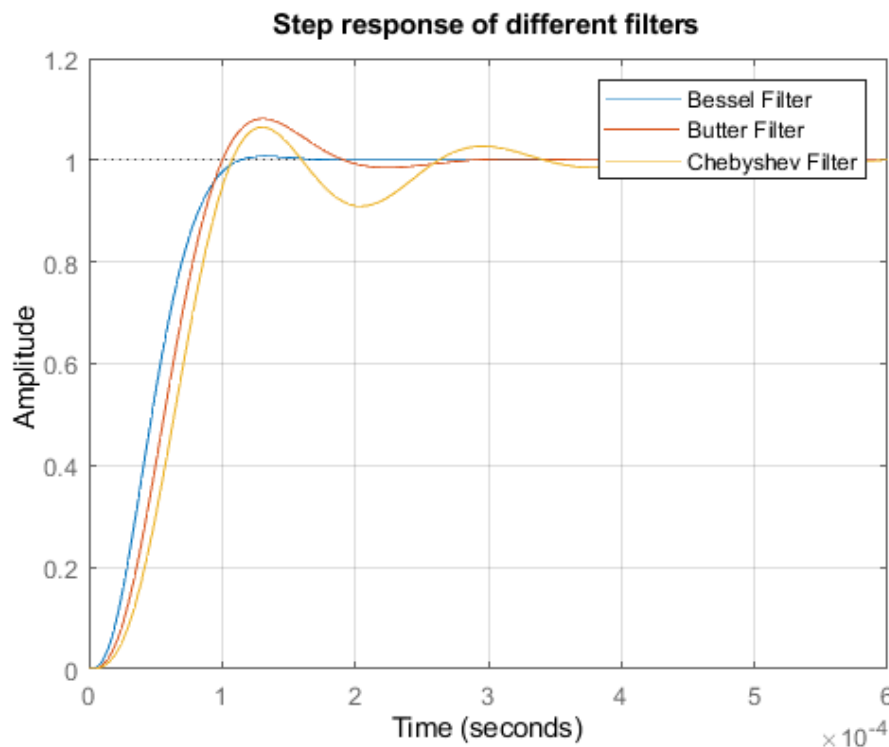


Figure 3.9: Step response of different filters

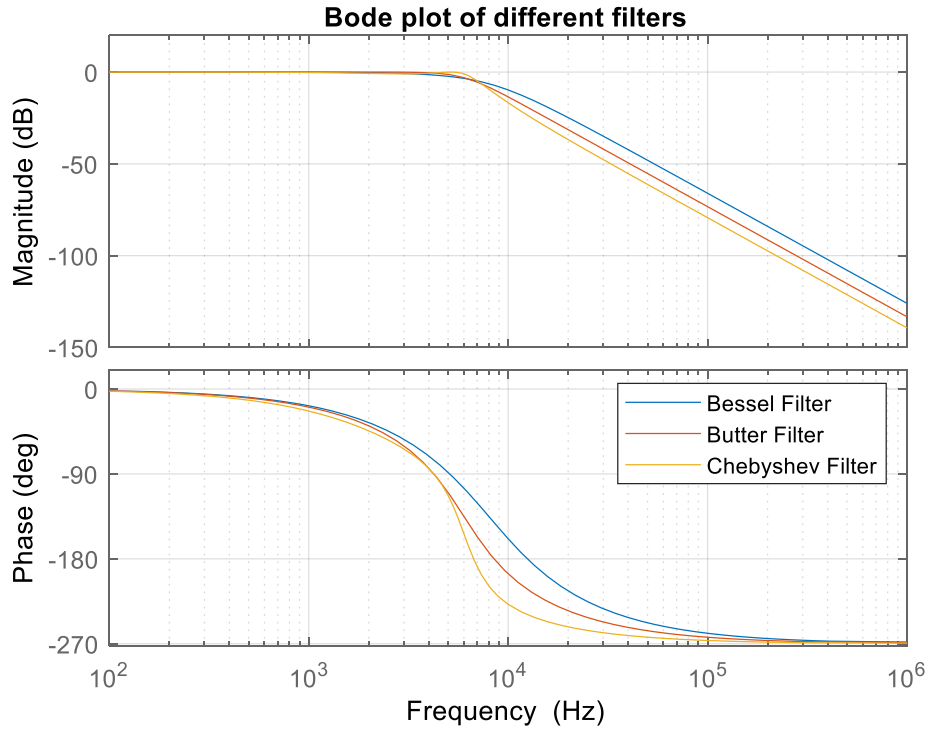


Figure 3.10: Bode plot of different filters

With different filters, the Bessel filter gives better performance than other filters. So, in this thesis, a third-order Bessel filter with a cut-off frequency of 6000 Hz is chosen.

A third-order Bessel filter is a system whose dynamics are described by the transfer function and assumes the form

$$G(s) = \frac{1}{(As^3 + Bs^2 + Cs + D)}$$

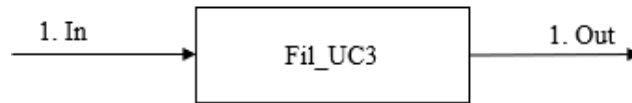


Figure 3.11: Third-order voltage measurement filter

3.3.2 A first-order current measurement system

A first-order measurement system is a system whose dynamics are described by a first-order differential equation. The transfer function assumes the form

$$G(s) = \frac{1}{(1 + \tau s)}$$

With τ being the time constant of the system

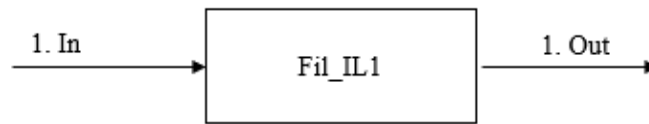


Figure 3.12: First order current measurement filter

3.3.3 Setting up the whole system

Adding current and voltage measurement filters to the LC+EMI filter. After adding measurement filters to the output filter, the system looks like in Figure 3.13.

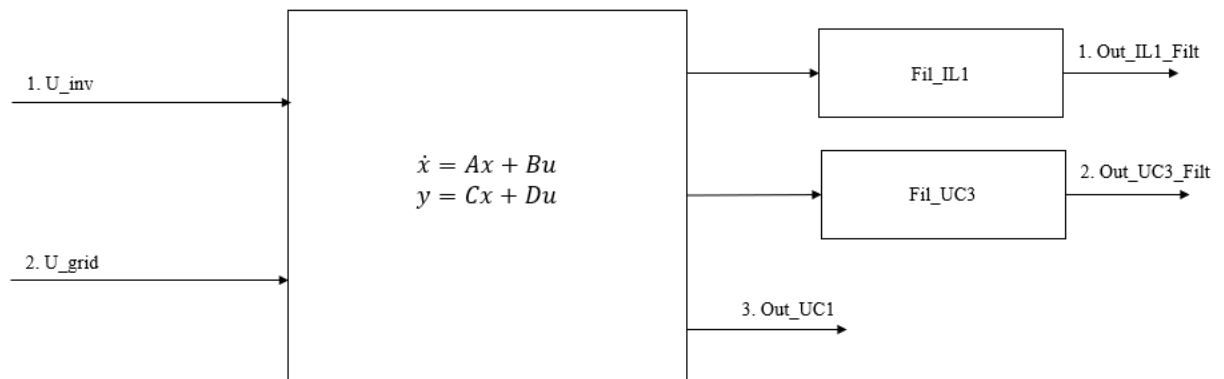


Figure 3.13: Adding filters to the output filter

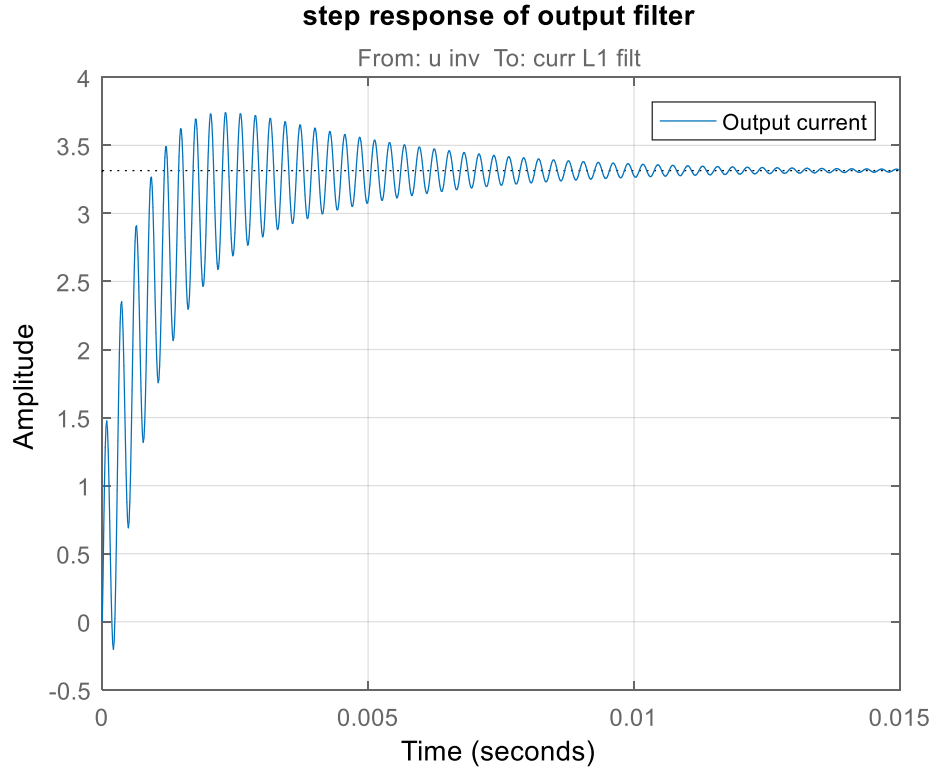


Figure 3.14: Step response of output current with measurement filters

As observed in Figures 3.8 and 3.14, the step response of the output current looks similar in both cases.

In the next step, adding a feedforward path from the voltage to the input changes the dynamics of the system. This removes the harmonics of the output filter. The block diagram of the output filter with a feed-forward loop looks like in Figure 3.15.

3.3.4 Adding a feedforward path to the system

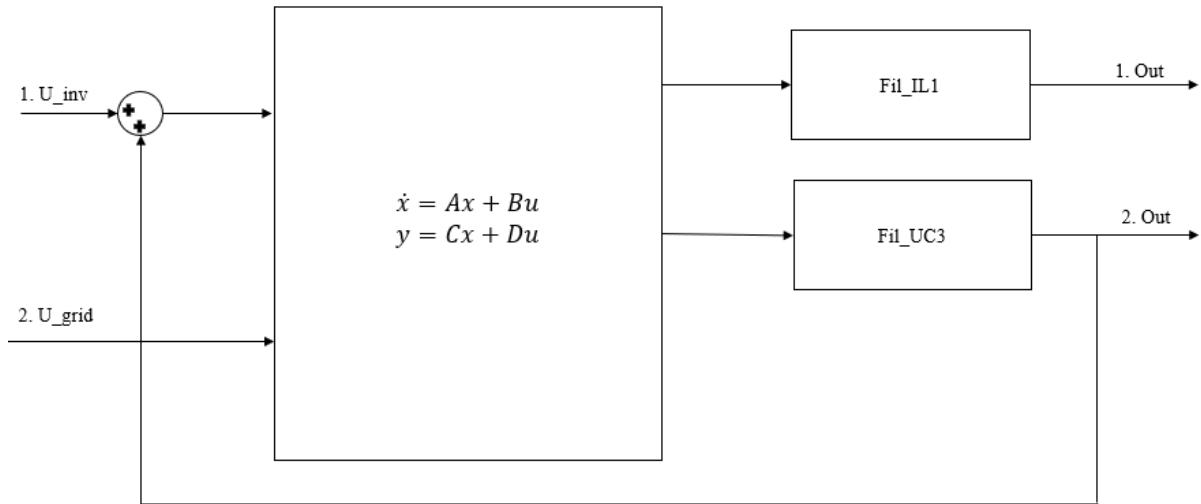


Figure 3.15: Feedforward path to the system

The block diagram looks like in Figure 3.15. This feedback reduces the harmonics of the system. Gives better dynamic behavior of the system. This can be observed in the step response of the system in Figure 3.16.

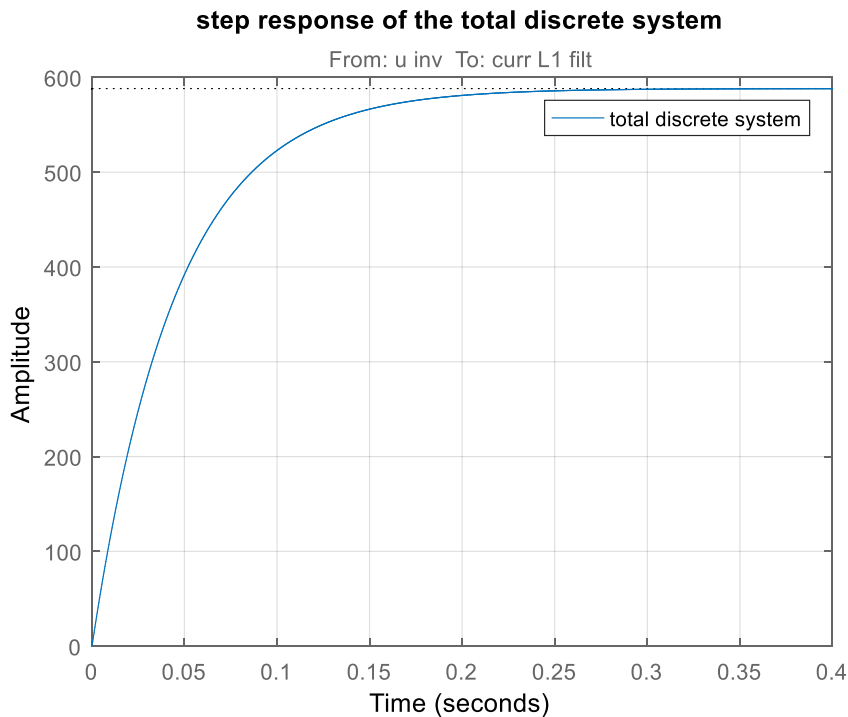


Figure 3.16: Step response of the discrete system with a feedforward loop

Figure 3.15 shows the total system setup. The root locus of the total discrete system can be seen in Figure 3.17. Implementation of the control strategies to the total system to achieve better performance of the system.

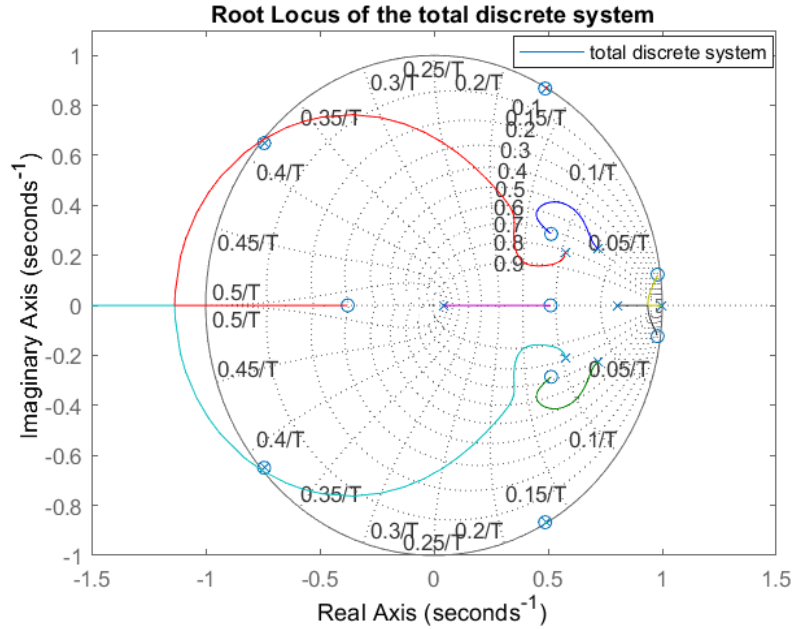


Figure 3.17: Root locus of the total discrete system

3.4 Control Schemes

In this thesis, the DC-bus link is assumed as a fixed bus and focuses on the current control of the grid-tie inverter. As discussed in chapter 2.5, the appeal of PI controllers stems mostly from the ease with which their control structures can be implemented and the reliability with which their control performance can be achieved. Select the PI controller parameters that would provide the optimal responses.

In this thesis, PI control with symmetrical optimum and PI control with root locus method is covered, and results are compared based on the performance specifications of the system like overshoot and settling time.

Symmetrical Optimum has the benefit of being robust in a variety of ways (phase margin, gain margin, sensitivity, and process dynamics). The SO technique aims to retain the phase difference symmetrical at all times. The SO technique is dependent on the system's time constants.

Root locus helps to obtain a clear picture of the transient response of the system for various values of open-loop gain K by moving the pole location and to determine the performance specifications.

A detailed explanation of the PI controller tuning methods and results are shown in the following sections.

3.4.1 Methodology

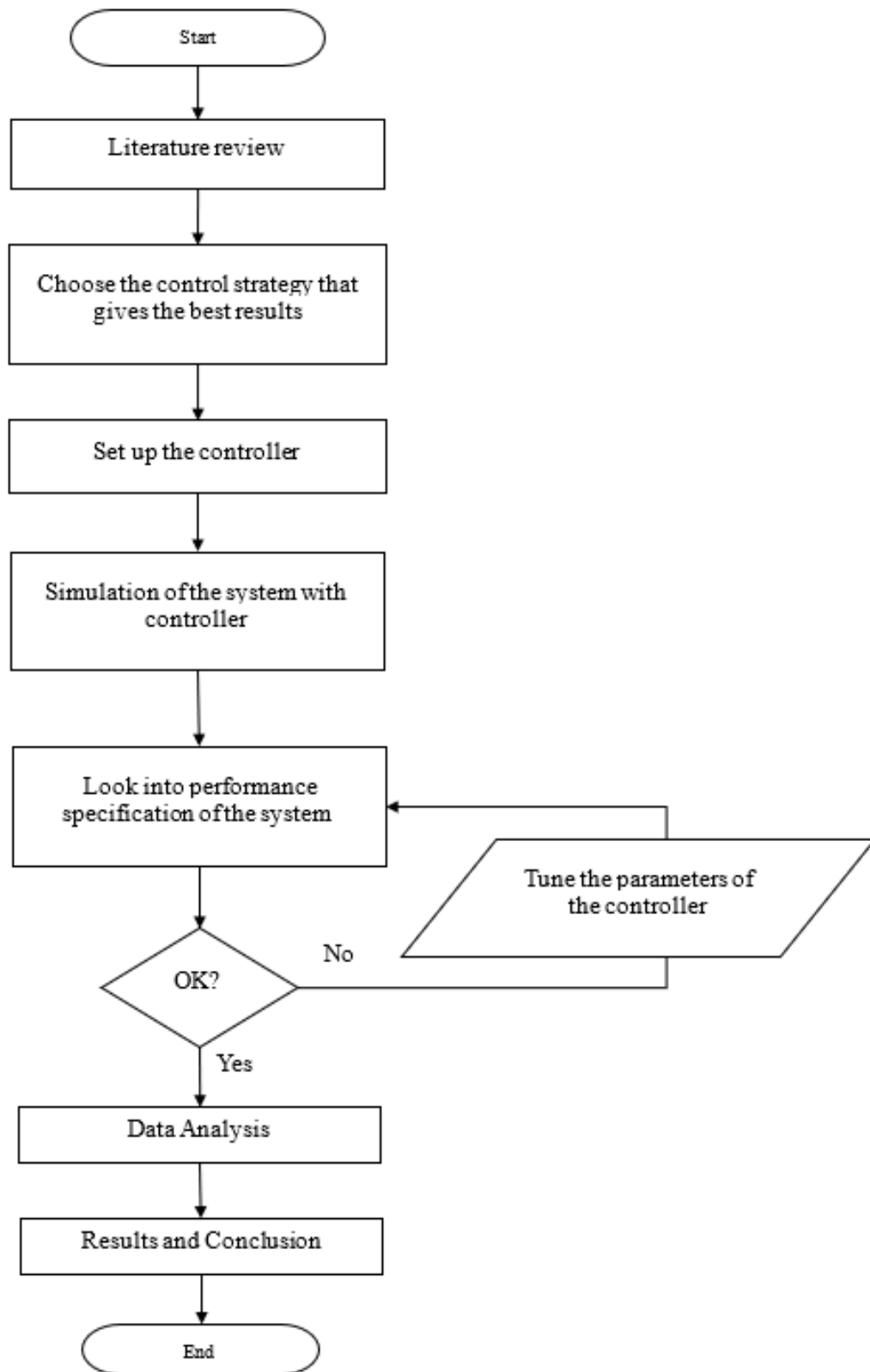


Figure 3.18: Flow chart for implementing control strategies

3.4.2 Symmetrical Optimum method

The popularity of PI controllers is mainly due to the simplicity of their control structure and the feasibility of their control performance. As an aside, this design process is usually carried out with a thorough understanding of the facility. A linear time-invariant continuous or discrete-time model is also commonly used to explain the plant. The controller's structure is chosen such that the system's reaction meets particular qualitative criteria, such as stability, suitable disturbance management capabilities, and so on. Techniques have evolved in the field of control engineering to discover the best set of controller parameters for a given plant and controller combination. The well-known symmetrical optimum tuning method was applied in this thesis. In German literature, this strategy appears to be well documented [54].

A controller that makes the system's frequency response as comparable to that of low frequencies as possible is produced by the symmetrical optimal design criterion. This method has been around for a while in the industry, although it doesn't appear to be widely documented in the English control engineering literature.

The advantage of this strategy is that it maximizes the phase margin. The system can tolerate larger delays when the phase margin is maximized for a given frequency, which is critical for all systems with delays. This strategy optimizes the behavior of the control system in response to disturbance input. The approach is well established in terms of tuning principles and has a high level of disturbance rejection [55]. This paper presents an expanded technique for tuning via symmetric optimum [56].

The proportional controller has no sense of time, and its actions are determined by the current error value. Based on past and future values, a suitable controller must make corrections. Combining proportional with integral action PI or proportional with derivative action PD can achieve this. The PID controller is one of the most prevalent commercially available controllers. Distinct processes require different proportional, integral, and derivative control combinations. The PI controller is employed in this case.

$$G_c(s) = K_p + \frac{K_i}{s} \quad (3.4.1)$$

3.4.2.1 PI Controller Design

The integral of the error, as well as the error itself, is used for control, and the controller transfer function is,

$$G_c(s) = K_p + \frac{K_i}{s} \quad (3.4.2)$$

Or

$$G_c(s) = \frac{K_p s + K_i}{s} = \frac{K_p(s + \frac{K_i}{K_p})}{s} = \frac{K_p(s + z_0)}{s} \quad (3.4.3)$$

Where,

$$z_0 = \frac{K_i}{K_p} \quad (3.4.4)$$

Integral control bases its corrective action on the cumulative error integrated over time

3.4.2.2 Symmetrical Optimum PI Tuning Method

In 1958, Kessler proposed the symmetrical optimum (SO) tuning method for the first time. The parameters of the PI controller for the plant model indicated in (3.4.7) could be found using (3.4.8) according to the SO criterion.

$$G_{SE}(s) = \frac{K_s}{(1 + sT_1)(1 + sT_E)} \quad (3.4.5)$$

$$T_1 \geq a^2 T_E, T_E = \sum_{i=2}^n T_i \quad (3.4.6)$$

$$G_R(s) = \frac{K_R(1 + sT_N)}{sT_N} \quad (3.4.7)$$

$$T_N = a^2 T_E, K_R = \frac{T_1}{aK_s T_E} \quad (3.4.8)$$

Where a is a parameter that defines the closed-loop transfer function phase margin and damping ratio: The higher the value of a the greater the phase margin and damping ratio will be. A more detailed explanation of the SO tuning approach may be found in [57].

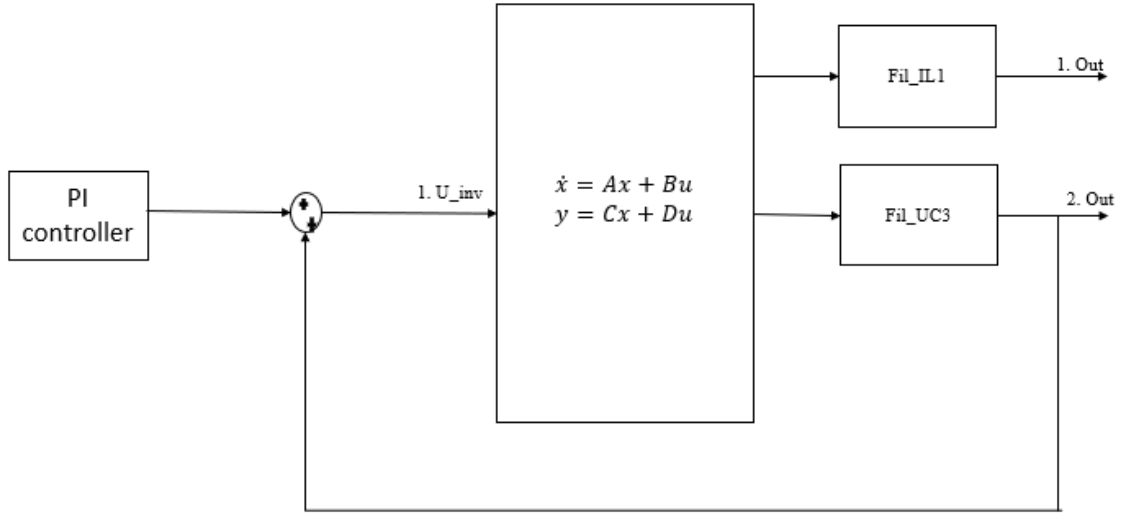


Figure 3.19: Total system with PI controller

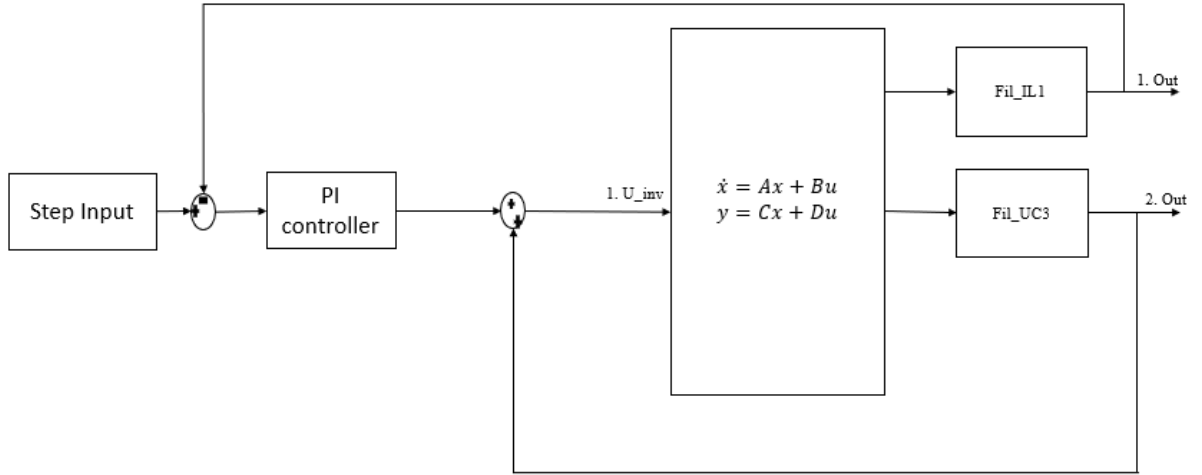


Figure 3.20: Step input to the system

Most of the literature use $T_N = 4T_E$ ($a = 2$) for the optimization according to conventional symmetrical optimum tuning [56]. The resulting performance gives an overshoot of around 35 % and a settling time of around 2.54 ms. The phase margin value is low and the system has a high overshoot.

The out (1) in Figure 3.19 the step response represents the output current at inductor L1 of the system in every plot.

From Figure 3.19, the system response to a step function gives an overshoot of 34.5 % and a settling time of 2.54 ms.

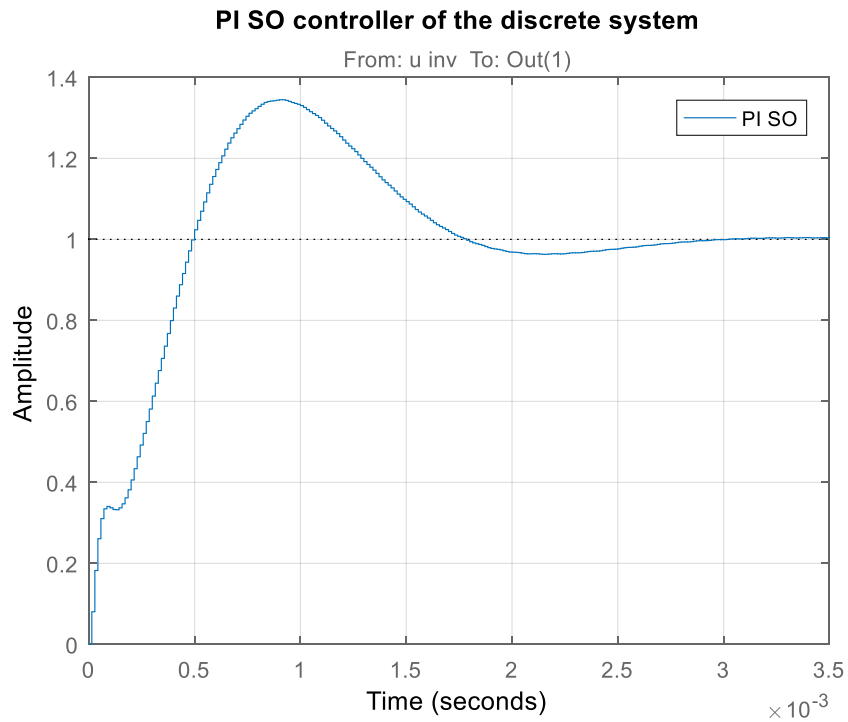


Figure 3.21: Step response with PI symmetrical optimum method

It is possible to compensate for the overshoot and enhance the performance of the controller by choosing a higher value of a so that the phase margin is increased and the damping is also improved, but then, the system is less dynamic. Hence the choice of the controller parameters from a design point of view is a compromise between the performances.

Increasing the value of a fits our criteria. This is shown in Figure 3.23.

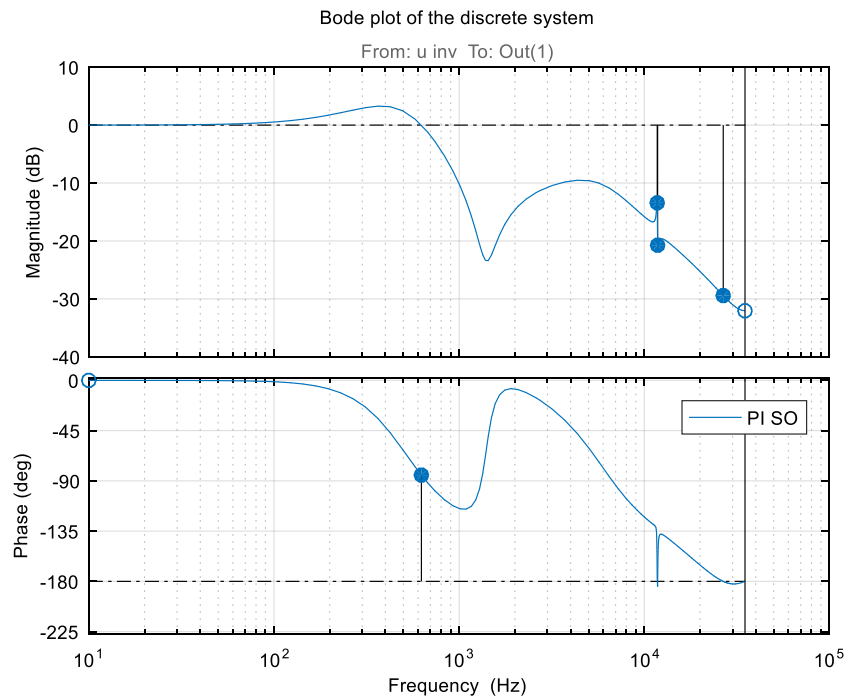


Figure 3.22: Bode plot of the system

From Figure 3.22, the minimum stability of the system with a gain margin of 13.4 dB at 11.7 kHz frequency and a phase margin of 95.2°.

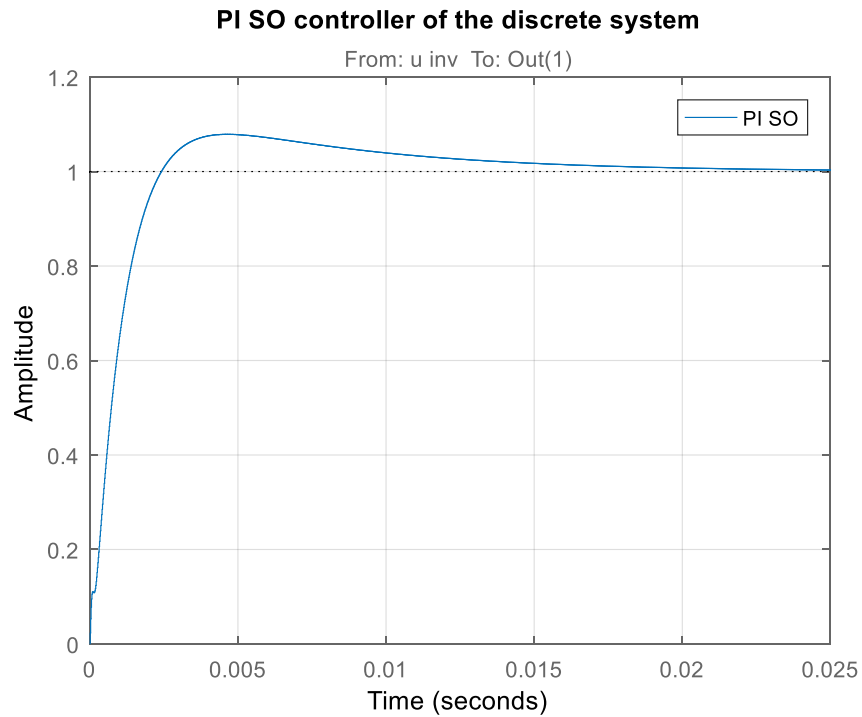


Figure 3.23: Step response with PI symmetrical optimum method

With an increase in a value the overshoot is reduced to 7.88 %, however, the settling time is increased to 14.2 ms.

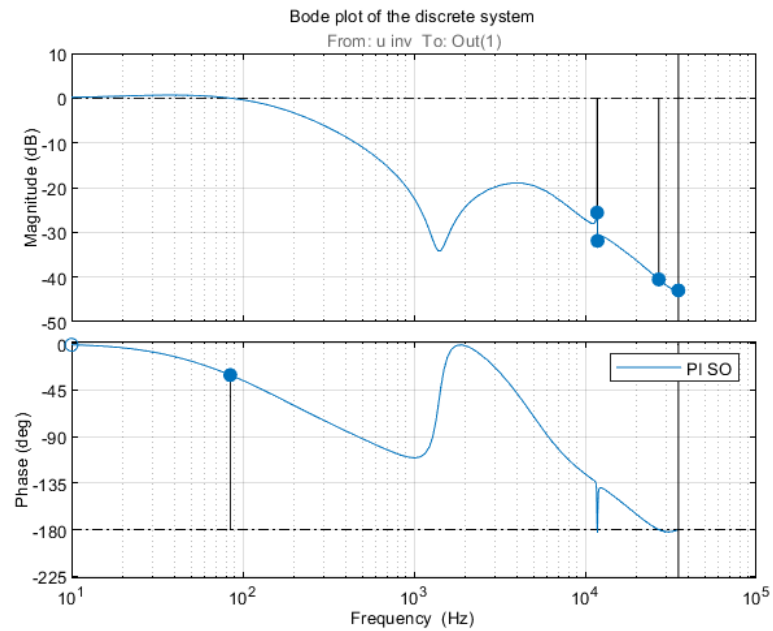


Figure 3.24: Bode plot of the system.

In Figure 3.24, the minimum stability of the system with a gain margin of 25.6 dB at 11.8 kHz frequency and a phase margin of 150°. With the increase in the value of a , it's observed that increase in gain and phase margins of the system.

The stability criterion was specified by Nyquist: that, for stability, the Nyquist plot of the loop gain must not encircle the point $(-1,0)$ in a clockwise direction; every clockwise encirclement of the $(-1,0)$ point corresponds to an RHP pole. If the loop gain instead intersects $(-1,0)$ then this corresponds to a resonant peaking in the closed-loop response.

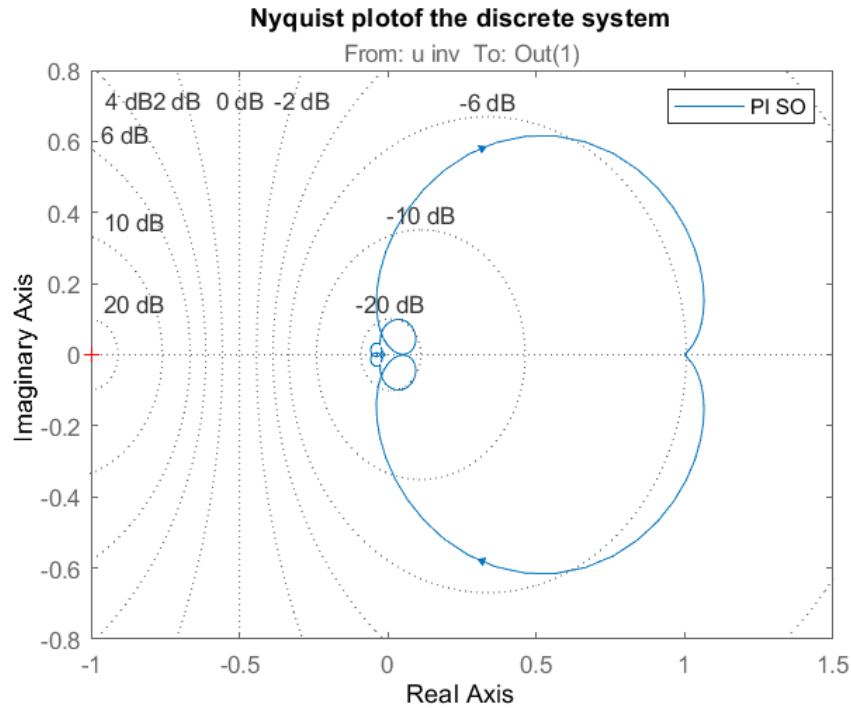


Figure 3.25: Nyquist plot of the system

The loop gain making a clockwise encirclement of $(-1,0)$ indicates an unstable system. It's easy to imagine a Nyquist plot that doesn't encircle the point $(-1,0)$ (i.e., it dips inside the unit circle at 180°) but which grows back outside the unit circle at phases greater than 180°. Such a system would be stable, as long as it doesn't encircle $(-1,0)$ on its second pass (540°) or its third pass (900°). Nyquist plot of the system doesn't encircle $(-1,0)$ with minimum stability of the system with a gain margin of 25.6 dB at 11.8 kHz frequency and a phase margin of 150°.

The PI control with the symmetrical optimum method gives a stable system and good performance specifications.

3.4.2.3 Grid Impedance Investigation

Grid Impedance, as stated in Chapter 2.4, is a critical characteristic that influences the control performance of grid-connected power converters. It's also known to cause current control to slow down. These values are chosen from a range of values. Grid resistance R_g in the range of 106 mΩ to 340 mΩ, and grid inductance L_g in the range of 100 μH to 500 μH.

Grid Inductance (L_g) (μH)	Settling time (ms)	Overshoot (%)
100	14.2	7.72
300	14	8.54
500	13.8	10.6

Table 3.3: Performance of system with different grid inductances

According to Table 3.3, the system with low grid inductance has a higher settling time and less overshoot, whereas the system with high grid inductance has a higher overshoot and lower settling time.

PI SO controller of the discrete system with varying grid impedance

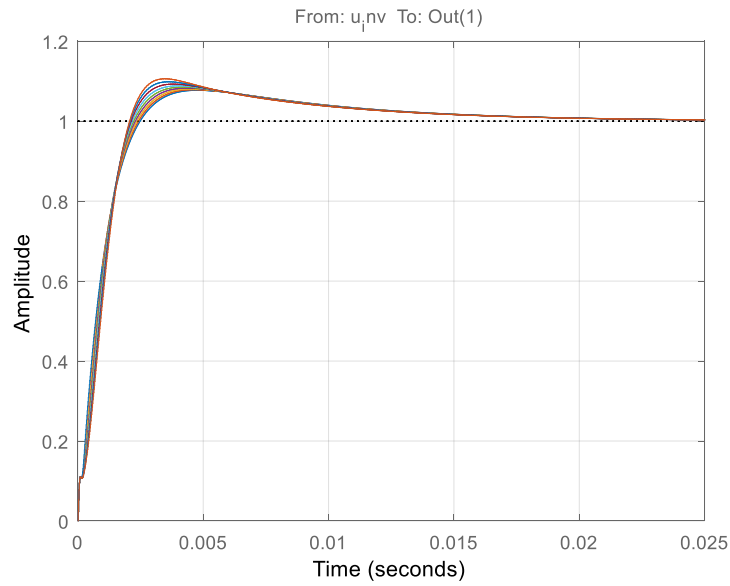


Figure 3.26: Step response with varying grid impedance

Nyquist plot of the discrete system with varying grid impedance

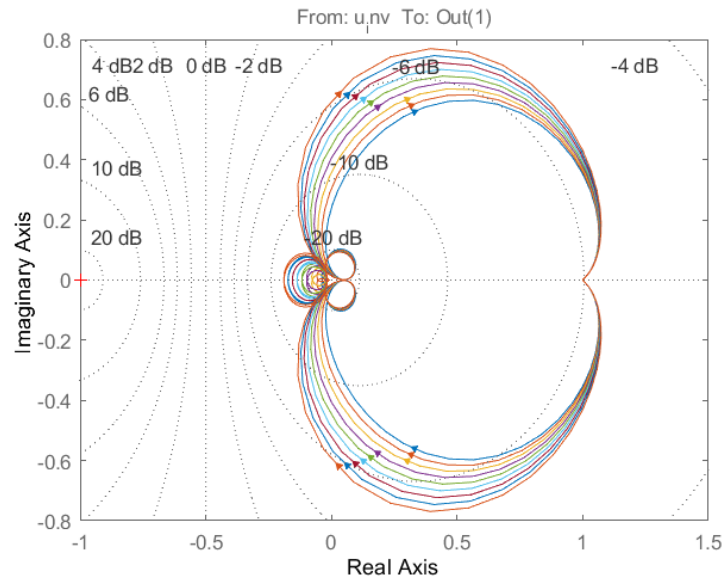


Figure 3.27: Nyquist plot of the system with varying grid impedance

Grid Inductance (L_g) (μH)	Gain margin (dB)	Phase margin ($^\circ$)
100	40.5	151
500	14.5	136

Table 3.4: Minimum stability of the system with varying grid impedance

The variation of grid Inductance in the range from 100 μH to 500 μH the gain margin of the system varies more compared to that of the phase margin of the system. The Nyquist plot tells the stability of the system with varying grid impedance.

In the whole range of grid inductance L_g , the system is stable. Choosing the grid impedance values is then completely based on the performance requirements. In this thesis, grid resistance R_g is 300 m Ω , and grid inductance L_g is 150 μH . This is based on the lab test.

With this investigation, the system is stable with varying grid impedance of the system.

3.4.2.4 Varying System Parameters

The goal is to see if the controller is stable when the parameters change. The fluctuation of nominal values to extreme values -20 % and +20 %. The effects of performance specification are investigated in this section. Within this range, the system's overshoot is less than 10 %.

Variation (%) w.r.t nominal values	Settling time (ms)	Overshoot (%)
-20	12.5	6.78
Nominal values	14.2	7.88
+20	15.5	8.92

Table 3.5: Performance of the system with varying system parameters

Parameter	Symbol	-20 % of nominal values	Nominal	+20 % of nominal values
Series resistance with L1	RL1	1 m Ω	1 m Ω	1 m Ω
Inductance 1	L1	32.5*0.8 μH	32.5 μH	32.5* 1.2 μH
Capacitance 1	C1	64.7*0.8 μF	64.7 μF	64.7* 1.2 μF
Series resistance with C1	RC1	10 m Ω	10 m Ω	10 m Ω
Series resistance with L2	RL2	0.6 m Ω	0.6 m Ω	0.6 m Ω
Inductance 2	L2	26.8 * 0.8 μH	26.8 μH	26.8 μH
Capacitance 2	C2	4.7* 0.8 μF	4.7 μF	4.7*1.2 μF
Series resistance with C2	RC2	5 m Ω	5 m Ω	5 m Ω

Series resistance with L3	RL3	0.1 m Ω	0.1 m Ω	0.1 m Ω
Inductance 3	L3	6.3 * 0.8 μH	6.3 μH	6.3 * 1.2 μH
Capacitance 3	C3	4.7*0.8 μF	4.7 μF	4.7*1.2 μF
Series resistance with C3	RC3	0.1 m Ω	0.1 m Ω	0.1 m Ω

Table 3.6: system parameter variations

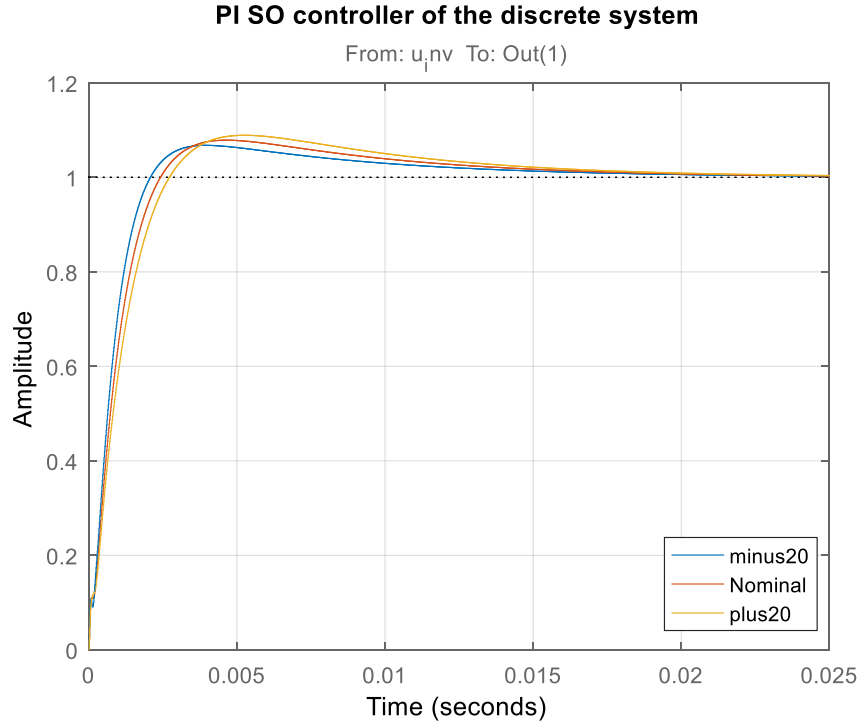


Figure 3.28: Step response of the system with varying system parameters

Figure 3.28 shows the response of the system to a step function with different system parameters

Variation (%) w.r.t nominal values	Gain margin (dB)	Phase margin (°)
-20	38.5	151
Nominal values	25.6	150
+20	20.6	148

Table 3.7: Minimum stability of the system with varying system parameters

From Figure 3.29, the minimum stability margin of the system is depicted in Table 3.7. With varying system parameters, the system is stable, however, there is a change in the stability margin of the system.

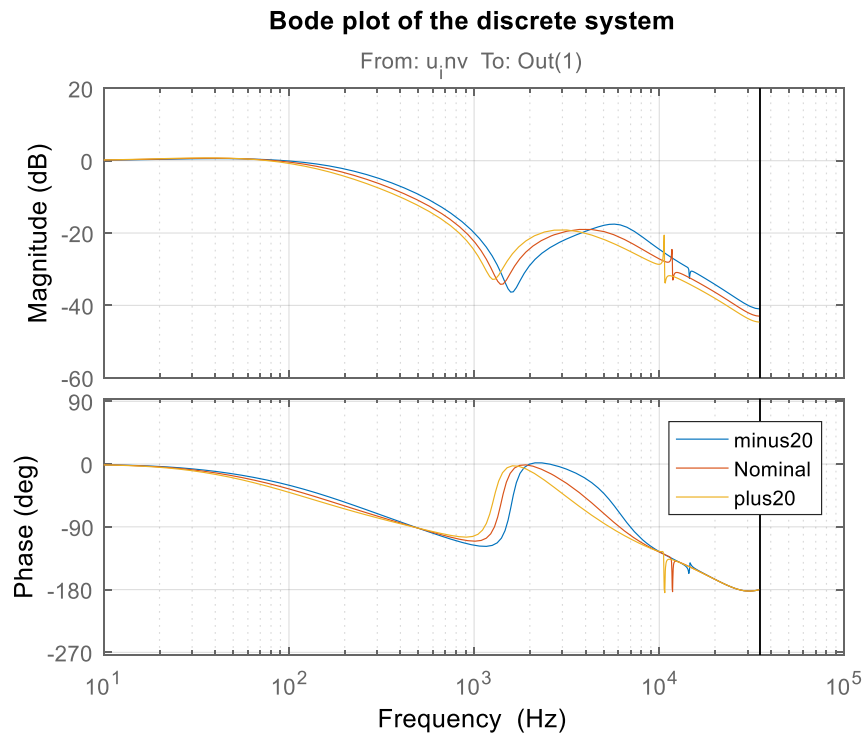


Figure 3.29: Bode of the system with varying system parameters

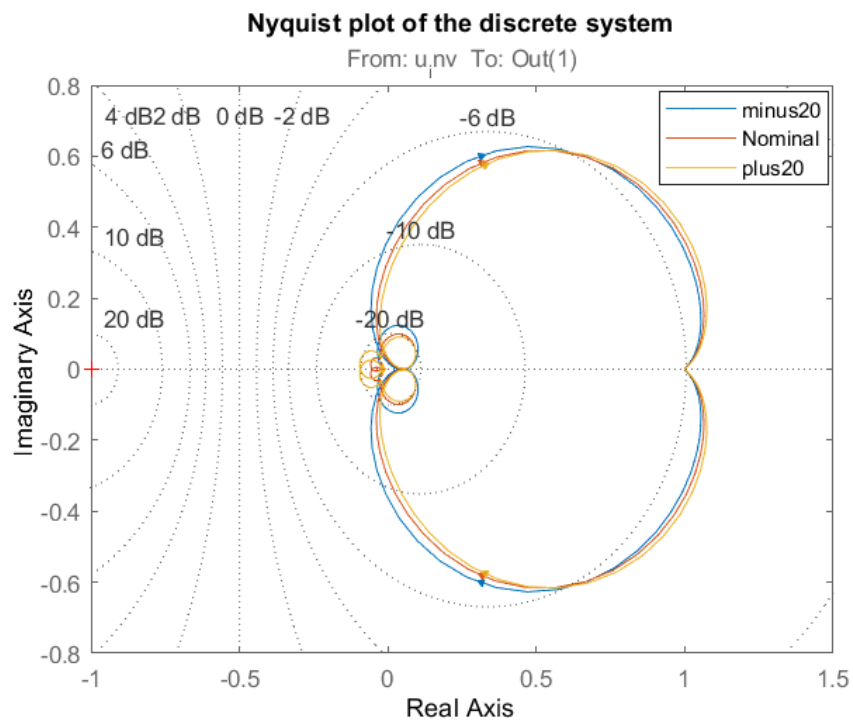


Figure 3.30: Nyquist plot of the system with varying system parameters

Figure 3.30 shows the Nyquist plot of the system doesn't encircle $(-1,0)$, which means the system is stable.

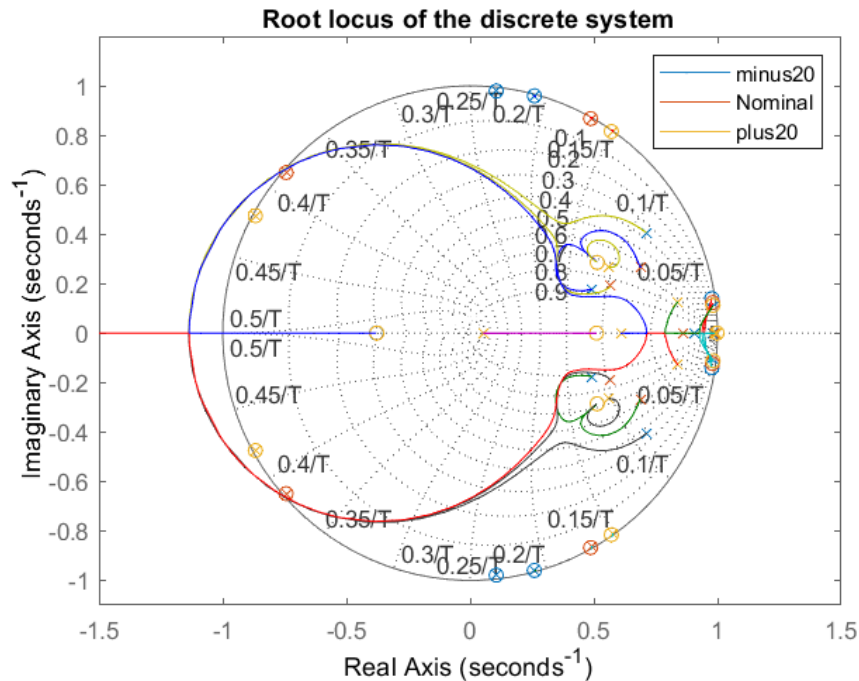


Figure 3.31: Root locus plot of the system with varying system parameters

In Figure 3.31, the change in location of poles is observed with a change in system parameters. With this investigation, the system is stable with varying system parameters.

3.4.3 PI Controller Root Locus method

The root locus method is to find the loop gain value that produces a satisfying closed-loop behavior. The proportional compensator, also known as a proportional controller, responds gradually to deviations from the set point. There are practical limits to the size of the gain. Instability is caused by extremely high gains. If the root-locus plot is such that the desired performance cannot be obtained by adjusting the gain, the root-loci must be reshaped by adding the additional controller $G_c(s)$ to the open-loop discrete system. The controller $G_c(s)$ must be chosen so that the root locus passes through the correct s-plane area. To meet the criteria, the uncompensated system's speed of response and/or damping must be increased in many circumstances. The prominent branches of the root locus must be moved to the left to accomplish this.

The root locus technique or method is a very handy graphical method for sketching the locus of roots in the s-plane as a parameter is varied. The parameter may be gain, phase, overshoot, or any other suitable control parameter. This method has been applied broadly in control engineering design problems.

Figure 3.32 depicts a closed-loop feedback mechanism. 'K' determines the system's gain. When we say feedback, we're referring to the fact that the loop has been closed. The input is fed back into the output.

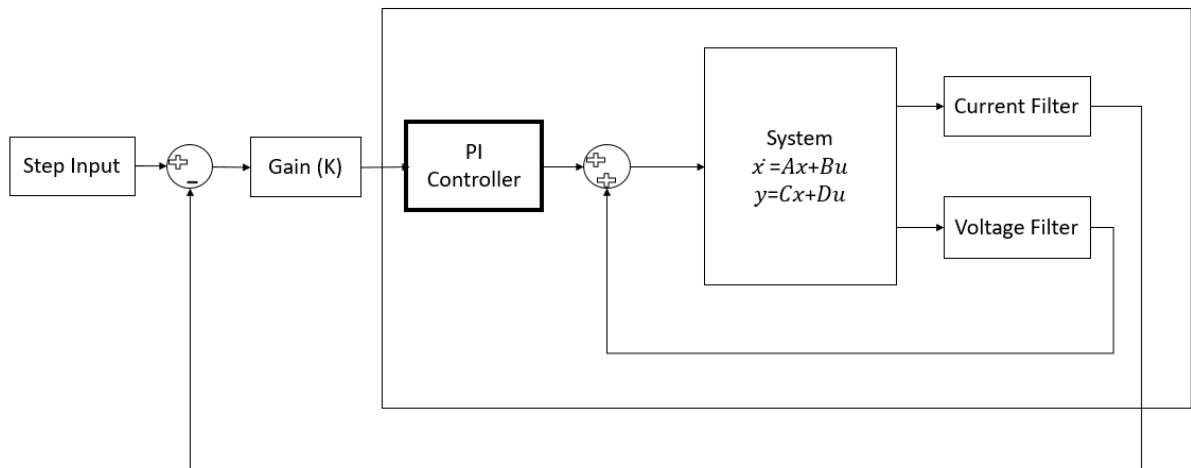


Figure 3.32: Total system setup with root locus method

3.4.3.1 Methodology

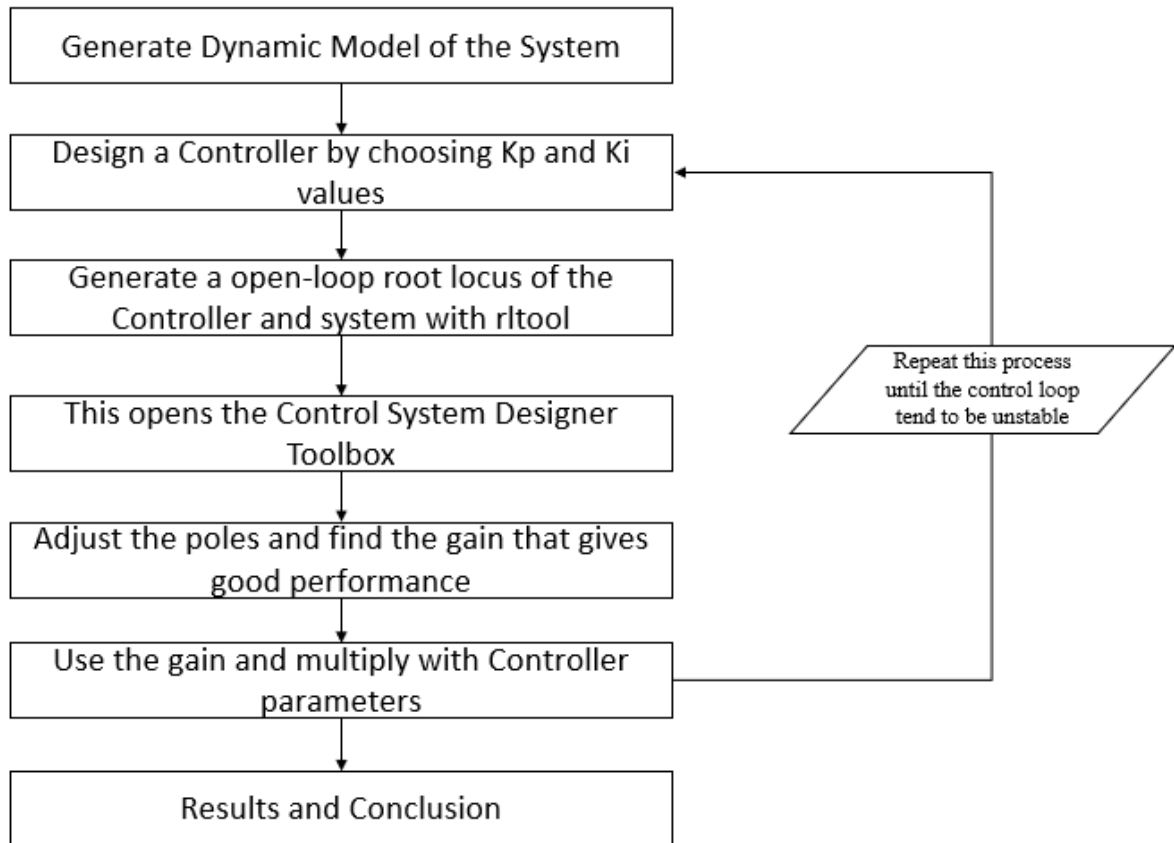


Figure 3.33: Root locus methodology

Follow the steps shown in Figure 3.33 to implement the PI root locus method.

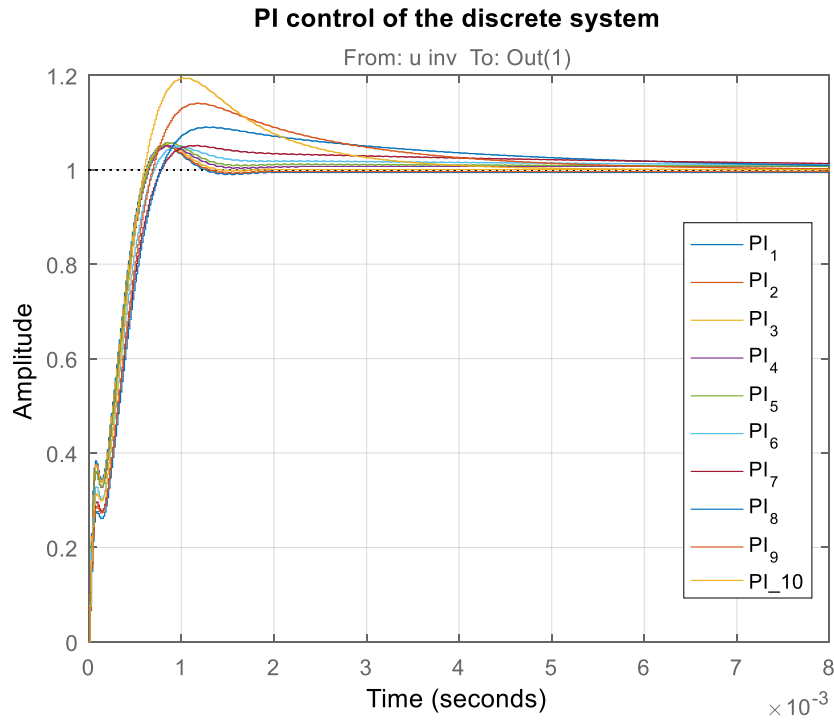


Figure 3.34: Step response of a system with PI root locus method

From Figure 3.34, the overshoot and settling of the system with different K_p and K_i values are shown in Table 3.8. Out of these parameters, $K_p = 1$, $K_i = 30$, and gain $K = 0.3315$ is chosen as control parameters because this value gives a better settling time of the system with varying system parameters and varying grid impedance of the system.

Proportional (K_p)	gain	Integral (K_i)	gain	Gain (K)	Overshoot (%)	Settling (ms)	time
1		1		0.34263	5.24	1.08	
1		10		0.33382	5.1	1.1	
1		30		0.3315	5.48	5.15	
1		50		0.31432	5.15	1.2	
1		75		0.31447	5.76	1.28	
1		100		0.27771	4.95	1.62	
1		150		0.24203	5.16	5.44	
1		300		0.21905	9.05	5.71	
1		500		0.22783	14.1	4.42	
1		750		0.25218	19.4	3.24	

Table 3.8: Different K_p , K_i , and K parameters

The step response of the system with the PI root locus with and without tuning the controller is shown in Figure 3.35. The system's step response without tuning the controller has a 16 % overshoot and a settling time of 1.6 ms. The system's step response with a tuned controller, on

the other hand, has a 5.48 % overshoot and a 1.13 ms settling time. Figure 3.36 depicts the shift in pole location.

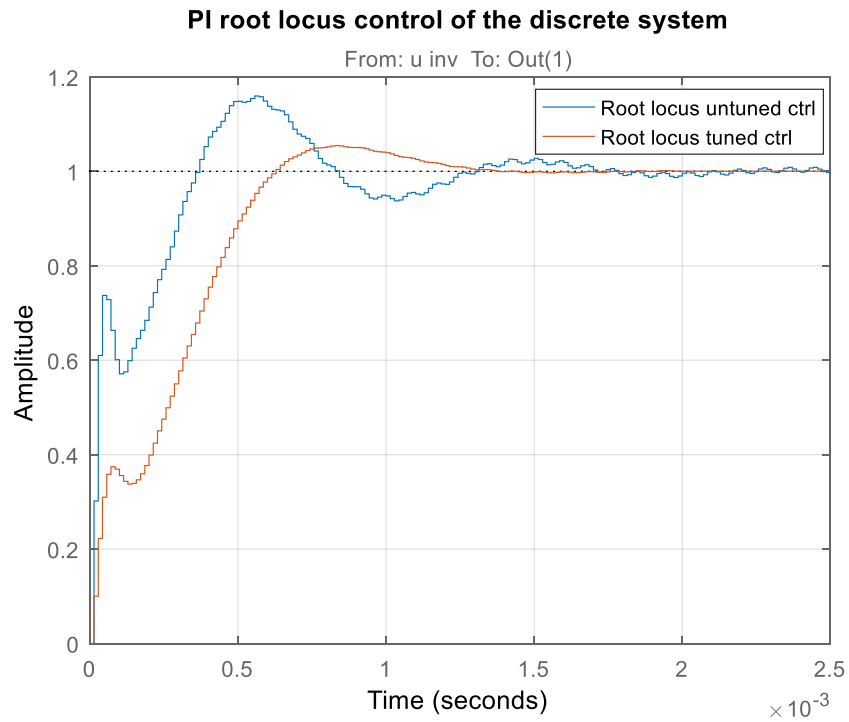


Figure 3.35: Step response of the system with and without gain

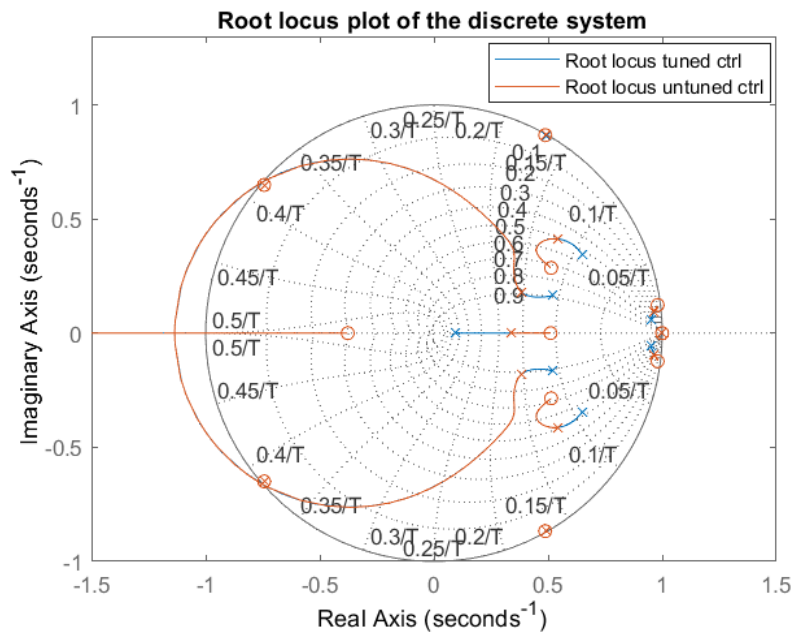


Figure 3.36: Root locus plot of the system with and without gain

3.4.3.2 Grid Impedance Investigation

PI root locus controller of the discrete system with varying grid impedance

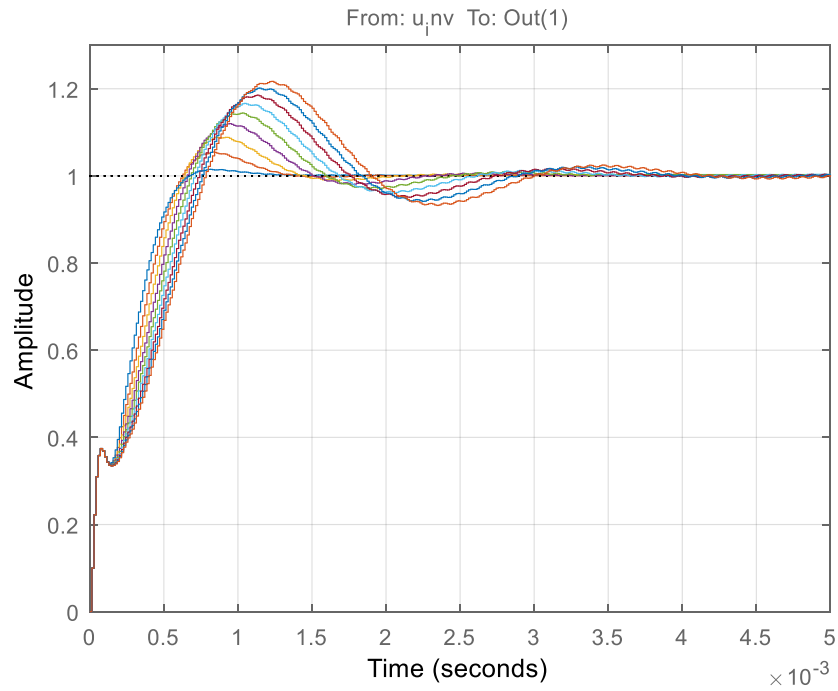


Figure 3.37: Step response of the system with varying grid impedance

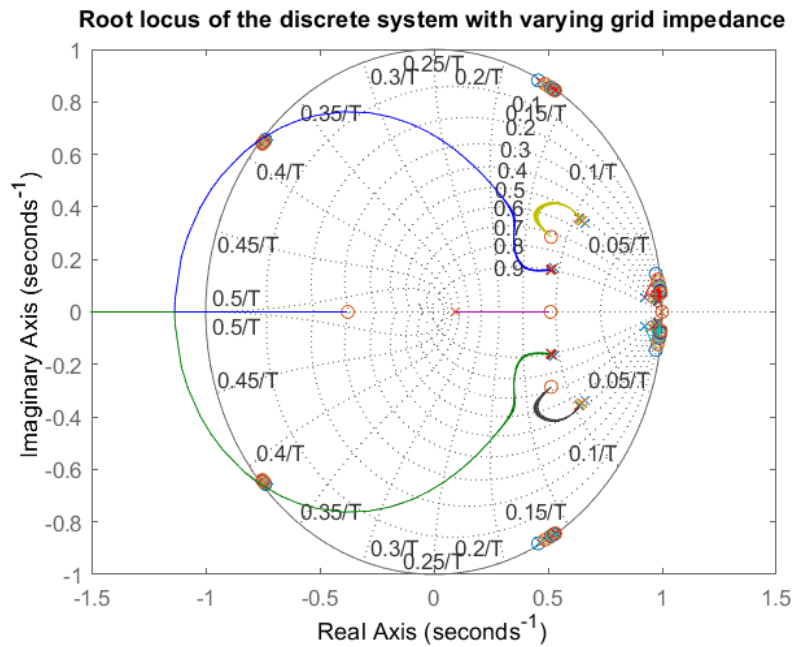


Figure 3.38: Root locus plot of the system with varying grid impedance

Figure 3.38 depicts the root locus plot. The locations of poles of the system and how it's affecting the performance of the system with varying grid inductance.

According to Table 3.3, the system with low grid inductance has a lower settling time and less overshoot, whereas the system with high grid inductance has a higher overshoot and higher settling time.

Grid Inductance (L_g) (μH)	Settling time (ms)	Overshoot (%)
100	0.604	1.5
300	2.14	14.4
500	3.66	21.7

Table 3.9: Performance of system with different grid inductances with root locus method

With this investigation, the system is stable with varying grid impedance of the system.

3.4.3.3 Varying system parameters

The goal is to see if the controller is stable when the parameters change. The fluctuation of nominal values to extreme values -20 % and +20 %. The effects of performance specification are investigated in this section. Within this range, the system's overshoot is less than 10 %.

Variation (%) w.r.t nominal values	Settling time (ms)	Overshoot (%)
-20	1.08	8.76
Nominal values	1.13	5.48
+20	1.13	3.03

Table 3.10: Performance of the system with varying system parameters with PI root locus method

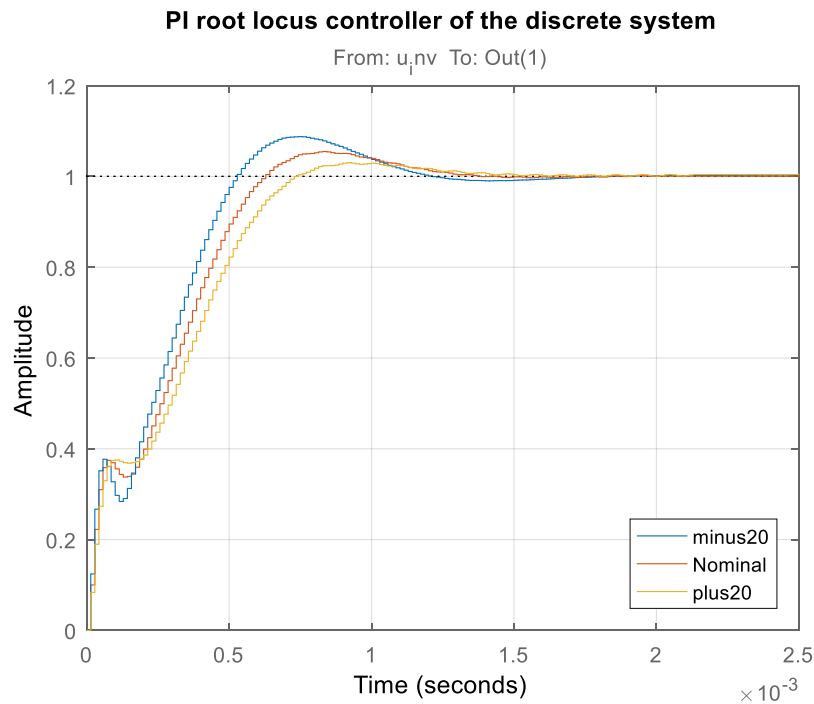


Figure 3.39: Step response of the system with varying system parameters

It has been demonstrated in this study that altering the nominal parameters of the system within the range of -20 % to +20 % with the same controller results in better system performance. The settling time is almost the same in the entire region.

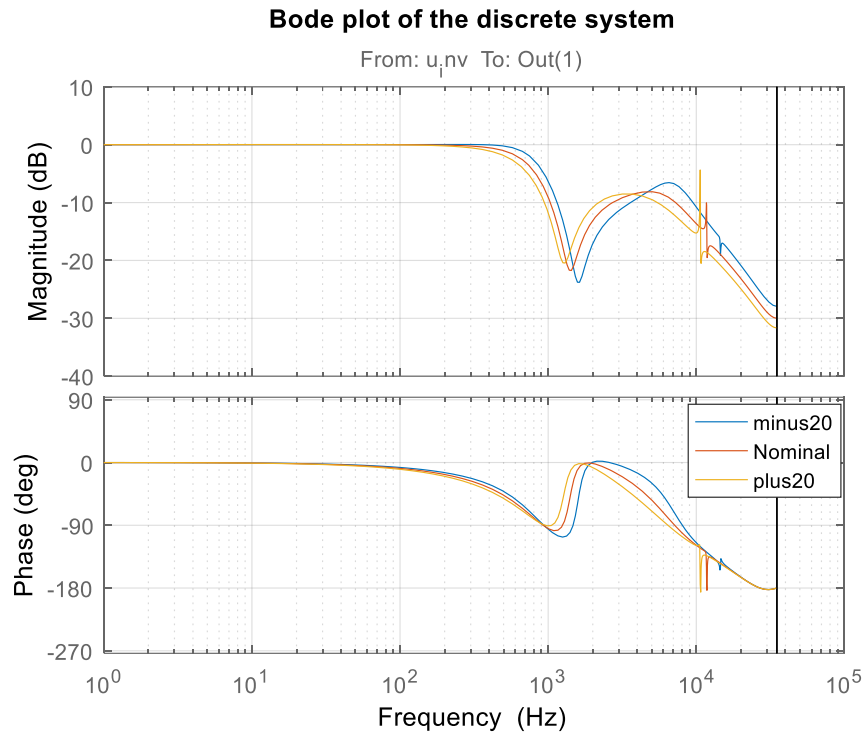


Figure 3.40: Bode plot of the system with varying systems parameters

Variation (%) w.r.t nominal values	Gain margin (dB)	Phase margin (°)
-20	25.3	152
Nominal values	11.1	173
+20	4.6	173

Table 3.11: Minimum stability of the system with varying system parameters

From Figure 3.40, the minimum stability margin of the system is depicted in Table 3.11. With varying system parameters, the system is stable, however, there is a change in the stability margin of the system.

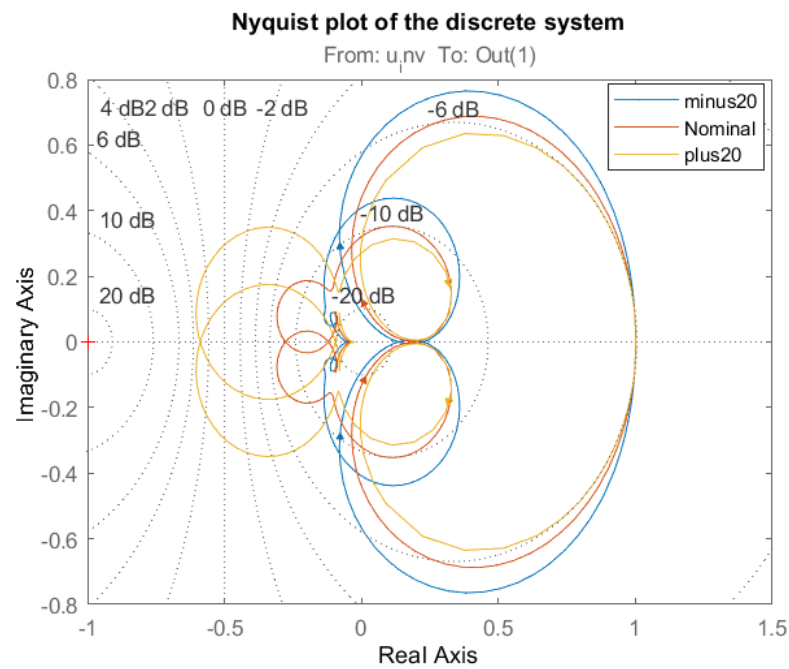
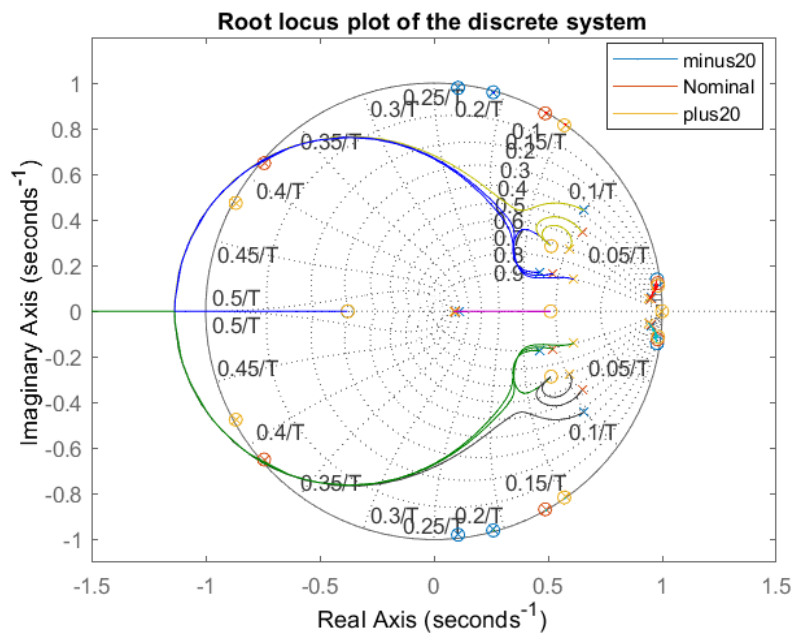


Figure 3.41 shows the Nyquist plot of the system doesn't encircle $(-1,0)$, which means the system is stable. However, the change in the stability margin of the system is shown in the bode plot in Figure 3.38.



In Figure 3.42, the change in location of poles is observed with a change in system parameters. With this investigation, the system is stable with varying system parameters.

4 Comparison and Investigation

4.1 Comparison of PI Symmetrical Optimum and Root Locus methods

In this chapter, the comparison of two PI controller tuning methods is shown. The performance specification of the system in the time domain and phase margin and gain margin of the system in the frequency domain. Change in location of the poles with PI SO and PI Root Locus.

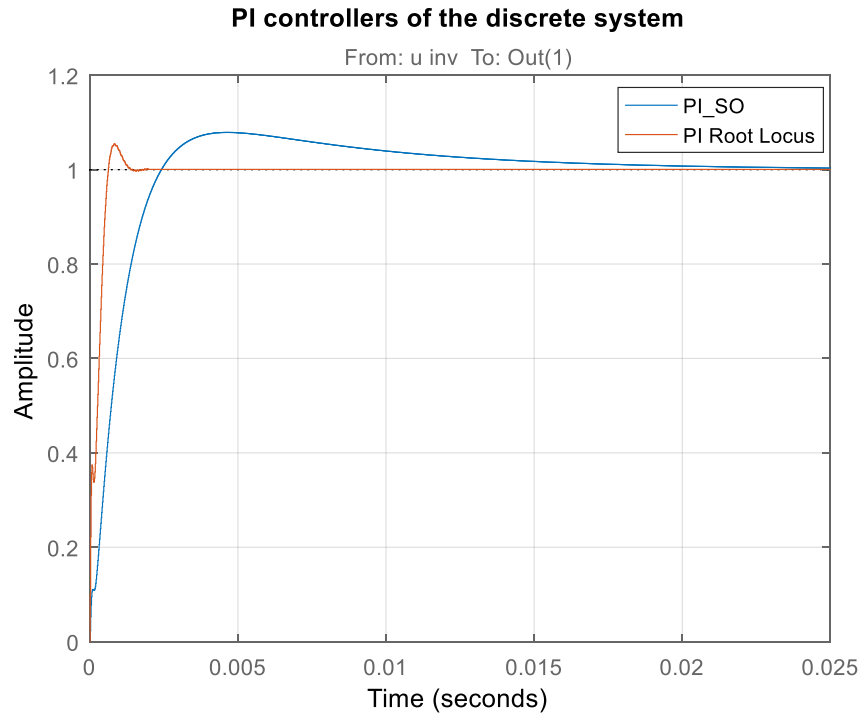


Figure 4.1: Step response of the system with two different controllers

The root locus approach of PI control outperforms the PI SO method in terms of system performance. In Figure 4.1, the system's overshoot is 5.48 % with root locus and 7.88 % with SO. The system with root locus has a settling time of 1.13 ms, while the SO has a settling time of 14.2 ms. The PI root locus method provides a faster settling time for the system.

In Figure 4.2, the root locus plot of the two controllers is plotted. The change in the location of the poles of the systems with different controllers is observed. Symmetrical optimum provides different pole locations of the system compared to the root locus method

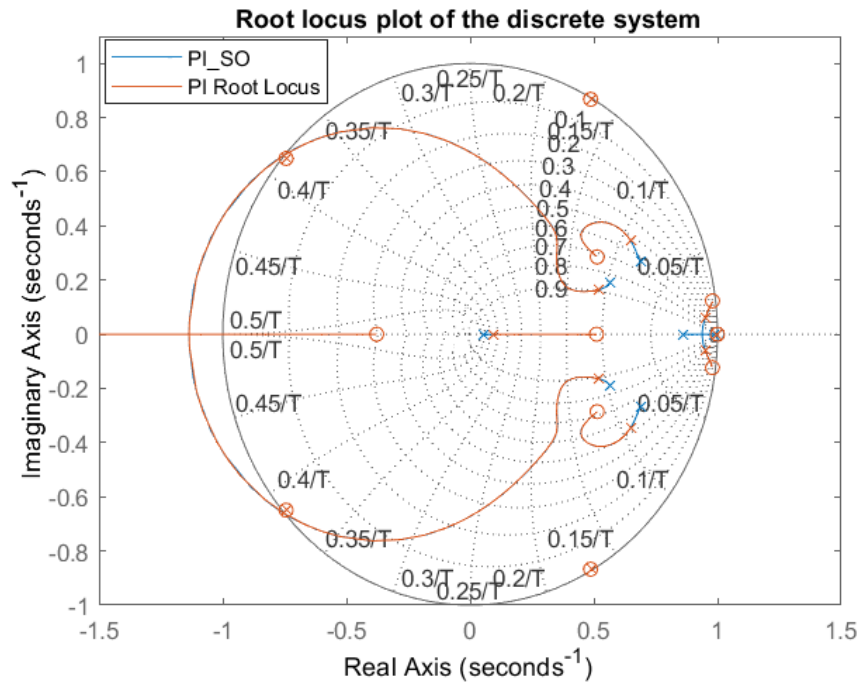


Figure 4.2: Root locus plot of the system with two different controllers

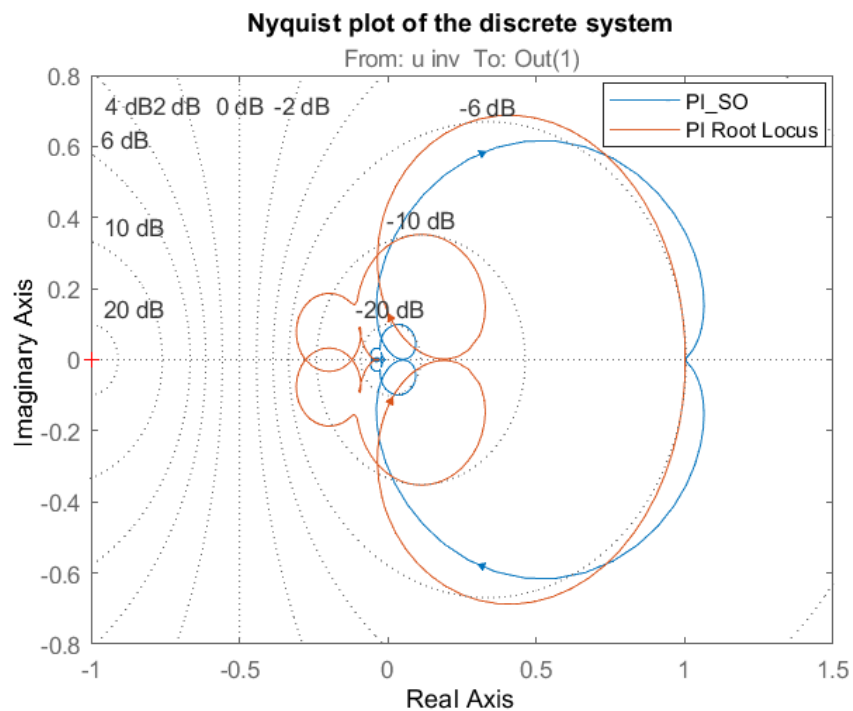


Figure 4.3: Nyquist plot of the system with two different controllers

From Figure 4.3, the minimum stability of the systems with the PI SO method with a gain margin of 25.6 dB and a phase margin of 150°. With the PI root locus method, the gain margin of the system is 11.1 dB with a phase margin of 173. The Nyquist plot tells the stability of the system with two different controllers.

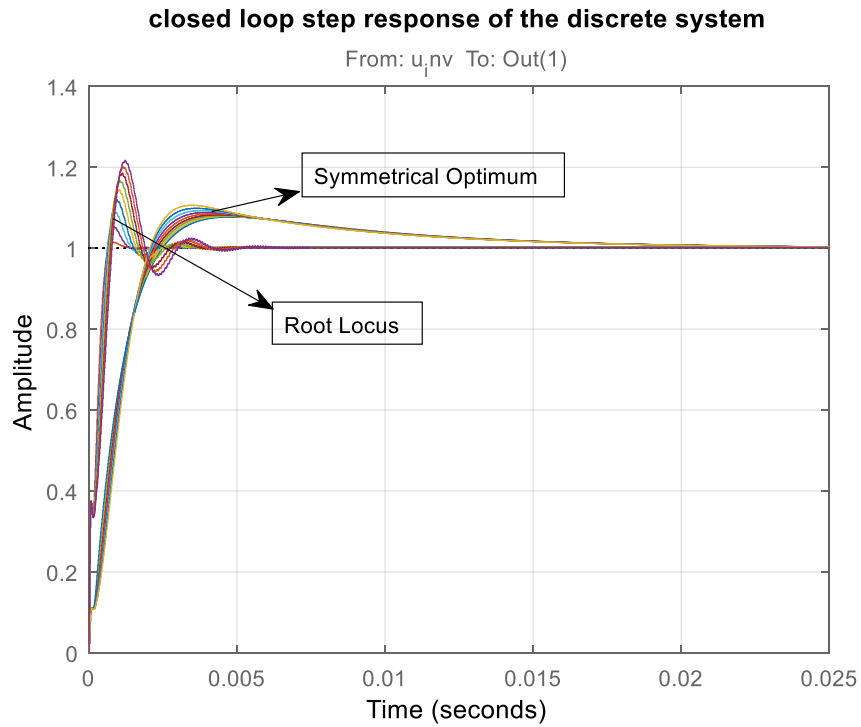


Figure 4.4: Comparison of step response of the system with varying grid impedance

Figure 4.4 shows the step response of the system with two different controllers with varying grid impedance. The system's overshoot is smaller with PI SO than with the PI root locus approach, but the settling time is significantly faster with the PI root locus method. The PI SO method has a maximum overshoot of 10.6 % and a settling time of 13.8 ms, whereas the system has a maximum overshoot of 21.7 % and a settling time of 3.66 ms at 500 μH . With the PI SO approach, the system's minimum overshoot is 7.72 %, and the settling time is 14.2 ms at 100 μH . The system's minimal overshoot is 1.5 % with a settling time of 0.6 ms when using the PI root locus approach. With a settling time of 14ms, the system overshoots by 8.54 % at 300 μH using the PI SO technique. The overshoot of the system using the PI root locus approach is 14.4 % with a settling time of 2.14 ms.

Rg 300 m Ω and Lg 150 μH are the system's chosen grid impedances. With PI SO, the system overshoot is 7.88 % and the settling time is 14.2 ms. The overshoot of the system using the PI root locus approach is 5.48 % with a settling time of 1.13 ms. It is observed that the settling time of the system is much faster with the root locus method. The PI root locus approach performs better than the PI SO method for these grid impedance settings.

comparision of PI SO and root locus controllers of the discrete system

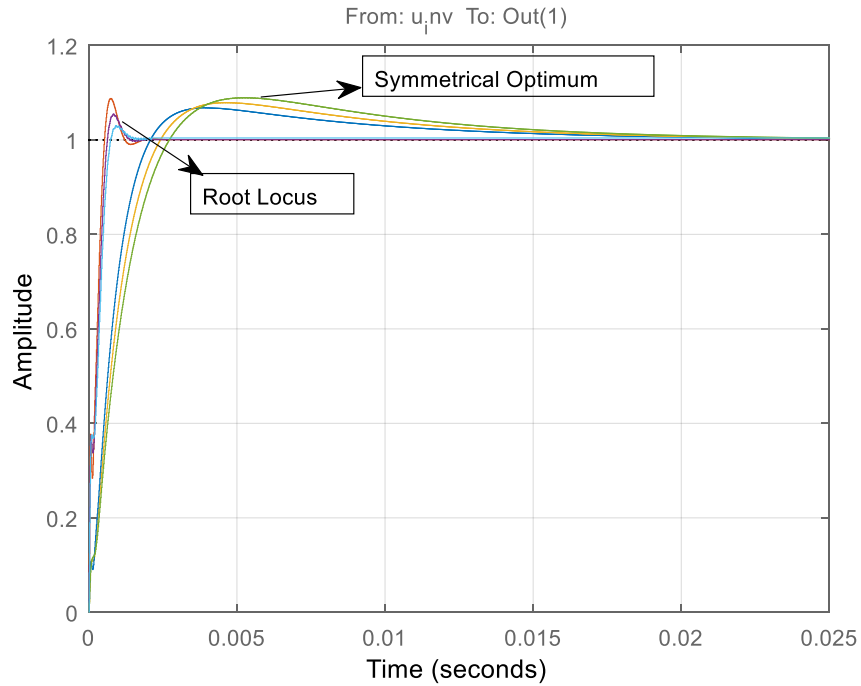


Figure 4.5: Comparison of step response with varying system parameters

With this step response in Figure 4.5, the root locus approach produces the best system performance, with a settling time of 1ms to 1.2 ms and an overshoot of less than 10 % in each situation. While SO's overshoot is similar to that of the root locus approach, the settling time varies greatly. It takes between 12.5 ms to 15.5 ms.

The settling time of the system is very fast even in changing the system parameters in a wide range. The system performs best with the PI control root locus approach.

4.2 Comparison of SS model with Simulink model

The Simulink model in Figure 4.6, represents the single-phase LC+EMI filter. The state-space representation derived in chapter 3.2.2 is for this circuit. This is to verify if the state-space model of the system and the Simulink model give the same step response of the filter or not.

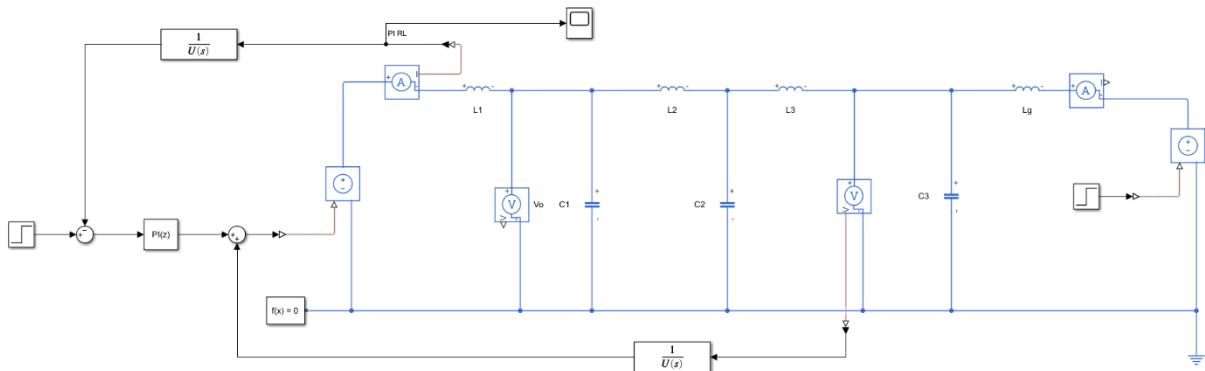


Figure 4.6: Simulink model of a single-phase filter

In Figure 4.7, the system's overshoot is 5.48 % with root locus and 7.88 % with SO. The system with root locus has a settling time of 1.13 ms, while the SO has a settling time of 14.2 ms. This shows that state-space and the Simulink model give the same results and it's verified.

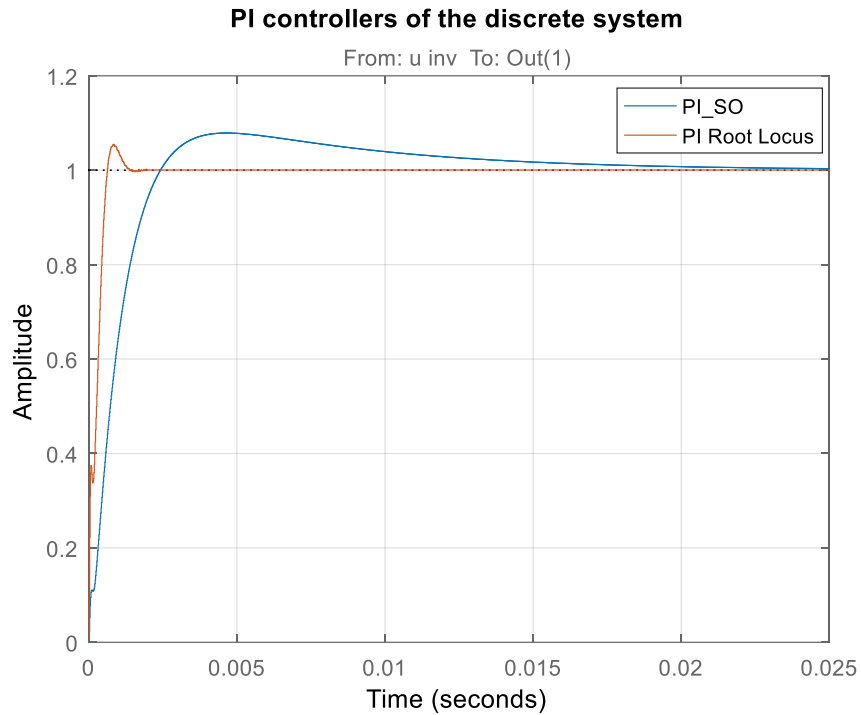


Figure 4.7: Simulink model step response of the LC+EMI

4.3 Comparison of a first-order filter and third-order Bessel filter

4.3.1 First-order Bessel filter with 35 kHz

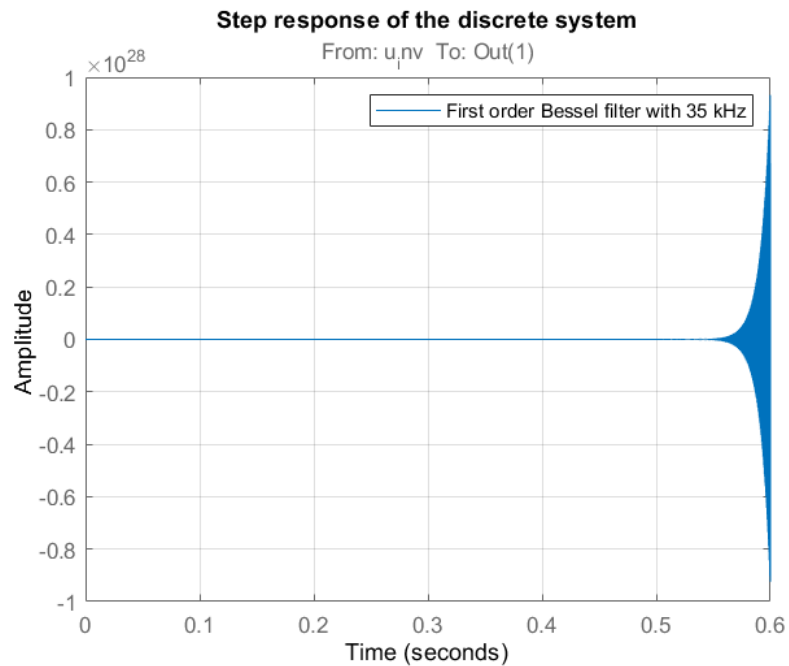


Figure 4.8: Step response of a first-order Bessel filter with 35 kHz

Figure 4.8 depicts the unstable system with a first-order Bessel filter with 35 kHz. To make the system stable, want to increase the order of the system and by decreasing the cutoff frequency. This implementation is shown in the following sections.

4.3.2 First-order filter with 35 kHz cut-off frequency and third-order Bessel filter with 6 kHz cut-off frequency

A comparison of a first-order filter with a cut-off frequency of 35 kHz to a third-order filter with a cut-off frequency of 6 kHz is presented in this section. The system's behavior is examined using two distinct voltage measurement filters.

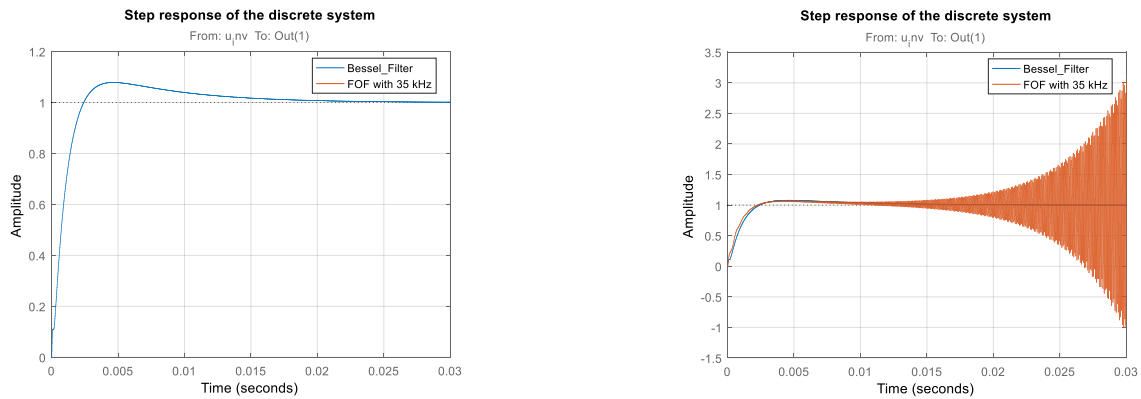


Figure 4.9: Step response of the system with two different voltage measurement filters

In Figure 4.9, the system with a third-order Bessel filter is stable and the system with a first-order filter is unstable because the pole is outside the unit circle and has negative damping.

The system's natural frequency is 11.74563 kHz with a Bessel filter and 12.239 kHz with a first-order filter. The system's negative damping is evident in Figure 4.10, resulting in an unbounded response. The damping ratio of the system affects the step response of the system, as shown in table 4.1.

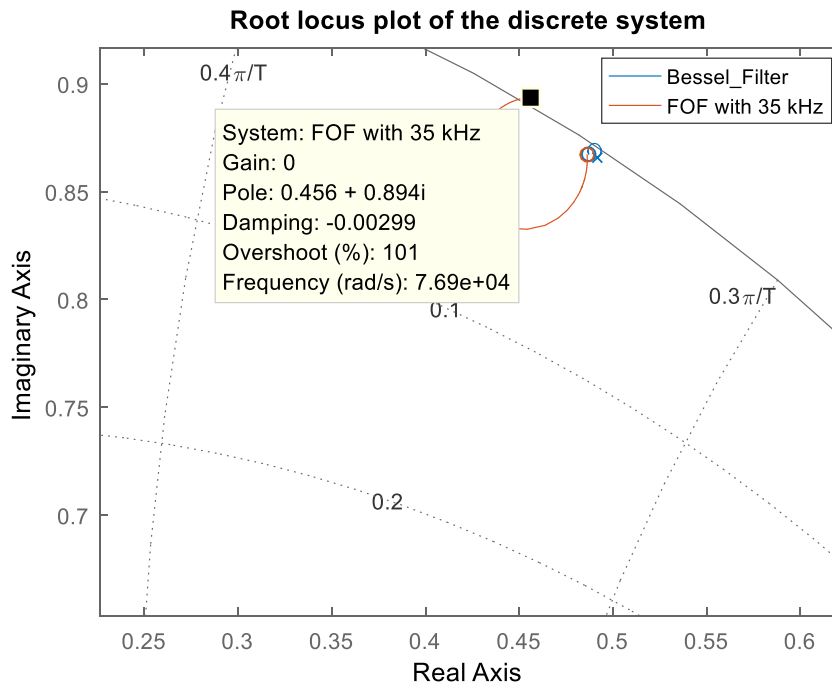


Figure 4.10: Zoomed PZ map of the system

Case	Damping Ratio	Eigenvalues	Unit Step Response
Overdamped	$\xi > 1$	Real and distinct	Slowest transient response
Critically damped	$\xi = 1$	Real and equal	Faster transient response without overshoot
Underdamped	$0 < \xi < 1$	Complex conjugate pair	Faster transient response but with overshoot and oscillation
Undamped	$\xi = 0$	Imaginary pair	Undamped oscillations
Unstable	$\xi < 0$	At least one with a positive real part	Unbounded response

Table 4.1: Damping ratio affects the step response

Changing the pole location and tweaking the control parameters with the Control System Designer toolbox. Using the gain of the system to identify the new controller parameters of the system by adjusting the pole with negative damping and bringing it inside the unit circle based on the overshoot and settling time. Figure 4.11 depicts the tuned controller's step response, whereas Figure 4.12 depicts the system's change in pole placements. The system has a 9.4 % overshoot and a settling time of 1.32 ms. However, the untuned system is unstable.

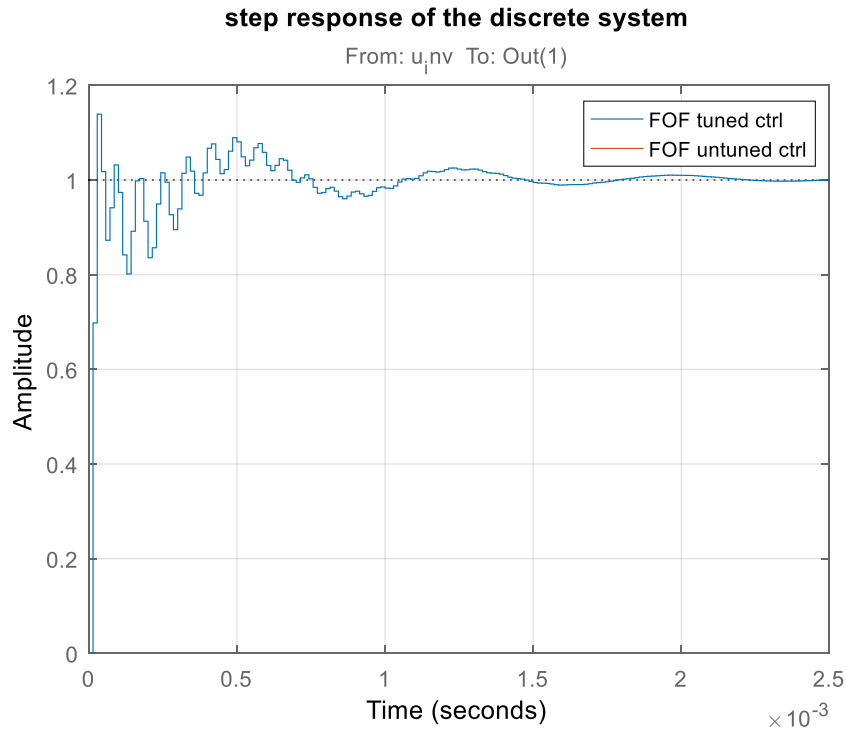


Figure 4.11: Step response of the system with tuned controller

The change in pole location of the system makes the system stable and the natural frequency of the system is 12.3822 kHz.

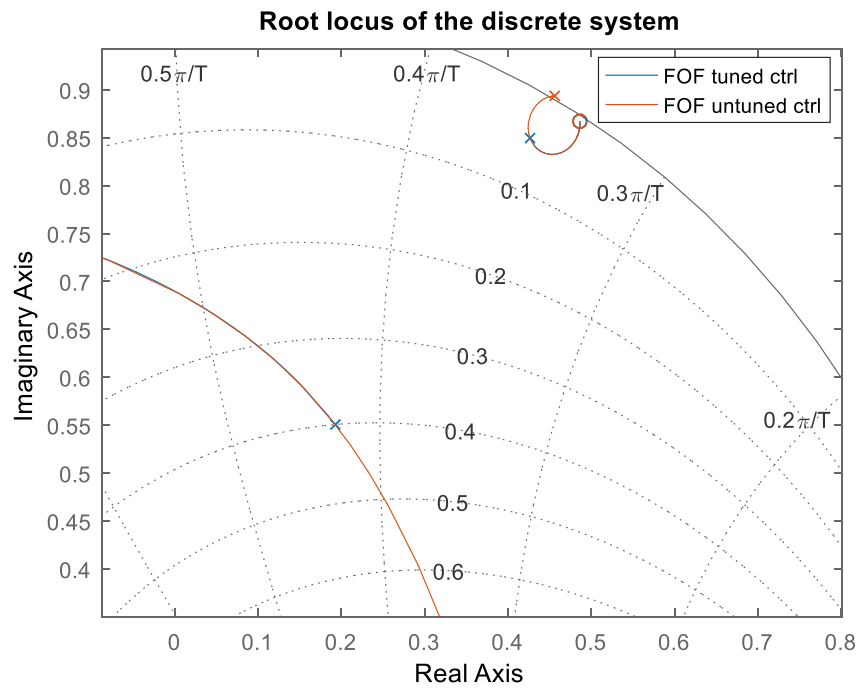


Figure 4.12: Change in pole location of the system

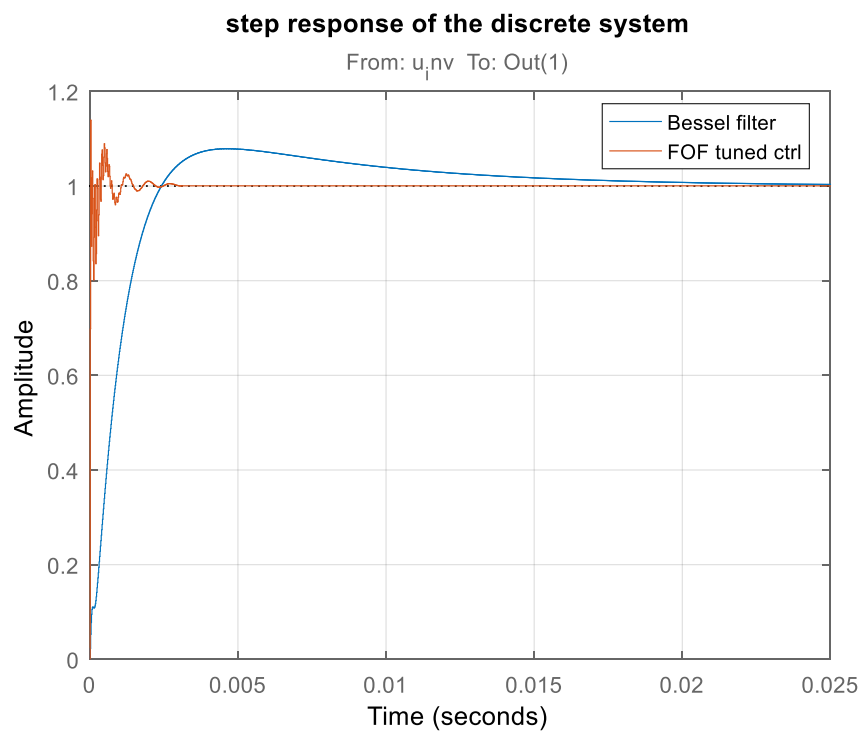


Figure 4.13: Step response of the system with a first-order filter with 35 kHz and Bessel filter

In Figure 4.13, the step response of the system with a Bessel filter and first-order filter with a tuned controller is plotted.

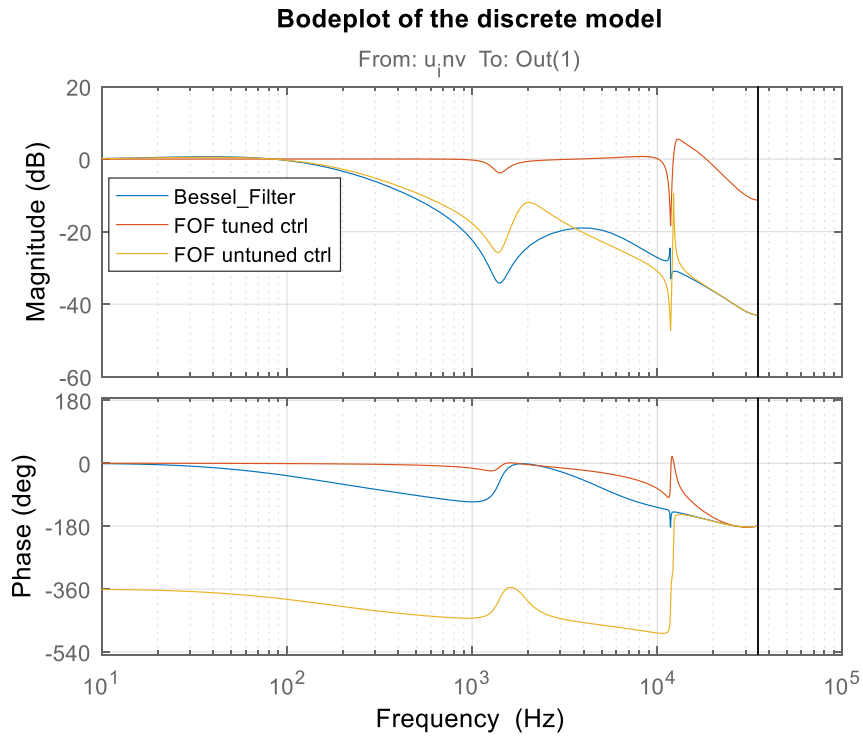


Figure 4.14: Bode of the different voltage measurement filters

In Figure 4.14, the bode plot of the system is shown and the change in Phase is observed in the first-order filter with 35 kHz with a tuned and untuned controller.

4.3.3 First-order filter with 6 kHz cut-off frequency and third-order Bessel filter with 6 kHz cut-off frequency

A comparison of a first-order filter with a cut-off frequency of 6 kHz to a third-order filter with a cut-off frequency of 6 kHz is presented in this section. The system's behavior is examined using two distinct voltage measurement filters.

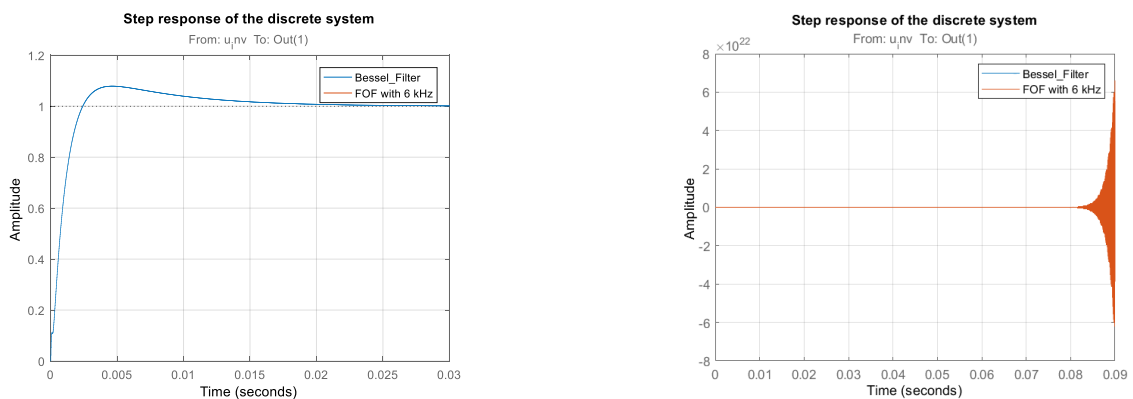


Figure 4.15: Step response of the system with two different voltage measurement filters

In Figure 4.15, the system with a third-order Bessel filter is stable and the system with a first-order filter is unstable because the pole is outside the unit circle and has negative damping.

The system's natural frequency is 11.74563 kHz with a Bessel filter and 11.96845 kHz with a first-order filter. The system's negative damping is evident in Figure 4.16, resulting in an unbounded response.

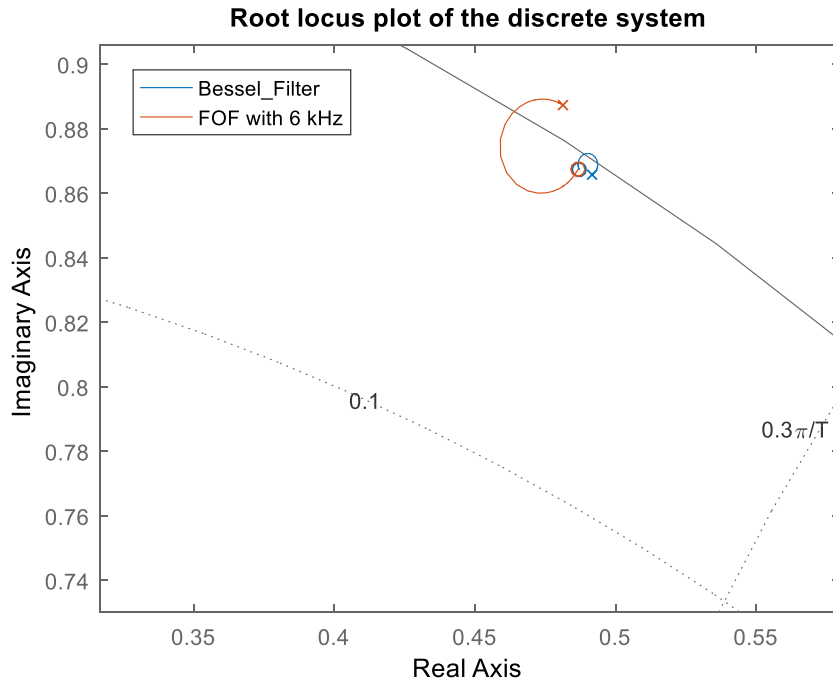


Figure 4.16: Zoomed PZ map of the system

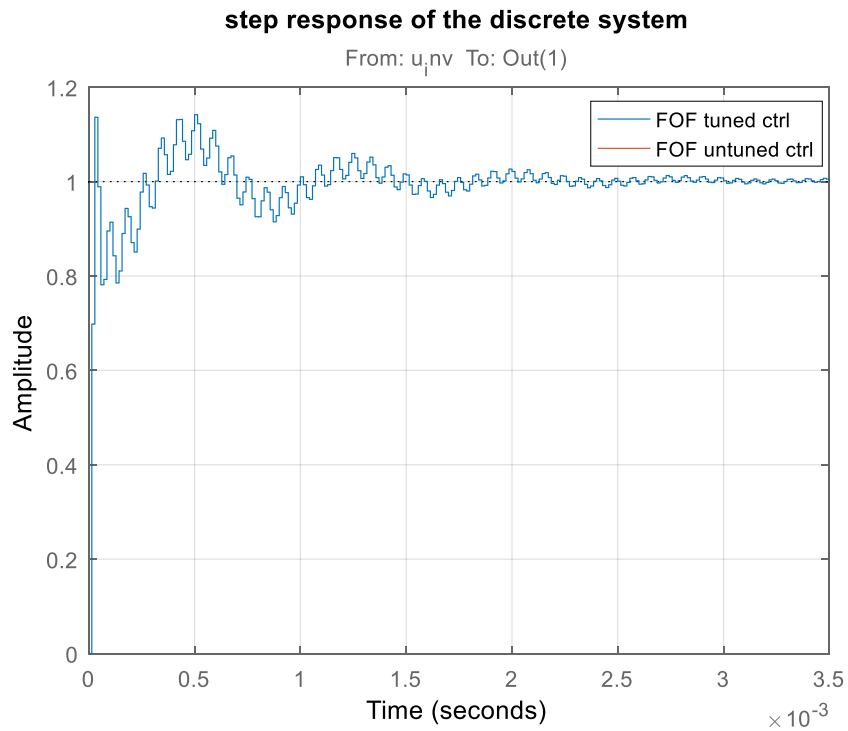


Figure 4.17: Step response of the system with tuned controller

FOF tuned ctrl in the legend represents the tuning of the system with the methodology depicted in Figure 3.33 using the root locus method. This uses the new control parameters. FOF untuned ctrl represents the system with the root locus method.

Changing the pole location and tweaking the control parameters with the Control System Designer toolbox. Using the gain of the system to identify the new controller parameters of the system by adjusting the pole with negative damping and bringing it inside the unit circle based on the overshoot and the settling time. Figure 4.17 depicts the tuned controller's step response. The system has a 14.2 % overshoot and a settling time of 2.08 ms. whereas Figure 4.18 depicts the system's change in pole location. The change in pole location of the system makes the system stable.

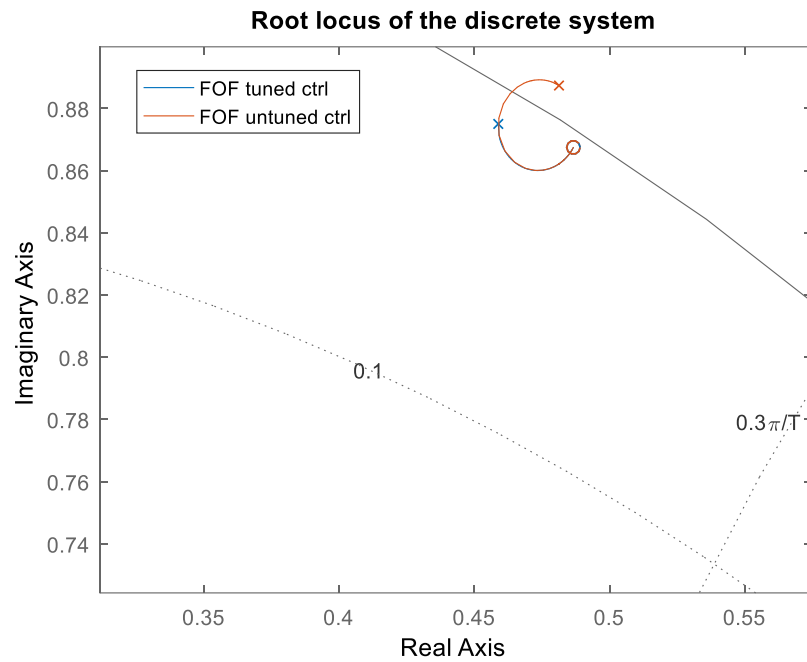


Figure 4.18: Pole-Zero map of the system with tuned and untuned controller

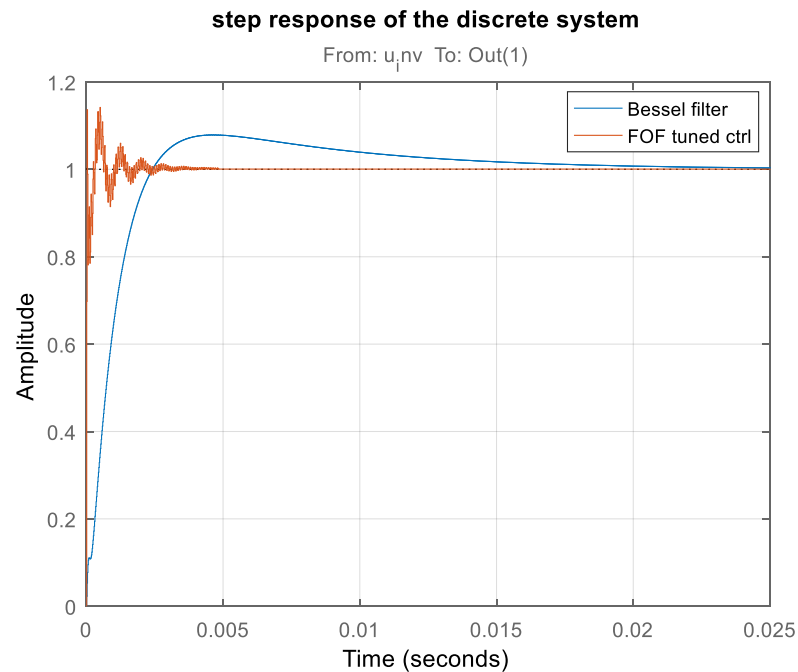


Figure 4.19: Step response of the system with a first-order filter with 6 kHz and Bessel filter

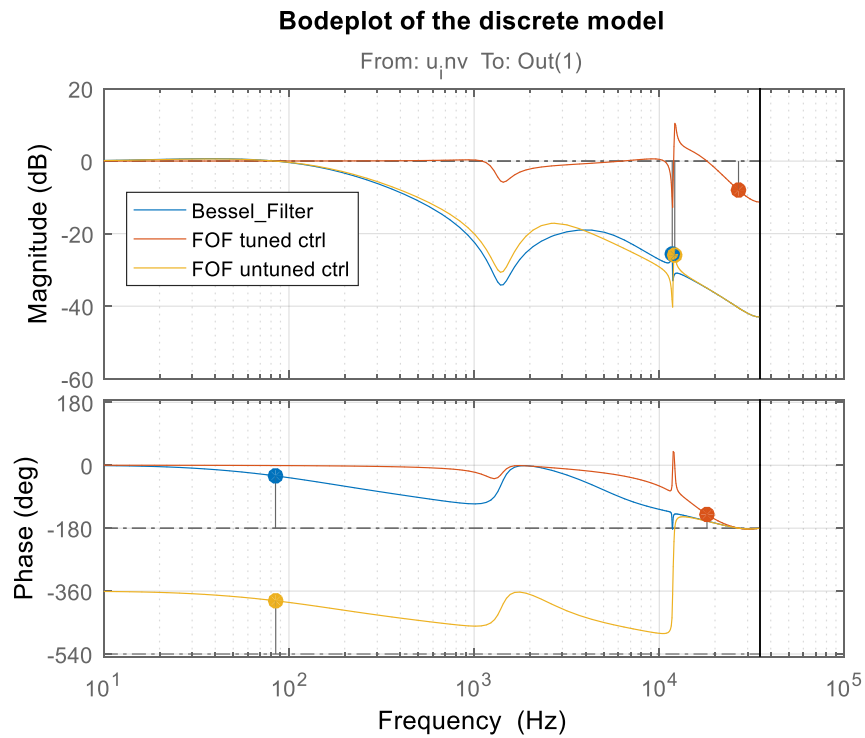


Figure 4.20: Bode of the different voltage measurement filters

In Figure 4.20, the bode plot of the system is shown and the change in Phase is observed in the first-order filter with 35 kHz with a tuned and untuned controller.

As observed in the simulation results with different filters, the third-order Bessel filter with 6 kHz gives better performance than the other filters.

5 Modeling and Simulation of 3-Phase, 3-Level ANPC

5.1 Simulation of power converters

Advantages of the simulation of power electronic converters are:

- Provides a forecast of the system performances without the expensive circuitry instruments.
- Gives performance analysis with varying conditions such as DC bus voltage, system parameters, grid impedance, etc.
- Predict the dynamic behavior of the system.

These are a few of the many advantages of simulation.

In power electronic converters there are two types of Simulations.

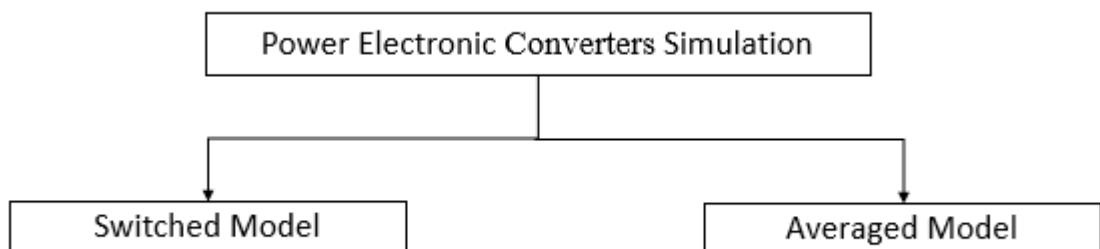


Figure 5.1: Types of PEC Simulations

5.1.1 Switched model

There is wide use of switched models in PEC. Circuits are simulated by switches such as IGBTs, MOSFETs, diodes, etc.

In addition to the dynamic response of a converter, it provides cycle-to-cycle variations in current and voltage.

Switched models provide a detailed analysis of circuit cycle-to-cycle variation, which is a significant advantage.

A major disadvantage of the system is its long simulation time.

5.1.2 Averaged model

The averaged model is based on circuit modeling, which means that the voltage and current are averaged.

Simulating this way is not time-consuming, yet it gives important information.

5.2 Averaged model of the 3-phase, 3-level ANPC

By using this model, grid-connected converters will be simulated faster and with less complexity while maintaining sufficient dynamic accuracy.

Description of the implemented model

- In this model, the average V-I terminal relationship on the AC side and the DC side is the same as if it were a fully switched model.

- It is possible to simulate time steps larger than the switching period since the switches are not modeled.
- Control circuit modeling is similar to that of a full switched model, except that gate pulse generation is not modeled.
- There is no way to use this model to analyze the effects of switching frequency and ripple phenomena.

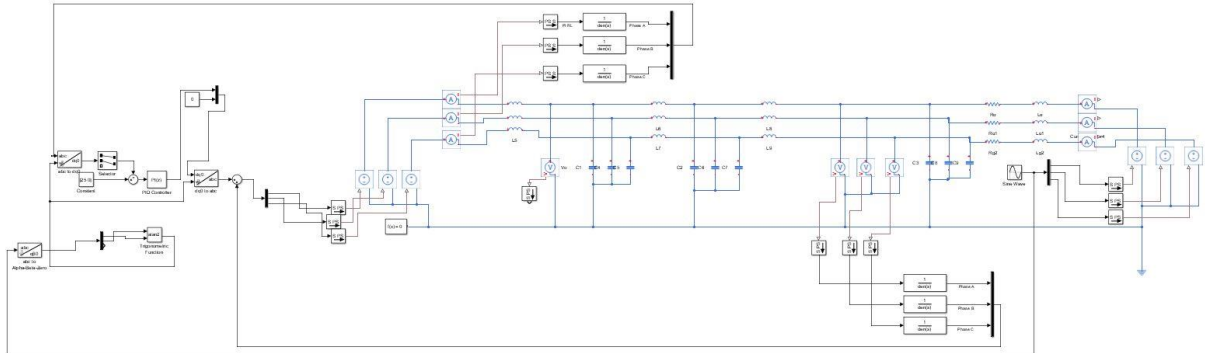


Figure 5.2: An averaged model of the converter

Figure 5.2 shows the averaged model of the converter modeled in Simulink.

In Figures 5.3, 5.4, and 5.5, the black line represents Phase A, the red line represents Phase B, and the blue line represents Phase C.

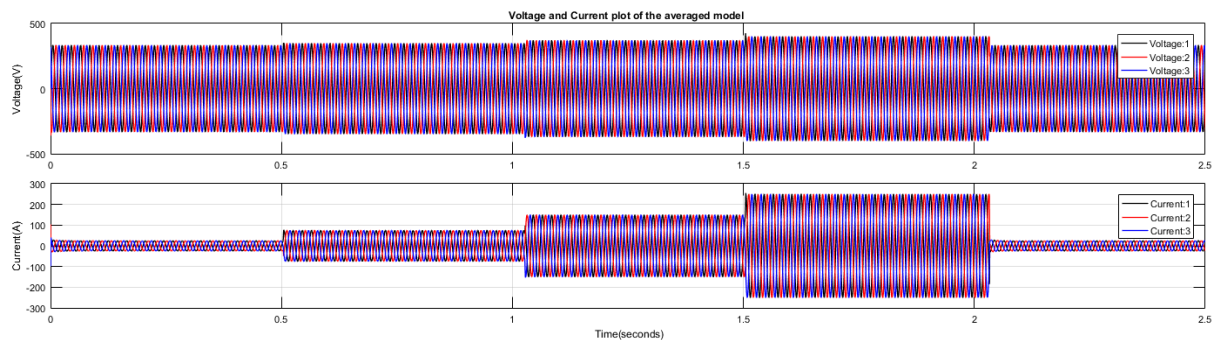


Figure 5.3: Voltage and Current of the averaged model with varying current set point

Figure 5.3 illustrates the voltage and current plot of the averaged model over time with a variable reference current. When the reference current is varied, the current and voltage of the system immediately change.

The reference current is 25 A from 0 s and 0.5 s, 75 A between 0.5 s and 1.1 s, 150 A between 1.2 s and 1.5 s, 250 A between 1.5 s and 2.1 s, and lastly 25 A between 2.1 s and 2.5 s. With these adjustments in the reference current of the system, the system adjusts quickly to changes in the current parameter and adapts swiftly with the control parameters that are determined using the root locus approach.

Figures 5.4 and 5.5 depict the system's behavior when the reference current is changed. As observed in both figures, the plots are highlighted in the rectangles where the change in the system takes place but adapts to the changes in the system quickly.

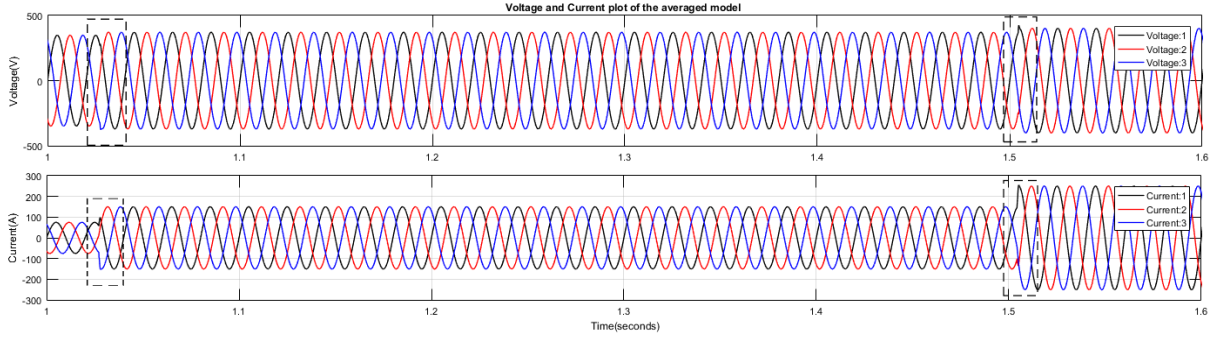


Figure 5.4: The behavior of the system at the time of change in set point

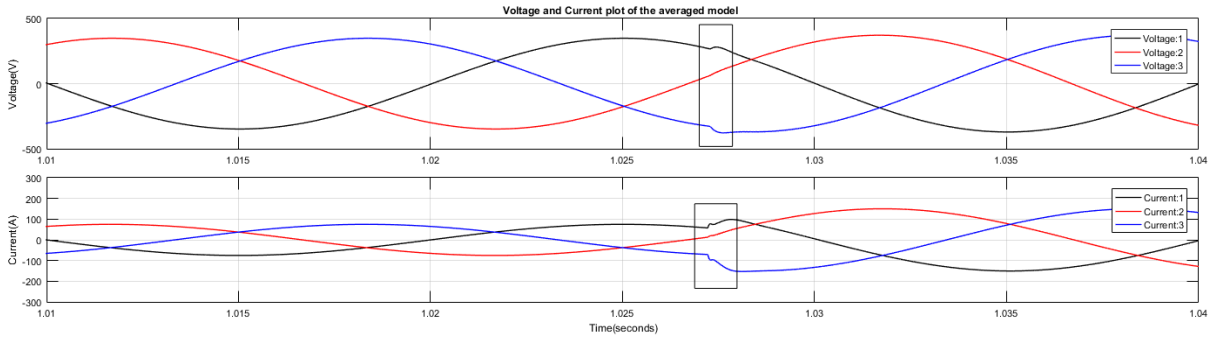


Figure 5.5: The behavior of the system at the time of change in set point

This shows that the control parameters determined with the help of a single-phase state-space model of the LC+EMI filter are valid and give good results with the averaged model of the converter.

5.3 Current control of the 3-phase, 3-level ANPC inverter (Switched model)

Controlling a three-phase inverter is one of the most significant and classic topics in power electronics, and it was intensively researched in the late 2000s [58].

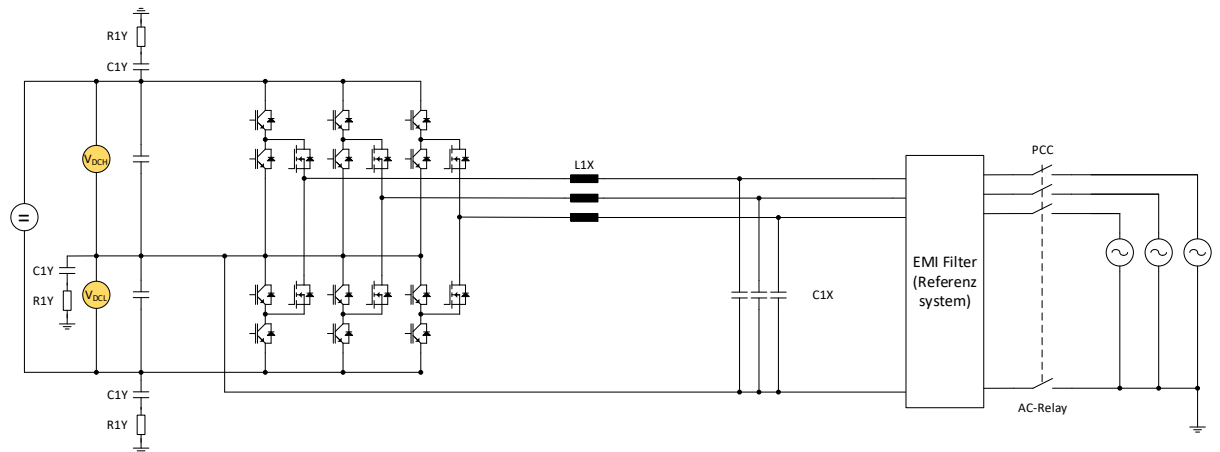


Figure 5.6: 3-phase, 3-level ANPC with LC+EMI filter and grid connection

Figure 5.6 shows the overall topology of the inverter.

inverter current can be used for the implementation. In this thesis, the inverter side current is used. The signal in the abc frame must first be translated to $\alpha\beta$ coordinates using Clark's transformation method before being converted to the dq frame using Park's transformation matrix and the expression (5.3.1). Two decoupled PI controllers are then used to control the active and reactive currents.

$$[x_{\alpha\beta}] = T^{-1}_{dq}[x_{dq}], \quad T^{-1}_{dq} = \begin{bmatrix} \sin(\omega_0 t) & -\cos(\omega_0 t) \\ \cos(\omega_0 t) & \sin(\omega_0 t) \end{bmatrix} \quad (5.3.1)$$

The normalized output of the PI controller is subjected to inverse Clark and park transformation (5.3.2). to generate the reference signals for the PWM controller [66].

$$[x_{abc}] = T^{-1}_{\alpha\beta}[x_{\alpha\beta}], \quad T^{-1}_{\alpha\beta} = \begin{bmatrix} 1 & 0 & 0 \\ -1 & \frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \end{bmatrix} \quad (5.3.2)$$

5.3.1.2 Grid Connection

The grid connection is based on the SCC with PLL is studied in this thesis. The PLL is added to provide the reference angle for the rotating frame. The overall setup of the power converter is shown in Figure 5.7 and the synchronous dq transformation of load current is shown in Figure 5.8.

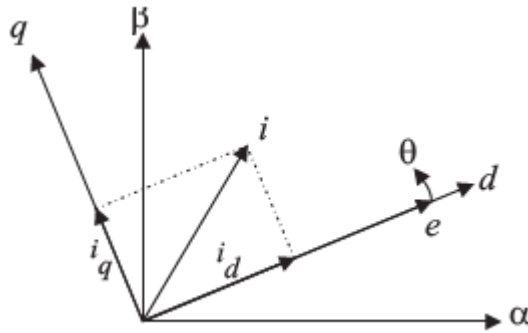


Figure 5.8: Synchronous dq transformation of load current

5.3.2 Phase-locked loop for 3-phase grid-connected inverter

PLL is used to generate the signal and the signal is used as a reference for the implementation of a current controller in a grid-connected inverter.

Voltages V_{abc} are converted to $\alpha\beta$ coordinates from the abc frame using Clark's transformation method, and then to the dq frame using Park's transformation. The voltages on the d- and q-axes will now be non-zero. To make q equal to 0, a PI controller is employed. V_{qref} thus equals 0. An integral is given the output of the PI controller to determine ωt . This ωt is referred to as

the system's phase angle. The main issue with this approach is that, in crucial grid situations, it may result in an unstable system. Because the PLL output contains incorrect angle information, it cannot tolerate situations like harmonics, surge noise, and spikes. There is an alternative method for solving this kind of issue. This is discussed in the below section.

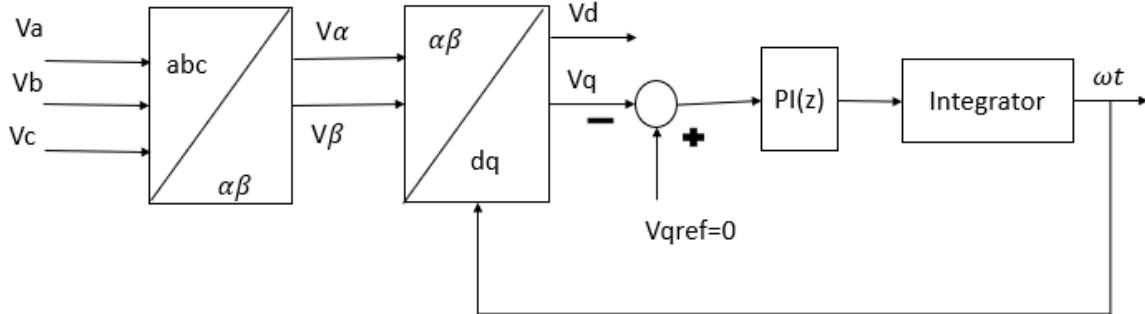


Figure 5.9: Phase-locked loop method

There are some advanced PLL implementations based on more complex controllers like Resonant controls e.g., a Second-Order-Generalized-Integrator (SOGI) or Kalman filters, that can even handle unbalanced grid voltages and offer good harmonics rejection. However, these topics are already well researched as in [67], [68], it will be not part of this thesis.

5.3.3 Proposed PWM Strategy

Two modulation schemes are the foundation of the PWM strategy suggested in this thesis. These two modulation techniques are based on a comparison between a triangle carrier at a high frequency (70 kHz) and a sinusoidal reference voltage V_{abcref} switching at a low frequency (50 Hz).

The ANPC converter consists of six active switches, S_1 - S_6 , connected according to Figure 5.10.

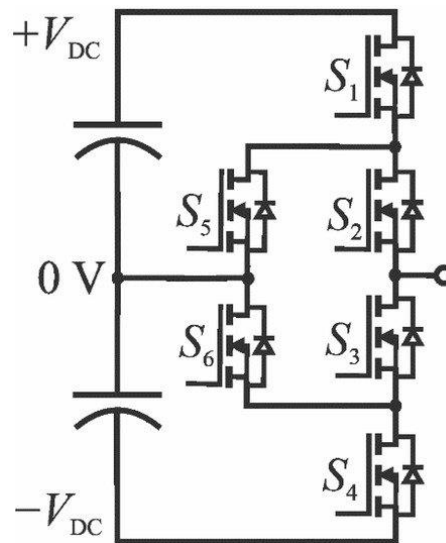


Figure 5.10: A single-phase leg of the ANPC converter

The switches S_1 and S_4 are complementary to each other and slow switches. S_5 and S_6 switches function similarly to S_4 and S_1 , respectively. The switches S_5 and S_6 are also complementary to

each other. These four switches operate at a 50 Hz frequency and switch slowly. Fast switching switches S_2 and S_3 are complementary to each other. They operate at a high frequency of 70 kHz. SiC MOSFETs are used for switches S_2 and S_3 , while IGBTs are used for the remaining switches. However, all six of the switches employed in the simulation are MOSFETs. because this thesis does not take switching losses into account.

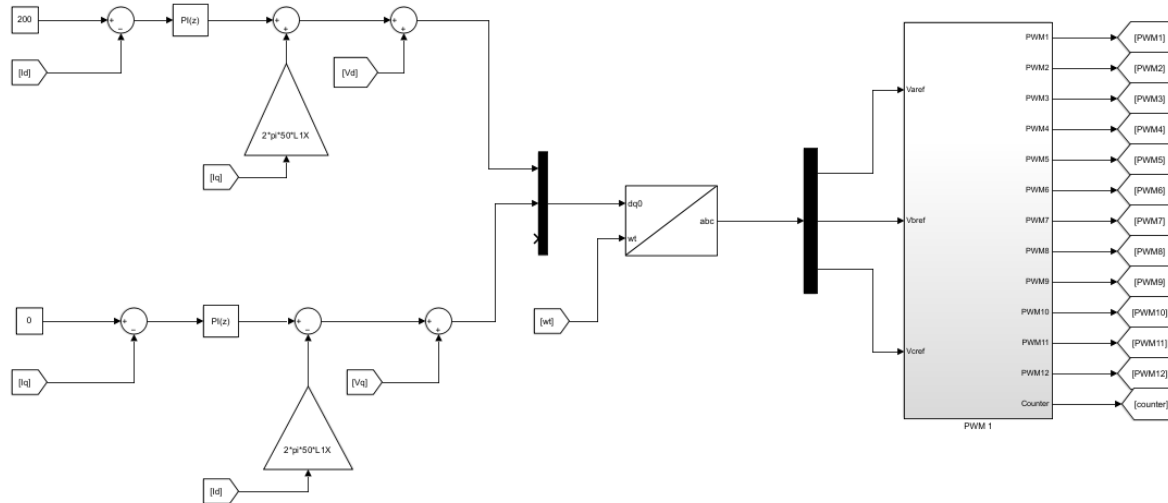


Figure 5.11: Control strategy and PWM generation block diagram

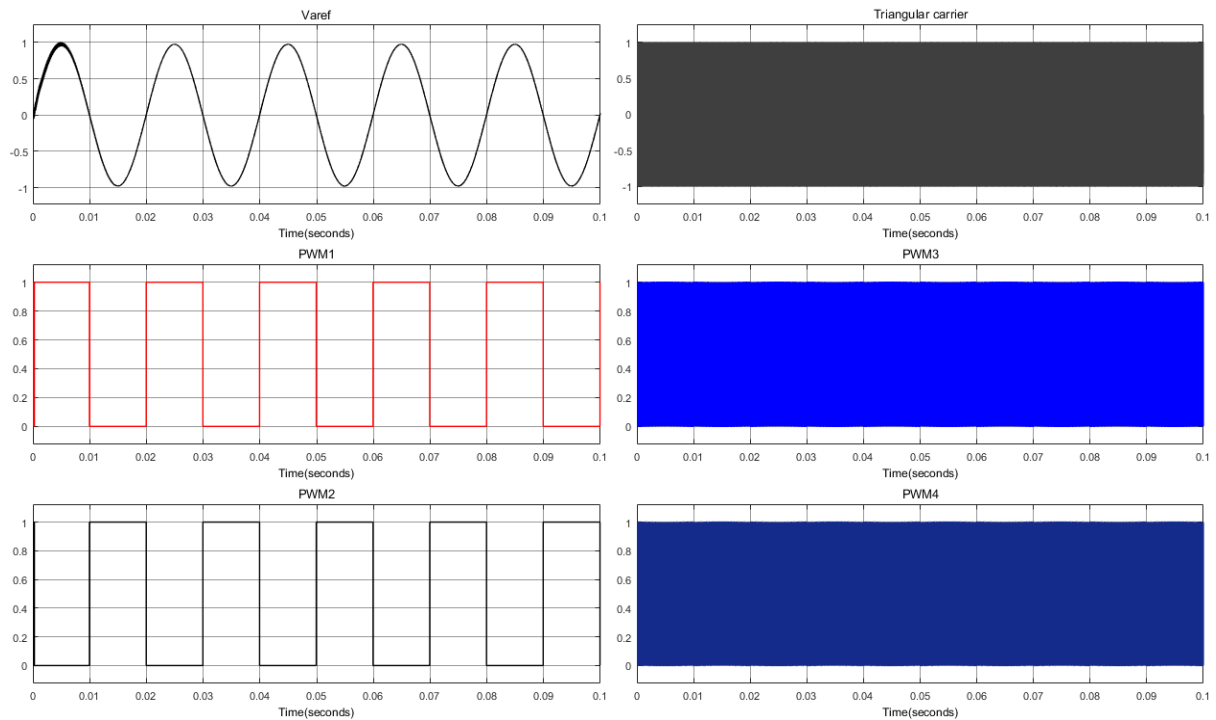


Figure 5.12: Principle and resulting gate signals of the PWM

As discussed above the gate signals are depicted in Figure 5.12. Vref, PWM1, and PWM2 are working at 50 Hz frequency. While the triangular carrier and the PWM3,4 are operating at a high frequency of 70 kHz. A zoomed-in gate signal of the triangular carrier, PWM3, and PWM4 is shown in Figure 5.13.

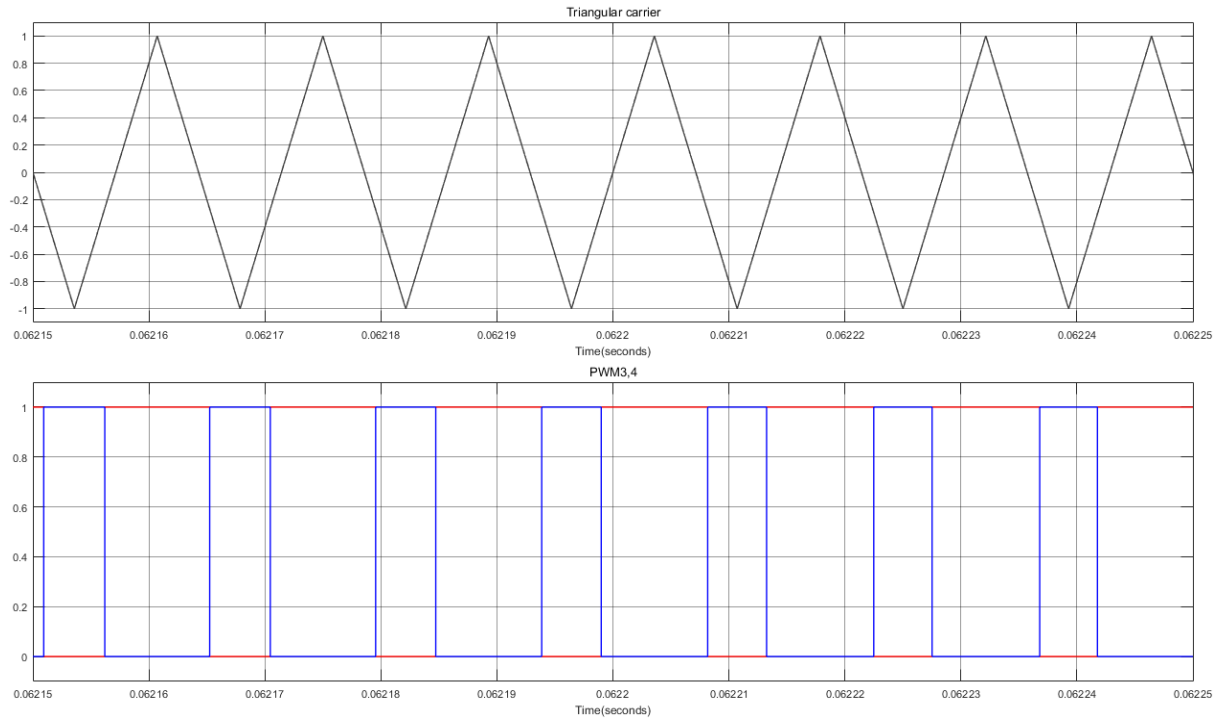


Figure 5.13: Resulting gate signals of the PWM3, 4

The simulation tests are performed on the Matlab/Simulink tools. The simulation parameters are presented in Table 5.1.

Parameter	Symbol	Value
Inductance 1X	L1X	32.5 μH
Capacitance 1X	C1X	60 μF
Capacitance 1Y	C1Y	10 nF
Resistance 1Y	R1Y	2.2 Ω
Capacitance 2Y	C2Y	100 nF
Inductance 2X	L2X	17.5 μH
Capacitance 2X	C2X	4.7 μF
Capacitance 3X	C3X	4.7 μF
Capacitance 4X	C4X	4.7 μF
Capacitance 3Y	C3Y	3.3 μF
Capacitance 4Y	C4Y	3.3 μF
Inductance CM1	L1CM	6.3 μH
Inductance CM2	L2CM	6.3 μH
Resistance 1Y	R1Y	200e3 Ω
Grid Resistance	Rg	300 m Ω
Grid Inductance	Lg	150 μH

DC link voltage	V _{dc}	800 V
Inverter switching frequency	f _{sw}	70 kHz
Sampling time	T _s	1/70000
Frequency	ω	50 Hz

Table 5.1: Simulation parameters

5.3.4 Simulation results

Simulation of the inverter system shown in Figure 5.6 is carried out with SCC and PLL, using Matlab/Simulink tools, to verify whether determined control parameters are giving good results are not. The parameters of the system are shown in table 5.1.

The amplitude of the reference current is set to 200 A, and the frequency is 50 Hz.

In Figures 5.14, 5.15, and 5.16, the black line represents Phase A, the red line represents Phase B, and the blue line represents Phase C in every simulation result.

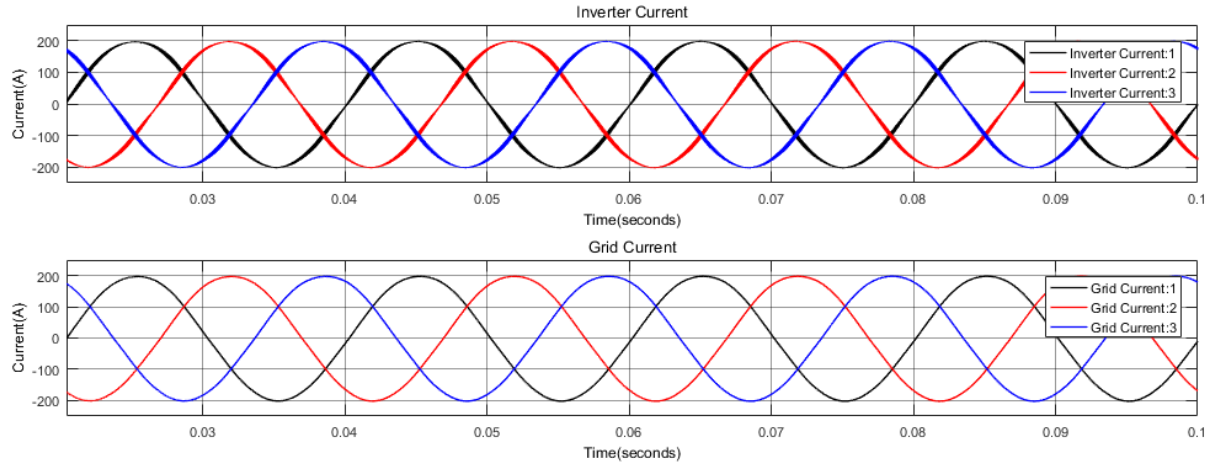


Figure 5.14: Simulation results: inverter current and grid current for a reference current of 200 A

Figure 5.14, shows that the grid current is sinusoidal with low distortions. However, the inverter current has a lot of aliasing effect. This aliasing effect can be overcome with the help of synchronous current sampling. A widely used technique today for current ripple suppression is sampling synchronization. It uses the fact that in the ideal case no ripple is present in the sampled current if the sampling is done at the peak or valley of the PWM carrier signal. This is discussed in the following section.

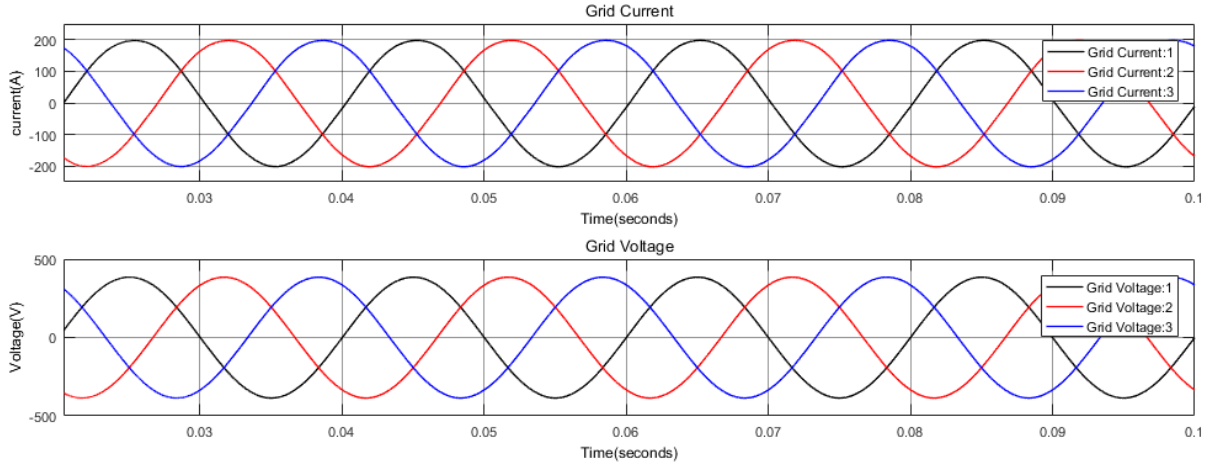


Figure 5.15: Simulation results: grid current and grid voltage for a reference current of 200 A

Similarly, Figure 5.16, shows that the grid voltage is sinusoidal with low distortions.

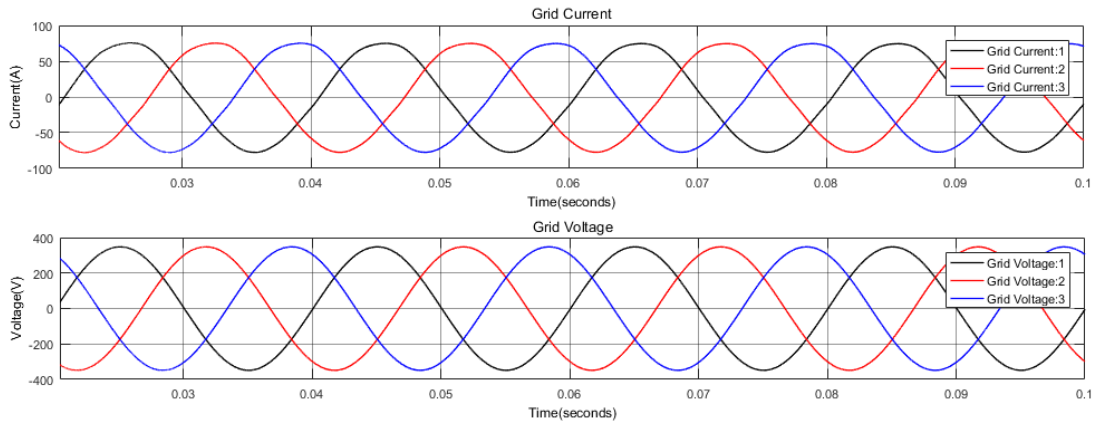


Figure 5.16: Simulation results: grid current and grid voltage for a reference current of 75 A

5.3.4.1 Implementation of synchronous current sampling

This reduction of continuous-time to a discrete-time signal is called sampling and some of the problems that can occur during this conversion process that deviate obtained signal from perfect reconstruction may include:

- Aliasing effect
- Jitter
- Noise
- Quantization

Inverters produce higher-order harmonics at the switching frequency and its multiples. To minimize the influence of the previously mentioned aliasing effect, a sampling technique is used.

Prevention of aliasing is one of the key requirements for accurate current sampling during inverter operation. The dominant part of the inverter's current ripple located in the out-of-band region comes from the PWM. With the ideal sampling, we would be able to perfectly reconstruct all signals below the Nyquist frequency without attenuation and phase lag, while rejecting all signals above it. Commonly used techniques for the PWM ripple suppression in

the sampled current include sampling and PWM synchronization, averaging over multiple samples, and filtering of the analog signal before digital conversion.

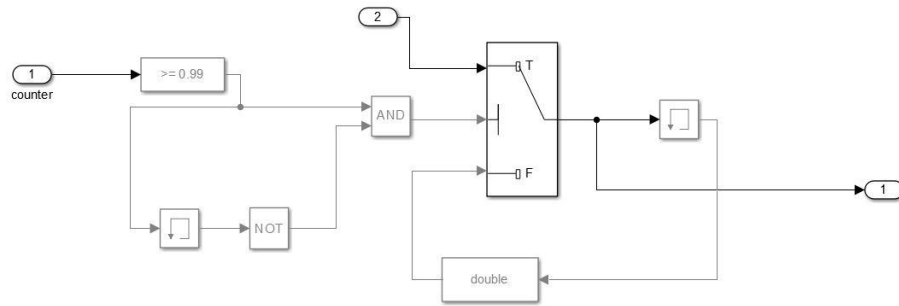


Figure 5.17: Implementation of synchronous current sampling

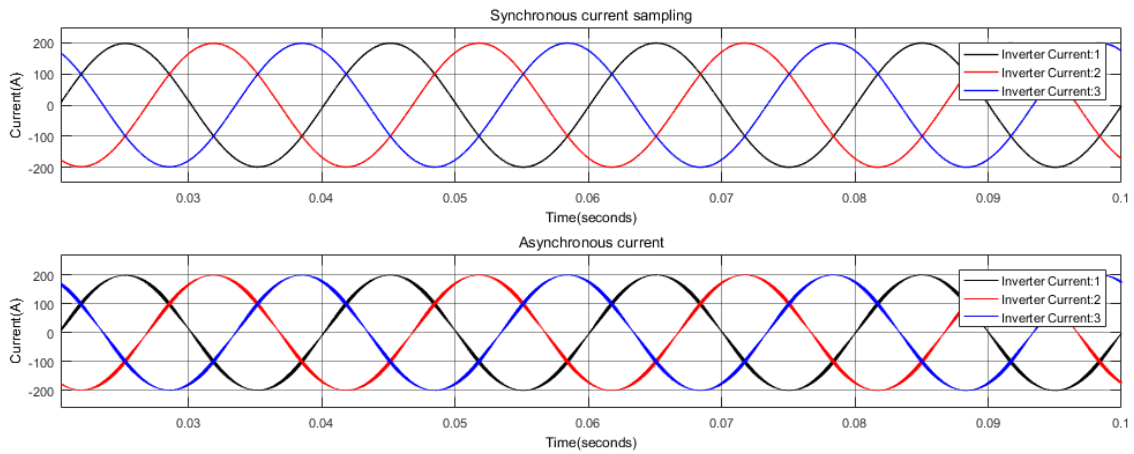


Figure 5.18: Simulation results: Inverter current with and without synchronous current sampling for a reference current of 200 A

As observed in Figure 5.19, the inverter current with synchronous current sampling has no ripple compare to the inverter current without synchronous current sampling. The zoomed-in simulation results are shown in Figures 5.20 and 5.21.

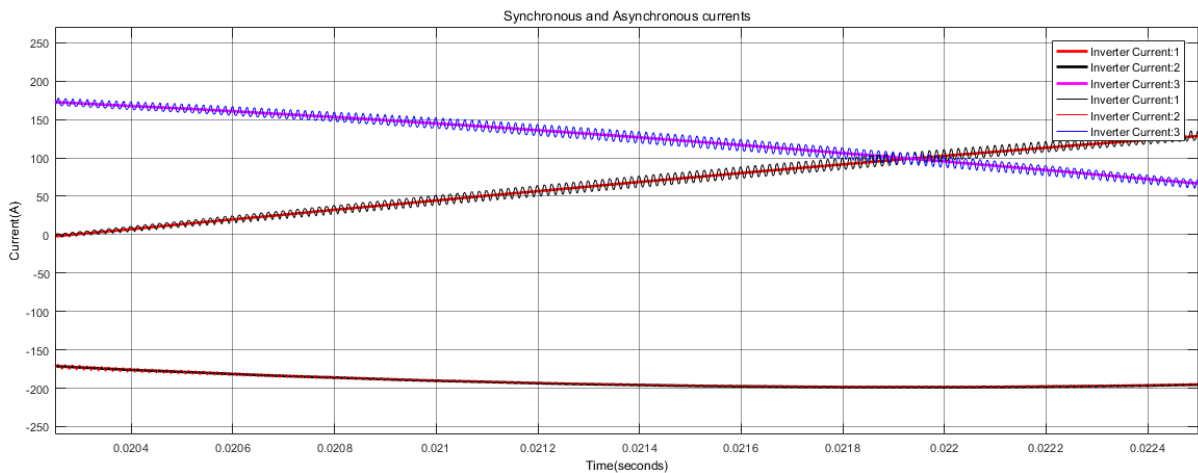


Figure 5.19: Simulation results: Synchronous and asynchronous current sampling

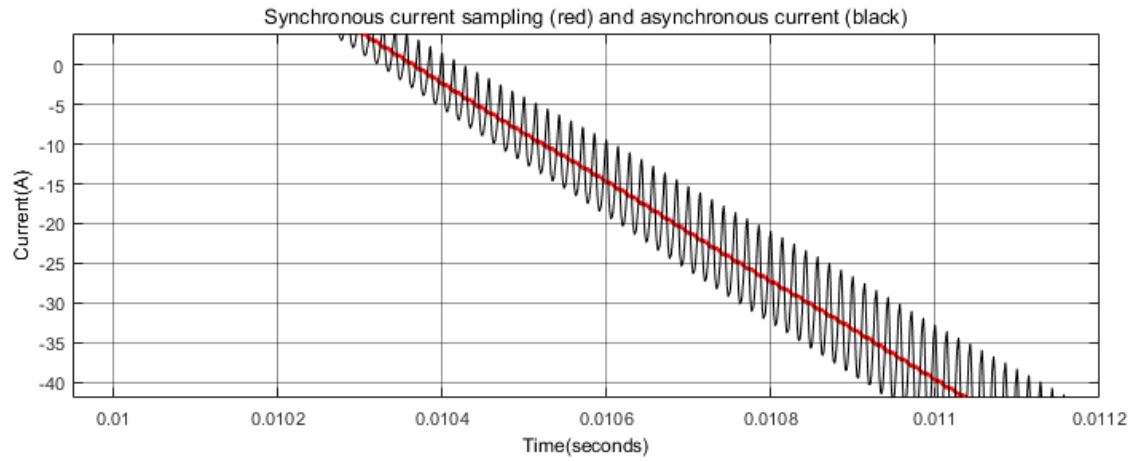


Figure 5.20: Synchronous current sampling and Asynchronous current of inverter currents

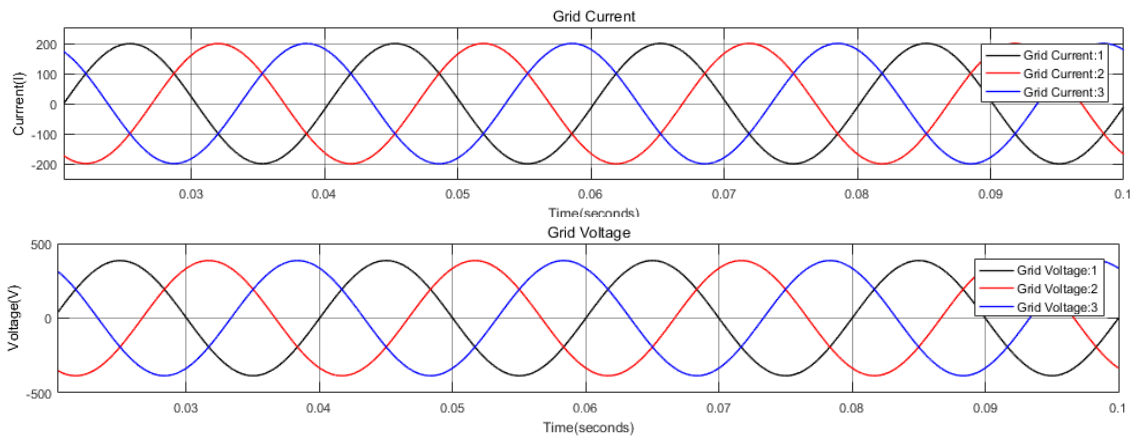


Figure 5.21: Simulation results: grid current and grid voltage for a reference current of 200 A

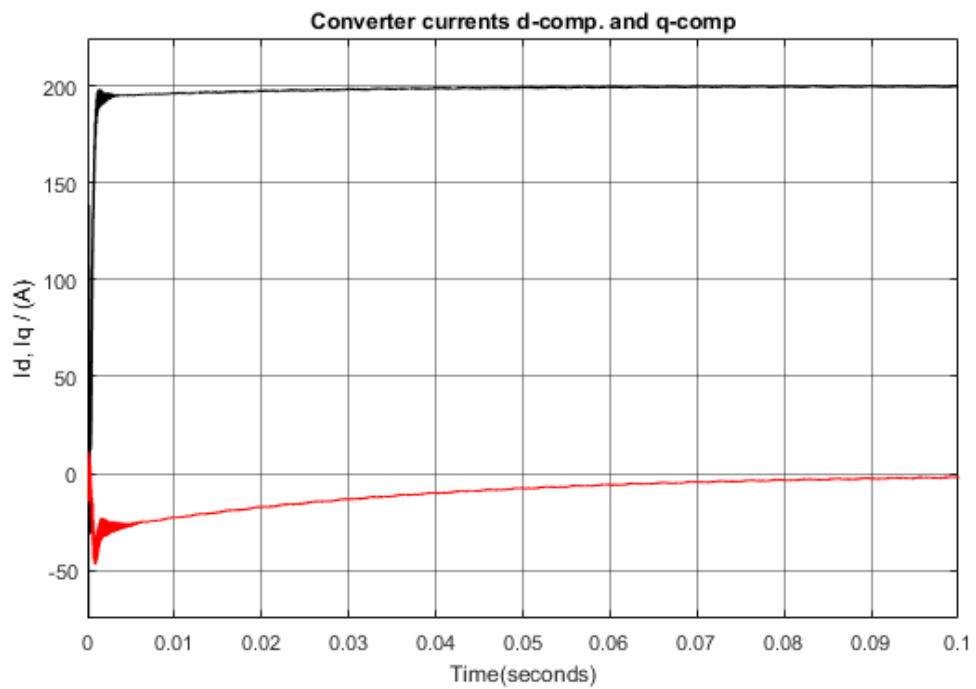


Figure 5.22: dq component inverter current

Figure 5.22 depicts the dq component inverter current of the system. It is observed that the d component maintains the reference current of 200 A and the q component reaches 0 A as time progress.

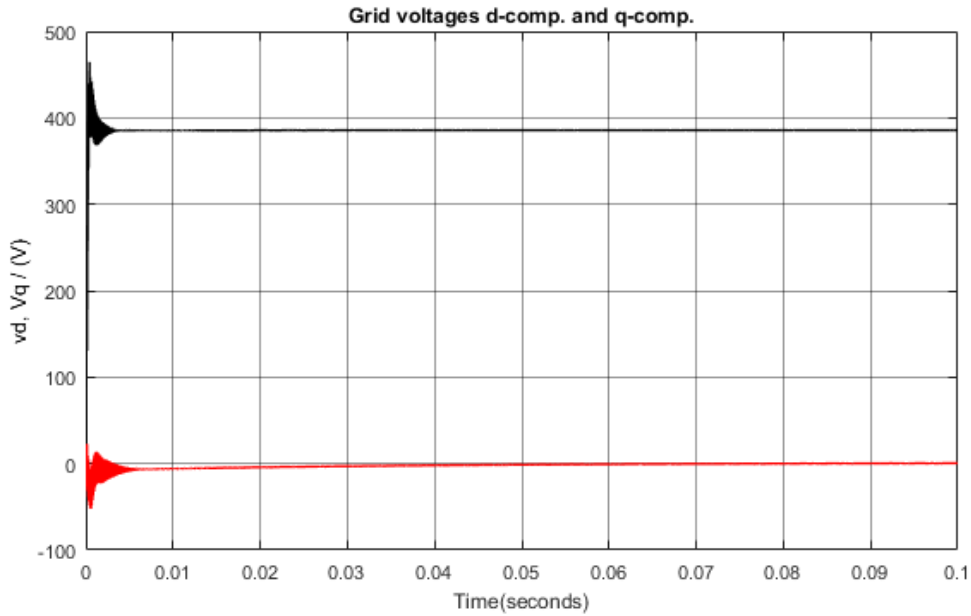


Figure 5.23: dq component grid voltage

Figure 5.23 depicts the dq component grid voltage of the system. It is observed that the d component maintains the grid voltage and the q component reaches 0 as time progress.

5.4 Current control for a parallel interleaved 3-phase 3-level ANPC inverter

The demand for power electronic converter systems with increasing output currents makes the parallelization of converters. In case communication between the parallel modules is not a limitation, interleaving can be implemented without significant additional effort. To avoid excessive converter losses and most importantly overheating, an equal distribution of the total current to the parallel modules has to be ensured.

A variety of different current sharing strategies for power electronic converters operated in parallel has been presented in the past. Droop methods are a group of strategies that reduce current imbalances by a current-dependent output voltage [69]. Alternatively, the currents of the parallel modules can be measured and the imbalances can be actively controlled to zero.

Figure 5.24 depicts the three-phase, parallel interleaved ANPC inverter topology.

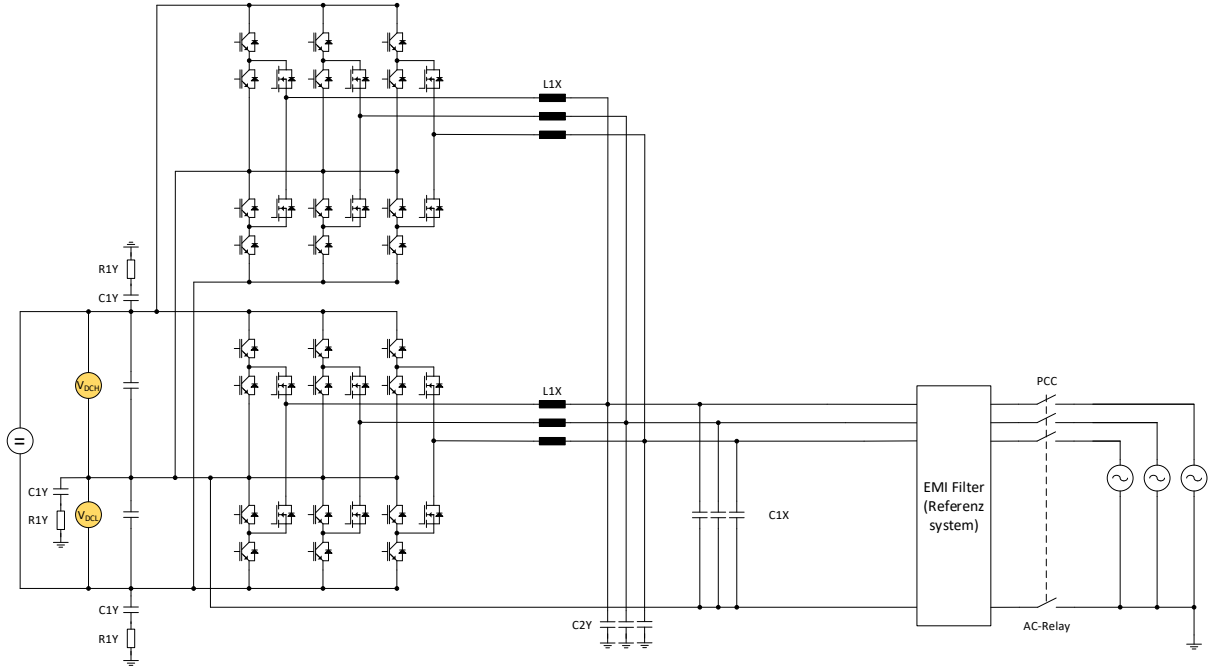


Figure 5.24: Circuit diagram of parallel interleaved three-phase, three-level ANPC inverter

The method proposed in this thesis utilizes a dq control and superposition of control strategy. The control strategy is similar to that used for the 3L ANPC. By taking the reference currents from both parallel inverters to balance the currents in parallel interleaved inverters. The measurements of currents and voltage of parallel interleaved inverter is shown in Figure 5.24. The inverter currents I_{abc} , and I_{abc2} are used in dq control. The V_{abc} is used for the PLL to calculate ωt . These 3-phase V_{abc} voltages are then transformed to 2-phase $\alpha\beta$ voltages using the Park's transformation. The $\alpha\beta$ voltages are then converted to dq voltages using Clark transformation. The voltages V_d and V_q are used in the dq control strategy.

The total reference current is shared for an equal distribution of the total current between the parallel inverters has to be ensured to avoid excessive losses.

The PWM generator is used to generate gate signals for the interleaved inverter and is phase-shifted by 180° . The PWM generator for an inverter 1 is 0° .

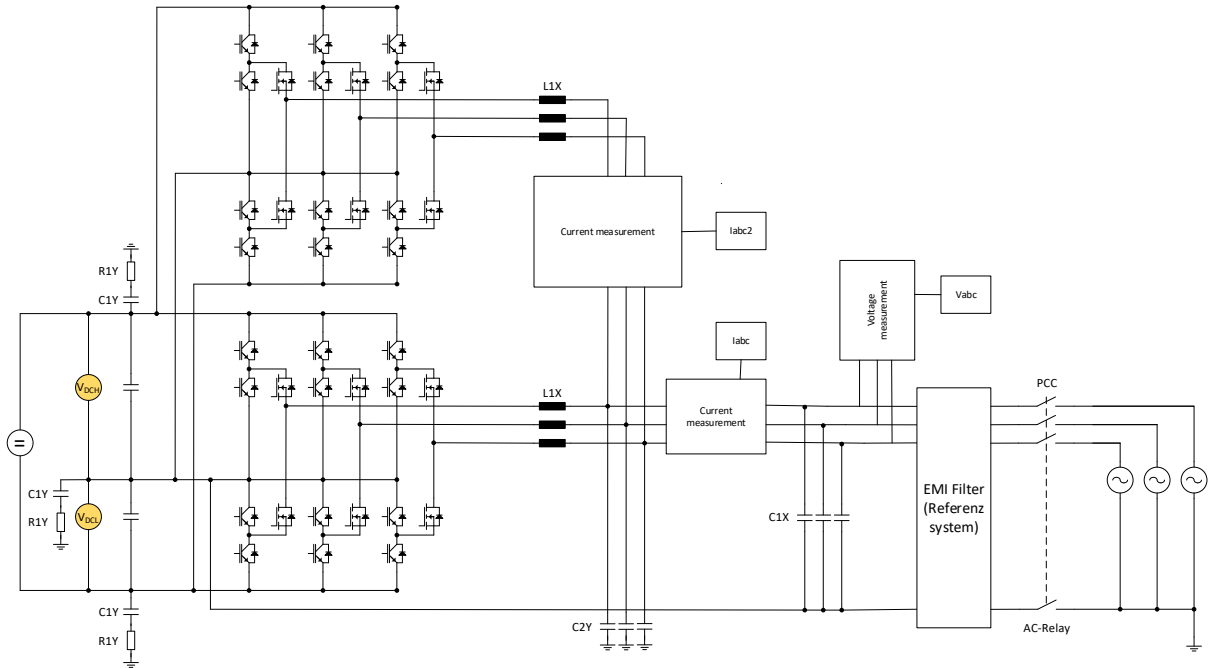


Figure 5.25: Current measurements and voltage measurement of interleaved inverter

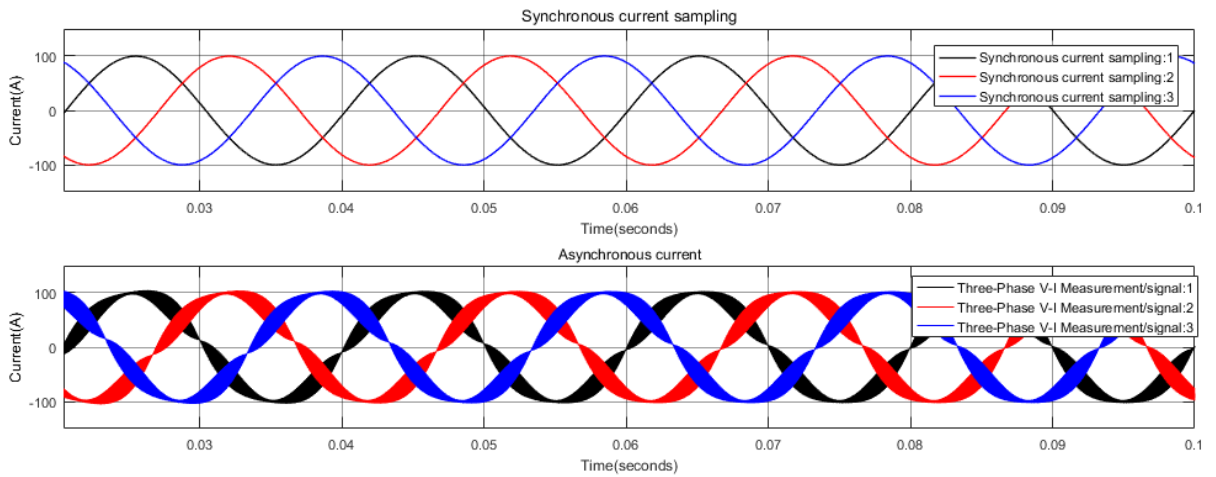


Figure 5.26: Simulation results: Inverter current with and without synchronous current sampling

As observed in Figure 5.26, the inverter current without synchronous current sampling has a lot of ripples on the bottom plot. The ripples can be easily eliminated by synchronous current sampling implementation. The inverter current with no ripples is shown in the upper plot. Inverter current in the interleaved mode has a high ripple compare to the 3L inverter. The zoomed-in simulation results are shown in Figure 5.27.

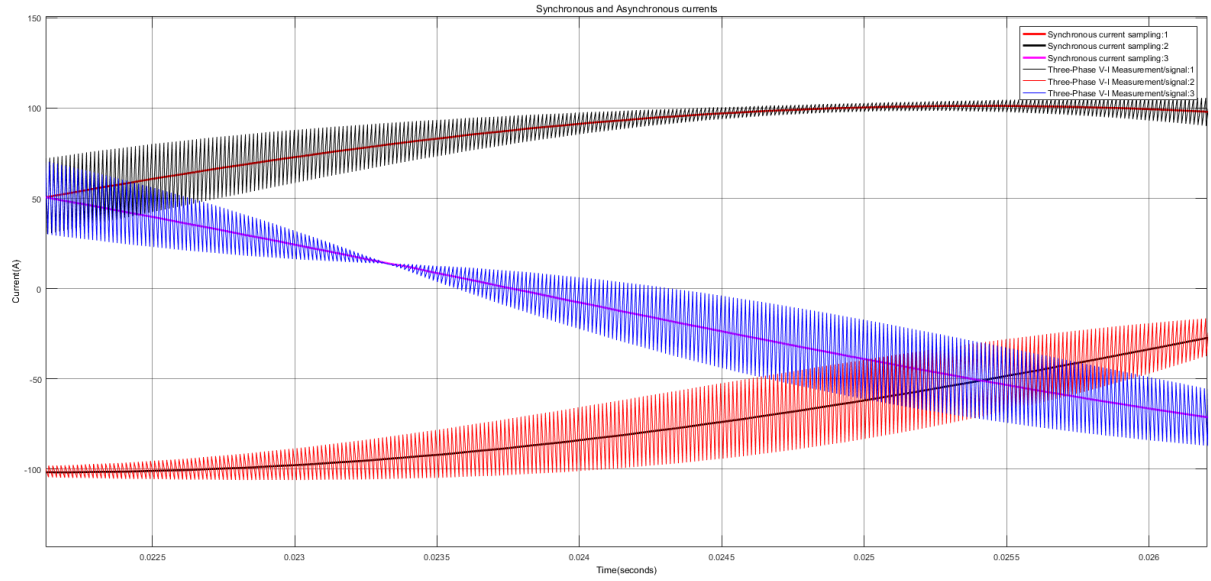


Figure 5.27: Simulation results: Synchronous and asynchronous current sampling

In Figure 5.28, the inverter current of both interleaved inverters is shown. The reference current used in the 3L inverter is 200 A. In interleaved mode, the reference current is split between the parallel inverters. In this case, the reference current of 100 A in each inverter. So that the grid current will be 200 A. With the implementation of synchronous current sampling, the current ripples are eliminated. The interleaved inverter current with 100 A reference current and no ripple is shown below.

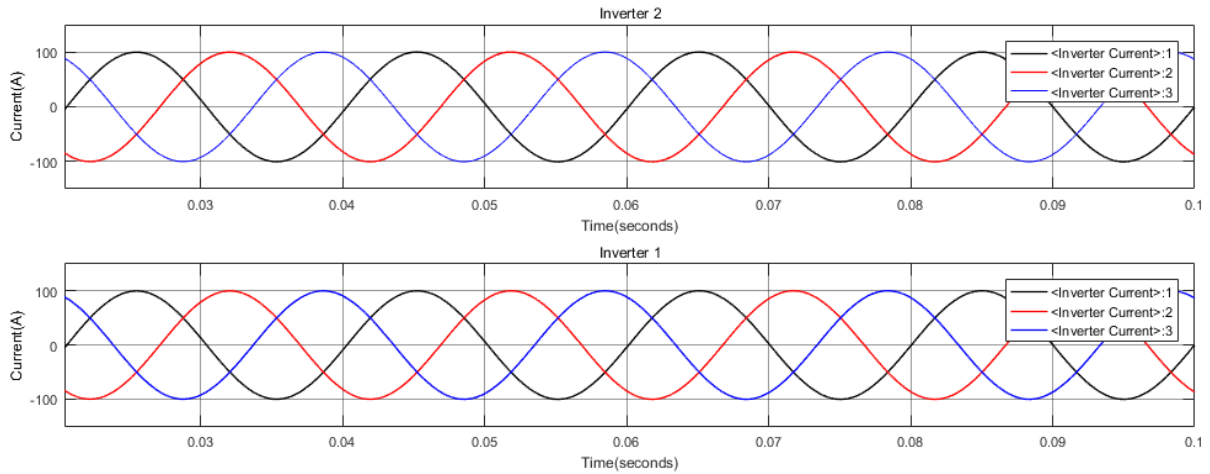


Figure 5.28: Simulation results: inverter current in parallel-connected inverters for a reference current of 100 A

In Figure 5.29, the grid current and grid voltage is shown. The grid current of the system is 200 A. The parallel operation of multiple converters allows the realization of power electronic systems with high output currents.

In Figure 5.30, with the dq control technique, the balance of the total current between the parallel modules is ensured to avoid excessive losses. The current is not filtered in this measurement.

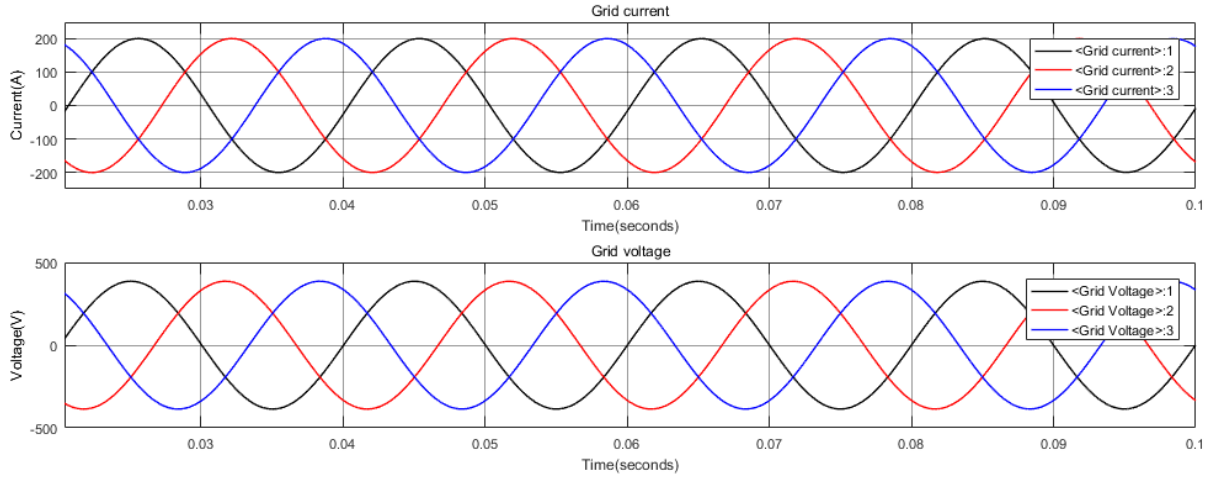


Figure 5.29: Simulation results: inverter current and grid current for a reference current of 100 A

The legend in Figure 5.30 shows the three phases of the two interleaved inverters. The top 3 represent phases A, B, and C of inverter 1 with a phase shift of 0° in PWM1, and the next 3 represent phases A, B, and C of inverter 2 with a phase shift of 180° in PWM2.

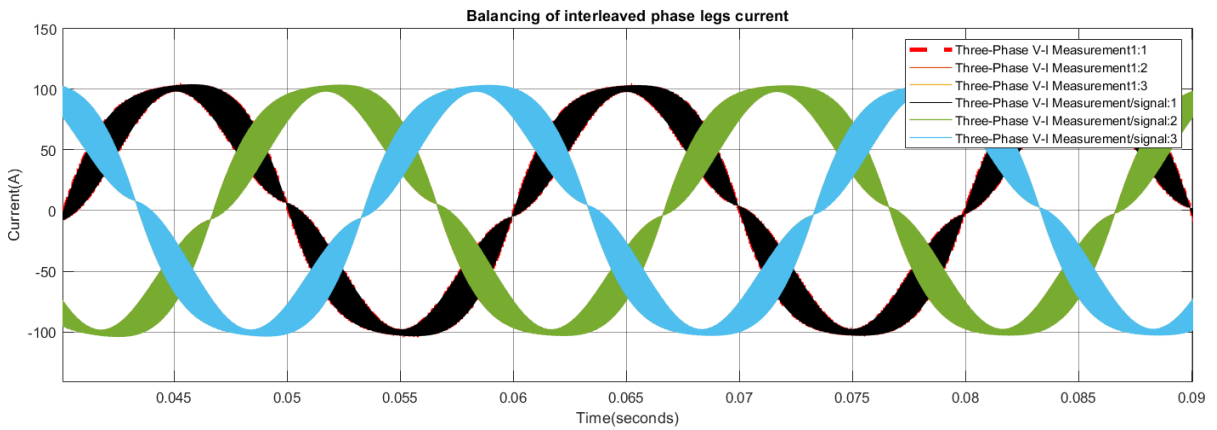


Figure 5.30: Current balance of multiple parallel-connected phase legs

Figure 5.30 depicts the current balance of multiple parallel-connected phase legs of the interleaved inverter with unfiltered inverter currents.

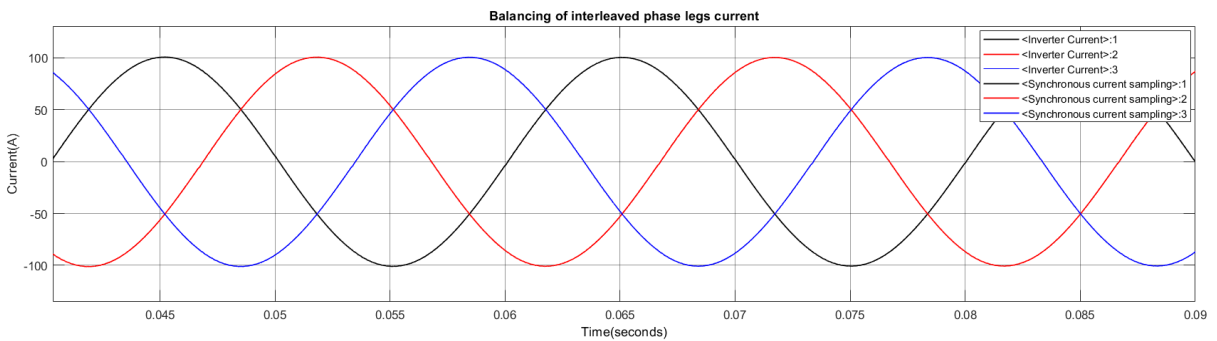


Figure 5.31: Current balance of multiple parallel-connected phase legs

Figure 5.31 depicts the current balance of multiple parallel-connected phase legs of the interleaved inverter with filtered inverter currents.

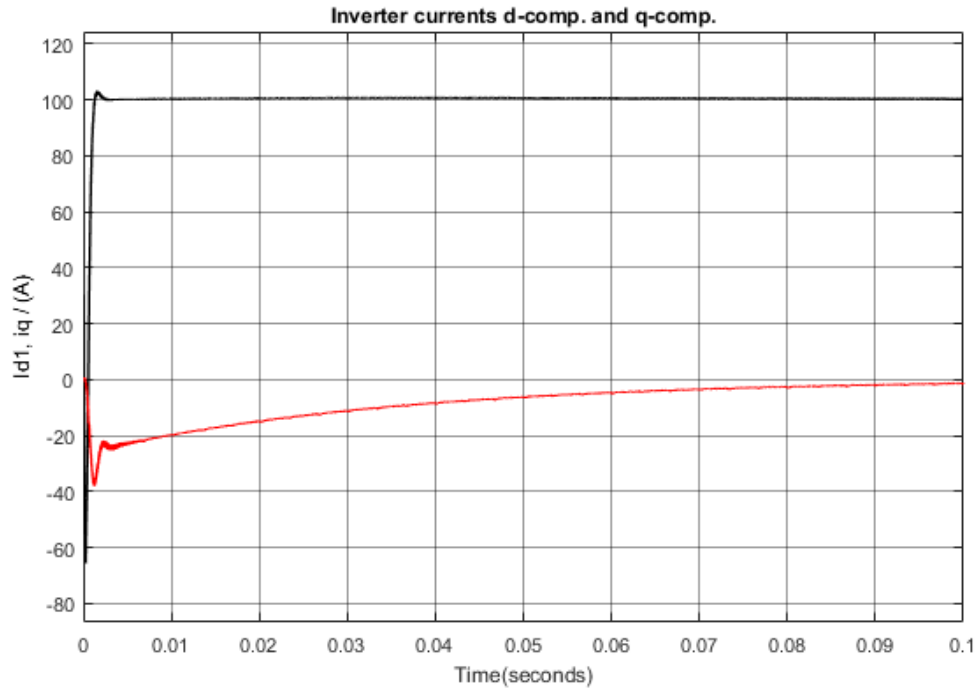


Figure 5.32: dq component interleaved inverter 1 current

Figure 5.32 depicts the dq component of interleaved inverter 1 current of the system. It is observed that the d component maintains the reference current of 100 A and the q component reaches 0 A as time progress.

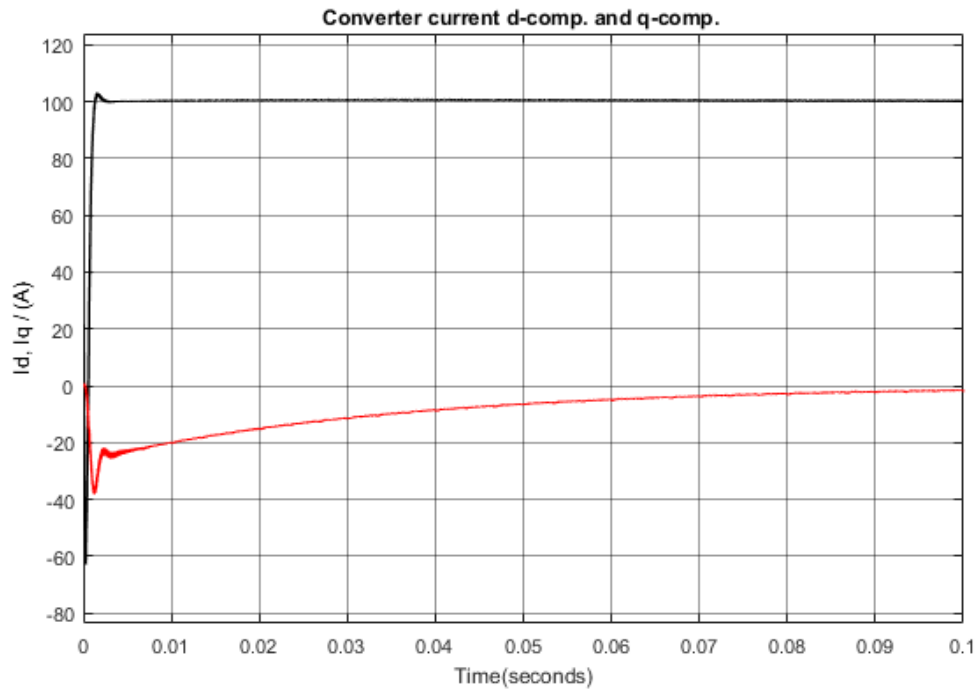


Figure 5.33: dq component interleaved inverter2 current

Figure 5.33 depicts the dq component of interleaved inverter 2 current of the system. It is observed that the d component maintains the reference current of 100 A and the q component reaches 0 A as time progress.

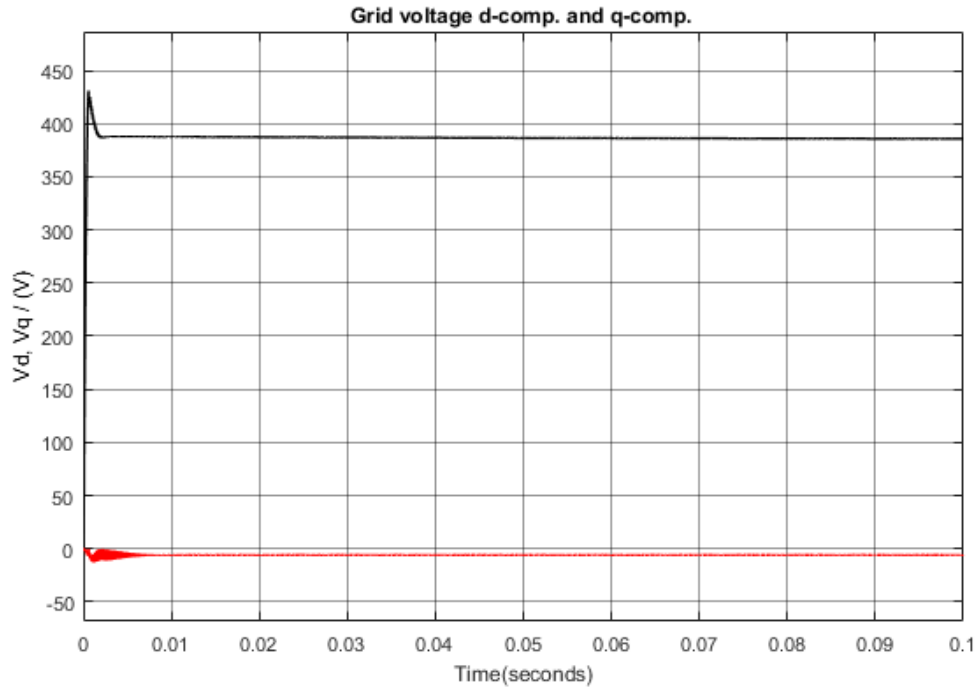


Figure 5.34: dq component interleaved inverter grid voltage

Figure 5.32 depicts the dq component of interleaved inverter grid voltage of the system.

6 Conclusion and Future Outlook

This thesis examines a 3P, 3L 4 wire ANPC inverter that is connected to the utility grid via an LC+EMI filter. To examine the stability of the system with various control strategies and by modifying the system parameters and grid impedance. The state-space model of the single-phase output filter is developed. Based on how the system performs in various scenarios, determine which controller is the most effective. In comparison to the PI symmetrical optimum approach, the PI control with the root locus method produces better outcomes. But it's important to test the state-space model created by creating a Simulink single-phase model and applying two different control parameters to see the system's step reaction. Third-order Bessel filter investigation with a first-order filter. The modeling of the averaged model and the switched model in Simulink. The current control of a 3L ANPC with SCC and also the current control of a parallel interleaved 3L ANPC inverter to balance the current is implemented.

6.1 Conclusion

Following is a summary of the work conducted in this thesis.

- In Chapter 2, a literature review was conducted with regards to the classifications of the power electronic converters, mainly the 3P, 3L ANPC topology, and the modulation strategy. The popular control strategies used in grid-connected inverter applications. Additionally, the basics of the EMI filter and its advantages were also discussed. Furthermore, the theoretical and mathematical background of state-feedback control was introduced to build the foundations for the design of these controllers.
- In Chapter 3, first, the LC+EMI was introduced and derivation of the mathematical model was presented, which is a prerequisite for the design of any control technique. The total system was created by adding the current and voltage measurement filters to the LC+EMI filter. PI Symmetrical Optimum method design procedure was presented to achieve better dynamic and steady-state performance. The simulation results were shown. Design of PI control parameters with root locus method was presented. Performance of the system under varying system parameters and varying grid impedance was investigated.
- In chapter 4, the results were compared with the two control design parameters. The performance of the system with varying system parameters and varying grid impedance was observed with two control strategies. A single-phase Simulink model was created to verify the state-space model derived earlier. Measurement voltage filters were compared with first order and third order with different cut-off frequencies.
- In Chapter 5, a 3-phase, 3-level ANPC inverter current control with dq control was implemented. The synchronous current sampling method was described and implemented to get rid of the inverter current ripple. The grid current and grid voltage of the system was studied. Current control for a parallel interleaved 3P, 3L ANPC inverter was implemented with a dq control strategy. The balancing of the parallel-connected phase legs was achieved.

6.2 Future outlook

Finally, I would like to add a few suggestions for further research on this topic.

- In the presented work, the DC-link bus is assumed as a constant voltage source. Implementation of a DC-link control is suggested.

- In this thesis, the state feedback was designed using PI control and parameters were found using the symmetrical optimum method and root locus method. An alternative approach would be to use PR, and LQR controllers and then compare the performances with different approaches.
- In this thesis, the control parameters were found using the single-phase topology of an LC+EMI filter in differential mode. Finding the control parameters using the common mode topology means taking the common-mode effects into account.
- Finally, this control scheme can be implemented on the hardware test bench and its response compared to the simulation results.

Abbreviations

DC	Direct Current
PV	Photovoltaic
AC	Alternating Current
ANPC	Active Neutral Point Clamped Inverter
MPPT	Maximum Power Point Tracking
CMV	Common-Mode Voltage
CO ₂	Carbon dioxide
SiC MOSFET	Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistor
THD	Total Harmonic Distortion
VOC	Voltage oriented Control
PI	Proportional Integral
PR	Proportional Resonant
LQR	Linear Quadratic Regulator
VSI	Voltage Source Inverter
PEC	Power Electronics Converters
IGBT	Insulated Gate Bipolar Transistor
MLIs	Multilevel Inverters
RERs	Renewable Energy Resources
FACTS	Flexible AC Transmission Systems
EMI	Electromagnetic Interference
CM	Common Mode
DM	Differential Mode
AIC	Ampere Interrupting Capacity
EMC	Electromagnetic Compatibility
IL	Insertion Loss
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
SS	State Space
SFC	State Feedback Control
LTI	Linear Time Invariant
ODE	Ordinary Differential Equations
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law

SO	Symmetrical Optimum
PI	Proportional Integral
PD	Proportional Derivative
PID	proportional Integral Derivative
SCC	Synchronous current control
PLL	Phase Locked Loop
3P	Three-phase
3L	Three-level
SOGI	Second-Order-Generalized-Integrator

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