21.1 % EFFICIENT PERC SILICON SOLAR CELLS ON LARGE SCALE BY USING INLINE SPUTTERING FOR METALLIZATION

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ABSTRACT

This work presents the first results for the production of highly efficient solar cells with industrial processes using the PERC structure. Two batches of FZ and Cz wafers were conducted to prove the applicability of a transfer from the PERC structure. Two batches of FZ and Cz wafers are discussed later on.

INTRODUCTION

Passivated emitter and rear cell (PERC) concepts are very well known for highly efficient crystalline silicon solar cells [2]. One important purpose is to transfer this promising cell concept into an industrial production environment. The Photovoltaic Technology Evaluation Center (PV-TEC) [3] at the Fraunhofer Institute for Solar Energy Systems (Germany) offers the possibility to manufacture PERC silicon solar cells on large scale with industrial related pilot systems. One of the key technologies for the metallization of these cell concepts features Physical Vapor Deposition (PVD) technologies instead of the standard screen printing of metal pastes for establishing either the complete metallization or a seed layer for subsequent electroplating. Less shadowing and a lower contact resistance are compared to screen printed contacts the two major advantages of sputtered contacts. Sputtering, instead of the standard thermal evaporation process, for metallization is interesting due to low costs for thin layer deposition of most metals. With a new pilot system from Applied Materials (AMAT) it is possible to sputter various metal layers with a high throughput.

EXPERIMENTAL

The process flow of the investigated PERC cells is shown in Figure 1. For a detailed analysis of the manufactured high efficient solar cell structure with inline sputtered front and rear side contacts, six inch shiny etched boron doped float zone (FZ) wafers (\(\rho_{\text{Si,Bulk}} = 1 \Omega\text{cm}\), 250 µm thick) were cut down to a size of 125*125 mm², because of the used carrier and tray systems of the PV-TEC equipment. Additionally in a second batch which was processed simultaneously with the FZ wafers monocrystalline Czochralsky (Cz) wafers with a bulk resistivity \(\rho_{\text{Si,Bulk}} = 1 \Omega\text{cm}\) were fabricated. Because of the complexity of the process, on every wafer 16 single cells were created to increase the number of cells per batch. Therefore different process steps for structuring were necessary. A masking oxidation of an approximately 250 µm thick wet SiO₂ was created. Afterwards the emitter windows (2×2 cm²) were defined by using inkjet hotmelt resist. The opening of the windows (selective oxide removal) was done by a wet chemical process. During the subsequent texturing, random pyramids were created. Afterwards the phosphorous emitter diffusion in a tube furnace (final sheet resistance \(R_{\text{SH}} = 120 \Omega/\text{sq.}\) ) was performed prior to the removal of the remaining diffusion barrier (SiO₂) and the phosphorus-silicate glass from the wafer in a wet chemical process. For the passivation layer on the front and rear side a 105 nm thick oxide was used. Within this step the emitter was driven in. For the rear side metallization a 2 µm thick aluminum layer was sputtered, followed by the laser-fired contact (LFC) process [4] (pitch 750 µm) and the annealing under forming gas (425 °C, 25 min.). Subsequent the photolithographical definition of the front side pattern was done.

Figure 1: Process overview for manufactured PERC silicon solar cells. Processes performed in PV-TEC and in clean room are indicated.
The front side contacts were deposited with inline sputtering technology. A two layer system of titanium (50 µm) and silver (100 µm) was deposited. Through a lift-off process the photo resist was removed. After that the front side contacts were annealed. The front side contacts were thickened by silver plating to ensure a sufficient conductivity. All processes (except the definition of the front side pattern and the lift-off process after the metal deposition) have been established in the PV-TEC with a high reliability and quality. With the new inline sputtering pilot system ATON 500 Ev + Sp (Figure 2) from Applied Materials (AMAT) it is possible to sputter front side contacts with industrial throughput. Depending on the final layer thickness the pilot system is capable to process 540 wafers per hour. Two rotatable targets in the process chamber allow sputtering different metal layers without breaking the vacuum. The tool installed in the PVTEC is in the moment able to sputter Ti, Ag, Al, NiCr and NiV.

Figure 2: Schematic of the pilot line PVD metallization system for thermal evaporation and DC sputtering.

The homogeneity of the sputtered metal layers has been determined by using the four-point-probe measurement [5]. For sputtered titanium on every wafer of one tray (consists of 3x3 wafers) 10x10 measuring points were taken which results in a total number of 900 measuring points for one tray. The deviation was determined to 5.41 % over the whole effective sputtering area for deposited titanium.

ANALYSIS OF INDUSTRIALLY FABRICATED PERC SILICON SOLAR CELLS

The experimental focus of the fabricated solar cells was on a variation of the annealing process and on the electrical losses due to the different contact formation of the front side contacts. Therefore the IV-parameters, the series resistance and the contact resistivity were determined.

Solar cell results

In the first batch 64 silicon solar cells (FZ) with a seed layer finger width of 15 µm and 64 solar cells (FZ) with a line width of 45 µm were produced. In a second batch 64 PERC cells (Cz) with a Ti-Ag seed layer of 15 µm finger width were fabricated (in total 192 solar cells). The results of the illuminated IV-curve for manufactured PERC cells show that both for Cz and FZ wafers constant high efficiencies are possible over a wide temperature range for the annealing process. Nevertheless, a non-negligible effect of the annealing step can be observed. The reason for that seems to be a slight difference of the silicide formation, depending on the chosen temperature and time. The depth of the titanium silicide silicon interface depends on the chosen annealing parameters [1], [6]. However, the overall high efficiencies show that the PV-TEC equipment allows fabricating PERC cells with industrially related throughput with high reliability.

In Figure 3 the results from IV-measurements for Cz and FZ wafers, annealed between \( T_{\text{min}} = 100 \, ^\circ \text{C} \) and \( T_{\text{max}} = 500 \, ^\circ \text{C} \) under forming gas for \( t_1 = 5 \, \text{min} \) and \( t_2 = 10 \, \text{min} \), are shown. The efficiency increases continuously from 100 °C to 400 °C for the FZ wafers and up to 450 °C for the Cz wafers. The highest efficiencies \( \eta_{\text{max,FZ}} = 21.1 \% \) and \( \eta_{\text{max,Cz}} = 19.4 \% \) are observed at 400 °C (\( t = 10 \, \text{min} \)) and at 450 °C (\( t = 5 \, \text{min} \)). The efficiency of the fabricated silicon solar cells with the 45 µm Ti-Ag seed layer decreases rapidly between 400 °C and 450 °C (i.e. for \( t = 10 \, \text{min} \) the efficiency drops from \( \eta_{400 \, ^\circ \text{C}, 10 \, \text{min}} = 19.5 \% \) to \( \eta_{450 \, ^\circ \text{C}, 10 \, \text{min}} = 4.6 \% \)). A further investigation of the front and rear side metallization was done later on by determining the series resistance and the contact resistance.

The detailed results of the optimized annealing process for FZ and Cz wafers are listed in Table 1. The open circuit voltage \( V_{\text{OC}} \) for the best PERC cell with sputtered 15 µm thick Ti-Ag seed layer is 667.1 mV at a current density of \( J_{\text{SC}} = 39.1 \, \text{mA/cm}^2 \) and an efficiency of 21.1 percent. The fabricated Cz wafers seem to be more stable at higher temperatures, because although FZ and Cz wafers were produced simultaneously the highest efficiencies were reached at 450 °C at a fillfactor of FF = 77.6 %.
Table 1: IV-parameters for the investigated PERC cells at the optimized annealing process.

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<tr>
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<th>T [°C]</th>
<th>t [min]</th>
<th>$V_{OC}$ [mV]</th>
<th>$J_{SC}$ [mA/cm²]</th>
<th>FF [%]</th>
<th>$\eta$ [%]</th>
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In Figure 4 it is shown that the blue response curve of the internal quantum efficiency of an industrial fabricated PERC cell with a Ti-Ag sputtered seed layer compared to a reference cell (clean room) shows no difference, only for longer wavelengths the IQE is slightly reduced, because of the lower $\rho_{Si,Bulk} = 0.5 \Omega \cdot cm$.

Figure 4: Comparison of the Internal quantum efficiency (IQE) of one industrial fabricated PERC cell and a reference cell prepared in the clean room.

The good results of the IQE of the fabricated PERC cells underline the capability of producing highly efficient solar cells with the pilot systems of the PV-TEC.

Investigation of the series resistance

The series resistance was determined by using the method [7], [8] of comparing the results of the SunsVoc measurement, introduced by Sinton [9] and the illuminated IV-curve.

The total series resistance $R_S$ was calculated from [10]:

$$R_{S,SunSoc} = \Delta V \over J_{mpp} = \frac{V_{mpp}(SunSoc) - V_{mpp}}{J_{mpp}} \quad (Eq. 1)$$

Whereas $V_{mpp}(SunSoc)$ is the voltage at the maximum power point from series resistance free SunsVoc measurement and $V_{mpp}$ and $J_{mpp}$ the voltage drop and current density from IV-measurements. In Figure 5 the calculated series resistance $R_S$ for highly efficient silicon solar cells with a seed layer finger width of 15 µm is plotted versus the annealing temperature. All cells were annealed for ten minutes under forming gas atmosphere. From 100 °C to 250 °C the series resistance increases from $R_{S,100 °C} = 0.37 \Omega \cdot cm^2$ to $R_{S,250 °C} = 0.49 \Omega \cdot cm^2$ which cannot be explained until now. The lowest $R_S$ was determined at 400°C ($R_{S,400 °C} = 0.16 \Omega \cdot cm^2$) which was also the annealing step leading to the highest cell performance (compare to Table 1).

Figure 5: Series resistance of PERC cells with 15 µm thick Ti-Ag seed layer, annealed between 100 °C and 450 °C for ten minutes.

The highest series resistance $R_{S,SunSoc} = 0.95 \Omega \cdot cm^2$ was determined at $T = 450 °C$.

Contact resistivity and normalized contact resistance

The contact resistivity of the sputtered front side contacts was determined with the transmission line model (TLM) [11], [12] by using the four point probe technique. Isolated fingers of the cells served as the TLM structure. For the determination of the contact resistivity and the width weighted contact resistance, the fingers of the front side contacts were isolated mechanically by sawing. Every measurement was done at eight isolated fingers. Because of the mechanical stress during the isolation process only cells from the second batch with the seed layer of 45 µm could be used for the TLM measurements. Figure 6 a sketch of the isolated area for the measurement (left) and the principle of extracting the contact resistance from the TLM measurement (right).
The total resistance $R_{\text{tot}}$ is given by:

$$R_{\text{tot}} = 2R_c$$

The slope $R_{\text{sh}}$ is:

$$R_{\text{sh}} = \frac{1}{d^2}$$

Contact distance $d$ was 0.8 mm.

The contact resistivity $\rho_C$ versus the annealing temperature is plotted in Figure 7.

The finger line width was approximately 65 µm (45 µm seed layer thickness and a further 20 µm from the silver plating process) and the contact width of $\sim$10 mm. The contact distance $d$ was 0.8 mm.

The contact resistivity $\rho_C$ versus the annealing temperature is plotted in Figure 7.

The contact resistivity $\rho_{C,100 \degree C} = 7.96 \, \text{m}\Omega \cdot \text{cm}^2$ continuously decreased to $\rho_{C,400 \degree C} = 0.36 \, \text{m}\Omega \cdot \text{cm}^2$ for the investigated solar cells. Because of a possible different contact width $w$ (due to the mechanical isolation of the fingers) the width weighted contact resistance was determined too (Figure 8).

In comparison with the behavior of the contact resistivity (Figure 7) the normalized contact resistance $R_{C^*w}$ shows only a slightly different characteristic between 250 °C and 300 °C. The normalized contact resistance $R_{C^*w} = 0.043 \, \text{m}\Omega \cdot \text{cm}$ remains the same for both temperatures. The reason is an already mentioned difference in the effective contact width.

The contact resistivity of the solar cells, annealed at 450 °C, could not be determined because the structure has been destroyed during the isolation process.

Optical analysis

An optical analysis with scanning electron microscopy (SEM) was conducted to determine the aspect ratio (height / width) for sputtered and subsequent silver plated front side contacts.

In Figure 9 (left) the cross section area (right) and the surface of a sputtered (Ti-Ag seed layer 45 µm) and subsequent silver plated contact is shown. The height of approximately 11 µm and the width of $\sim 60 \mu$m lead to an aspect ratio of 1/5, for 15 µm thick seed layer deposition and subsequent silver plating the aspect ratio changed to 1/3 and a further reduction of shading losses.

CONCLUSION

The major objective of this work was to investigate the feasibility of fabricating highly efficient solar cells with industrial equipment of the PV-TEC. The front and rear side metallization was conducted with a new inline sputtering pilot system from AMAT. The front end and the most cru-
cial processes of the back end were performed in the PV-TEC, only the definition of the front side pattern and the lift-off process were done in the clean room. Over 190 PERC cells (FZ and Cz material) were manufactured reaching efficiencies up to 21.1 percent. The sputtering technology allows depositing homogenous metal layers (i.e. the deviation of sputtered titanium is only 5.41 %). The investigated PERC cells had a phosphorous emitter with a sheet resistance R\text{SH} = 120 \Omega/\square and 105 nm SiO\text{2} passivation / antireflection layer, sputtered aluminum on the rear side and a Ti-Ag (50 nm / 100 nm) seed layer on top prior the silver plating. The highly efficient solar cells were annealed between 100 °C and 450 °C for five and ten minutes under forming gas. For the optimized annealing temperature the highest efficiency for FZ wafers was determined to $\eta_{\text{max,FZ}} = 21.1 \%$ and for the second batch with Cz material at 450 °C to $\eta_{\text{max,Cz}} = 19.4 \%$. Furthermore the investigation of the series resistance and the contact resistivity underline the applicability of fabricating highly efficient silicon solar cells with industrial equipment. The lowest contact resistivity $\rho_{C,400 °C} = 0.36 \text{m}\Omega\cdot\text{cm}^2$ was observed at T = 400 °C and t = 10 min. The aspect ratio of the front side contacts was determined by SEM pictures. Over a broad temperature range PERC solar cells with high efficiencies were manufactured. These results in combination with the high throughput of the pilot systems (for example with the inline sputtering tool it is possible to process 540 wafers per hour) underline the feasibility of producing PERC silicon solar cells with industrial related machines.

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