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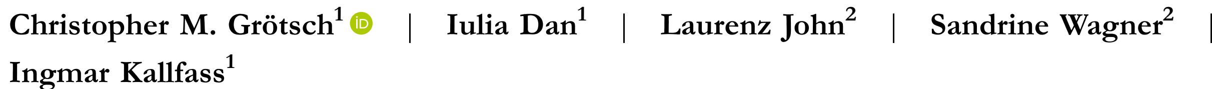
ORIGINAL RESEARCH PAPER

Comparison of active dual-gate and passive mixers for terahertz applications



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Abstract

The authors propose four versions of a dual-gate active down-conversion mixer for H-band applications. The mixer operates at a local oscillator (LO) frequency of 240 GHz. It is designed for maximum conversion gain and a large bandwidth of at least 50 GHz from 220 to 270 GHz. Furthermore, the mixer is .optimised to operate at low LO power levels beneath 0 dBm. This renders power hungry LO buffer stages redundant. Hereby, the necessary chip size and the overall power consumption of fully integrated receivers can be drastically reduced. Four different versions of the downconverter were designed. Firstly, the layout of the transistors was changed from a conventional multi-transistor cell design to a mixer topology within the multi-finger transistor cell. Secondly, two on-chip solutions to decouple the drain voltage from the intermediate frequency (IF) signal were realised to facilitate zero-IF conversion: a resistive and an active load. The results are presented and the advantages and disadvantages of the four versions for the usage in terahertz applications are thoroughly analysed. Finally, the active dual-gate mixers are compared to a state-of-the-art resistive mixer for H-band with regard to conversion gain, bandwidth, linearity, noise figure and chip size.

1 | INTRODUCTION

The demand for wireless data rate is increasing exponentially and there is no end in sight for this trend. New promising applications fuel this development even further. These applications include the so-called data kiosks or data-showers [1], wireless chip-to-chip communication [2] in data centres as well as high-capacity wireless links, which are meant to provide rural areas [3] with connection to high-speed internet.

To satisfy this continuous growth, high-frequency bands, especially the H-band (220–325 GHz), get more into the focus of current research and development, and data rates exceeding 100 Gbit/s haven been reported. For all-electronic setups 96 Gbit/s were achieved over a distance of 40 m [4] at a frequency centred around an local oscillator (LO) of 240 GHz. By aggregating 6 channels, CMOS transmitters capable of a date-rate of 105 Gbit/s were reported by [5] but, to the best of the authors' knowledge, no transmission experiment was conducted. As another example, by combining photon- and electron-based systems a data rate of 100 Gbit/s have already been shown in transmission experiments in [3] and [6].

Although ultra-high data rates were shown, these results all come at a price. The generation of high output power in these frequency bands poses a big challenge. Additionally, components are lossier and less efficient than at lower frequencies. The highest output power in H-band of a power amplifier in InGaAs-based metamorphic high electron mobility transistor (mHEMT) technology reported so far achieves more than 13 dBm over a frequency from 286 to 310 GHz [7]. In InP heterojunction bipolar transistor (HBT) technology, due to the higher breakdown voltage, more than 20 dBm of measured output power have been demonstrated over a frequency range from 185 to 225 GHz [8]. This result was achieved by massive parallelisation of 16 power amplifier cells.

However, by cascading and parallelising amplification stages on one chip, the power consumption as well as the necessary chip size will increase. In terms of integrating a full receiver in H-band, this can lead either to disadvantageous aspect ratios of chips or the need to rearrange or to meander

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the stages to generate a preferable aspect ratio, as performed in [9].

Another option is to split the receiver chip into two parts, for example LO generation plus mixer and low-noise amplifier (LNA) as described in [10]. However, such a solution requires bondwires for the connection of the chips at H-band frequencies which introduce additional losses that have to be compensated. The other problem includes resonances in the package due to finite isolation or cavity modes in waveguide-packaged modules. Especially in millimetre-wave bands, cavity-resonances are a major problem [11]. In order to avoid this, additional measures have to be adopted, like using non-rectangular chip dies [12].

To convert the data signal from baseband to H-band the most commonly applied technique is the implementation of diode mixers or passive FET mixers. These topologies show good performance in terms of bandwidth and linearity [13,14]. The downside is the high necessary LO drive power and the high conversion loss. As already discussed especially the generation of this high LO power presents a challenge not only for the circuit designer but also for the packaging of the chip because of the increase in chip size due to additional driver amplifier stages.

Also, there is an issue in high LO power levels which is of high demand in the isolation of LO to the radio frequency (RF) port and LO to the intermediate frequency (IF). Both are critical in order to avoid saturation of subsequent amplifier stages and self-mixing effects due to reflections. All of which can result in an overall degradation of the error vector magnitude (EVM) [15].

Furthermore, the advantage of near-zero DC power consumption in comparison to active mixers only holds to the first view. The high conversion loss and the necessary LO power has to be compensated by additional amplifier stages. Therefore, it is worth taking a closer look at active mixer alternatives also for high frequency bands such as the H-band with a lower demand in necessary LO power.

Here, we present a single-ended active dual-gate downconverter for communication applications in the H-band. The LO frequency is 240 GHz and the 3-dB bandwidth of the chip is larger than 50 GHz. This makes the mixer suitable for wideband, high data-rate wireless transmissions. To increase the efficiency, the circuit was designed to operate at a low LO power of less than 0 dBm which makes large and power hungry amplifier stages operating as LO buffer obsolete. Thereby, not only the integration of this downconverter in a receiver chain and its packaging will be simplified but also the overall power consumption is reduced. Four different versions of the downconverter were designed and will be presented in detail in the following sections.

2 | CIRCUIT DESIGN

The different versions of the downconverter show variations in two properties: First, the type of load that was used to decouple the drain voltage on-chip from the IF signal path will be either active or passive and the second will be in the layout of the transistor cell. On one hand, two conventional transistor cells were used for the dual-gate mixer and, on the other hand, the two transistor cells were merged into one multi-finger transistor cell.

For further reference the versions or models will be addressed as follows: The mixer with a resistive load consisting of a single transistor cell is RL1, the version with two transistors is RL2. AL1 and AL2 describe the downconverters with an active load and with one or two transistor cells, respectively. The first version of AL1 and first measurements were already presented in [16], but no in-depth analysis and comparison was performed. Table 1 gives a summary of the nomenclature.

A single-ended resistive downconverter fabricated with the same technology is used to compare the results of the active approach with a passive one. All chips are realised in the in-house 35 nm mHEMT technology of the Fraunhofer Institute for Applied Solid State Physics, IAF, with cut-off frequencies f_t and f_{max} of more than 500 GHz and approximately 1000 GHz, respectively [17]. The parts that were varied for the different versions and the design consideration, that were done, will be treated in more detail. Additionally, an overview of the passive mixer cell that is used as a reference will also be given.

2.1 | Dual-gate mixer

A dual-gate mixer presents a good bases to evaluate active mixers for terahertz applications, since knowledge gained from this design can later also be used for more complex solutions like a Gilbert cell. The top of Figure 1 shows a general schematic representation of the dual-gate mixer.

Two transistors each with a gate finger width of 19 μm and two fingers form the heart of the mixer are considered. In simulation, 19 μm has shown the best compromise between conversion gain, linearity and necessary LO power. As already mentioned, two versions of the physical implementation of the transistor cell for the dual-gate mixer were fabricated.

Figure 1, bottom, shows the two versions of the layout of the transistor. In the first version, the two transistor cells were kept separated, and the source of T1 is connected to the drain of T2 by a short piece of transmission line. In the second version T1 and T2 are integrated in one multi-finger transistor cell sharing the same extrinsic device environment. For clarification, a schematic of both implementations of the transistor cells and a photograph of the section of the chip are shown in Figures 2 and 3.

The LO is fed to the gate of T1. To match the LO input port to the gate impedance transmission lines TL1, TL2 and

TABLE 1 Overview of the four fabricated H-band mixer versions and the corresponding names

	Single transistor cell	Double transistor cell
Resistive load	RL1	RL2
Active load	AL1	AL2

TL3 are used. C1 operates as a decoupling capacitor and prevents DC current from flowing into the LO port. TL2 in combination with C2 also decouples the high-frequency LO signal from the DC supply path for the gate bias of T1. In order to do so, the length of TL2 is set to lambda quarter at 240 GHz.

The RF signal is applied to the gate of transistor T2. In the same way as the LO, the RF port is matched by the transmission lines TL5–TL7. The gate bias for T2 is fed to the circuit via TL6. TL6 in combination with C5 ensures no RF signal is flowing into the DC source. C6 is used as a DC block. The gate bias of T1 is 0.3 V and for T2 0.18 V. The simulated current density at these bias points is around 350 mA/mm.

The IF is extracted at the drain of T1 where the drain voltage is also applied. The drain bias lies at 2 V for the active load and 3.7 V for the resistive load version. The downconverter will be employed as a so-called zero-IF mixer, meaning that the IF ranges from DC to in this case 25 GHz. Around 25 GHz was targeted, because this is the necessary bandwidth to transmit 100 Gbit/s using a 16-QAM modulation and an idealised rectangular filter. On-chip matching of the IF at these low frequencies is hard to accomplish using transmission lines and MIM capacitors. Additionally, it complicates the on-chip decoupling of the IF signal path from the DC source. Typically, transmission lines or inductors are used for that purpose. But, for transmission lines to operate properly as distributed elements for impedance transformation, their length has to be $>\lambda/20$ [18]. This is impossible to implement on-chip for the range from DC to several tenth of gigahertz. The problem with inductors is their low-pass behaviour. Hence, replacing the 'Load' in Figure 1 with an inductor, creates a high-pass filter for the IF signal. The part of the baseband spectrum below the cut-off of the filter is lost to the short presented by the parallel inductor in the DC supply. In [15] a threshold is defined at which the overall data signal starts to be negatively affected by a suppression of low frequency components. According to [15] the threshold lies at 0.1% of the baseband bandwidth. Moreover, the size of the inductor has to be increased to minimise the cut-off frequency. However, an on-chip inductor with a cut-off frequency of less than 25 MHz would already exceed the total chip size of the mixers presented here.

Here two different versions for IF decoupling were implemented as shown in the bottom of Figure 1.

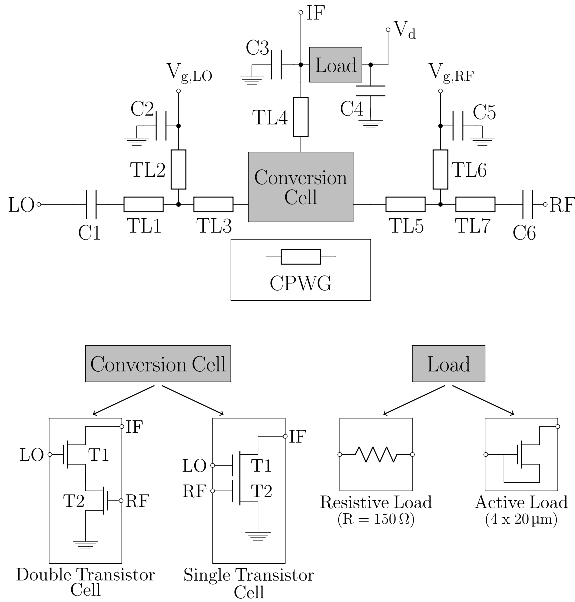

FIGURE 1 Top: The simplified schematic of the active dual-gate downconverter. Bottom: The options for replacing the grey rectangle placeholder. The rectangle with the description 'Load' is replaced by either an active or resistive load depending on the version. The rectangle labelled 'Conversion Cell' will be replaced by either a double or single cell transistor

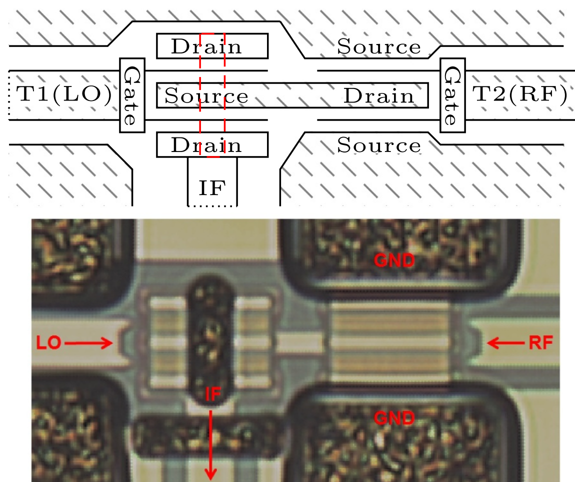

FIGURE 2 The simplified schematic of the double transistor cell (top) and a magnified photograph of the section of the chip (bottom). The transmission line environment is coplanar, where the centre signal lines are embedded into ground planes. The red dash is an airbridge connecting the two drain terminals of T1

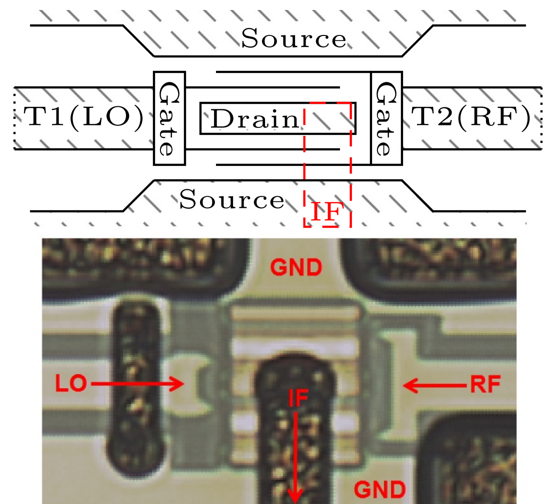

FIGURE 3 The simplified schematic of the single transistor cell (top) and a magnified photograph of the section of the chip. Here dashed red is the airbridge that is used to apply the IF to the drain of T1

Version 1 is a resistive load, a 150-Ω resistor in series with the DC supply. This is a simple, robust and frequency-independent measure for decoupling. The higher the resistance, the better the decoupling will become. Also, the necessary drain voltage and the power dissipation in the resistor will increase. About 150 Ω is proved to be a good compromise between those parameters.

Version 2 is an active load. The active load is realised by connecting the gate of a normally on transistor with its source. In the employed technology, $V_{gs} = 0$ does not represent the bias condition for maximum gain. The source is then connected to the drain of the dual-gate transistor via TL4. The drain voltage is fed to the drain of the active load. Due to its non-linear channel resistance the active load is able to conduct the same current, but it creates a lower DC voltage drop. Thereby, the overall necessary drain voltage can be reduced for the same drain current and the same decoupling. To match the resistive load with its 150 Ω, a four-finger transistor with a gate width of 20 μm was chosen. The resulting real part of the input impedance, Z_{in}, presented to the circuit by the active load was extracted by an S-parameter simulation and using

$$Z_{in} = \frac{1 + S_{11}}{1 - S_{11}} \cdot Z_0 \tag{1}$$

where Z_0 is the reference impedance of the simulation. The results are shown in Figure 4. The inlet in Figure 4 visualises the point of extraction of Z_{in} within the circuit for better understanding.

For low IF frequencies up to 10 GHz, the active load shows a resistance between 140 and 160 Ω. For higher frequencies the quality of the decoupling decreases to 60 Ω at 30 GHz due to the parasitic capacitances. This affects the overall achievable bandwidth of the circuit. For the range of the LO and RF frequencies the decoupling network presents a very low resistance of 2 Ω and therefore acts like a bypass.

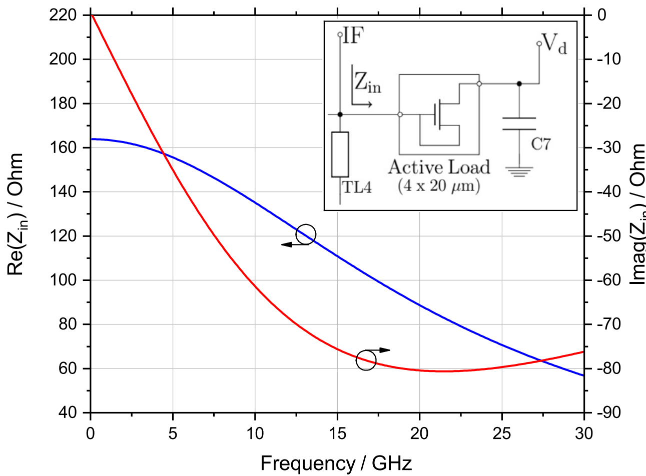

FIGURE 4 Simulated real and imaginary part of the impedance of the active load over frequency. The schematic in the inlet visualises the point of extracting the input impedance Z_{in} of the active load

The overall port matching for all four versions is similar. The simulated results for AL1 were already discussed in [16] and are shown in Figure 5.

For the LO and RF reflection coefficients the frequency was swept from 200 to 280 GHz, for the IF from DC to 35 GHz. The LO is matched more narrowly for a minimum reflection of less than −40 dB at 240 GHz since the LO is fixed at that frequency for the targeted application. Nonetheless, the frequency range where the LO lies below −10 dB is from 235 to 245 GHz to make the circuit more stable with respect to fabrication tolerances which might lead to a shift of the optimum in frequency. By exchanging the active load with the resistive one, the LO matching becomes more broadband and the IF matching improves by 3 dB.

The active dual-gate mixer was primarily selected because of the low requirement of LO power especially when compared to a resistive mixer. This is due to the different mixing principles that are applied in the two mixer types. In a dual-gate mixer the mixing is based on a variation of the transconductance of T2. This is achieved by varying its drain voltage which in turn is achieved by applying a signal to the gate of T1. If the gate of T1 is biased properly, already a small change in the gate voltage, that means a small LO signal, can have a large impact on the transconductance of T2 [19].

The resistive mixer, on the other hand, uses the variation of the transistor's channel resistance to produce intermodulation products. That means the transistor behaves like a time-varying resistance. There is no drain voltage applied; the larger the input signal at the gate , the larger will be the variation of the channel resistance. This is true until the voltage swing is large enough to drive the gate voltage below the threshold voltage, where the channel presents an open circuit, and above the maximum gate voltage, where the channel is close to a short. In

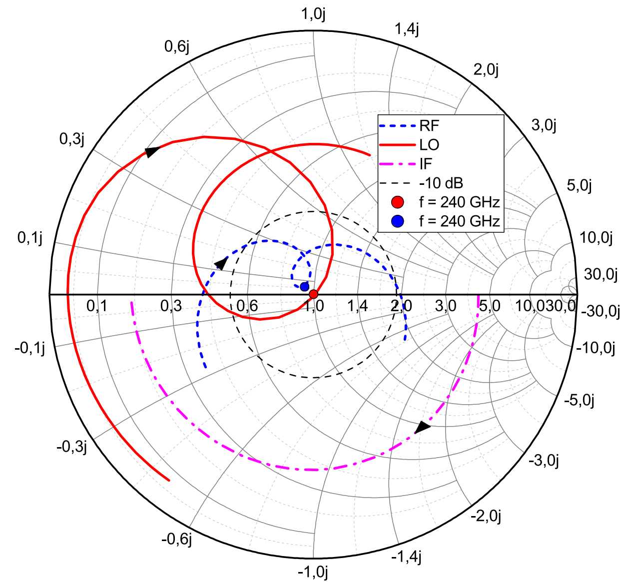

FIGURE 5 Simulated port matching of AL1 for LO (200–280 GHz), RF (200–280 GHz) and IF (DC–35 GHz). The dashed black line shows the −10 dB-circle as reference. The reference impedance is 50 Ω. [16]

this state the mixer can be represented by a time-varying switch. In order to achieve the maximum conversion gain, the voltage swing has to be large enough to maximise the change in the channel resistance, hence the high necessary LO drive power [20].

A chip photograph of version AL2 is shown in Figure 6.

The overall chip size is 1000 μm x 750 μm including RF and DC pads. The active area amounts to 300 μm x 400 μm including the large RF bypass capacitors. Excluding those, the active area reduces to only 300 μm x 300 μm.

2.2 | Resistive mixer

The schematic representation of the passive mixer is given in Figure 7.

The centre of the resistive mixer is formed by a two finger transistor with a gate width of 20 μm. The LO is applied to the gate of the transistor. In order to match the LO input to 50 Ω, TL2–TL5 and the capacitors C1 and C2 form the input matching network. TL3, TL5 and TL6 in combination with C3 decouple the gate voltage supply from the high frequency path.

The IF and the RF are both connected to the drain. TL7–TL10 with C5 and C4 form both a diplexing and matching network. That means a low-pass is presented looking in the direction of the IF port and a high-pass for the RF port. The resistive mixer was designed for a 260-GHz LO frequency and a 50-GHz RF bandwidth from 235 to 285 GHz. The simulated return loss for all three ports is shown in Figure 8.

The reflection coefficient at the LO port is well below −10 dB from 225 to 300 GHz.

The return loss of the RF is above 10 dB for the entire simulated frequency range 235–285 GHz. Although the same problem with matching the IF due to the low frequencies is true for the resistive mixer, the intrinsic impedance presented by the drain of the mixer already shows good matching. Therefore, the IF is well-matched (<−10 dB) up to 25 GHz and does not exceed −8 dB even at 35 GHz.

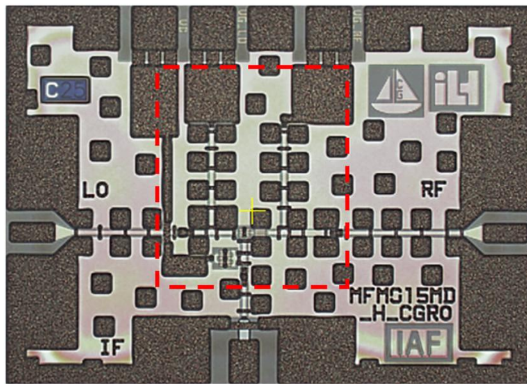

FIGURE 6 Chip photograph of the dual gate-mixer version with active load and a double transistor cell (AL2). The chip size is 1000 μm x 750 μm with an active area of 300 μm x 400 μm (dashed red)

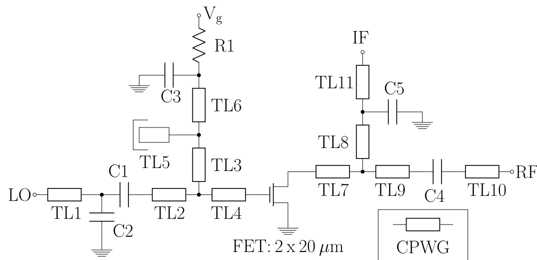

FIGURE 7 The simplified schematic of the resistive downconverter

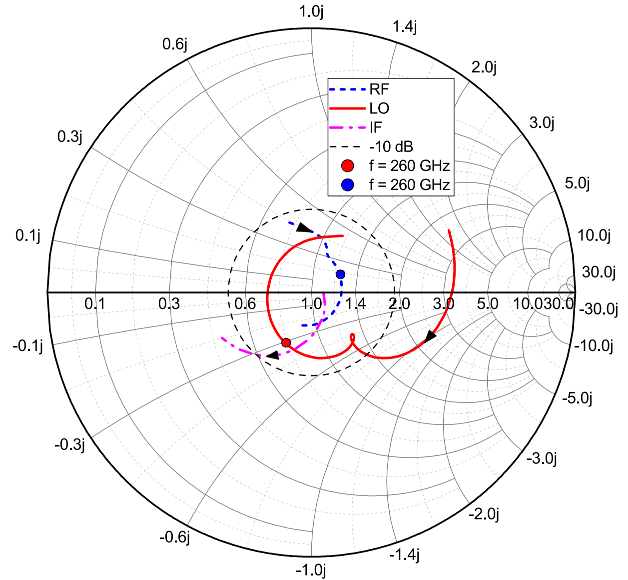

FIGURE 8 Simulated port matching of the resistive mixer for LO (200–300 GHz), RF (200–300 GHz) and IF (DC–35 GHz). The dashed black line shows the −10 dB-circle as reference. The reference impedance is 50 Ω

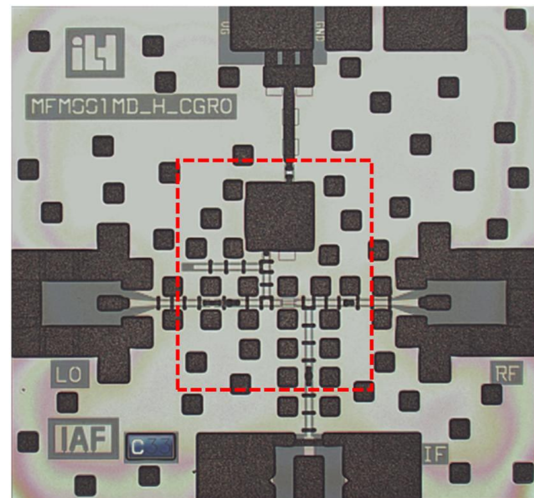

FIGURE 9 Chip photograph of the resistive mixer. The size of the chip is 1000 μm x 1000 μm with an active area of 400 μm x 400 μm (dashed red)

A photograph of the chip is shown in Figure 9. The overall chip size is 1000 μm x 1000μm. However, this includes large RF and the DC pads. The active chip size is 400 μm x 400 μm.

3 | MEASUREMENT SETUP

The active dual-gate millimetre-wave monolithic integrated circuit (MMIC) was characterised in an on-wafer testing environment. To excite the 240 GHz LO, a signal was first generated at 10 GHz. This signal was fed to a chain of frequency multipliers with an overall multiplication factor of 24. To increase the output power an IAF in-house H-band amplifier was used as the output stage. For the RF signal generation, a synthesized sweeper (10 MHz–50 GHz) with a frequency multiplication factor of 8 was used. Both the RF and LO signals were applied to the device under test (DUT) via H-band waveguides (WR-3) and on-wafer measurement probes. The lowest applicable RF frequency of the measurement setup was 220 GHz. The extracted IF output signals were evaluated using a signal analyser. To avoid power flowing from the drain bias into the input port of the signal analyser an external DC block was used.

A careful power level calibration was conducted over the desired frequency range using power meter measurements at the waveguide outputs which are connected to the on-wafer probes. To shift the reference plane to the tip of the RF probes, the losses of the probes were taken from the data-sheet and included in the calibration.

The resistive downconverter was measured using a similar setup where just the input frequencies were shifted to generate an LO at 260 GHz and an RF ranging from 235 to 285 GHz. The resistive mixer was only characterised down to a minimum RF frequency of 235 GHz. The maximum available power for this measurement was −2 dBm.

4 | MEASUREMENT RESULTS

Figure 10 shows the measured conversion gain of the four active mixer versions versus the LO input power at an LO frequency of 240 GHz and a RF frequency of 241 GHz. All measurements were conducted with a low RF power of −25 dBm to ensure linear conversion gain behaviour.

The maximum achieved conversion gain was −4.8 d B for RL2 at an LO input power of 0 d Bm. The corresponding single-transistor version has a less steep gain curve. Therefore, it exhibits higher conversion gain at lower LO input powers. Already at −10 dBm, a conversion gain of −8.5 dB was achieved. The maximum gains lies at −5.6 dB for −3 dBm input power.

The versions with the active load did not perform very well. They have the same gain shape as their counterparts with resistive load but show a lower conversion gain. The curve of the single transistor version, AL1, is shifted by around 2 dB to lower values, and AL2, by 4 dB.

The conversion gain over RF frequency of the dual-gate mixers is compared in Figure 11. For all four measurements, the LO power was set to the value that showed the maximum conversion gain, which means for RL2 and AL2 it is 0 dBm and for RL1 and AL1 it is −2 dBm. The LO frequency was kept at 240 GHz and the RF power at −25 dBm.

As expected, RL2 exhibits the highest conversion gain near the carrier frequency and AL2 the lowest. For all versions of the active mixer, the conversion gain in the lower sideband only decreases by around 1 dB. The upper sideband shows a steeper descent, especially for AL2. This leads to the assumption that the RF matching for the higher sideband is not as good as simulated in Figure 5 and the optimum might have shifted to lower frequencies. This shift in frequency could

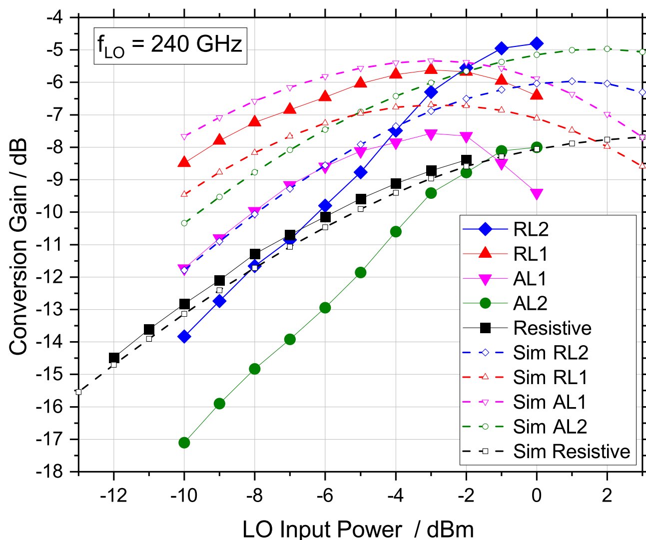

FIGURE 10 Measured and simulated conversion gain versus LO input power at an IF frequency of 1 GHz, an RF power of −25 dBm and an LO frequency of 240 GHz for the active dual-gate downconverters and 260 GHz for the resistive mixer

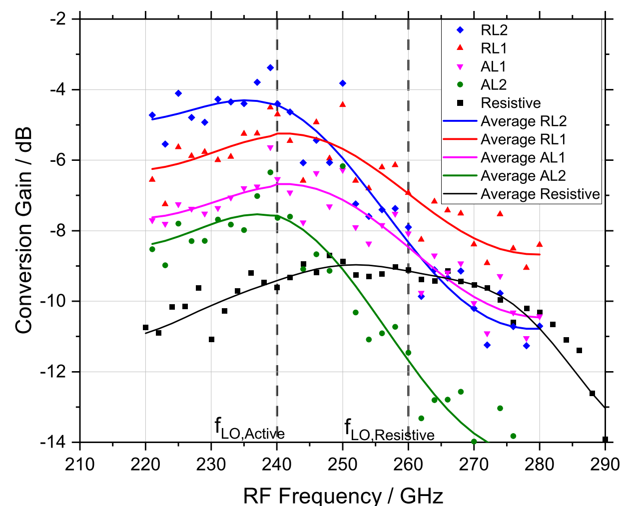

FIGURE 11 Measured conversion gain versus RF frequency at an RF power of −25 dBm and an LO frequency of 240 GHz for the active dual-gate downconverters and 260 GHz for the resistive mixer. An average of the curves was generated for better visualisation

also explain the ripple on the measured results. The calibration, that was performed, is prone to deviation caused by a mismatch between the DUT and the measurement setup. Depending on the magnitude of mismatch between setup and DUT, a ripple on the measurement results will be the consequence. For example, a 15-dB probe match and a 10-dB return loss will lead to a ripple of ± 0.5 dB. For a 15-dB probe match and a deteriorated DUT return loss of 4 dB, the overall error range would be around ± 1.5 dB.

Because the measurement setup was limited to a lowest frequency of 220 GHz, the lower corner of the 3-dB bandwidth for all four downconverters could not be determined. The resulting measured 3-dB bandwidths of the four versions are given in Table 2.

Figure 10 also shows the behaviour of the conversion gain of the resistive mixer over LO power at an LO frequency of 260 GHz and an RF input power of −30 dBm. The maximum LO power of the measurement setup is not sufficient to drive the mixer in saturation. The highest measured conversion gain lies at −8.4 dB for an LO power of −2 dBm. The simulation shows a very good agreement with the measurement, and predicts saturation at 3 dBm LO input power with a conversion gain of −7.6 dB.

The resistive mixer exhibits a flat conversion gain curve over RF frequency as shown in Figure 11. The 3-dB bandwidth exceeds the measurement range at the lower sideband and amounts to 65 GHz ranging from 220 to 285 GHz.

Additionally, measurements of the active mixer with resistive load were conducted for a different LO frequency of 220 GHz with the same setup. Figure 12 shows the conversion gain versus LO power.

Still RL2 exhibits the highest conversion gain. It reaches almost zero loss at an LO power of −1 dBm. RL1 achieves −3 dB at the same LO power. The effect of a declining conversion gain did not occur.

The RF frequency behaviour of RL1 and RL2 for an LO of 220 GHz is shown in Figure 13. Due to the limitation of 220 GHz as the lowest RF frequency, only the upper sideband of the mixer was measured.

The single sideband 3-dB bandwidth in these cases is larger than 20 GHz. For RL2, 24 GHz was measured while it was 35 GHz for RL1.

5 | DISCUSSIONS OF RESULTS AND COMPARISON WITH A RESISTIVE MIXER

5.1 | Influence of the transistor layout

In Figure 10, a similar behaviour can be observed for both the resistive and the active load version: For the single transistor layout the conversion gain at lower LO input power is noticeably higher, starts to saturate earlier and hits a maximum at −3 dBm. Also, the conversion gain is decreasing for higher LO power. As can be seen in Figure 10, the double transistor versions saturate at 0 dBm which is the maximum available LO input power. Therefore, no clear statement can be given if the effect will also take place in the measurements at higher LO powers for this design. Simulations shown later will predict that it does.

The decrease of input power is unusual for a dual-gate mixer, where the operation principle is of multiplicative mixing and not additive mixing. In additive mixing such a behaviour can be traced back to a reduction of the conduction angle due

TABLE 2 3-dB bandwidth for all four versions of the dual gate-mixer at an LO frequency of 240 GHz

RL2	RL1	AL2	AL1
38 GHz	48 GHz	31 GHz	52 GHz

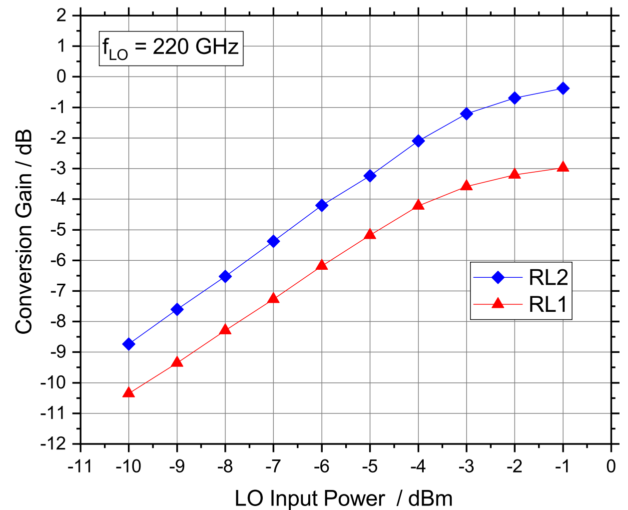

FIGURE 12 Measured conversion gain versus LO input power at an IF frequency of 1 GHz, an RF power of −25 dBm at an LO frequency of 220 GHz for the active dual-gate downconverters

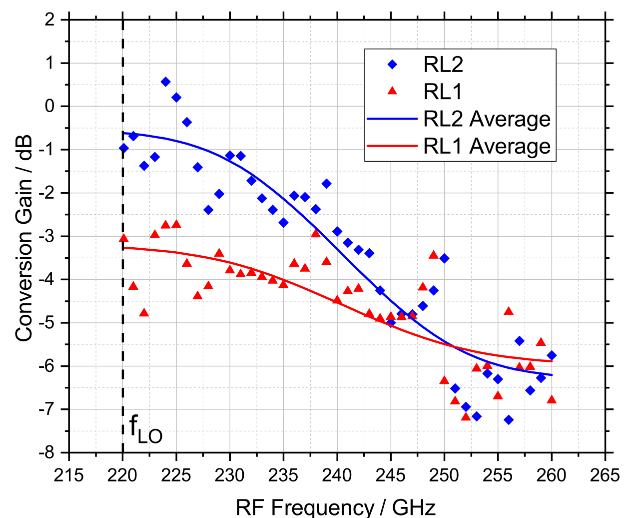

FIGURE 13 Measured conversion gain versus RF frequency at an LO power of 0 dBm, an RF power of −25 dBm and an LO frequency of 220 GHz for the active dual-gate downconverters. The average of the curves was generated for better visualisation

to the high voltage swing of the LO signal. But for a large voltage swing, the dual-gate mixer enters a quasi-switching mode of operation, where the conversion gain saturates. In theory, increasing the LO power has no further influence on the conversion gain.

To answer the question why the conversion gain drops, a closer look at the differences in the layouts of the mixers and the voltages at certain nodes is necessary. Simulating and extracting the time domain voltage signal at the gate of T1, the gate where the LO is applied, is a first indication. In Figure 14, the time domain voltage signals of both AL1 and AL2 are given.

Ideally, only the LO sine wave should be present. This is true for low LO power levels. But, increasing the LO power, distortions of the sine wave become visible. For example, at 2 dBm, the positive amplitude of AL1 (solid black line), decreases by around 15 % and the rising edge is 'dented'. Its phase is clearly shifted. However, for AL2 at 2 dBm (solid red line) the amplitude only decreases by around 5 %, but also a phase shift is visible. The gate voltage of AL1 deviates visibly more from the desired sine wave than that of AL2. For higher LO power, the time domain signal of AL2 gets distorted too. At 5 dBm (dotted red line), it is cropped as well during the positive half wave of the sine. This is an indicator for harmonics present at the gate.

For harmonic frequency components to occur in the gate voltage, a feedback of the output signal of the transistor to the gate must take place. To suppress that feedback, an ideal filter is introduced directly at the drain. It presents a short exclusively to the fundamental LO frequency. Filtering out the LO at the drain leads to the disappearance of the distortion in the gate voltage of T1 (black and red dashed line).

The simulation of the conversion gain versus LO power of all four mixer versions with and without the ideal filter is shown in Figure 15. A visualisation of the configuration with the filter is shown in the inlet.

The simulations predict a similar behaviour as measured. The single transistor versions AL1 and RL1 have a higher conversion gain for lower power levels start to saturate earlier and then decrease. The decrease in conversion gains is also visible for the double transistor versions; however, it starts at a 6 dB higher LO power. In simulations, the active load mixers, AL1 and AL2, perform better than their resistive load counterparts. However, in the measurements it is vice-versa. The next section will give the reason for this.

The most important observation here is, that after introducing the filter, the behaviour of the conversion gain now matches the theoretical behaviour with a linear increase and a saturation for higher LO powers. No decrease in the conversion gain takes place.

The difference of AL1 and AL2, besides layout of the transistor cell, lies in the manner in which the IF is connected to the drain of T1. This can also be seen in Figures 2 and 3. In the single transistor cell, version the IF is fed to the drain by an airbridge in comparison to the double transistor cell version, where it is done via a coplanar wave guide. The latter one has the advantage of a better defined characteristic impedance. Furthermore, the length from the drain of T1 to the connection of the load, depicted as TL4 in Figure 1, decreases by around 10 μm from 35 to 25 μm. These small changes are enough to change the suppression of the fundamental and harmonics of the LO at the drain and cause a significantly different behaviour of AL1 and AL2 or RL1 and RL2, respectively.

By decreasing the LO frequency, the wavelength increases. The absolute difference in length of TL4 for AL1 and AL2 or RL1 and RL2 is constant. But the relative difference in terms of electrical length of TL4 between the two version decreases. This leads to the more similar characteristic of the single and

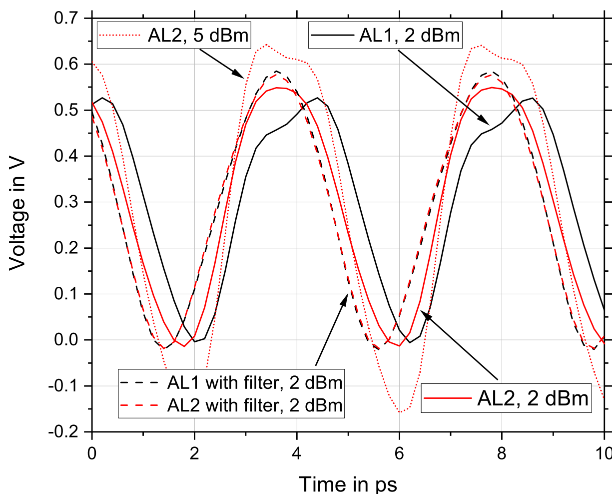

FIGURE 14 Simulated time domain signal of the voltage at the gate of transistor T1 for AL1 and AL2 at an LO power of 2 dBm with (dashed line) and without (solid line) filtering of the fundamental at the drain of T1. Red, dotted: time domain signal of AL2 at a higher LO power level of 5 dBm

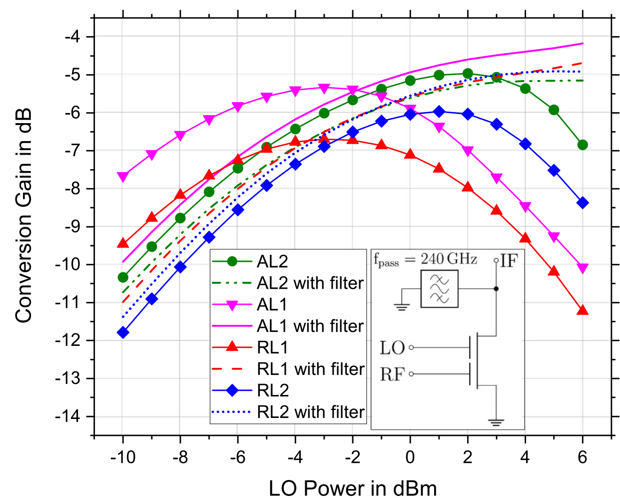

FIGURE 15 Simulation of the conversion gain with and without the LO filter at the drain for all four downconverter versions AL1, AL2, RL1 and RL2 for an LO frequency of 240 GHz and an RF power of −25 dBm. The inlet shows the configuration with band-pass filter

double transistor cell versions at 220 GHz (Figure 12) than at 240 GHz (Figure 10).

Therefore, for future designs a higher focus has to be put on the modelling of the IF connection. By using a load-pull analysis and an optimum termination for the fundamental and its harmonics, this effect might be used to reduce the necessary LO power even further.

5.2 | Influence of the load

According to Figure 10, the overall conversion gain of the circuits with an active load is lower than with a resistive load. Simulations of the circuits, as shown in Figure 15, did not lead to the same result as the measurement. Since only the load was exchanged and the rest of the circuitry was kept constant, the reason for the deterioration has to be found within the active load transistor.

It was observed that the drain current decreased by around 15% by employing the active load both for the single and the double transistor version. The active load was designed in order to maintain the same DC drain current in the active load dual-gate mixer as it was before in the resistive load version. The lower drain current is an indicator that the channel resistance of the active load, R_{DS}, is different with that of the simulation. A higher resistance also leads to a larger voltage drop over the active load and a lower drain voltage supplying the dual-gate mixer. To model this effect and to verify the assumption a serial resistor was introduced in the drain supply path. The resulting plot is shown in Figure 16.

Although this is just a first-order approximation, it reproduces the effect from Figure 10 quite well. While a higher resistance in the drain path could have been compensated by a higher drain voltage, this is not possible for the active load since the drain current is already saturated for the given drain voltage and does not increase linearly any more.

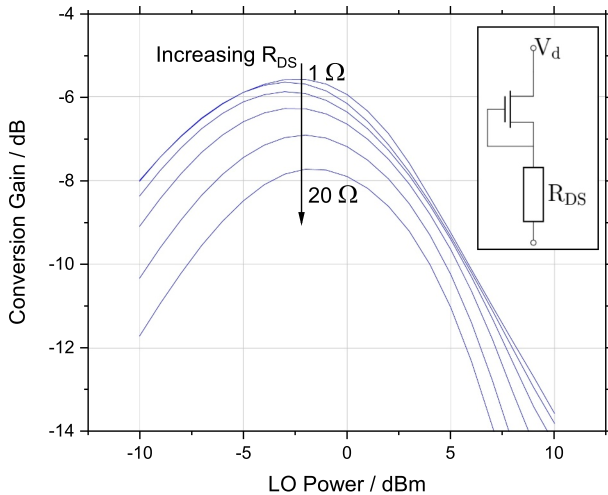

FIGURE 16 Simulated conversion gain of the mixer AL1 versus the LO power for different serial resistances. The simplified schematic of the configuration with the serial resistor is shown in the inlet

5.3 | Comparison with the resistive mixer

To generate the local oscillator signal in H-band, usually the frequency multiplier MMICs are used. A single stage frequency multiplier by two or three as proposed in [21] would be sufficient to drive the active mixer, RL1, and can still have a higher conversion gain as the resistive mixer in saturation requiring 3 dBm of LO power as observed in Figure 10. For the resistive mixer, an additional amplification stage has to be integrated to generate the necessary LO power. The advantage of a low necessary LO power of the active mixer becomes even more impressive for more complex systems, like communication receivers, where several mixer cells are used in parallel for quadrature modulation and demodulation, and in balanced designs.

For two parallel stages a nominally 3 dB higher LO power is necessary and for four parallel stages, even 6 dB, excluding the losses of the couplers which cannot be neglected in the mmW regime, is required. In total, this leads to a need for large buffer stages following the frequency multiplication to drive the mixer stage, as for example presented in [22] and [10]. These drivers can occupy up to half the chip space of the entire receiver. Additionally, the buffer amplifier not only adds length to the overall chip size but might also increase its height since transistors have to be parallelised in order to achieve high output power. Altogether, large chip sizes and extreme aspect ratios lead to the challenges in circuit design and the problems in mechanical chip handling and packaging as already described in Section 1.

Thus, replacing the resistive mixer in a receiver/transmitter and therefore getting rid of the large LO buffer stage not only reduces the chip size and the costs, but also increases the efficiency of the chip.

In case of [22] in the same technology the total receiver consumes 295 mW of DC power and 200 mW fall upon the LO buffer amplifier. The active dual-gate mixer with a resistive load needs 55 mW per mixing stage so 110 mW in a quadrature receiver. By employing the mixer 'RL1' in the proposed topology of [22] the necessary chip area cannot only be cut in half but also the necessary DC power.

The mixer with an active load consumes even less, only 20 mW. Therefore, by changing the load to an active load, the overall DC power is only a fifth compared to the resistive approach and still achieving a better conversion gain.

A valid argument for resistive mixers is the high linearity that can be achieved.

Since no measurement was conducted on this version, simulations will be used for this discussion. This approach is not unusual as can be seen later in the state of the art and is due to a lack of high power sources in H-band. For a linearity measurement, not only a high LO power must be generated but additionally requires a high RF power to saturate the mixer. However, the simulated values of the resistive mixer show a good resemblance to measured values from other publications with similar architectures [13,14] which supports the validity of the transistor models and the simulations.

Figure 17 shows the conversion gain and the IF output power in dependency of the RF power. The version RL1 was chosen for this simulation, but the results do not change drastically for the other versions. Especially the output referred 1-dB compression point, OP_{1dB}, remains constant while the input referred 1-dB compression point, IP_{1dB}, shifts to higher input powers due the lower conversion gain.

The curves prove the statement of a higher linearity of the resistive downconverter. When the resistive mixer is driven in saturation with an LO power of 3 dBm, the achieved IP_{1dB} is 3 dBm, leading to a OP_{1dB} of −6 dBm.

The corresponding OP_{1dB} of the dual-gate mixer lies at 7.5 dB below that at −13.5 dBm which corresponds to a IP_{1dB} of −7 dBm.

However, for communication receivers, the prerequisites of linearity are in general more relaxed. In a transmitter, the input signal is generated in the baseband where high power levels are easy to achieve. In contrast, transmitted output powers in H-band are generally low as already explained in the introduction. Secondly, the large free space path loss reduces the RF power even further. Therefore, the resulting RF-input power levels, which need to be handled by the receiver, are typically very low.

Additionally, in a communication receiver the RF input signal has to be further distributed to the I and Q channel. Assuming an ideal power divider, the power per mixer cell is hereby reduced again by 3 dB and because of this, the overall IP_{1dB} increases by 3 dB. Therefore an I/Q receiver with the presented active mixer and a 20- dB LNA still operates in a 10 - dB back-off from the IP_{1dB} for a high input power of up to −34 dBm. This power corresponds to the received power given in [23] for an electronic transmitter with an output power of −7 dBm, operating at 300 GHz, transmitting over 0.5 m using a QPSK modulation format.

In the case of systems with high receiving power, for example radar systems, the lower linearity might be a concern and the resistive mixer is clearly the better choice.

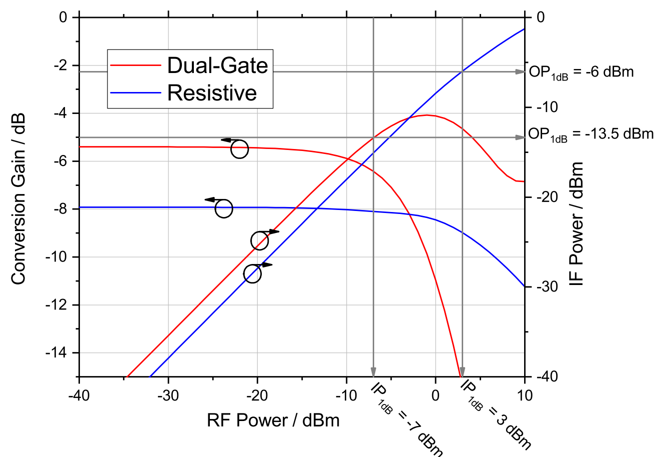

FIGURE 17 Simulated conversion gain and IF outputs in dependency of RF power for the active mixer RL1 and the resistive mixer. The input and output referred as the 1-dB compression point is marked with grey lines in the plot

Simulation showed that the noise figure of the dual-gate mixer employing an active load is around 16 dB. This is 6 dB higher than the noise figure of its passive, resistive counterpart. The simulation of the single sideband noise figure versus the LO power is shown in Figure 18.

The behaviour of the noise figure clearly follows the conversion gain curve. Assuming an approximately constant noise contribution of the transistors and the passive components, increasing the signal level at the output translates directly into an improvement of the noise figure. As can be seen in Figure 18, the lowest noise figure is achieved where the conversion gain is at its maximum.

To improve the overall system noise figure LNAs are used. But, due to the lower linearity, the applicable gain is limited. Figure 19 shows the contribution of the mixer noise figure to the total receiver noise figure at maximum conversion gain.

The influence is calculated using Friis' formula for noise of cascaded stages,

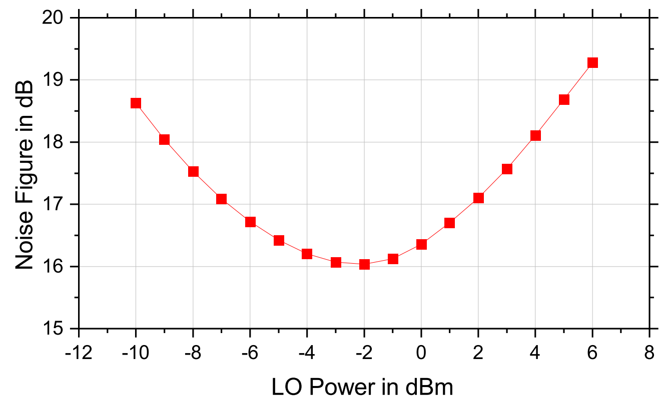

FIGURE 18 Simulated single side band noise figure of the mixer AL1. The noise figure was evaluated at the IF output at 1 GHz which corresponds to the LO and RF input frequencies of 240 and 241 GHz,

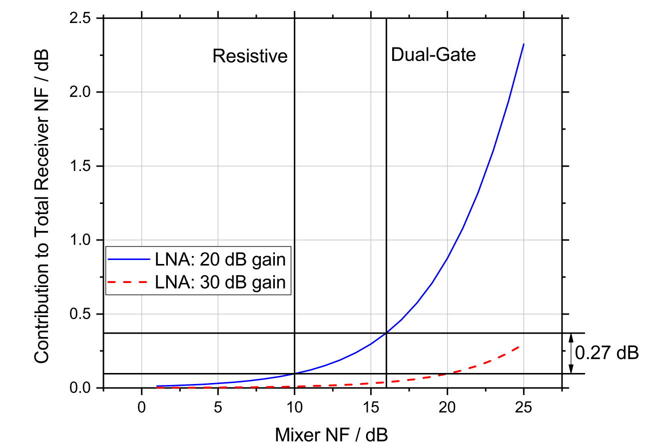

FIGURE 19 Contribution of the mixer noise figure to the total receiver noise figure in dependence of the latter for two different LNAs with 20 and 30 dB gain and a 6.5 dB noise figure

TABLE 3 Comparison of state-of-the-art H-band mixers

Ref.	RF BW (GHz)	f_{LO} (GHz)	CG (dB)	P_{LO} (dBm)	IP_{1dB} (dBm)	OP_{1dB} (dBm0	DC Power (mW)	Topology	Technology
[14]	N/A	209	−8.7	1.5	0[1]	−10[2]	0	Resistive mixer	100 nm mHEMT
[13]	30	270	−15	5	−1	−16	0	Resistive mixer	80 nm InP-HEMT
[24]	33	290	−18	2	N/A	N/A	416[6]	Buffer + x3 + resistive mixer	40 nm CMOS
[25]	30	300	−15	−5	N/A	N/A	N/A	Half Gilbert cell mixer	250 nm InP HBT
[26]	12 (IF BW)	240	8[3]	5	N/A	N/A	915[6] (30.4[7])	x16 + buffer + I/Q-mixer + antenna + BB amp	130 nm SiGe HBT
[27]	N/A	240	11[3]	−16	−7[4]	3[2]	160[6]	LO amp + SH[5] Gilbert cell + IF buffer	130 nm SiGe BiCMOS
[28]	55	240	13[3]	−10	−12[4]	0[2]	500[6]	x4 + x2 + LO amp + Gilbert cell + BB amp	130 nm SiGe BiCMOS
This work									
RL1/RL2	52/38	240	−5.6/−4.8	-3/0	−7[4]	−13.5[4]	55/55	Dual-gate mixer,	35 nm
	30/25 SSB	220	−3/0	−1			55/55	Resistive load	mHEMT
AL1	52	240	−7	−3	−6[4]	−14[4]	20	Dual-gate mixer, Active load	35 nm mHEMT
Resistive	65	260	−8.4	−1	3[4]	−6[4]	0	Resistive mixer	35 nm mHEMT

[1]Operating as upconverter.
[2]Calculated from IP_{1dB} and CG.
[3]Including IF buffers.
[4]Simulated.
[5]Subharmonic.
[6]Total power consumption of full topology.
[7]Halved power consumption of I/Q downconversion stage.

$$NF|_{dB} = 10 \cdot \log_{10}\left(F_1 + \frac{F_2 - 1}{G_1}\right) \tag{2}$$

The first term, F_1, is the contribution of the LNA to the overall noise figure. The second term reflects the influence of the mixer noise, F_2. Two LNA versions with a different gain, G_1, of 20 and 30 dB were simulated. For both, a noise figure of 6.5 dB was assumed which is a state-of-the-art value for InGaAs-mHEMT MMICs in H-band [12].

Especially the difference between the 10 and the 16 dB downconverter noise figure is of interest. In simulation, the load has only a very small influence on the noise of the active mixer. The delta in noise figure for the active and the resistive mixer is only 0.3 dB for the 20 dB LNA and even lower, 0.1 dB for $G_1 = 30$ dB. From these results, it can be concluded that the higher noise figure of the presented active mixer will have only a neglectable impact on the overall noise figure of a typical receiver, at least in this particular technology.

6 | STATE OF THE ART

Table 3 gives an overview of state-of-the-art mixers in H-band. Unfortunately, for systems where the downconverter was integrated with amplifiers, not all figures of merit could be extracted or were given by the authors which make a fair comparison hard to achieve. To avoid confusion, the given RF bandwidth is the bandwidth for a fixed LO with a swept RF frequency as shown in Figures 13 and 11, not a simultaniously swept RF and LO resulting in a fixed IF. For a homodyne communication system this bandwidth limits the overall possible data bandwidth and is therefore considered of more interest.

Single stage passive mixers for H-band are reported in [13] and [14]. The resistive mixer presented by the authors outperforms these in terms of conversion gain, bandwidth and necessary LO power.

Even with a lower bandwidth than the presented resistive mixer, the active dual-gate mixers, RL1, RL2 and AL1, exhibit a higher bandwidth than the cited passive state of the art at a lower LO input power.

Active mixers are presented in [25], [26], [27] and [28]. Not only the conversion gain achieved in [26] and [25] is lower compared to the presented mixers, but also the RF bandwidth of these circuits is limited to 12 GHz and 32 GHz, respectively. Neither a statement on linearity nor on noise figure was given in these publications. [27] and [28] present a high conversion gain at a good LO input power. However, both employ additional IF amplification without stating any gain partitioning for the stages. Unfortunately, [27] gives only a bandwidth for a swept LO with a fixed IF because the targeted application is radar. The circuit in [28] has a bandwidth of 55 GHz and is therefore slightly more broadband than the presented circuits.

The presented resistive mixer performs the best in terms of compression. The presented active mixers are in the same range as the state of the art or slightly better.

Please note that the DC power consumption in Table 3 always refers to the full topology. This might include several additional stages for LO generation which increase the overall necessary DC power. The power dissipation for a single frequency conversion stages is added in brackets if published in the reference. Since a fair comparison is hardly possible in these cases, the values for the fully integrated circuits are given for the sake of completeness and not for a comparison.

7 | CONCLUSION

The authors present four versions of an active dual-gate downconverter in H-band, with a centre RF frequency of 240 GHz. The mixers employ two different implementations of the load, which is used to decouple the IF path from the drain bias. Additionally, two layout versions of the dual-gate transistor are compared—a single and a double transistor cell. With an LO of 240 GHz, the version with the single transistor cell and resistive load exhibits a very good conversion gain of −6 dB at a low LO power of −2 dBm. The corresponding version with a dual transistor cell achieves an even better conversion gain of −5 dB at a slightly higher LO input power of 0 dBm. This opens up great opportunities to decrease the demand of chip-space and to reduce the overall DC power consumption of conventional receivers in InGaAs technology.

The maximum measured 3-dB bandwidth was 52 GHz which makes the mixer suitable for high data-rate communication systems. The versions with an active load achieved a lower conversion gain but at the same time reducing the necessary DC power by half. Additionally, the observed effect of declining conversion gain for high LO powers in the single transistor mixers was explained and traced back to its root. For future designs this can be used to optimise the behaviour of the dual-gate mixer for even a less LO power.

Furthermore the resistive load versions were also characterised for a 220-GHz LO. Here the double transistor version exhibits a peak conversion gain of around 0 dB at an LO power of 0 dBm with a single sideband 3-dB bandwidth of 25 GHz. The single transistor solution has, on the one hand, a lower conversion gain of −3 dB, but, on the other hand, a higher SSB bandwidth of 30 GHz. Additionally, a case study of the impact of the mixer noise figure on a typical receiver was given for different scenarios using a 20 and 30 dB LNA. It can be concluded that the influence of the active dual-gate mixer can be neglected.

Eventually, the active mixer was compared to a state-of-the-art resistive mixer in a similar frequency range and in the same technology. By using the presented active mixer instead of a resistive one, it is not only possible to reduce the chip area of receivers immensely but also the DC power consumption by making a large LO buffer amplifier obsolete.

To the best of the authors' knowledge, this study is the pioneer in the implementation and detailed analyses of not only the dual-gate mixer concept in H-band, but also of the usage of active loads in the same technology for millimetre-wave circuits.

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