Presented at the 22nd European Photovoltaic Solar Energy Conference and Exhibition, 3 - 7 September 2007, Milan, Italy

INVESTIGATION ON GETTERING OF IMPURITIES DURING PHOSPHORUS DIFFUSION IN MULTICRYSTALLINE SILICON

D. Schwaderer[1], S. Riepe[2], H. Habenicht[1], O. Schultz[1], W. Warta[1]
[1]Fraunhofer Institute for Solar Energy Systems (ISE), Heidenhofstr. 2, 79110 Freiburg, Germany
[2]University of Freiburg, Material Research Center, Stefan-Meier-Str. 21, 79104 Freiburg, Germany
phone: +49 (0) 7 61 / 45 88-5148, fax: +49 (0) 7 61 / 45 88-92 50, e-mail: daniel.schwaderer@ise.fraunhofer.de

ABSTRACT: In this work the influence on the gettering efficiency of varying cooling down ramps following a *phosphorus-emitter-diffusion* in a high-efficiency solar cell process is investigated. A hold-time ramp is applied at low temperature where the emitter sheet resistance remains nearly unchanged and recombination active defects are still mobile. We observed a significant enhancement of the effective minority carrier lifetime measured by the Carrier Density Imaging (CDI) and Quasi Steady State Photoconductance (QSSPC) methods. This improvement is explained by an increased diffusion of metal impurities into the gettering layer and by formation or growth of precipitates due to a lower solubility of impurities in silicon at low temperatures.
Keywords: Multi-Crystalline Silicon, Gettering, Diffusion

1 INTRODUCTION

High temperature steps like phosphorus diffusions and oxidations as they are currently used in solar cell processes are known to have considerable influence on the quality of solar grade silicon material. An important factor is the mobility of recombination active impurities predominantly represented by the 3d-transition metals at elevated temperatures.

During the diffusion with $POCl_3$ metal impurities diffuse towards the phosphorus-doped region due to a higher solubility compared to the wafer volume. In this layer as well as in precipitates these defects are less detrimental for the electrical properties of the silicon crystal than in an interstitially dissolved state.

In this paper we will use carrier lifetime measurements to investigate the influence on the material quality of varied cooling down ramps after a *phosphorus-emitter-diffusion*.

Several experiments with the objective of increasing the getter efficiency due to an improved cooling down ramp have been published [1-4]. While these authors used highly doped emitters with sheet resistances less than 60 Ω/sq, in this work a shallow emitter of 120 Ω/sq for the use in a high-efficiency solar cell process was applied.

Furthermore, a *getter-diffusion* at the beginning and an oxidation step at the end of the process were accomplished. Therefore the decisive high-temperature steps of a high-efficiency solar cell process are considered in the investigation.

2 EXPERIMENTAL

2.1 Material

For the experiments adjacent wafers (125 x 125 mm^2) of multicrystalline silicon (mc-Si) having comparable grain structure were taken out of the centre region of two different ingots (material A and C) and out of a corner column of a third ingot (material B). All ingots had a base resistivity of 1 Ωcm and were produced with the directional solidification method under industrial conditions.

The wafers were investigated within a solar cell process based on a high-efficiency process developed at Fraunhofer ISE [5]:

After removing saw damage by an acidic etch a *phosphorus-getter-diffusion* was applied to both sides of all wafers. Impurities collected in this layer were removed by etching away the diffused layer. This was followed by a wet oxidation at a low temperature of 800°C. Again a wet-chemical etch was applied to remove the oxide on the front surface. The oxide on the rear was protected and used to mask the following *phosphorus-emitter-diffusion*. After chemically etching away the phosphorus silicate glass (PSG) a thin passivating oxide on the front was grown under dry conditions.

2.2 High temperature processes and lifetime

The *phosphorus-diffusions* were performed in a tube furnace under $POCl_3$–gas atmosphere. With the *getter-diffusion* at 880°C for 45min a highly phosphorus-doped layer was reached capable of efficiently gettering mobile impurities from the volume of the wafer. To obtain an emitter for the use in solar cell application *a phosphorus-emitter-diffusion* at 810°C for 30min was accomplished and resulted in a sheet resistance of about 120 Ω/sq. A following oxidation at 840°C for 20min was applied to ensure a good passivation of the surface.

As high temperature steps are known to have huge impact on recombination active impurities in mc-Si wafers and therefore the solar cell efficiency, wafers were taken out after each crucial stage of the solar cell process (as indicated in Figure 1). The diffused layers or the grown oxide layers from the extracted samples were removed by an etching procedure. A subsequently applied SiN_x layer with excellent surface passivating properties enabled the characterisation via lifetime measurements.

To assure that external contamination could be excluded, monocrystalline silicon FZ samples were used as reference wafers.

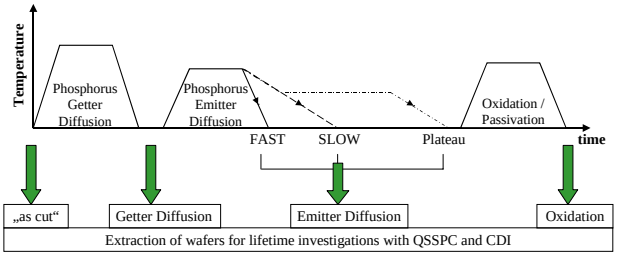

Figure 1: Decisive steps of the high efficiency solar cell process used for the experiments. Samples were extracted after the process steps as indicated and investigated via lifetime measurements.

2.3 Lifetime measurement

The effective lifetimes of the samples were determined by the QSSPC method [6]. Two measurements in the opposed corners, covering an area of about 11 cm^2 each, were averaged and evaluated at an injection level of $\Delta n=1x10^{15}$ cm^{-3} where the lifetime measurement is not affected by trapping artefacts.

With the CDI method a high spatially resolved image of the lifetime was taken [7].

2.4 Lifetime spectroscopy of iron-boron pairs

At ambient temperature interstitial iron in the boron doped silicon crystal is predominantly present as FeB pairs. These pairs can be dissociated (Fe_i and B_s) through a suitable illumination source and re-paired after storage in the dark. In both states iron shows different recombination activity due to different capture cross sections and defect energy levels in the band gap of Si. Therefore QSSPC measurements on samples after “light soaking” show significantly higher lifetimes above an injection level of $\Delta n=2x10^{14}$ cm^{-3} than measurements before “light soaking” if Fe-contamination is present. The iron concentration in the sample can then be calculated via

$$[Fe_i] = C(\Delta n, p_0) \cdot \left(\frac{1}{\tau_{Fe_i}(\Delta n)} - \frac{1}{\tau_{FeB}(\Delta n)} \right).$$

assuming that the change in lifetime is only due to iron defects. Herein τ_{Fei} and τ_{FeB} are the injection dependent lifetimes after and before illumination, respectively. C denotes an injection dependent prefactor that was also calculated from the recombination parameters of FeB and Fe_i [8].

3 RESULTS

For the wafers extracted from the solar cell process (cf. Figure 1) the minority carrier lifetime and the interstitial iron concentration in the samples were measured. The use of vertically adjacent wafers allowed determining the influence of the single high temperature steps on the lifetime. This is shown exemplarily for the Plateau ramp in Figure 2 and 3. For material C the process was investigated with the FAST ramp only.

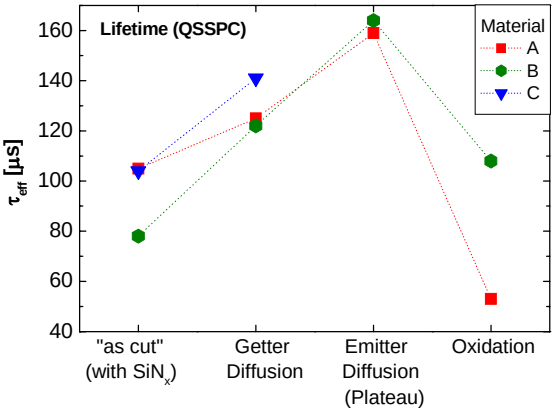

Figure 2: Development of the lifetime during the solar cell process with plateau ramp.

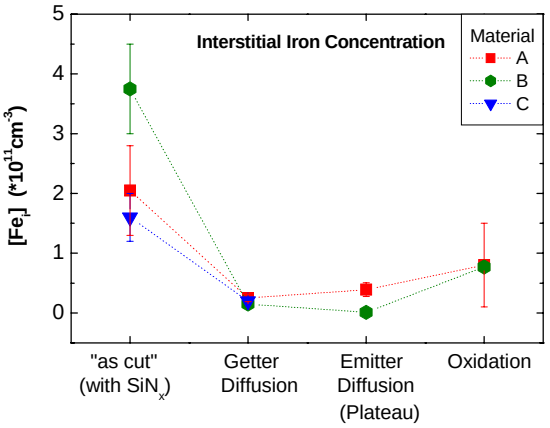

Figure 3: Successive change of the concentration of interstitial iron in samples during the solar cell process with plateau ramp. Bars indicate the variance of multiple measurements on different parts of the sample.

Getter-Diffusion. The recombination lifetime values of the “as cut” samples (with SiN_x passivation) and the sample after getter-diffusion shown in Figure 2 reveal an increase in lifetime of a factor 1.2–1.6 depending on the gettered material. This is partly due to a reduction of the interstitial iron concentration which is lowered drastically to a value of about $[Fe_i]=0.2 \times 10^{11}$ cm^{-3} (cf. Figure 3). After gettering, other defects beside interstitial iron become responsible for the limitation of the carrier lifetime although the concentration of these defects was as well reduced during the diffusion.

With the spatially resolved CDI lifetime measurement method further effects of the *getter-diffusion* can be observed.

Figure 4 shows the samples of material C before and after *getter-diffusion*. White circles indicate the area investigated with the QSSPC method. Due to gettering the minority carrier lifetime is increased in some areas where it is thought that the dislocation density is low and gettering acts efficiently. In other parts of the wafer where the lifetime is degraded contrariwise the dislocation density is thought to be high. Herein precipitates which are predominantly sited at dislocations

serve as source of metal impurities during the high temperatures of the getter-diffusion.

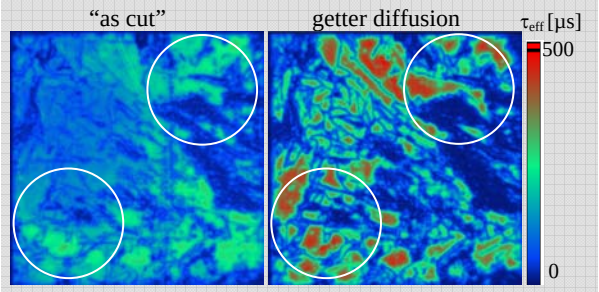

Figure 4: Samples of Material C in the "as cut"-state and after *getter-diffusion* exhibit improvement or degradation of the minority carrier lifetime depending on the investigated region on the wafer.

A significant improvement in the carrier lifetime is observed especially for the highly contaminated edges of the ingot. The edges are clearly visible in CDI image of the "as cut" sample of material B in Figure 5 and disappear after gettering.

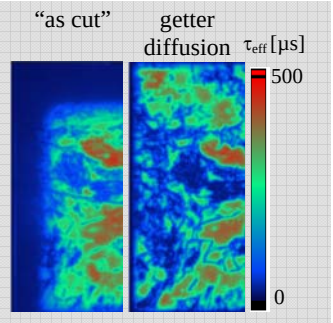

Figure 5: Part of the samples of Material B in the "as cut"-state and after getter-diffusion. The clearly visible edges of the ingot disappear after gettering.

Cooling down ramp. The high-temperature step following the *getter-diffusion* is the *emitter-diffusion* for which different cooling down ramps were applied (cf. Figure 1). The lifetimes obtained with QSSPC measurements are shown in Figure 6. Compared to the standard ramp ("Fast") a decelerated cool down increases the lifetime of carriers. This enhancing proves to be highest for the plateau temperature-time-profile in the cool-down ramp. Compared to the lifetime after *getter-diffusion* the "Plateau" ramp yields in an enhancement while the "Fast" ramp leads to a degradation (exception: material B is slightly improved).

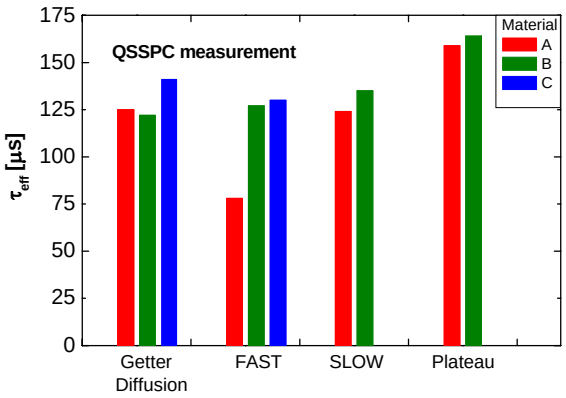

Figure 6: Lifetimes obtained after the getter-diffusion and after three cooling down ramps subsequent to the phosphorus-emitter-diffusion.

In Table I the calculated iron concentrations corresponding to the process step in Figure 6 are listed and show that the concentrations stay for all steps at a low level (exception: FAST ramp of material A).

Table I: Calculated iron concentrations and measured lifetimes of Figure 6.

	A		B		C	
	τ_{eff} [µs]	$[Fe_i]$ [$^{*}10^{-11}$ cm^{-3}]	τ_{eff} [µs]	$[Fe_i]$ [$^{*}10^{-11}$ cm^{-3}]	τ_{eff} [µs]	$[Fe_i]$ [$^{*}10^{-11}$ cm^{-3}]
"as cut"	105	2.1	78	0.8	104	1.6
getter diffusion	125	0.3	122	0.2	141	0.2
FAST	78	2.2	127	0.2	130	0.1
Slow	124	0.5	135	1.1	--	--
Plateau	159	0.4	164	0.0	--	--

Thermal degradation. In the high-efficiency solar cell process the phosphorus emitter diffusion is followed by an oxidation providing a good passivation of the front surface. This additional high temperature step results for every cooling down ramp in a reduction of lifetime (cf. Figure 7). It has been shown that high temperatures enable the out-diffusion of metal impurities from precipitates into the silicon matrix [9, 10]. This effect is suggested to be responsible for the negative influence of the oxidation. As Figure 3 shows the concentration of interstitial iron is enhanced only slightly by the oxidation and can't explain the strong decrease in lifetime further defects have to be accountable.

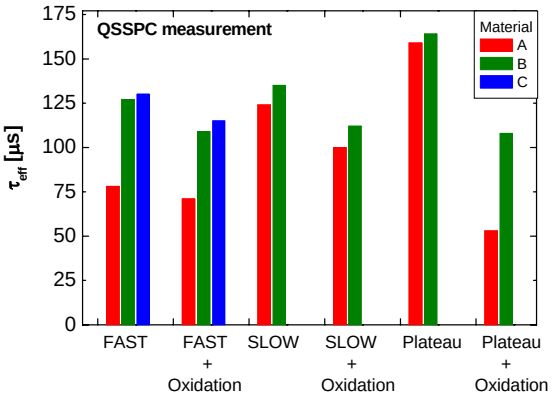

Figure 7: Minority carrier lifetimes of the samples after the cooling down ramps and the subsequent oxidation step.

4 DISCUSSION

The *getter-diffusion* applied to all samples generates a highly phosphorus-doped layer at the wafer surface. Due to the elevated solubility of metal impurities in this region the transport of metal atoms from the volume of the wafer into this layer is determined via a segregation coefficient - the ratio of the equilibrium solubilities of both areas.

With this diffusion a strong gettering effect was reached and the concentration of the fast diffusing interstitial iron atoms was reduced to 1/10 of the concentration before gettering. The interstitial iron is supposed to be transported into the gettering layer and subsequently removed from the wafer. The residual iron atoms in the sample are then predominantly present in form of precipitates.

The investigation with the spatially resolved CDI method showed that an improvement in lifetime was reached only in some parts of the sample while other parts degrade. The decrease in lifetime is explained with the dissolution of metal precipitates which are predominantly sited in areas with high dislocation density and serve as source for recombination active metal impurities.

It is suggested that during the following *emitter-diffusion* the dissolution of precipitates and the simultaneous gettering into the phosphorus-doped layer continues. In a SLOW cooling down ramp compared to FAST cooling the clustering and gettering conditions are improved. This is why higher lifetimes were reached.

With the applied temperature-time-plateau, where highest lifetimes after the emitter diffusion were achieved, two aspects of gettering are presumed. Due to the long duration of the plateau more diffusing metals can segregate into the phosphorus layer. This could be of advantage especially for slow diffusing elements. The coefficient of this segregation is enhanced because of the applied low temperature. It is assumed that these temperatures reduce the solubility for metals in the wafer volume and interstitially dissolved metals in an oversaturated state begin to form precipitates.

During the final oxidation step the carrier lifetime degrades. This might be due to an out-diffusion effect of other impurities beside iron into the silicon matrix [10, 11].

5 CONCLUSION

With a reduced of cooling down rate at the end of a *phosphorus-emitter-diffusion* the minority carrier lifetime in industrial produced multicrystalline silicon wafers is increased. An applied temperature-time-plateau in the cooling down ramp results in a lifetime improvement compared to standard (FAST) cooling of a factor 1.6.

A *phosphorus-getter-diffusion* preceding the *emitter-diffusion* reduces the concentration of interstitial iron in the silicon crystal and the lifetime becomes limited by other defects besides interstitial iron.

An oxidation step at elevated temperature subsequent to the *emitter-diffusion* has a detrimental effect for the carrier lifetime possibly due to out-diffusion of impurity atoms beside Fe from precipitates into the silicon matrix.

ACKNOWLEDGEMENTS

The authors would like to thank A. Leimenstoll and H. Lautenschlager for technical assistance. This work was supported in part by the European Commission within the “CrystalClear” integrated project.

REFERENCES

[1] J. Härkönen, V-P. Lempinen, T. Juvonen, and J. Kylmäluoma. Recovery of minority carrier lifetime in low-cost multicrystalline silicon. Solar Energy Materials and Solar Cells, **73**:125–130, 2002

[2] L. J. Geerligs and P. Manshanden. Improved phosphorous gettering of multicrystalline silicon. Solar Energy Materials and Solar Cells, **90**:998–1012, 2006

[3] Andreas Bentzen. Phosphorous Diffusion and Gettering in silicon solar cells. PhD thesis, University of Oslo, 2006

[4] J. Lossen, L. Mittelstädt, S. Dauwe, K. Lauer, C. Beneking, Making use of Silicon wafers with low lifetimes by adequate POCl3 Diffusion

[5] Oliver Schultz. High-Efficiency Multicrystalline Silicon Solar Cells. PhD thesis, University of Konstanz, 2005

[6] R. Sinton and A. Cuevas. Contactless determination of current-voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steadystate photoconductance data, Appl.Phys.Lett., **69**:2510–12, 1996

[7] J. Isenberg, S. Riepe, S.W. Glunz, and W. Warta, Carrier density imaging (CDI)-measurement principles and first applications. Journal of Applied Physics, **93**(7):4268, 2003

[8] D.H. Macdonald, L.J. Geerligs, and A. Azzizi, Iron detection in crystalline silicon by carrier lifetime measurements for arbitrary injection and doping, J. Appl. Phys. 95 (3), 1021-8 (2004)

[9] S. Riepe, O. Schultz, and W. Warta, Redistribution of recombination active defects and trapping effects in multicrystalline silicon after wet thermal

oxidation, Proceedings of the 4th World Conference on Photovoltaic Energy Conversion, Hawaii, 2006

[10] O. Schultz, S.Riepe and S.W. Glunz, Influence of High-Temperature Processes on Multicrystalline Silicon, Solid State Phenomena Vols. 95-96, 235-240, 2004