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CRYSTALLINE SIC DEPOSITED BY APCVD AS A MULTIFUNCTIONAL INTERMEDIATE LAYER FOR THE RECRYSTALLISED WAFER EQUIVALENT

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ABSTRACT: The Recrystallised Wafer Equivalent (RexWE) is an approach to substitute high purity silicon wafers with cost effective sintered ceramic compounds. This design unites the potential to significantly reduce wafer costs with very large wafer sizes. To separate the highly contaminated substrate material from the active silicon layer we implemented a crystalline 3C-SiC intermediate layer (IL), which is deposited by APCVD at 1100°C. This IL combines thermal and chemical stability above 1420°C, good electrical conductivity, textured surfaces and diffusion barrier properties against all types of metallic contaminations. The deposited SiC-IL was hereby doped with nitrogen (N_2) during the deposition and basic crystallographic, optical and electrical investigations were performed.
Keywords: APCVD Deposition, Intermediate Layer, Silicon Carbide, c-Si Thin Films

1 INTRODUCTION

1.1 The Recrystallized Wafer Equivalent

To reduce the costs of Si substrates for crystalline Silicon solar cells, the Recrystallized Wafer Equivalent (RexWE) was introduced [1]. Today, with decreasing wafer costs, this advantage is decreasing as well. Nevertheless the design of the RexWE includes a potential to escape the comparison with the Silicon-wafer as the RexWE, based on tape-cast or sintered ceramics, is not limited in size which opens new potential for cost reduction in the module.

With the introduction of crystalline siliconcarbide (c-SiC) as a multifunctional intermediate Layer (IL), the selection of possible substrate materials can be increased even further. The chemical vapor deposition at atmospheric pressure (APCVD) also allows the RexWE to be produced in large sizes with high throughput in-line tools like the ProConCVD [2].

1.2 Crystalline SiC intermediate layer

The c-SiC IL separates the active Si absorber layers from the highly contaminated ceramic substrate. This diffusion barrier needs to withstand the high temperatures during the Si deposition (~ 1150°C) and the recrystallization of the Si from the liquid phase at 1420°C.

It is furthermore necessary, that the c-SiC prevents wet chemicals from infiltrating the substrate and e.g. metals or organic compounds from contaminating the etch solvents.

High deposition rates and cost-effective precursor gases allow the c-SiC IL to be up to 10 µm thick. This helps strengthening weaker- or porous substrates mechanically and leveling surface irregularities. Therefore the requirements on the substrate can be decreased significantly.

The deposition of c-SiC also allows to infiltrate substrates with high porosities [3]. This enables the application of electrically isolating substrates for rear-contacted solar cells as shown in Figure 1 (right).

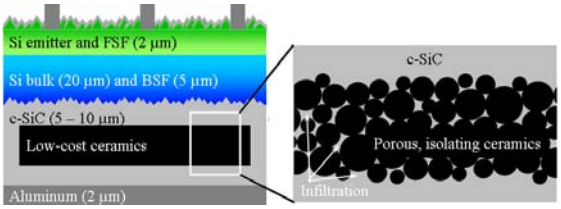

Figure 1: RexWE solar cell design on a ceramic substrate (left); Approach to realize conductivity by infiltration of porous, non-conductive ceramics with highly doped c-SiC (right).

In case of isolating but infiltrated substrates the conductivity of the deposited c-SiC is even more important. To increase the conductivity of the c-SiC IL we used nitrogen as a doping gas present during the deposition.

To use the full potential of the very thin Si bulk layer in the RexWE cell design (20 – 30 µm), this concept depends on a good optical confinement. A c-SiC IL could hereby function as a diffuse backside reflector due to its textured, crystalline surface covered with 50 nm high pyramids and its refractive index of $n_{(467\ nm)} = 2{,}55$ [4].

2 EXPERIMENTAL

2.1 SiC deposition

To deposit the crystalline SiC layers we use a deposition reactor called RTCVD160 which was designed by Fraunhofer ISE. This optically heated deposition tool was originally invented to deposit epitaxial silicon layers. We modified the gas system to use methyltrichlorosilane (CH_3SiCl_3; MTS) as a precursor gas for the deposition of c-SiC. The used MTS is of technical grade with 99% purity. Argon was used as carrier gas. This set up of a RTCVD160 now allows samples up to 125x250 mm² in size, to be completely encapsulated. A schematic of the reaction chamber is shown in Figure 2.

To increase deposition homogeneity we used gas deflectors to cause mostly turbulent gas flow in the reaction chamber. We furthermore added argon to increase the gas flow velocity and therefore to compensate the depletion of reaction gas and increase homogeneity in the direction of flow.

The doping with nitrogen was realized by adding N_2 to the reaction. Nitrogen, as a not flammable, not toxic and cost-effective gas bares the potential of high n-type doping for very good conductivity of the SiC layer. However, to incorporate significant amounts of nitrogen one needs high temperatures to break the N_2 triple bond in quantity. At 1100°C only a small fraction of the N_2 molecules present, might incorporate into the SiC. To determine the exact amount of nitrogen that is available for incorporation we deposited at various MTS/N_2 ratios from 0 – 10%.

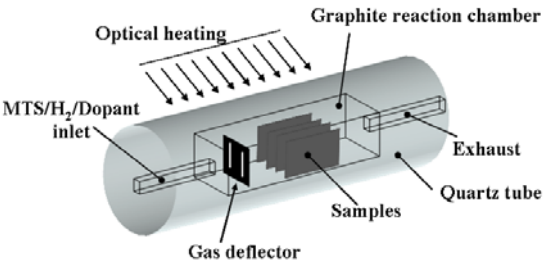

Figure 2: Reaction chamber of the RTCVD160 tool, modified for all-side encapsulation of flat substrates with c-SiC.

2.2 Si deposition and recrystallization

To form a RexWE, deposition of two Si layers and a recrystallization step are needed [5]. After the encapsulation of the substrate with c-SiC a highly boron doped, microcrystalline p^+-Si-seeding layer is deposited by APCVD from Trichlorosilane ($HSiCl_3$, TCS) at 1000°C. This seeding layer is then recrystallized by Zone Melting Recrystallization (ZMR) at 1420°C. This increases the Si crystal sizes from only a few µm to mm in width and several cm in length [6]. Three different stages in forming a RexWE on graphite substrate are shown in Figure 3.

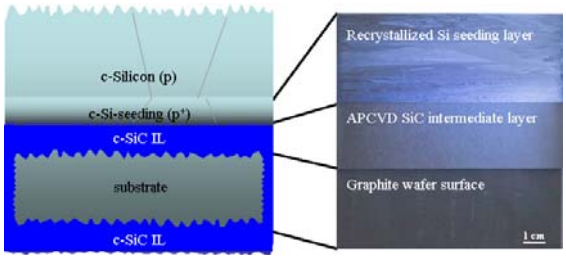

Figure 3: Schematic of the RexWE with substrate, encapsulating c-SiC, recrystallized p^+-Si seeding and epitaxial p-Si bulk (left); Actual photographs of selected steps during the manufacturing process of a RexWE (right).

Adopting these processes to ceramics encapsulated in c-SiC proofed to work very well. No breakage of the c-SiC IL, used on graphite or silicon, could be observed. There was also no influence on the liquid silicon what so ever. Nevertheless, on some ceramics, with differing thermal expansion coefficients (e.g. Al_2O_3), the deposited layers tended to crack during the ZMR process at 1420°C. Furthermore, bowing of those substrates could be observed. As reference substrates we therefore used mainly graphite and silicon wafers.

3 INTERMEDIATE LAYER CHARACTERIZATION

To determine whether the deposited SiC is of pure phase, we used X-Ray diffraction (XRD) and dispersive X-Ray Spectroscopy (EDX) measurements.

As there is only stoichiometric SiC known, any excess of silicon or carbon is forming a separate crystalline phase. This reduces the crystal size due to increased amounts of crystal seeds and thereby increases the number of grain boundaries. An increased amount of grain boundaries may result in weaker diffusion barrier properties.

Furthermore a separate Si or C phase may result in weaker chemical stability and oxidation resistance. Varying grain sizes are easily visible by Scanning Electron Microscopy (SEM) as seen in Figure 4. SiC deposited in pure phase shows large crystals, with excess of silicon the crystal size decreased drastically showing no more structure at all.

To form only c-SiC without any side products a defined ratio of H_2/MTS (α) between 3 and 6 is needed. This range of excess H_2 proofed to be suitable to deposit crystalline, cubic (β)-3C-SiC at temperatures ranging from 1000°C - 1150°C [7].

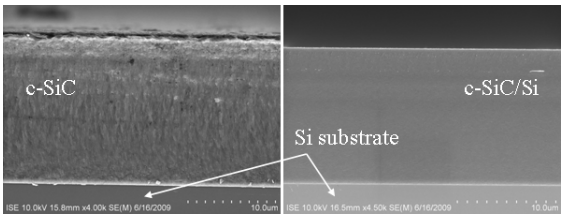

Figure 4: Breaking edges of SiC layers with different grain sizes on Cz-Si-Substrate. Stoichiometric SiC deposited with few Hydrogen (α = 5) (left); SiC with excess Si, deposited with much Hydrogen (α = 20), showing no crystal structure (right).

While excess carbon could not be observed even with low hydrogen flows ($\alpha < 3$), an additional phase of crystalline Si was deposited with H_2/MTS ratios $\alpha > 10$.

Depositing with $\alpha = 5$, results in pure 3C-SiC with good crystal quality as can be seen in the XRD-pattern in Figure 5.

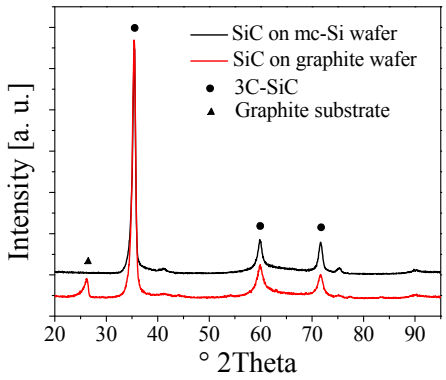

Figure 5: X-Ray Diffraction pattern of 3C-SiC deposited at 1100°C on mc-Si Wafer (black) and on graphite (red).

The relative intensity of the (111) reflex at 35.4° indicates a preferred growth in [111] direction. Silicon, which would occur as a separate crystalline phase at this deposition temperature, could not be indicated.

To determine the carbon amount, we used EDX measurements of the deposited c-SiC layers (see Table I). A 6H-SiC single crystal was used as standard.

Table I: Increasing Si fraction with increasing H_2/MTS-ratios (α). Measured with EDX on 10 µm thick c-SiC layers, deposited at 1100°C.

α	Carbon [At.-%]	Silicon [At.-%]
3	51	49
6	48	52
14	39	61

The different amounts of hydrogen present during the deposition showed a direct impact on the Si/C-ratio in the layer. Results of the EDX measurements are shown in Table I. All layers with thicknesses of 10 µm were deposited from 250 sccm MTS at 1100°C on Si substrates. Depositing with $\alpha = 3$ and $\alpha = 6$ resulted in stoichiometric SiC. Increasing the amount of hydrogen to $\alpha = 14$ results in 20 At.-% of excess silicon in the deposited layer.

3.1 Optical properties

Depending on deposition conditions and the substrate, c-SiC layers showed a textured surface, covered with random pyramids of 50 – 100 nm in size. This texture, combined with the refractive index $n_{(467\ nm)} = 2{,}55$, bares the potential to act as a back side reflector, thus increasing the optical thickness of the Si bulk. A SEM image of a graphite substrate, covered with c-SiC pyramids is shown in Figure 6.

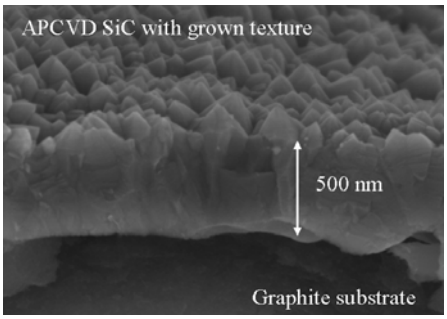

Figure 6: Graphite substrate covered with 500 nm of c-SiC and pyramids on top.

The effect of the textured c-SiC IL on the optical behavior of the RexWE is not yet fully characterized. To obtain the full potential, one needs the textured surface and the contrast in the refractive index to the following Si layers. Therefore the optic is best characterized by fabricating solar cells and measuring the current.

With a fine textured, diffuse reflecting IL it is possible to obtain suitable optical confinement without texturing the solar cells front side. A simple anti reflection coating could be sufficient.

The texturing of the c-SiC surface is mainly influenced by the deposition speed. This gives the opportunity to encapsulate a substrate with high growth rates of >1 µm/min and subsequent cover this encapsulation with pyramids by changing gas flows in-situ. No further treatment like etching of the IL is necessary, which means fewer stress or damage to the IL as well decreased costs.

3.2 The 'ConTow' concept

The conductivity of the c-SiC IL is one major issue in this concept. For a standard solar cell process with bifacial one needs a substrate with a low resistivity. Back-contacting of the base layer using an encapsulated substrate however bares several difficulties:

- Need of good ohmic metal – c-SiC contact on the back of the substrate.
- Possible hetero-junction of n-Type c-SiC and the p^+-Si from BSF.
- Sufficiently low resistivity of the c-SiC layer which is equal to high dopant incorporation.

To avoid difficulties with metal/SiC contact formation, we measured the conductivity of a whole wafer equivalent using a graphite substrate covered with 5 µm SiC and 5 µm recrystallized, and highly boron doped silicon. Both sides were contacted with 2 µm evaporated aluminum and subsequent sintering for 30 min at 400°C.

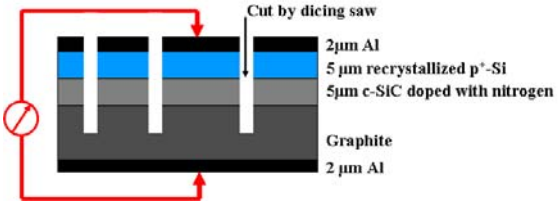

Figure 7: Schematics of the layers used in a RexWE, cut for conductivity measurements creating the so called 'ConTow' concept**.**

To achieve spatial resolution for different sample positions we used a measuring concept called 'Conductive Towers' or 'ConTow'. Hereby we cut through the deposited layers into the substrate by dicing saw, leaving defined 'towers' with a base area of 2 - 8 mm². A sketch of this concept is shown in Figure 7.

3.3 Measurement results

I-V measurements without illumination showed a non linear coherence of current density and voltage. This can be expected for the p-n-hetero-junction between the p^{++}-Si and the IL.

Without additional nitrogen present during the deposition the sample showed a resistivity of 8±0.5 Ωcm² at 500 mV. Adding 2% and 6% nitrogen to the MTS resulted in an increase of sheet resistivity (red and green curve in Figure 8). That might be explained with contaminations in the MTS precursor, resulting in p-type background doping.

With 10% nitrogen in MTS the resistivity decreased to 5±0.5 Ωcm² at 500 mV (blue curve in Figure 8). This may indicate an overcompensation of p-type dopants with the incorporated nitrogen.

For each dopant concentration we measured five towers of 8 mm², representing different regions of the sample.

The comparison of towers with different sizes proofed to be difficult. This may be caused by damaging of to the metallization which occured during the sawing. The I-V-curves comparing equal towers, but different sample positions, are shown in Figure 8. Each position is printed as a separate curve, showing marginal inhomogeneity over the sample.

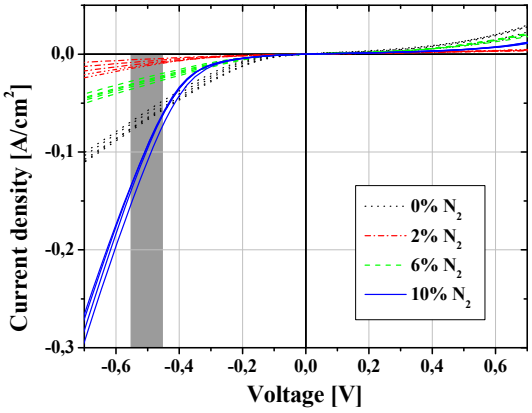

Figure 8: Dark I-V-measurement of 'ConTow' samples doped with 0% - 10% N_2 present at the deposition. The region with the estimated cell voltage of 500 mV is highlighted.

The measured sample resistances are still about one order of magnitude too high for a successful incorporation in a RexWE. Nevertheless, the incorporation of nitrogen as a dopant works out well and the resistivity of the deposited c-SiC layers is significantly decreasing. It could be shown, that when using technical grade MTS a p-type background doping can be expected. For further works additional nitrogen incorporation is needed. We therefore already modified the gas system with regard to increased nitrogen flows.

4 CONCLUSION

We introduced crystalline SiC ILs into the RexWE concept, investigating basic characteristics like crystal quality, purity of phase and conductivity. The gained knowledge was used to optimize the APCVD deposition of 3C-SiC from methyltrichlorosilane.

This IL proved to withstand the very harsh conditions during Si-deposition and recrystallization steps (ZMR) without cracking, bowing or other problems.

Depending on the conditions during the deposition, one can obtain a fine textured surface or flatten "as-cut" ceramics with macroscopic roughness.

Crystalline SiC IL expands the possible choices of substrates to be used in recrystallized CSiTF solar cells. The mechanically, chemically and thermally strong c-SiC layer bares potential to encapsulate very highly contaminated and therefore more cost-effective ceramics with sizes exceeding those of common Si wafers.

The optical properties of the c-SiC IL are not yet fully understood. However, the majority of light reflected is diffuse.

Doping of the high band gap 3C-SiC was done with nitrogen (N_2) present during deposition, giving resistivity of so far 5±0.5 Ωcm² at 500 mV. This resistivity will be further decreased in future works with a modified deposition tool enabling increased nitrogen flows.

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