

DEPLETION OF BORON-DOPED SURFACES PROTECTED WITH BARRIER LAYERS DURING POCL₃-DIFFUSION

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ABSTRACT: Different diffusion barrier layers applied on the boron-doped surfaces of silicon wafers with saw-damage etched surfaces are investigated with respect to their applicability in the fabrication process of n-type silicon solar cells using sequential tube furnace diffusions with a first BBr₃- and a subsequent POCl₃-diffusion. The barrier layers consist of silicon oxide and/or silicon nitride deposited either by plasma-enhanced chemical vapor deposition or sputter technology. The layer itself must act as barrier against phosphorus diffusion into the silicon wafer during POCl₃-diffusion. Furthermore, it has to ensure that no substantial depletion of boron occurs at the wafer surface. The boron doping surface concentrations and profile depths measured after POCl₃-diffusion depend on the applied diffusion barrier. If solely silicon oxide barrier layers are used, depletion of boron at the wafer surface and deeper profiles are observed, which we attribute to oxygen diffusion through the barrier and growth of a thin thermal oxide film at the silicon. With a thin silicon nitride layer incorporated into the diffusion barrier system, no significant change in the boron doping profile is detected. Numerical simulations of the boron diffusion during the POCl₃-process agree well with the measurements and support these findings.

Keywords: diffusion barrier, boron depletion, process simulation, n-type, silicon solar cell

1 INTRODUCTION

Several solar cell concepts on n-type silicon, e.g. the bifacial concept shown in Fig. 1, feature a boron-doped emitter on the front and a phosphorus-doped back surface field (BSF) on the rear [1–3]. To provide the differently doped surfaces, the use of sequential tube furnace diffusion processes with first a boron tribromide (BBr₃) and then a phosphorus oxychloride (POCl₃) source is an option (see Fig. 2). Hence, the boron-doped surface after the BBr₃-diffusion needs to be protected from the POCl₃-ambient by using appropriate diffusion barrier layers. The barrier layer not only has to prevent phosphorus diffusion into the silicon wafer during the POCl₃-diffusion but also should ensure that no substantial depletion of boron occurs at the wafer surface during the diffusion process, which might affect the specific contact resistance for screen printed contacts.

The most obvious choice is silicon oxide because it is commonly used as diffusion barrier in POCl₃-processes [4] and it can be easily removed in hydrofluoric acid (HF) solution [5,6]. Unfortunately, thermally grown

silicon oxide is known to lead to a significant surface depletion of boron [7]. Hence, alternatives to thermal oxidation are required. In this work, we investigate silicon oxide (SiO_x) layers deposited by plasma-enhanced chemical vapor deposition (PECVD) or sputtering.

Another option is the use of silicon nitride (SiN_x) layers [8], which unfortunately feature low etching rates in HF solution [5,6,8]. Thus, only thin SiN_x layers are preferred, which are also applied either by PECVD or by sputtering in this work.

We perform two experiments to investigate the diffusion barrier properties of SiO_x and SiN_x layers. First, the barrier properties of the layers against phosphorus diffusion during POCl₃-diffusion are analyzed (experiment A). Second, the impact of POCl₃-diffusion on the boron doping profile underneath the barrier layer is investigated (experiment B). For the latter, also layer stacks consisting of SiO_x and SiN_x are considered.

2 APPROACH

2.1 Sample preparation

For both experiments p-type Czochralski-grown silicon (Cz-Si) wafers with an edge length of 156 mm and a thickness of 200 μm are used (see Fig. 3).

First, thermal donors that might exist in the material are dissolved during high-temperature tube furnace processes with peak temperatures ≥ 880 °C. The wafers are then subjected to a wet chemical saw-damage etching process and the specific base resistivities are measured with an inductive inline measurement tool [9].

The wafers assigned to test the barrier properties of the dielectric layers against phosphorus diffusion during the POCl₃-diffusion (experiment A) are then capped with either SiN_x or SiO_x on both sides using PECVD or sputtering. Table I lists the investigated layers and their nominal thicknesses. Subsequently, all samples are subjected to a common POCl₃-diffusion process at ≈ 835 °C. After removal of the barrier layers in HF solution, the resulting sheet resistances are determined.

For experiment B, in which the impact of a POCl₃-diffusion on already existing boron doping profiles is

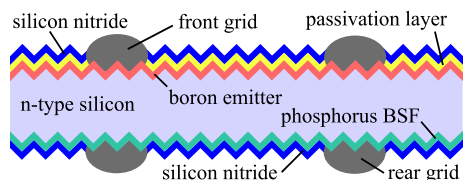


Figure 1: Schematic cross section of an n-type silicon H-pattern solar cell with the boron emitter on the front.

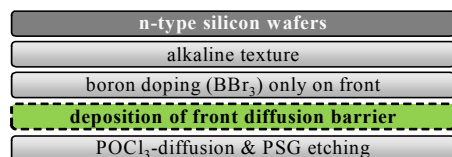


Figure 2: Part of the process sequence for fabrication of n-type silicon solar cells using sequential tube furnace diffusion processes to form front boron emitter and rear phosphorus BSF. Different diffusion barrier layers for the highlighted process step are studied in this work.

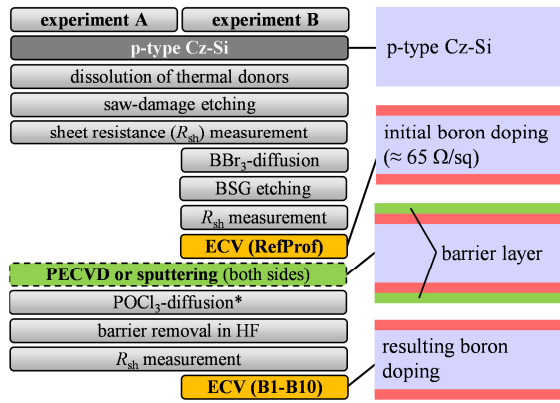


Figure 3: Schematic process flow for experiment A and B. The schematic cross sections on the right show the silicon wafers of experiment B at four different process stages.*For barrier layer B4 in experiment B, oxygen instead of $POCl_3$ is introduced into the tube during the deposition step.

characterized, the BBr_3 -diffusion process for the realization of the initial boron dopings is performed in a tube furnace at $\approx 935^\circ C$, followed by an in-situ oxidation step at the end of the process. After removal of the borosilicate glass (BSG) in HF solution, the initial sheet resistance of $\approx 65 \Omega/sq$ for the boron doped surfaces is measured inductively. SiN_x and SiO_x barrier layers are then applied on both wafer surfaces by PECVD or sputter technology, see also Table I. Subsequently, a common $POCl_3$ -diffusion is performed at $\approx 820^\circ C$. To test the influence of higher oxygen content, pure oxygen instead of $POCl_3$ is introduced into the tube during the 15 minutes deposition step while leaving the rest of the process parameters unchanged. After etching of the barrier layers in HF solution, the sheet resistances are measured and the resulting charge carrier concentration profiles are determined by electrochemical capacitance-voltage (ECV) measurements [10].

2.2 Numerical simulations

The boron diffusion during the $POCl_3$ -process is simulated with *Sentaurus Process* [11], to identify the reasons for the variations between measured boron profiles after the $POCl_3$ -process using different diffusion barriers. To be more sensitive to the differences in the boron profiles which evolve during the $POCl_3$ -process, the measured boron profile RefProf after the BBr_3 -process is used as input. The process condition, i.e. temperature profiles and gas fluxes, are taken as in the corresponding experiments. We use the same models and diffusion parameters as in [12]. Only the diffusivity of oxygen in the PECVD- SiO_x is fitted. The diffusion of oxygen to the reacting silicon/silicon oxide interface determines the oxidizing velocity and thus the oxidation enhanced diffusion (OED) of boron [13,14].

3 RESULTS

3.1 Barrier against phosphorus diffusion (experiment A)

In experiment A, only the single layers in Table I are tested. Therefore, the sheet resistances were inductively measured before and after the $POCl_3$ diffusion process. By comparing the respective values, no differences in the measured sheet resistances are obtained for all tested

Table I: Overview of the investigated dielectric barrier layers (B1-B10). In experiment A, the diffusion barrier properties during a $POCl_3$ -diffusion are tested, whereas in experiment B the impact on the boron doping profile underneath the barrier layer is characterized. Wafer RefProf serves as reference for the initial charge carrier concentration profile of the boron doped surface in experiment B.

wafer ID	deposition method	barrier layer	nominal layer thickness (nm)	exp.
RefProf	-	-	-	B
B1	PECVD	SiN_x	15	A, B
B2	PECVD	SiN_x	25	A, B
B3	PECVD	SiO_x	100	A, B
B4*	PECVD	SiO_x	100	B
B5	PECVD	SiO_x	300	A, B
B6	PECVD	$SiO_x + SiN_x$	100 + 25	B
B7	PECVD	$SiN_x + SiO_x$	25 + 100	B
B8	sputter	SiO_x	100	A, B
B9	sputter	SiO_x	300	A, B
B10	sputter	$SiN_x + SiO_x$	25 + 100	B

*oxygen instead of $POCl_3$ is introduced into the tube during the 15 minutes deposition step in experiment B

barrier layers on saw-damage etched wafer surfaces: the determined sheet resistances of $\approx 150 \Omega/sq$ after $POCl_3$ -diffusion equal the values measured before the diffusion process within the standard deviation of $\approx 1 \Omega/sq$. Thus, the SiN_x and SiO_x single layers investigated in this work act as barrier against phosphorus diffusion during the $POCl_3$ -diffusion, irrespective of whether they were deposited by PECVD or sputtering. Layer thicknesses of only 15 nm for SiN_x and 100 nm for SiO_x proved to be sufficient to prevent significant phosphorus-doping of the silicon wafer surface.

3.2 Impact of $POCl_3$ -diffusion on boron doping protected with barrier layer (experiment B)

For experiment B, the wafer IDs in Table I are used to denote the wafer as well as the corresponding profiles.

3.2.1 PECVD- SiN_x barrier layers

Fig. 4 shows the charge carrier concentration profiles of the diffused boron dopings obtained by ECV measurements for reference wafer RefProf, which was measured after BSG removal (see Fig. 3), as well as wafers B1 and B2 with PECVD- SiN_x barrier layer with thicknesses of 15 nm and 25 nm, respectively.

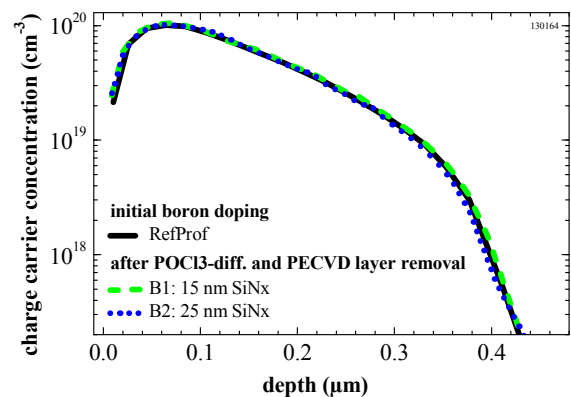


Figure 4: Charge carrier concentration profiles (boron doping) obtained by ECV measurements. The profiles B1 and B2 hardly differ from the reference profile RefProf.

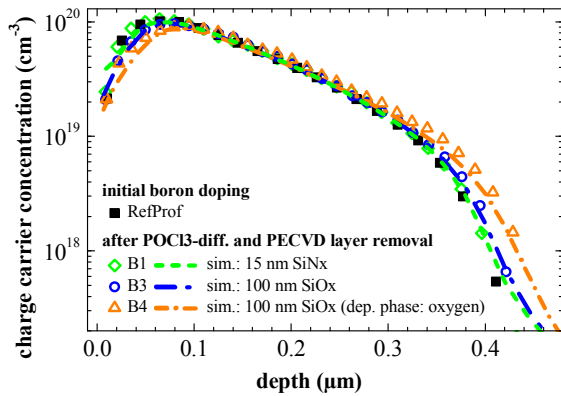


Figure 5: Measured ECV profiles for wafers B1, B3 and B4 as well as the corresponding simulated profiles, which are illustrated as lines in this graph. The simulation results agree quite well with the measured profiles.

Assuming that the boron dopants are completely electrically active, which is legitimate for this concentration, the measured charge carrier concentration is identical to the boron doping concentration. Since the solubility of boron in silicon oxide is higher than in silicon [7], the used oxidation step at the end of the BBr_3 -diffusion process leads to boron depletion at the wafer surface [7], which is clearly visible for the reference boron doping profile RefProf as well as for profiles B1 and B2. Profile RefProf is set as reference throughout this work and all other profiles are compared to it.

Obviously, the boron doping profiles B1 and B2 hardly differ from the reference profile RefProf. No significant differences are visible neither for the surface doping concentrations nor the profile depths. Hence, already the 15 nm thick SiN_x layer can sufficiently protect the boron doped surface from depletion. Due to the much lower temperature of the $POCl_3$ -diffusion, the temperature loading shows no significant impact on the already existing boron profile as well. These findings are also supported by our performed simulations, as Fig. 5 shows exemplarily for wafer B1.

3.2.2 Surface depletion of boron with PECVD barriers

The boron doping profiles shown in Fig. 6 and Fig. 7 (Fig. 7 shows the enlargement of the near-surface region of Fig. 6), which were measured after $POCl_3$ -diffusion and barrier layer removal, show significant dependency

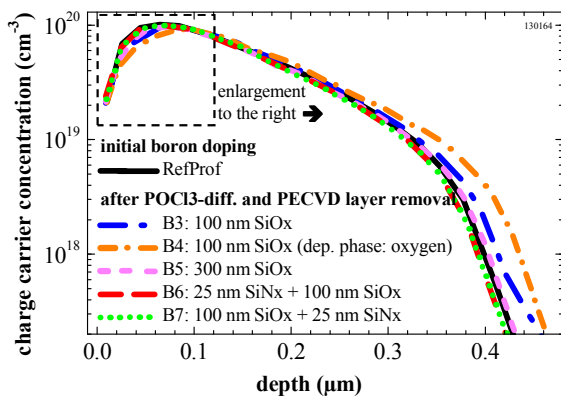


Figure 6: ECV boron doping profiles of wafers RefProf and B3-B7 with PECVD capping layers. The profiles B3-B5 differ from the reference profile RefProf, whereas profiles B6 and B7 show almost no deviation.

on the applied diffusion barrier layers for wafers B3-B7. Apart from surface depletion due to the oxidation step at the end of the BBr_3 -diffusion process, as already discussed, further depletion of the surface doping concentration is apparent for wafers B3-B5 which were protected by single PECVD- SiO_x layers with a thickness of 100 nm (B3, B4) or 300 nm (B5). Also, the profile depths are increased, especially for wafers B3 and B4. The most pronounced surface depletion and the deepest profile is found for wafer B4, for which a high oxygen flow instead of $POCl_3$ was used during the deposition step of the diffusion process. With an additional 25 nm thick PECVD- SiN_x layer, neither surface depletion nor profile deepening is observed for wafers B6 and B7, irrespective of whether SiO_x and SiN_x is deposited first. This result is consistent to the findings obtained for wafers B1 and B2 in Fig. 4, which were capped by only a 15 nm (B2) or 25 nm (B3) thick PECVD- SiN_x layer and also show no change in the doping profile. Obviously, by omitting SiN_x in the barrier layer system, a pronounced depletion of boron occurs at the surface as well as a deepening of the profiles.

As shown in section 3.1, all investigated layers within this work act as diffusion barriers against phosphorus and the pure temperature budget of the $POCl_3$ -diffusion process does not change the boron doping profile. Since oxygen has a higher diffusion coefficient in silicon oxide than phosphorus [8,15], oxygen originating from the gas atmosphere during the diffusion process is suspected to reach the interface between barrier layer and silicon for wafers B3-B5 and to cause an oxidation which leads to surface depletion and triggers OED of boron.

However, this applies for the barrier layers which only consist of PECVD- SiO_x since the diffusion coefficient of oxygen is drastically higher in silicon oxide than in silicon nitride, i.e. silicon nitride masks silicon against oxygen [8]. The results also clearly indicate a clear dependence of the resulting profile depths on the degree of surface depletion: The greater the surface depletion, the deeper the resulting profile.

The oxygen which is assumed to react at the silicon interface and to trigger OED most likely originates from the $POCl_3$ -atmosphere. By comparing the results for wafers B6 and B7, a contribution of oxygen from the PECVD- SiO_x barrier layer itself is very unlikely. The segregation of boron into the barrier layer is most probably insignificant, since both profiles are equal whether the surface is in direct contact with the PECVD-

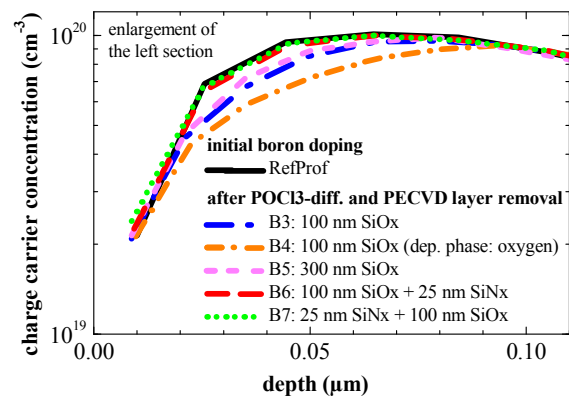


Figure 7: Enlargement of the marked near-surface region in Fig. 6 on the left. The boron surface concentration for profiles B3-B5 are lower compared to reference profile RefProf, whereas profiles B6 and B7 are almost identical.

Table II: Inductively measured sheet resistances of wafer RefProf and wafers B1-B10 as illustrated in Fig. 3 and Table I.

measurement of	sheet resistance (Ω/sq)										
	RefProf	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
initial boron doping	64.9	65.0	65.2	64.2	65.2	65.6	65.6	64.4	64.0	64.4	64.5
resulting boron doping (after barrier removal)	-	66.4	66.3	67.7	72.0	68.4	66.3	65.5	71.3	70.8	65.7

SiN_x or the PECVD- SiO_x layer. Also, oxygen present in the silicon wafer due to the Cz-Si fabrication process can be excluded; otherwise also wafers with a PECVD- SiN_x barrier layer should show altered boron doping profiles.

The simulation results shown in Fig. 5 are in very good agreement with the ECV measurements for an oxygen diffusivity D_{ox} in the PECVD- SiO_x layer of

$$D_{\text{ox}} = 5 \cdot 10^{-4} \cdot \exp\left(-1.23 \frac{\text{eV}}{k_{\text{B}}T}\right) \frac{\text{cm}^2}{\text{s}}.$$

The found diffusivity D_{ox} for the applied PECVD- SiO_x layer is about 10 times higher than the diffusivity in thermally grown silicon oxide. The good agreement for the different process conditions supports the findings from the measured ECV profiles.

The inductively measured sheet resistances of the boron dopings before and after the POCl_3 -diffusion are shown in Table II. All wafers with PECVD- SiN_x barrier layer (B1, B2, B6 and B7) show only minor deviation in the sheet resistance of $\approx 1 \Omega/\text{sq}$ which is within the measurement accuracy. With only PECVD- SiO_x barrier layer, wafers B3 and B5 show an increase of $\approx 3 \Omega/\text{sq}$ in the sheet resistance.

In summary, the barrier layers not only have to mask the boron doped surface against phosphorus but also against oxygen. PECVD- SiN_x layers with a thickness of only 15 nm already meet both requirements.

3.2.3 Surface depletion of boron with sputtered barriers

For the investigated sputtered SiO_x and SiN_x layers, see Table I, qualitatively similar results are obtained.

Again, with solely SiO_x layers as diffusion barrier surface depletion of boron and profile deepening is observed for wafers B8 and B9. The measured sheet resistances in Table II confirm this rearrangement of the boron doping.

In contrast, a SiN_x layer incorporated into the barrier system almost preserves the boron doping profile underneath the barrier layer for wafer B10.

However, the measured profiles B8-B10 show both somewhat more surface depletion and somewhat deeper profiles. Presumably, the sputter process introduces additional surface defects supporting the boron diffusion.

4 CONCLUSION

For fabrication of n-type silicon solar cells, sequential tube furnace diffusion processes with first a BBr_3 - and subsequently a POCl_3 -source offer the possibility to provide the differently doped wafer surfaces.

Within this work, the diffusion barrier properties of SiN_x and SiO_x layers against POCl_3 -diffusion were investigated on p-type Cz-Si wafers with saw-damage etched surfaces. The barrier layers were either applied by PECVD or sputter technology.

All investigated layers mask silicon against phosphorus during the POCl_3 -diffusion, whereas layer thicknesses of 15 nm for SiN_x and 100 nm for SiO_x proved to be sufficient.

An impact of the POCl_3 -diffusion on boron dopings underneath the barrier layer is only observed when solely SiO_x barrier layers are used. In these cases, depletion of boron at the wafer surface and deeper profiles are observed. We attribute this to oxygen diffusion through the barrier and growth of a thin thermal oxide film at the silicon which triggers oxidation enhanced diffusion of boron. Process simulations support these findings.

In contrast, if a SiN_x layer with a thickness of 15 nm is incorporated into the barrier layer system, the POCl_3 -diffusion shows no significant impact on the boron doping profile underneath the barrier layer. Furthermore, the boron profile is not significantly affected by the temperature loading during POCl_3 -diffusion.

By using diffusion barrier systems with a thin SiN_x layer, independently pre-optimized boron and phosphorus dopings can be unchanged implemented into n-type silicon solar cell fabrication processes using sequential diffusions.

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REFERENCES

- [1] R. C. G. Naber, N. Guillevin, A. R. Burgers et al., "ECN n-type silicon solar cell technology: an industrial process that yields 18.5%", *Proc. 24th EU-PVSEC*, Hamburg, Germany, pp. 2177–2179, 2009.
- [2] N. Guillevin, L. J. Geerligs, R. C. G. Naber et al., "High Efficiency n-type Metal Wrap Through Si Solar Cells for Low-Cost Industrial Production", *Proc. 25th EU-PVSEC*, Valencia, Spain, pp. 1429–1431, 2010.
- [3] E. Lohmüller, B. Thaidigsmann, F. Clement et al., "Transfer of the HIP-MWT solar cell concept to n-type silicon", *Energy Procedia*, vol. 38, pp. 436–442, 2013.
- [4] E. Lohmüller, B. Thaidigsmann, M. Pospischil et al., "20% efficient passivated large-area metal wrap through solar cells on boron-doped Cz silicon", *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1719–1721, 2011.
- [5] K. R. Williams, R. S. Muller, "Etch rates for micromachining processing", *J. Microelectromech. Sys.*, vol. 5, no. 4, pp. 256–269, 1996.
- [6] K. R. Williams, K. Gupta, M. Wasilik, "Etch rates for micromachining processing-part II", *J. Microelectromech. Sys.*, vol. 12, no. 6, pp. 761–778, 2003.

- [7] A. S. Grove, O. Leistiko, C. T. Sah, "Redistribution of acceptor and donor impurities during thermal oxidation of silicon", *J. Appl. Phys.*, vol. 35, no. 9, pp. 2695–2701, 1964.
- [8] V. Doo, "Silicon nitride, a new diffusion mask", *IEEE Trans. Electron Devices*, vol. 13, no. 7, pp. 561–563, 1966.
- [9] M. Spitz, U. Belledin, S. Rein, "Fast inductive inline measurement of the emitter sheet resistance in industrial solar cell fabrication", *Proc. 22nd EU-PVSEC*, Milan, Italy, pp. 47–50, 2007.
- [10] E. Peiner, A. Schlachetzki, D. Krüger, "Doping profile analysis in Si by electrochemical capacitance-voltage measurements", *J. Electrochem. Soc.*, vol. 142, no. 2, pp. 576–580, 1995.
- [11] Synopsys, Synopsys TCAD, "Sentaurus Process", release G-2012.06, available online: <http://www.synopsys.com>, 2012.
- [12] J. Schön, A. Abdollahinia, R. Müller et al., "Predictive simulation of doping processes for silicon solar cells", *Energy Procedia*, vol. 38, pp. 312–320, 2013.
- [13] P. Stolk, A. van Brandenburg, A. Montree, "Oxidation enhanced diffusion during the growth of ultrathin oxides", *Materials Science in Semiconductor Processing*, vol. 2, no. 1, pp. 29–33, 1999.
- [14] K. Taniguchi, K. Kurosawa, M. Kashiwagi, "Oxidation Enhanced Diffusion of Boron and Phosphorus in (100) Silicon", *J. Electrochem. Soc.*, vol. 127, no. 10, pp. 2243–2248, 1980.
- [15] G. Schumicki, P. Seegebrecht, "Prozesstechnologie: Fertigungsverfahren für integrierte MOS-Schaltungen", Springer, 1991.