Back-Gated GaN-on-Si HEMTs in Multistage Cascodes

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***Abstract*— This work presents multistage cascodes by using back-gated GaN-on-Si high-electron mobility transistors (HEMTs) as direct-driven stacked follower transistors. Back-gating is to be used here as a new concept enabling depletion-mode transistors with very negative threshold voltages of about $V_{TH,\,BG} \approx -300$ V, instead of using the front gate for controlling the transistor, as is usually the case. The highly negative threshold reduces the number of stages required in the cascode. These self-compatible devices are used as discrete connected transistor "bricks." Characterization of back-gating provides deeper insight into this mechanism and shows a reproducible drain–source voltage-dependent threshold shift driven by lateral fields. Double-pulse measurements demonstrate high-voltage capability. With a Si-MOSFET controller transistor, a multistage cascode with two back-gated follower transistors is switched up to 900 V, and exceeds therewith the lateral 600-V-class limit of conventional GaN-on-Si technologies by directly driven self-compatible back-gated GaN-HEMTs in a multistage cascode. In another assembly, voltages up to 850 V are demonstrated using a cascode with a normally-OFF GaN controller transistor. A key finding is the leakage management: buffer leakage from upper back-gated transistors requires a bypass. Without a highly ohmic resistor in parallel to the controller transistor, leakage higher its drain voltage, increases vertical field stress above the follower, and risks damage. Thus, back-gated GaN-HEMTs in multistage cascodes offer a solution to exceed the lateral 600-V-class limit of today's established GaN-on-Si technologies.**

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***Index Terms*— Cascode configuration, gallium nitride, high-electron mobility transistor (HEMT), high-voltage techniques, modular construction, power semiconductor devices, stacking, substrate biasing.**

I. Introduction

BRICKS are stackable due to their self-compatible properties, enabling a variety of stable constructions. Mass production of identical components makes them cost-effective. The question is: how can this concept be applied to power transistors? Transistors, with their three terminals: gate, drain, and source, are usually not self-compatible components. However, in the arrangement as multistage cascode, transistors can be directly stacked one above the other [1], [2]. This concept has been demonstrated in different technologies and embodiments [3], [4], [5], [6], [7], [8]. Multistage cascodes enable distribution of the total blocking voltage across the transistor segments. In voltage-limited technologies such as the commercial lateral GaN-on-Si technology, its 600-V-class limit can be overcome by stacking discrete transistor "bricks" [7], [8]. This approach thus provides a solution to the urgent need for cost-effective wide bandgap semiconductors for higher voltages, targeting the 1200-V class.

Multistage cascodes differ from super-cascodes [9], [10], [11], [12], [13], [14], [15], which require a network with peripheral components such as resistors, diodes, and capacitors to control the gates. These components introduce undesirable resistance–capacitance (RC) time constants, resulting in delays. In contrast, in multistage cascode, the transistor segments are directly coupled. A multistage cascode consists of several self-compatible stacked transistors (followers) and one control transistor at the base (controller), as shown in Fig. 1. The gates of the followers are connected to the source contacts of the transistors below. Transistors are self-compatible if they have certain properties: first, they must be depletion-mode (normally-ON), second, they should exhibit a very negative threshold voltage V_{TH}, and third, their breakdown voltage must be greater than the absolute threshold voltage of the follower transistor stacked above. The threshold voltage of the controller transistor can be different from the threshold voltage of the followers. The controller gate determines the transfer characteristic of the overall cascode. Thus, a controller with enhancement-mode (normally-OFF) behavior is typically desired. In contrast, follower gates with a strongly negative threshold voltage are advantageous because they reduce the number of stages required to block high voltages. For this reason, transistor segments with highly negative threshold voltages in the range of $V_{TH} = -100$ V were developed in

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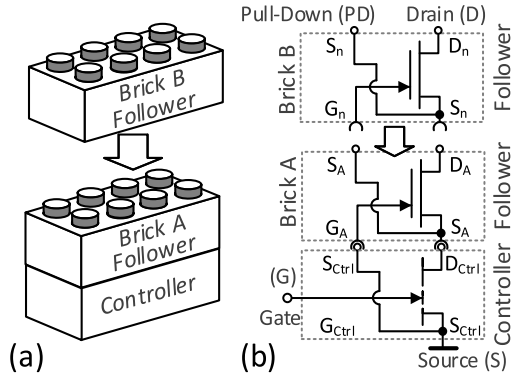

Fig. 1. (a) Stacking of self-compatible LEGO[1] bricks in analogy to self-compatible transistors. (b) Stacking of self-compatible transistors in a multistage cascode.

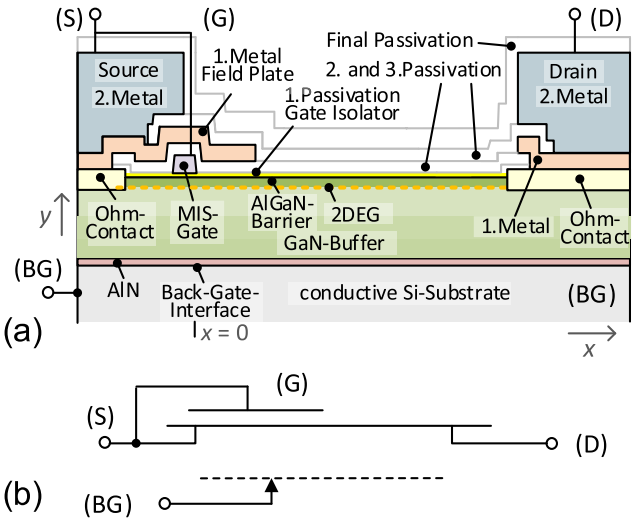

Fig. 2. (a) Cross section of a GaN-on-Si HEMT structure. The normally-ON MIS front gate is connected to the source. The Si-substrate contact is used as back gate. (b) Equivalent circuit diagram and symbol of the back-gated HEMT and source-connected front gate.

[8]. For this purpose, a field plate metallization was used as metal–insulator–semiconductor (MIS) gate. However, even lower threshold voltages would be desirable. To achieve such a negative value, the thickness of the insulator must be further increased. However, even with relatively thick gate insulation layers in the range of 700 nm, it is challenging to achieve gate threshold voltages below −100 V. In addition, high isolation from the other terminal drain and source in the passive layers would also have to be achieved. In this work, we used back-gating to achieve very negative back-gate threshold voltages below $V_{TH,BG} = -300$ V for the stacked follower transistors. These back-gated high-electron mobility transistors (HEMTs) (see Fig. 2) are used and characterized as self-compatible transistors in multistage cascodes. Previous publications on multistage cascodes have focused on the functional principle, realization, and static characterization [3], [4], [6], [8]. In this article, we want to examine the switching behavior of the multistage cascade in a double pulse test setup. The experiments validate the proof-of-concept of this approach in an application-oriented environment.

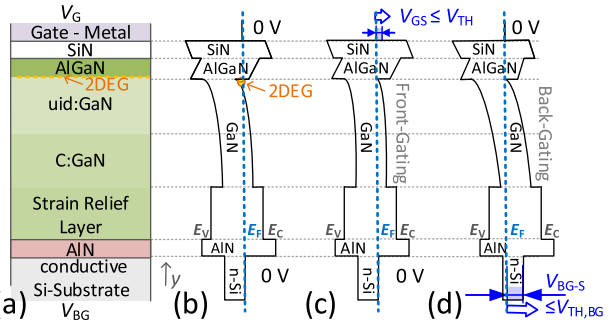

Fig. 3. (a) Schematic vertical layer stack of the depletion mode MIS HEMT GaN-on-Si under gate (x = 0). (b) Schematic band diagram in equilibrium. (c) Band diagram with depleted 2DEG by negative front-gate voltage $V_{GS} \leq V_{TH}$. (d) Band diagram with depleted 2DEG by negative back-gate voltage $V_{BG\text{-}S} \leq V_{TH,\,BG}$.

Fig. 3 shows the vertical layer stack of the GaN HEMT located under the gate and the related band diagrams for equilibrium $V_{GS} = V_{BG-S} = 0$, depleted front-gate $V_{GS} \leq V_{TH}$, and depleted back-gating $V_{BG-S} \leq V_{TH,BG}$. On one hand, back-gating occurs in practically every GaN-on-Si HEMT at each switching cycle, even if the transistor is controlled at the front gate, because the conductive Si-substrate is connected to the source potential and leads to depletion in the 2-D electron gas (2DEGs) channel in the OFF-state at higher drain voltages. Backside floating or carrier enhancement by a positive potential would lead to dynamic problems [16]. On the other hand, back-gating is rarely used as a control mechanism to switch GaN-on-Si transistors. Due to the buffer thickness of a few micrometers, the threshold voltage from the back is very negative. Transistors with such a negative threshold are not commercially available, and such behavior is typically not applied in power electronics. The impact of back-gating by the Si-substrate potential is investigated in terms of static and dynamic parameters in [16], [17], [18], [19], [20], [21], and [22].

A GaN-MIS-HEMT is investigated in Section II with regard to its behavior under back-gating. In Section III, such back-gated HEMTs are connected as followers in a multistage cascode and characterized in a double pulse measurement setup.

II. Characterization of the Back-Gated MIS-HEMT

In this work, we have investigated a 00-V-class power HEMT with insulated gate and normally-ON characteristics. The GaN-HEMT was fabricated using our in-house 4-in AlGaN/GaN-on-Si technology [23] and has typical device dimensions. The intrinsic structure is shown in Fig. 2 and has the following dimensions: $L_{GD}/L_G/L_{GS}$ = 17/1/2 μm. The structure is designed with a source-connected field plate. The epitaxial stack comprises a 150-nm AlN interlayer, a 4-μm step-graded GaN buffer [24], as shown in Fig. 3(a), an AlGaN barrier with 25 nm and 25% Al content, and a 3-nm GaN cap-layer. A 2DEG is formed at the AlGaN/GaN interface with a sheet resistance of about 700 Ω/□. The process for manufacturing high-voltage transistors comprises a total of 11 mask layers and approximately 130 process steps. The main process modules are ohmic and gate contacts, device isolation, three different SiN dielectric layers, two metallization layers (first and second metal), and final passivation. The ohmic contacts

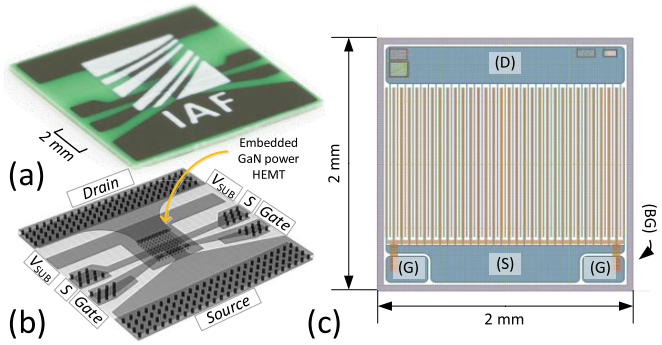

Fig. 4. (a) In-house fabricated GaN-HEMT in a commecial PCB-embedding package, (b) X-ray image of the package incl. GaN-HEMT, and (c) extrinsic layout of the GaN-HEMT.

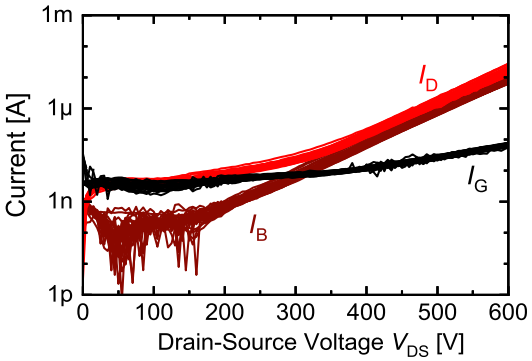

Fig. 5. Off-state characteristics of the GaN-HEMT. The leakage current for drain I_D, gate I_G, and buffer I_B are characterized in on-wafer mapping measurements up to a drain–source voltage of 600 V.

use a Ti/Al/Ni/Au metal stack and are alloyed at 825 °C for 30 s in a nitrogen atmosphere. The typical contact resistance is 0.2 Ω·mm. The gate contact consists of Ni/Au metal deposited on the SiN gate insulator as a passivation layer. It has a thickness of 40 nm and is deposited by plasma-enhanced chemical vapor deposition (PECVD) at around 300 °C. The film has a refractive index of $n = 2.0$ and has a threshold voltage of this MIS front gate of around $V_{TH,FG} = -12$ V.

Device isolation is achieved by Ar ion implantation. Before dicing, the GaN-on-Si wafers are thinned to 125 μm, and a backside metal is deposited for assembly and interconnection. The first metal layer is realized by sputtering 0.4 μm of Au. It is connected to the ohmic contacts at the drain and source through vias formed after the second passivation and is used as a source-connected field plate. The second metal layer is deposited on top after the third passivation and is realized by Au electroplating to a thickness of about 7 μm. The chip layout is shown in Fig. 4. The HEMT is designed with an interdigital comb layout on an active area $A = A_{ACTIVE} = 1.85 \times 1.2$ mm^2 and has a total gate width of $W = 73$ mm. Including the bond pads for the drain, gate, and source, the chip has a die area of $A_{CHIP} = 2 \times 2$ mm^2.

The OFF-state leakage currents at drain, gate, and through the buffer are shown in Fig. 5 and are characterized in on-wafer measurements. It was performed with a front-gate voltage of $V_{GS} = -17$ V, which is below the front-gate threshold voltage. The drain leakage current is mainly caused by the increasing vertical buffer leakage current and reaches a value in the range of $I_D \approx I_B \approx 10$ μA at 600-V drain voltage.

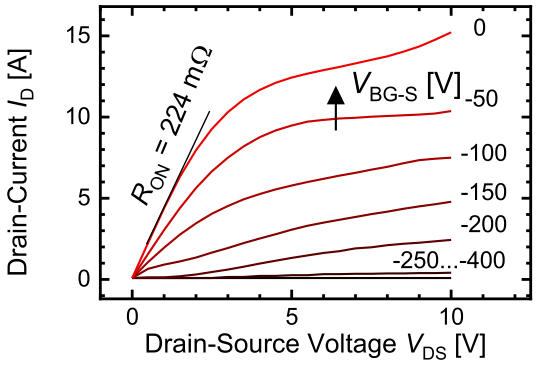

Fig. 6. Output characteristics of the back-gated GaN-HEMT. The high current measurement unit was set with a pulsewidth of t_{PLS} = 1 ms. The back-gated voltage V_{BG-S} is increased in 50 V steps.

The gate leakage current increases only slightly and is in the range of $I_G \approx 10$ nA. In the subsequent characterization, the HEMT is controlled via the back gate rather than the front gate. The front gate is connected externally to the source, as shown in Fig. 2, and acts as a source-connected field plate. As mentioned above, the gate metal is realized on a 40-nm SiN layer and has a threshold voltage of $V_{TH,FG} = -12$ V. We believe that the back-gate threshold is only mildly influenced by the choice and properties of the gate insulator. However, one might think that with a normally-ON gate with a gate–source voltage of $V_{GS} = 0$ V has a minor influence on the characteristics, but it is relevant for pinning the band diagram on the front side in the front-gate region. The output characteristics of the back-gated HEMT are shown in Fig. 6. The ON-state resistance has a value of $R_{ON} = 224$ mΩ, which corresponds to a specific ON-state resistance of $R_{ON} \cdot A = 5$ mΩ·cm^2 when referred to the active area. Thus, this device achieves a typical specific ON-resistance in the same range as other state-of-the-art 600-V-class GaN-on-Si devices [27]. The back-gate voltage was increased in 50 V steps from $V_{BG-S} - 400$ V to 0. The I–V curves show a typical behavior, which was reproducible and was unlikely to be caused by a measurement error. The drain current curves show a rising shape with increasing drain–source voltage. Furthermore, in the I–V curves, the knee voltages are noticeably weaker than in GaN-HEMTs, which are controlled by a front gate. We explain this behavior by the depletion field acting over the entire drift length, and not locally under the front gate.

Another remarkable behavior can be seen in the transfer characteristics shown in Fig. 7. The transfer measurement was performed at different drain–source voltages V_{DS}. The starting value was a voltage of $V_{DS} = 1$ V and a rising back-gate voltage from $V_{BG-S} = -350$ to -230 V. The transfer measurement was performed for rising drain–source voltages, as shown in Fig. 7. It is shown that the back-gate threshold voltage V_{BG-S} shifts significantly to negative values for rising drain–source voltages. This effect was reproducible. A final measurement was performed with $V_{DS} = 1$ V, and the threshold voltage was approximately at the starting point, with a value of $V_{BG-S} = -280$ V. This shows that the lateral electric field components have a high effect on the back-gate threshold voltage. To prevent thermal destruction, a drain current compliance of 1 mA was set for higher drain–source voltages. Fig. 8 shows the shift in back-gate voltage as a function of drain voltage in a separate plot. The inset shows

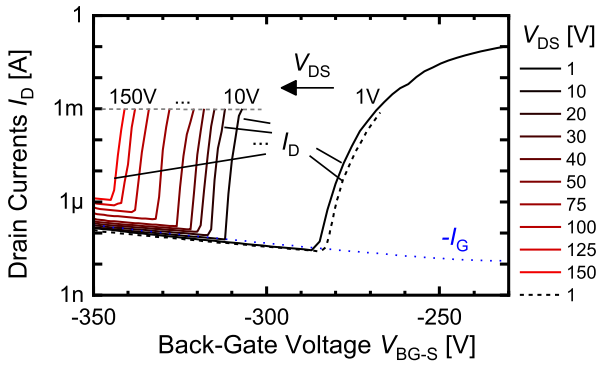

Fig. 7. Transfer characteristics of the back-gated HEMT. The threshold voltage is dependent on the drain–source voltage. The drain voltage was increased in steps from 1 V up to 150 V and finally back to 1 V. The characteristics were reversible (compare solid with dashed line). Current compliance for $V_{DS} > 1$ V was set to 1 mA to avoid thermal destruction.

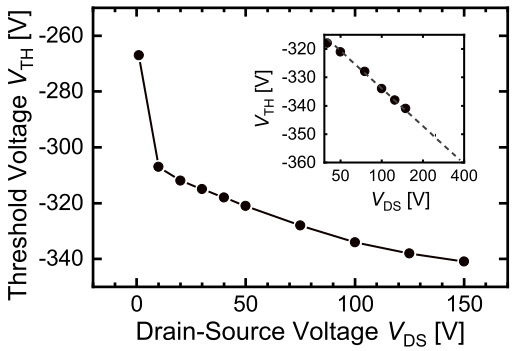

Fig. 8. Back-gate threshold voltage as a function of the drain–source voltage. Values are taken from the same measurements, as shown in Fig. 7, at a drain current level of $I_D = 1$ mA.

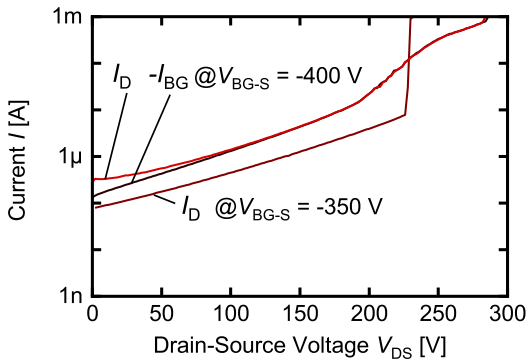

Fig. 9. Off-state characteristics of the back-gated HEMT with source-connected front gate. The OFF-state leakage was measured for two back-gate voltages, for $V_{BG-S} = -350$ and -400 V.

the same measurement data plotted with a semi-logarithmic x-axis, revealing that the threshold shift exhibits a logarithmic dependence on the V_{DS}. More detailed investigations are required to fully clarify the underlying physical mechanism; this, however, lies beyond the scope of the present work. The leakage current and breakdown behavior of the samples are shown in Fig. 9. First, an OFF-state sweep was performed at a back-gate voltage of $V_{BG-S} = -350$ V, during which an abrupt increase in drain current was observed at a drain–source voltage of approximately $V_{DS} = 220$ V. The measurement was

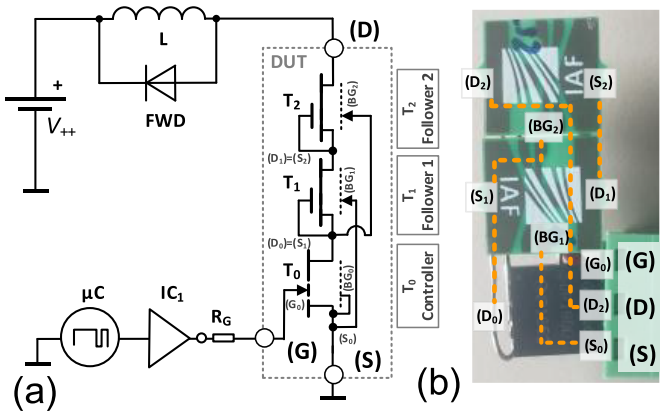

Fig. 10. (a) Double pulse measurement setup and a multistage cascode with back-gated followers and normally-OFF controller transistor. (b) Assembly of a discrete connected multistage cascode used in this work.

nondestructive, and the device remained fully functional. A subsequent measurement at $V_{BG-S} = -400$ V did not exhibit such an abrupt current increase. This behavior is consistent with the threshold-voltage shift extracted from the inset plot shown in Fig. 8. The extrapolated characteristics predict a back-gate threshold voltage of around $V_{BG-S} = -350$ V at a drain voltage $V_{DS} = 220$ V, so that an abrupt current increase at these bias conditions can be expected. It should be noted that this measurement represents enormous vertical field stress on the GaN buffer. This results in a vertical voltage of $V_{DS}-V_{BG-S} \approx 680$ V under this condition.

III. Back-Gated GaN-on-Si HEMTs in Cascodes

The back-gated MIS-HEMT characterized in Section II fulfills the requirements for a self-compatible transistor as a follower in multistage cascodes. It exhibits depletion-mode behavior with a very negative threshold voltage $V_{TH,BG} \approx -300$ V, and the transistor is capable of blocking the absolute value of its own threshold voltage $V_{BD} > |V_{TH}|$. In the following, we apply such HEMTs in multistage cascodes, and their behavior is investigated in a double pulse measurement setup.

The multistage cascode assembly and measurement setup are shown in Fig. 10. A commercial normally-OFF transistor is used as the controller transistor. In-house fabricated GaN-MIS-HEMTs are used as follower transistors. The front gates are connected to the individual source. The source contacts are connected to the substrate (back-gate) of the transistor stacked above. The in-house fabricated devices are packaged in a commercial PCB-embedding technology, as published in [25], and the devices are experimentally soldered as a pluggable cascode assembly for double pulse testing (see Fig. 10). The dynamic properties of back-gated HEMTs have been rarely studied till now. Furthermore, the dynamic behavior of multistage cascodes has also been little investigated so far. Therefore, this work focused on these properties and investigated them in a double pulse setup shown in Fig. 10. The circuit contains a power inductor $L = 860$ mH, a 600-V-class SiC free-wheeling diode, a gate-driver MIC4452, and a TI-MSP430 microcontroller that generates signals, including triggers, for oscilloscope and voltage source.

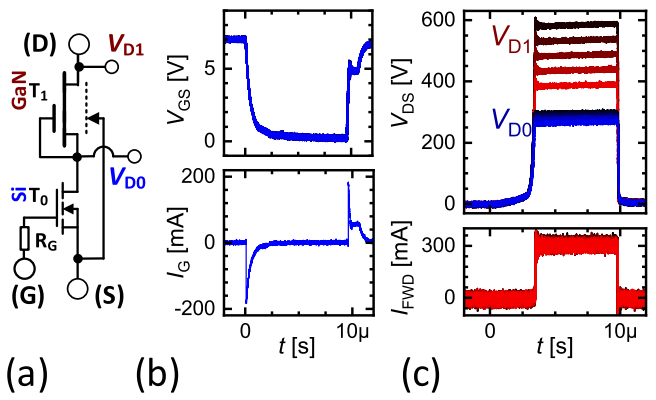

Fig. 11. (a) Cascode couple with a commercial normally-OFF Si-MOSFET (IPP60R099C6) as controller (blue) and stacked back-gated GaN-HEMT as follower (red). (b) Transient pulse characteristics. Gate voltage and gate current, which were measured above a gate resistor R_G = 39 Ω. (c) Transient pulse characteristics at the drain terminals V_{D0}, V_{D1}, and the freewheeling current I_{FWD}.

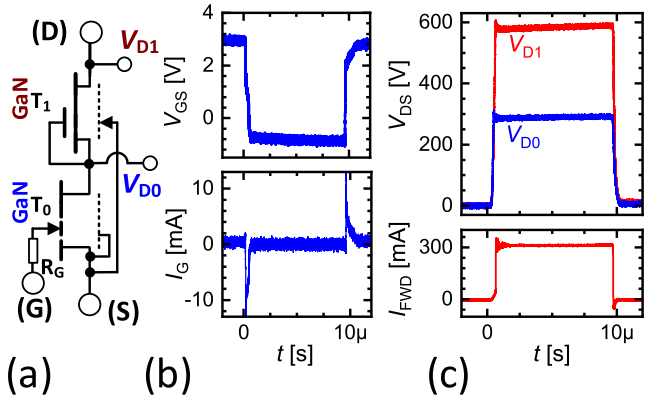

Fig. 13. (a) Cascode couple with a commercial normally-OFF GaN-HEMT (IGLD60R190D1) as controller (blue) and stacked back-gated GaN-HEMT as follower (red). (b) Transient pulse characteristics. Gate voltage and gate current, which were measured above a gate resistor R_G = 330 Ω. (c) Transient pulse characteristics at the drain terminals $V_{D0,D1}$, and the freewheeling current I_{FWD}.

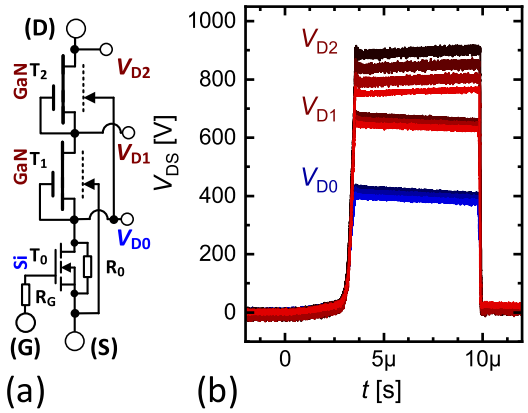

Fig. 12. (a) Multistage cascode with normally-OFF Si-MOSFET (IPP60R099C6) as controller (blue) and two back-gated normally-ON GaN-HEMT followers (red), a gate resistor R_G = 39 Ω, and bypass resistor R_0 = 1 MΩ. (b) Transient pulse characteristics at the drain terminals V_{D0}, V_{D1}, and V_{D2}.

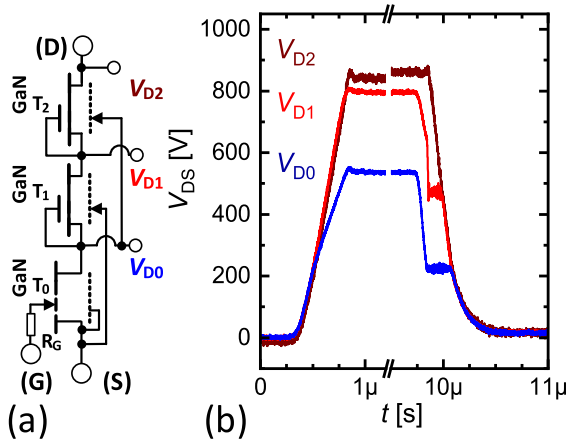

Fig. 14. (a) Multistage cascode with a commercial normally-OFF GaN (IGLD60R190D1) as controller (blue) and two back-gated normally-ON GaN-HEMT followers (red), and a gate resistor R_G = 330 Ω. (b) Transient pulse characteristics at the drain terminals V_{D0}, V_{D1}, and V_{D2}.

A. Double Pulse Measurement of a Multistage Cascode With Si-Controller and GaN-Follower(s)

In the first experiment, a back-gated MIS-HEMT (see Section II) was stacked above a 600-V-class Si-MOSFET (IPP60R099C6), as shown in Fig. 11. A robust Si-MOSFET with a relatively high gate charge and high gate resistance R_G was selected for this measurement. The cascode assembly is not optimized for fast switching. Thus, the selected conditions are intended to prevent uncontrolled switching from parasitic components (stray inductances, coupling, etc.). The transient behavior of the turn on and turn off is shown in Fig. 11. Gate voltage and current is shown in Fig. 11(b). The current was measured above a gate resistor R_G = 39 Ω with about $I_{G,MAX}$ = 200 mA (peak) and a gate charge of Q_G = 86 nC. A driver output voltage was chosen with V_{DRV+} = 7 V and V_{DRV} = 0. The transient signals of the drain terminals for rising voltage up to V_{DS} = 600 V are shown in Fig. 11(c). The stacked HEMT turns off starting at about V_{DS} = 300 V. Below this value, transistor T_1 is in the ON-state, since the back-gate threshold voltage has not yet been reached. This corresponds to the amount of the back-gate threshold voltage $V_{D0,MAX} \approx |V_{TH,BG,T1}|$ and is therefore to be expected. This OFF-state voltage $V_{D0} \approx |V_{TH,BG,T1}|$ remains stable at the MOSFETs drain for increasing V_{DS}. The differential voltage is blocked by the back-gate HEMT. The cascode was measured in the double pulse setup up to an OFF-state voltage of V_{DS} = 600 V.

In the next measurement, the setup was extended by a further stage by stacking another back-gated HEMT, as shown in Fig. 12. It is shown that both followers T_1 and T_2 turn off, which is expected. However, upon closer investigation, T_1 turns off at a voltage of about V_{D0} = 400 V in this measurement, which differs from the measurement in Fig. 10, where the same device turns off at V_{D0} = 300 V. This effect was only fully understood after the measurement campaign. The buffer leakage current from T_2 can only flowthrough the drift zone of T_0, but since T_0 is blocked, the drain voltage at T_0 increases. This can be solved by using a highly resistive bypass resistor, which was selected for this measurement at a value of R_0 = 1 MΩ. The bypass current would be approximately 300 μA at a back-gate threshold voltage $|V_{TH,BG,T1}|$ = 300 V.

TABLE I
COMPARISON OF THIS WORK VERSUS PREVIOUSLY REPORTED GAN-BASED CASCODES

Reference	[4]	[5]	[6]	[7]	[8]	[13]	[This Work]	[This Work]
Cascode Concept	Multi-Stage Cascode	Multi-Stage Cascode	Multi-Stage Cascode	Multi-Stage Cascode	Multi-Stage Cascode	Super Cascode	Multi-Stage Cascode	Multi-Stage Cascode
Controller	intgr. GaN-Segment	intgr. GaN-Segment	intgr. GaN-Segment.	40V-Si MOSFET	intgr. GaN-Segment	30 V-Si MOSFET	600V-Si MOSFET	600V GaN GIT-HEMT
Mode/Threshold Volt.	D / -3 V	E / ≈ 0 V	D / -2.4 V	E / 3 V	D / -70 V	D / -0.2 V	E / 3 V	E / 1.2 V
Number of Trans. Segm.	5	33	5	5	10	3	3	3
Bricks Concept	single Chip 600 V-Class	single Chip 600 V-Class	single Chip 600 V-Class	HEMTs+ BG-HEMTs 2x600 V	Self-comp. Mult.St.Cas. 2×600 V	D-MODE HEMTs 2×650 V	BG-MIS-HEMTs 2×600 V	BG-MIS-HEMTs 2×600 V
Follower Technology	GaN-on-Si	Si	GaN-on-SiC	GaN-on-Si	GaN-on-Si	GaN-on-Si	GaN-on-Si	GaN-on-Si
Follower Threshold Volt.	-70 V	-5 V	-125 V	-28V/-480V	-110 V	0 ..-20 V	≈ -350 V	≈ -350 V
Total Number of Dies	1	1	1	3	2	4	3	3
On-State Resistance	3.5 Ω	3.39 Ω	0.94 Ω	0.31 Ω	0.5 Ω	0.19 Ω	0.55 Ω	0.59 Ω
Blocking Voltage	600 V	790 V	1000 V	>1.2 kV	1000 V	>1.2 kV	-	-
Switched Off-Voltage / Switched On-Current	500 V / ≈ 0.3 A	400 V / 0.05 A	-	770 V / 0.3 A	-	800 V / 3 A	900 V / 0.3 A	850 V / 0.3 A

However, the actual buffer leakage current of T_2 is higher, so the voltage V_{D0} rises to the corresponding voltage value at which the leakage current can flow (≈400 μA). In double pulse testing, this cascode was able to block a voltage of up to V_{DS} = 900 V.

B. Double Pulse Measurement of a Multistage Cascode With GaN-Controller and GaN-Follower(s)

In the second experiment, a back-gated MIS-HEMT (see Section II) was stacked above a 600-V-class normally-OFF GaN-HEMT (IGLD60R190D1), as shown in Fig. 13. The GaN-HEMT has a significantly smaller gate charge with a value given in the data sheet of Q_G = 3.2 nC. This value corresponds with the measured value $Q_G = \int I_G \, dt$, which was measured above a gate resistor with R_G = 330 Ω, and is illustrated in Fig. 13(b). A driver output voltage was chosen with V_{DRV+} = 3 V and V_{DRV-} = −1 V. The transient signals of the drain terminals for rising voltage up to V_{DS} = 600 V are shown in Fig. 13(c). As in the assembly with the Si-controller above, the drain voltage of T_0 does not exceed $V_{D0,MAX} \approx |V_{TH,BG,T1}|$ = 300 V, since it is protected by the back-gated GaN-MIS-HEMT stacked above. As done in the experiment above, the cascode was extended by a further back-gate GaN-HEMT to build a multistage cascode with a normally-OFF GaN-HEMT controller and two back-gate normally-ON HEMTs as followers, as shown in Fig. 14. The controller GaN-HEMT (IGLD60R190D1) is realized as gate-injected transistor (GIT) gate [26]. The data sheet specifies an average gate current of max. $I_{G,avg}$ = 7.7 mA, which is relatively high. However, it seems that this only occurs at maximal drain current saturation. It is not visible under the condition as used in Fig. 13. The OFF-state gate leakage current of normally-ON Schottky gates usually corresponds to the negative drain leakage current. It was assumed in this experiment that the buffer leakage current of T_2 can be provided by gate–drain leakage and buffer leakage current of T_0. For this reason, a bypass resistor was not used. However, the experiment showed that this assumption was false under the given conditions. The drain voltage of the controller V_{D0} is increased up to about 500 V, which, with a V_{BG-S} = −500 V and a total vertical buffer spanning of about 800 V, means an enormous voltage stress for T_1 and led to destruction. It also shows that a bypass resistor is necessary for a GIT GaN-HEMT. In double pulse testing, this cascode was able to block a voltage of up to V_{DS} = 850 V.

IV. CONCLUSION, DISCUSSION, AND OUTLOOK

This work demonstrates that back-gated GaN-on-Si MIS-HEMTs can serve as self-compatible follower transistors in multistage cascodes. Separation of the overall OFF-state voltage V_{DS} across discrete stacked transistors ("bricks") in a direct-driven multistage cascode enables exceeding the 600-V limit of conventional lateral GaN-on-Si technologies. We investigated the back-gating characteristics of in-house 600-V-class MIS-HEMTs, which have a back-gate threshold of $V_{TH,BG} < -300$ V. The transfer curves show a reproducible drain–source voltage-dependent threshold shift driven by lateral electric fields.

Double-pulse measurements validate the concept: a cascode with a Si-MOSFET controller and two stacked back-gated GaN-HEMT followers is switched up to a voltage of 900 V. In a further experiment, a cascode with a GaN-HEMT controller with a GIT gate and two stacked back-gated GaN-HEMT followers is demonstrated up to 850 V. A key system insight is leakage management: buffer leakage from upper followers (T_2) requires a dedicated bypass path; without it, the controller drain rises toward the followers' back-gate threshold, increasing vertical field stress and risking failure. A high-ohmic resistor R_0 = 1 MΩ in parallel to the controller's drain–source terminals provides a suitable bypass for the buffer leakage of the upper back-gate HEMT T_2.

Table I compares the approach and results of this work with previous studies on related GaN-based cascodes. The key difference is that, using the back-gated approach, we successfully employ a standard 600-V-class MIS-HEMT structure as follower bricks for a multistage cascode with only minor adaptations, and demonstrate transients with voltages up to 900 V in application-relevant double-pulse measurements.

In future work, MIS-HEMTs should be specifically designed and optimized for the proposed multistage cascode concept. We expect that the currently large drain–source length of L_{DS} = 17 μm can be significantly reduced, leading to a lower drift-region resistance.

The experimental demonstrator shown in Fig. 10 was designed as proof of concept and, in its present form, is

neither electro-thermally optimized nor suitable for commercialization. From an electrical and thermal perspective, the modular bricks concept offers several opportunities but also introduces challenges, which are discussed in the following. First, distributing the overall blocking voltage across the cascode elements enables operation at very high voltages, in principle well beyond the levels demonstrated here, provided that sufficient isolation between the individual elements is ensured. At the same time, the individual transistors within the cascode should be arranged in a compact layout to avoid additional series inductances that degrade the switching performance. An advantage of the concept is that, in the linear operating region of the output characteristics, the cascode configuration distributes the power dissipation across the cascode stages (separation of the drift path). Different options can be considered to optimize the electro-thermal performance of the cascode. Bricks were attached to a PCB using thermal glue and interconnected by wire bonds in [8]. This assembly is electrically advantageous and compact, but still insufficient from a thermal point of view. Using an insulated metal substrate (IMS) could improve the thermal performance of this approach; similarly structured direct-bonded copper (DBC) substrates are also possible, particularly if power and voltage are further scaled up. Instead of discrete die attach and wire bonding, alternative integration technologies such as PCB embedding [25] or heterogeneous integration could be employed. Beyond that, a long-term vision is to develop a modular assembly technology that is stackable in a LEGO-like manner, using pluggable contacts to provide the electrical interconnection, while the heat is removed through an electrically insulated path to a heatsink to one side of the elements.

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