Master's Thesis

Thermal Characterization of GaN Power Switch HEMTs on Different Substrate Materials

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Abstract

The high demand for efficient and reliable power electronics motivates this comprehensive exploration into GaN-based power switch HEMTs, with a focus on thermal resistance characterization and simulation. Recognizing the variability in thermal properties reported in literature, this study investigates the influences of different epitaxy and substrate technologies on the junction temperature.

The thesis focuses on characterizing GaN power switching HEMTs with temperature sensors across diverse carrier substrates, aiming to determine thermal resistances via precise junction temperature measurements. Additionally, it explores GaN-on-GaN devices due to limited data availability, conducts thermal simulations to model these devices including GaN-on-Sapphire power HEMTs, and investigates the impact of substrate thickness variations on thermal resistance. The study also utilizes traditional methods like IR imaging to cross-verify results.

The thesis findings shed light on the influence of carrier substrate material on the thermal behavior of GaN power switch HEMTs, with varying thermal characteristics observed across different substrates. GaN-on-GaN devices demonstrated significantly superior thermal performance compared to GaN-on-Si devices. Additionally, thermal simulations revealed discrepancies in thermal conductivity values, emphasizing the importance of accurate parameterization for comprehensive understanding of device behavior. Cross-validation with IR thermography validated the effectiveness of the integrated sensor method, providing reliable temperature measurements crucial for device characterization and simulation.

In conclusion, this study offers a comprehensive analysis of thermal characteristics in GaN-based power switch HEMTs, highlighting the significance of substrate material, thickness, and buffer layer composition. By highlighting key factors influencing thermal resistance, the research contributes to the advancement of GaN-based power electronics and informs design decisions in thermal management strategies.

Zusammenfassung

Die hohe Nachfrage nach effizienter und zuverlässiger Leistungselektronik motiviert diese umfassende Untersuchung von GaN-basierten Leistungsschalter-HEMTs, wobei der Schwerpunkt auf der Charakterisierung und Simulation des thermischen Widerstands liegt. Angesichts der in der Literatur hohen Variabilität der thermischen Eigenschaften werden in dieser Studie die Einflüsse verschiedener Epitaxie- und Substrattechnologien auf die Sperrschichttemperatur untersucht.

Die Arbeit konzentriert sich auf die Charakterisierung von GaN-Leistungsschaltungs-HEMTs mit Temperatursensoren auf verschiedenen Trägersubstraten und zielt darauf ab, thermische Widerstände durch präzise Messungen der Sperrschichttemperatur zu bestimmen. Darüber hinaus werden aufgrund der begrenzten Datenverfügbarkeit GaN-on-GaN-Bauelemente untersucht, thermische Simulationen durchgeführt, um diese Bauelemente einschließlich GaN-on-Sapphire-Leistungs-HEMTs zu modellieren, und die Auswirkungen von Substratdickenvariationen auf den thermischen Widerstand untersucht. Die Studie nutzt auch traditionelle Methoden wie IR-Imaging, um die Ergebnisse zu überprüfen.

Die Ergebnisse der Arbeit beleuchten den Einfluss des Trägersubstratmaterials auf das thermische Verhalten von GaN-Leistungsschalter-HEMTs, wobei unterschiedliche thermische Eigenschaften auf unterschiedlichen Trägersubstraten untersucht wird. GaN-auf-GaN-Transistoren zeigten eine deutlich bessere thermische Performance im Vergleich zu GaN-auf-Si-Transistoren. Darüber hinaus zeigten thermische Simulationen Diskrepanzen bei den Werten der thermischen Leitfähigkeit, was die Bedeutung einer genauen Parametrisierung für das umfassende Verständnis des Bauelementverhaltens betont. Die Validierung mit IR-Thermografie bestätigte die Wirksamkeit der Methode mit dem integrierten Temperatursensor und lieferte zuverlässige Temperaturmessungen, die für die Charakterisierung und Simulation der Bauelemente unerlässlich sind.

Zusammenfassend bietet diese Studie eine umfassende Analyse der thermischen Eigenschaften von GaN-basierten Leistungsschalter-HEMTs und betont die Bedeutung von Substratmaterial, -dicke und Pufferschichtzusammensetzung. Durch die Untersuchung der Schlüsselfaktoren, die den Wärmewiderstand beeinflussen, trägt diese Studie zur Weiterentwicklung der GaN-basierten Leistungselektronik bei und liefert Informationen für Designentscheidungen bei Wärmemanagementstrategien.

1. Introduction

In the last decade, gallium nitride (GaN) has established itself as a superior material in the realm of power semiconductor devices [1]. GaN's impact is felt across diverse technological landscapes. Notably, GaN high electron mobility transistors (HEMTs) have found substantial deployment in power electronics, automotive electronics, high-frequency power amplifiers, wireless communication systems etc [2]. In each of these domains, GaN demonstrates remarkable performance, enabling advancements in efficiency, power density, and system miniaturization. GaN's emergence stems from its exceptional combination of a wide bandgap, high electron mobility, and thermal stability, making it an ideal candidate for a wide range of applications across various industries, compared to their silicon (Si) and silicon carbide (SiC) counterparts [1].

GaN power switches represent a paradigm shift, facilitating high efficiency and low system cost for power conversion applications through fast-switching and low losses. The promise of GaN HEMTs as switching power transistors is underscored by their high off-state breakdown strength and superior channel conductivity during operation [3].

Current advancements in GaN technology showcase static on-state resistance that outperforms silicon-based devices and rivals the performance of silicon carbide (SiC) counterparts [5]. The inherent characteristics of GaN, including high voltage and current density capabilities, enable the realization of very high-power densities in electronic systems. However, the manifestation of Joule heating effects during device operation necessitates effective thermal management strategies to mitigate self-heating effects and ensure device reliability, performance, and longevity.

Optimizing thermal resistance is paramount to fully harnessing the high operating temperature and power density capabilities of GaN HEMT devices. The choice of substrate materials significantly influences device junction temperature, making the extraction of junction temperature a fundamental aspect of thermal resistance characterization.

1.1 Motivation

Characterization and modeling of transistor thermal resistance are indispensable for designing circuits and packages that optimize heat dissipation of active devices, thereby enhancing the reliability and performance of transmission electronics. As such, this thesis deals with the characterization, simulation, of thermal resistance in GaN power switch HEMTs, aiming to unlock their full potential in power switching applications.

1.2 Problem and Scientific Question

The thermal properties of GaN HEMTs have been extensively studied in existing literature, predominantly focusing on high-frequency applications rather than power electronics. However, the thermal characteristics reported in these studies exhibit significant variability, posing challenges in their applicability to specific device structures. This variability arises from differences in layout, buffer layer thicknesses, doping concentrations, and operating conditions, leading to diverse heat sources within GaN HEMTs. Moreover, lateral GaN power technologies are being developed on alternative carrier substrates such as GaN-on-sapphire, GaN-on-SiC, and GaN-on-GaN. While literature exists on these carrier substrates, it often pertains to high-frequency technologies, utilizing buffer concepts that differ substantially from those employed in power devices. As a result, the transferability of findings from these studies to power electronic applications is limited.

In this study, a diverse selection of GaN wafers is available, each featuring different buffer layers and carrier substrates. Additionally, the devices fabricated from these wafers share a similar layout, enabling a direct comparison. Leveraging these resources, this work aims to investigate various scientific questions through both measurements and simulations:

- Which factors influence the thermal resistance in GaN HEMTs, particularly concerning different epitaxy and substrate technologies?
  - What impact does the material of the carrier substrate have on thermal resistance?
  - How does the thickness of the carrier substrate affect thermal resistance?
  - What influence do different buffer layers and structures exert on thermal resistance?
- What are the advantages and disadvantages of the characterization methods used in this study?
  - How effective is characterization with the temperature sensor?
  - What are the strengths and limitations of characterization with the IR camera?
  - What benefits are gained from using 3D FEM simulation in thermal characterization?
- Which simulation parameters from existing literature align with the findings of this study's own characterization efforts?

Ultimately, this research aims to facilitate the development of more efficient and reliable GaN-based power switch HEMTs and advance the field of thermal management strategies for power electronics.

1.3 Approach

Central to the thesis is the characterization of GaN power switching HEMTs integrated with a temperature sensor utilising different carrier substrates such as GaN-on-Si, GaN-on-SiC, and GaN-on-GaN, aiming to extract the thermal resistances of these devices through precise measurement of junction temperature. This integration of temperature sensing allows for precise monitoring of device temperatures providing valuable insights.

Furthermore, GaN-on-GaN characterization is an integral part of this thesis, as there is limited data available on this design. Studying the thermal behavior of these devices is crucial for understanding their performance characteristics and optimizing their operational parameters.

Leveraging thermal simulation approaches, this research aims to construct models based on characterization results to extract the thermal conductances of various materials. Moreover, the development of thermal simulation models derived from characterization data allows for predictive insights into up-coming technologies as GaN-on-Sapphire[9], [10]. The research plan also includes an exploration of the impact of varying substrate thicknesses on thermal resistance values. Simulating different thicknesses aims to elucidate the interplay between substrate thickness and the efficacy of various buffer layers in reducing junction temperature.

In addition to thermal simulations, traditional methods such as infrared (IR) imaging are used to cross-verify the results, providing a solid foundation for the work. By addressing these research objectives, this study aims to contribute to the advancement of GaN-based device technology and facilitate informed design decisions in thermal management strategies.

1.4 State of the Art

In this chapter, existing research relevant to GaN-based power switch HEMTs and thermal resistance characterization will be reviewed. Similar works in the field will be explored to provide context for this thesis, along with an explanation of the rationale behind choosing this topic. Additionally, traditional methods commonly used for thermal resistance extraction of GaN HEMTs will be outlined.

Kuzmik *et al*. [13] investigated AlGaN/GaN HEMTs grown on silicon and sapphire substrates using transistor DC characterization methods. They utilized 330-µm-thick sapphire or silicon wafers for their study. Their findings revealed that devices grown on silicon exhibit better cooling performance, with the AlGaN/GaN HEMT on silicon showing approximately four times lower thermal resistance compared to the device on sapphire. However, a direct comparison with our own layouts is not possible because no further details of the component dimensions were given.

Jeong Park *et al*. [14] examined the thermal performance of dual-gate-finger AlGaN–GaN heterojunction field effect transistors built on both sapphire and SiC substrates. They measured

peak temperatures on the device surface using nematic liquid crystal thermographic, a nondestructive and real-time temperature measurement technique. The study utilized an RF heat source. Their findings indicated that the junction-to-case thermal resistance of the device fabricated on a sapphire substrate is 4.4 times higher than that of the device built on a SiC substrate. Here too, a direct comparison is not meaningful, as the component dimensions differ greatly, the component area is very small and the component structure differs greatly.

In [15], the author compares pulsed I-V characteristics at different temperatures with direct-current (DC) measurements of AlGaN/GaN HEMTs grown on sapphire and silicon substrates. This technique allows for the determination of mean channel temperature and device thermal resistance, particularly relevant for RF applications.

Zhytnytska *et al*.'s [11] examining the dynamic thermal properties of large periphery AlGaN/GaN power switching HEMTs fabricated on both Si and SiC substrates. Their approach involves employing pulsed I_{DS} characterization at varying base plate temperatures and correlating it with ANSYS simulation results. Additionally, the heat source utilized for simulation reflects the methodology of this research work. However, it's worth noting that the thermal conductivity values utilized for simulation purposes are not explicitly stated, and they may differ from those employed in the present thesis work. Furthermore, no thermal resistance was determined experimentally or by simulation.

A. El-Helou *et al*. [12] conducted research similar to the focus of this thesis, utilizing a reverse modeling approach to extract thermal conductivity values of GaN HEMTs on various substrates, including GaN-on-silicon, GaN-on-SiC, and GaN-on-Diamond. However, their study primarily revolves around an optimized thermal model without comparisons with other methodologies. Notably, details regarding the epitaxial layers used with different substrates and the thicknesses of both the substrates and layers are not provided.

The majority of existing research in this domain primarily addresses RF devices, resulting in variations in buffer layers and heat sources compared to power switching HEMTs. Hence, it's crucial to conduct a comparative study involving GaN power switching HEMTs with diverse substrates, assessing the impact of substrate thicknesses and differing buffer layers on junction temperature. Additionally, measuring these parameters across various temperatures is crucial for a comprehensive understanding.

Some other traditional techniques utilized for thermal extraction in GaN HEMTs include:

Alternating Current (AC) Method: This approach analyzes the device's electrical characteristics under AC conditions to accurately extract thermal resistance. Employed in [16], it provides insights into the thermal behavior of GaN HEMTs on Si substrates.

Thermo-Sensitive Electrical Parameters (TSEPs): Utilized in [17], TSEPs involve correlating the device's electrical parameters with junction temperature to estimate thermal resistance. This

method, verified by infrared (IR) and simulation methods, offers convenience in measuring thermal resistance without breaking the package.

Pulse Recovery Data Analysis: Proposed in [18], this method extracts thermal resistance from pulse recovery data, providing insights into the dynamic thermal response of GaN HEMTs. It has been applied to Schottky-gate HEMTs on SiC substrates, demonstrating applicability to packaged devices.

Micro-Raman Method: This non-destructive approach, as demonstrated in [19], infers temperature distribution and thermal resistance by analyzing phonon vibrations within the device structure. It complements other thermal characterization techniques, providing insights into local thermal behavior.

Infrared Thermography: Employed in [20], Infrared (IR) visualizes temperature distributions across GaN HEMTs, identifying hotspots and temperature gradients. It offers valuable insights into localized heating effects and thermal management strategies.

Thermal simulations: Conducted using Finite Element Analysis (FEA) or Computational Fluid Dynamics (CFD) software, thermal simulations predict temperature distributions within GaN HEMTs. These simulations provide detailed insights into heat transfer mechanisms and aid in optimizing device structures [3].

While IR thermography may struggle with micron or sub-micron scale features and Raman thermography faces challenges with metal contacts obstructing optical access, TSEP methods encounter limitations due to trapping effects and specific device structures. Similarly, AC conductance has restricted applicability to certain device configurations and operating conditions, while thermal simulations demand accurate material properties and intensive computational resources.

To address these challenges, this thesis pursues a holistic approach that includes an integrated temperature sensor near the channel. This strategy aims to provide an accurate representation of junction temperature and extract thermal resistance across GaN HEMTs with various substrates including GaN-on-GaN. By complementing this experimental approach with simulations and IR measurements, the study endeavors to enhance result reliability and advance understanding in this critical area of GaN device technology.

1.5 Overview of this Thesis

This thesis embarks on a thorough investigation of GaN power switching HEMTs, equipped with a temperature sensor, with a specific focus on their linear region. The primary objective is to explore how different substrates influence junction temperature and to compare these findings with thermal simulations in order to extract material thermal conductivity. Furthermore, the study employs cross-validation using IR to ensure the reliability of the results.

Chapter 2 provides insights into the distinctions between RF microwave and power switching devices, along with an in-depth analysis of heat distribution within GaN HEMTs.

In chapter 3, attention shifts towards understanding the thermal properties of various materials relevant to GaN power switching HEMTs, laying the groundwork for subsequent thermal analyses.

Chapter 4 is dedicated to characterizing GaN HEMT devices thermally using an integrated temperature sensor method. This chapter explores various substrates, including Si, SiC, and GaN, and derives thermal resistance values crucial for developing thermal simulation models.

Moving to chapter 5, electro-thermal simulations are conducted using the established model. These simulations are then meticulously compared with characterized values to fine-tune the thermal parameters associated with each material used in GaN power switching HEMTs.

Chapter 6 introduces the IR method, serving as a robust validation mechanism by comparing simulation results with measured values.

Lastly, chapter 7 offers a comprehensive discussion of the results, examining their implications and potential applications. Additionally, this chapter outlines future research directions and advancements in GaN power switching HEMTs and thermal management strategies.

2. GaN High Electron Mobility Transistors

The literature [1]-[5] extensively discusses the fundamental structure and operation of GaN HEMTs, including the formation of the two-dimensional electron gas (2DEG). However, this thesis narrows its focus to the characterization and simulation of GaN power switching devices operating within the linear region. Consequently, this chapter shifts its attention towards outlining the differences between RF microwave and GaN power switching devices, as well as analyzing the heat distribution within these devices.

2.1 RF Microwave vs. DC Power Switching Devices

This section analyzes between GaN power switching devices and GaN microwave power devices, highlighting their operational conditions.

GaN power switching transistors designed for higher voltage operation differ significantly from GaN power electronic devices optimized for microwave capabilities. GaN power electronic devices are designed to operate safely at the 600 V or even the 1200 V node, whereas lower frequency devices typically operate at a drain bias of around 50 V. Consequently, the development of GaN power switching devices necessitated the introduction of novel technological concepts such as modified epitaxial buffer structures, field plates, and passivation layers [5].

The operational principles of power devices differ from those of standard microwave devices as shown in figure 1. Analogue microwave amplifiers utilize the entire I/V characteristic and operate around a fixed bias point, allowing for voltage and current overshoots. In contrast, power switching devices exhibit quick transitions between the off-state and on-state bias points (labelled as I and II in figure). For power switching devices, minimizing the transition time between states is essential to ensure energy-efficient operation. Ideal power switching devices

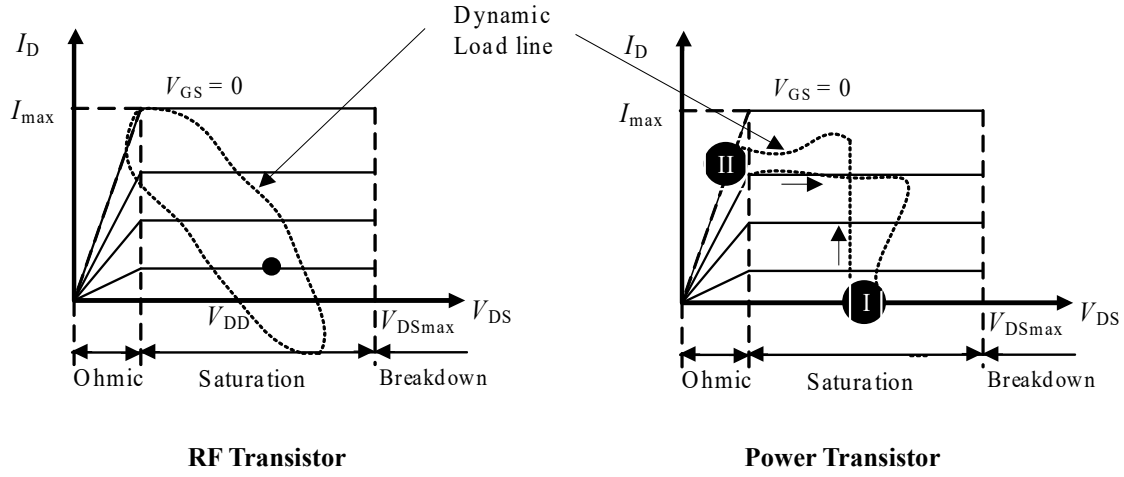


Figure 1 Comparison of typical operational modes for RF microwave (left) and DC power switching devices (right) [5].

strive for a balance between low on-state resistance and high breakdown voltage during off-state conditions to minimize reduce residual drain voltage at on state and device leakage currents at off state [5].

Efficient operation of power switching devices also necessitates quick transition times between states to switch significant power levels without excessive dissipated power. Conversely, microwave amplifiers in analogue amplification mode incur thermal losses and have strict heat dissipation limitations due to the dynamic load point's location in the I/V characteristics [5].

In summary, power switching GaN devices differ from microwave amplifiers in their operational modes and efficiency standards. The adaptability of power switching devices across various applications is enhanced by their relaxed thermal design conditions.

2.2 Heat Distribution in GaN HEMTs

Heat generation in GaN HEMTs primarily stems from Joule heating, which is fueled by the high current density and electric fields present within the channel. Understanding the distinctive heat distribution patterns in different operational regions is essential for devising effective thermal management strategies aimed at mitigating localized heat accumulation and ensuring optimal device performance and reliability.

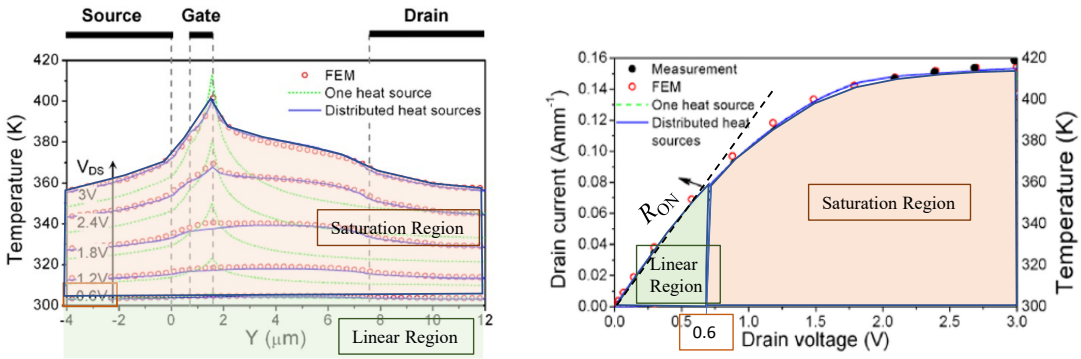
In GaN HEMTs, the distribution of heat is influenced by various factors and differs between the linear and saturation regions of operation.

In the linear region, where partial depletion is absent along the drift length, the on-state resistance is primarily determined by the sheet resistance, drain-source length, and width of the device $R_{ON} = R_{SH} \cdot L_{DS}/W$. Consequently, power loss and heat generation along the drift line are relatively uniform, resulting in a predominantly flat power dissipation profile across the active area of the transistor.

Conversely, in the saturation region, partial depletion occurs near the gate edge on the drain side, leading to an uneven distribution of heat along the drift length. This non-uniform heat distribution results in localized heat accumulation, particularly near the gate edge on the drain side.

Figure 2 illustrates the evolution of temperature within the HEMT structure [21]. At lower drain-source voltages, the temperature distribution appears more uniform. However, as the voltage increases, a notable temperature peak emerges at the drain side of the gate, indicating a shift towards non-uniform heat distribution.

This thesis primarily centers on characterizing and simulating power switch devices operating within the linear region. Consequently, it takes into account a uniform distribution along the channel during simulations.



a) **b)**

Figure 2 a) Illustrates the evolution of temperature inside the HEMT structure and b) shows the measured and simulated I-V characteristics, as published in reference [21] where measurements and simulations were conducted using both one heat source and distributed heat sources approaches, and compared with FEM simulation results.

3. Thermal Properties of GaN Power Switch HEMTs

This chapter deals with a comprehensive literature review focusing on the thermal conductivity of various layers within AlGaN/GaN power switch HEMTs. The thermal properties of these layers play a pivotal role in the overall performance and reliability of HEMT devices. Additionally, this chapter aims to identify crucial thermal parameters for the materials employed as substrates in HEMT fabrication.

3.1 Thermal Conductivity: A Literature Review

Thermal conductivity is a critical parameter governing the self-heating dynamics within AlGaN/GaN HEMTs, profoundly influencing device performance and reliability. While it's enough to consider bulk thermal conductivities for substrate materials, the epitaxial layers require careful attention due to their complex roles.

The epitaxial growth process typically starts with the deposition of an aluminum nitride (AlN) nucleation layer (NL), essential for initiating crystalline growth on the substrate utilizing either MBE (Molecular Beam Epitaxy) or MOCVD (Metal Organic Chemical Vapor Deposition) processes. The AlN NL is considered in isolation because it occurs in every AlGaN/GaN epitaxy and several studies examine the resistance of this layer separately. These nucleation layers are then followed by a relatively thick buffering layer, which usually consists of either a stepwise mixed AlGaN layer or a superlattice (SL) [7], to provide both electrical isolation from the underlying films to reduce substrate leakage and a lattice transition to the GaN channel layer. The active GaN and AlGaN layers follow, with the aluminum content in the barrier layer typically ranging between 22% and 32%. The epitaxial heterostructure is then capped with a GaN layer to mitigate oxidation of the underlying AlGaN film [6]. The layer structure, depicted

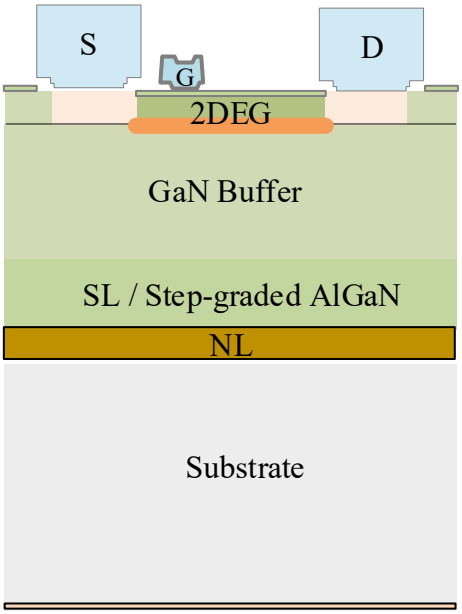


Figure 3 Typical GaN power switch HEMT cross-section layer structure.

in figure 3, illustrates the composition and arrangement of the epitaxial layers grown during the manufacturing process.

It's worth noting that thin film conductivity reduction due to scattering processes necessitates careful consideration. Additionally, the temperature-dependent nature of thermal conductivity, often described by equation (3.1), underlines the dynamic nature of heat dissipation mechanisms in these materials [3].

$$k(\mathrm{T}) = k_{300} \cdot \left(\frac{\mathrm{T}}{300}\right)^{\alpha} \tag{3.1}$$

where k_{300} is the thermal conductivity at reference temperature (300 K), T is the absolute temperature and α is a negative number [24].

According to Kevin Bagnall [3], equation (3.1) could also be expressed as

$$k(\mathrm{T}) = k_{300} \cdot \left(\frac{300}{\mathrm{T}}\right)^{n} \tag{3.2}$$

where n is a positive number.

Doping introduces further complexity, impacting lattice thermal conductivity through additional phonon-scattering mechanisms associated with impurity atoms [32], [38]. Ignoring doping dependencies in thermal modeling may lead to underestimations of device self-heating, consequently affecting performance and reliability [39]-[42].

The subsequent sections deal with the thermal conductivities of individual layer components, shedding light on their specific contributions to overall heat dissipation in AlGaN/GaN HEMTs.

3.1.1 AlGaN

Evaluations of the thermal conductivity of thin films made of GaN and its alloys are crucial for addressing concerns related to device self-heating. In AlGaN/GaN layers, the gradual reduction of aluminum content during growth introduces complexities in thermal behavior. Point defect scattering, arising from the mixing of aluminum and gallium in the ternary solid solution, significantly impacts thermal conductivity, diminishing it compared to pure AlN and GaN [4].

Liu and Balandin [22] utilized the differential 3ω technique to measure the thermal conductivity of $Al_xGa_{1-x}N$ thin films (x = 0 and 0.4) grown via hydride vapor phase epitaxy (HVPE). Their findings, obtained at room temperature (300 K), yielded a value of approximately 25 W/mK, aligning well with predictions based on the virtual crystal model.

Table 1 AlGaN film thermal conductivity values from literature.

***k* (@ 300 K) (W/mK)**	**x-portion**	**Reference**
25	0.4	[22]
25 - 55	0.4 – 0.1	[23]
3.1	N/A	[24]

In a subsequent study, Liu and Balandin [23] further investigated thermal conduction in $Al_xGa_{1-x}N$ alloys, employing the differential 3ω technique across a temperature range of 80 to 400 K. They observed room-temperature thermal conductivity varying between 25 and 55 W/mK as the aluminum mass fraction changed from 0.4 to 0.1.

Stanislov Vitanov's dissertation [24] contributed to this body of knowledge by comparing two models, alongside other existing models and experimental data. His work models thermal conductivity as a function of aluminum content, adopting a value of 3.1 W/mK.

The values are summarized in table 1.

3.1.2 GaN

The reported values for the thermal conductivity of GaN bulk material and thin films exhibit significant discrepancies, primarily attributed to scattering mechanisms such as point defects and dislocations within the GaN layer.

Thomas Bougher [25] investigated the impact of transition layers in GaN-on-Si wafers using the time-domain thermo-reflectance (TDTR) method. For a 50 µm GaN film grown by hydride vapor phase epitaxy, a thermal conductivity value of 135 W/mK was reported. For thinner films with thickness ranging from 0.3 to 1.3 µm grown via metal-organic chemical vapor deposition (MOCVD), thermal conductivity values were in the range of 127-136 W/mK. He found that the reduction in thermal conductivity due to defect density dominates over boundary scattering, indicating that GaN thermal conductivity is not strongly dependent on layer thickness.

Table 2 GaN film thermal conductivity values from literature.

***k* (@ 300 K) (W/mK)**	**Thickness (µm)**	**Substrate**	**Growth method**	**Reference**
127-136	0.3-1.3	Si	MOCVD	[25]
>155	5	Al_2O_3	LEO	[26]
150	1.2	Si & SiC	MOCVD	[27]
185	0.5-0.7	Si	MBE	[28]
167	0.6-1.6	SiC	MBE	[28]
150	1	SiC & Sapphire	N/A	[29]
110-180	3-4	N/A	MOCVD	[34]
0-120	0.015-1	N/A	MBE	[35]
150	0.064	N/A	MBE	[37]

Luo *et al*. [26] reported a thermal conductivity exceeding 155 W/mK for a 5 µm GaN film grown via lateral epitaxial overgrowth (LEO). For bulk single crystals, a value of 130 W/mK was reported, measured using third-harmonic electrical measurement.

Using Raman Spectroscopy, Sarua *et al*. [27] measured the thermal conductivity of a 1.2 µm thick GaN film grown via MOCVD and reported a value of 150 W/mK.

Cho *et al*. [28] employed the TDTR method to measure the thermal resistance of AlN layers for GaN-on-Si and GaN-on-SiC. For GaN-on-SiC, a thermal conductivity value of 167 W/mK was reported for a thickness of 0.6-1.6 µm, while for GaN-on-Si, a value of 185 W/mK was reported for a thickness of 0.5-1.7 µm.

Table 3 GaN Bulk thermal conductivity values from literature.

***k* (@ 300 K) (W/mK)**	**Thickness (µm)**	**Growth method**	**Reference**
160-226	100	High Pressure synthesis	[30]
130	400	HVPE	[31]
86.5-201	260-505	HVPE	[32]
195-230	N/A	HVPE	[33]
164-196	N/A	Ammonothermal	[36]
170	N/A	N/A	[44]

Ali M. Darwish *et al*. [29] utilized a model to calculate the thermal resistance of a multi-finger AlGaN/GaN HEMT device, employing a thermal conductivity value of 150 W/mK for a 1 µm thick GaN film.

Jeżowski *et al*. [30] measured the thermal conductivity of bulk GaN crystals for the temperature interval of 4.2-300 K under high pressure. Three samples of bulk n-type differing in impurity/defect concentration and one heavily magnesium-doped GaN were used for the experiment. The thermal conductivity values recorded at 300 K are 226 W/mK for sample No. 1, 188 W/mK for sample No. 2, and 160 W/mK for sample No. 3. They mentioned that for n-GaN crystal, Umklapp phonon scattering processes dominate, whereas for other samples, scattering of phonons by point mass defects represents the main contribution.

E.K. Sichel *et al*. [31], investigated the thermal conductivity of 400 µm GaN fabricated by HVPE for temperatures ranging from 25 to 360 K, reporting a value of 130 W/mK at room temperature (300 K). The low thermal conductivity value was attributed to the high impurity concentration, which was around10^{18} cm^{-3}.

Yiwen Song *et al*. [32], studied HVPE-grown bulk GaN substrates with various doping schemes and concentrations, including Fe-doped (92.7±13 W/mK), Mg-doped (152±9.4 W/mK), Si-doped (86.5±5 W/mK), and unintentionally doped (UID) (193±22 W/mK). Among these samples, the heaviest Si-doped n+ sample exhibited the highest thermal conductivity value of 201±9.4 W/mK.

The non-linear temperature behavior of thermal conductivity for GaN, as described by equation (3.1) and equation (3.2), indicates a decrease in thermal conductivity with increasing

Table 4 GaN model parameters from literature.

***k* (@ 300 K) (W/mK)**	**α/n**	**Reference**
130	-0.43	[24]
220	-1.2	[24]
150-220	-0.43	[4]
150	1.4	[3]

temperature. These temperature-dependent variations in thermal conductivity are detailed in the accompanying table 4.

These diverse findings underscore the complexity of accurately characterizing the thermal conductivity of GaN materials and highlight the influence of growth methods, film thickness, doping concentrations, and measurement techniques on reported values and also the non-linear temperature behavior.

Table 5 AlN thin film thermal conductivity values from literature.

***k* (@ 300 K) (W/mK)**	**Thickness (µm)**	**Reference**
25	100	[25]
19	100	[4]
6	0.06	[3]
6-7	N/A	[72]
30.5	0.6	[74]

3.1.3 Nucleation Layer

AlN serves as an essential interface to alleviate stresses in GaN and diminish the occurrence of defects, crucial for enhancing the quality, performance, and longevity of devices in the absence of a suitably matched substrate [25].

Robert Rounds *et al*. [36] conducted an analysis of the thermal conductivity of single crystal AlN samples with varying impurity concentrations, utilizing the 3 ω method across temperature ranges of 30-325 K. They reported a high thermal conductivity value of 341 W/mK at room temperature for bulk AlN crystal.

Intrinsic single-crystal AlN demonstrates a notably high thermal conductivity, surpassing 200 W/m-K. However, thin defective films commonly employed in transition layers exhibit thermal conductivity values approximately one order of magnitude lower. Bougher *et al*. [25] measured the thermal conductivity of a 100 nm thin AlN layer to be 25 W/(mK) at room temperature.

Zonghui Su *et al.* [72] conducted thickness-dependent thermal conductivity measurements on aluminum nitride (AlN) thin films grown via two methods on (0001) surfaces of silicon carbide (SiC) and sapphire substrates with varying surface roughness. Their findings suggest a thermal conductivity of approximately 6–7 W/mK for CMP-SiC-based devices when predicting operating temperatures.

The non-linear temperature behavior of thermal conductivity for AlN are shown in table below.

Table 6 AlN model parameters from literature.

***k* (@ 300 K) (W/mK)**	**α/n**	**Reference**
350	-1.7	[24]
285-340	-1.58	[4]
6	2.76	[3]

3.1.4 Substrates

Bulk GaN has already been discussed above where they are used as substrates. Other materials like Si, SiC, sapphire, QST and diamond which are considered as carrier substrates for GaN HEMTs are discussed in this section

3.1.4.1 Silicon

Silicon has emerged as the preferred substrate for GaN-based power HEMTs due to its cost-effectiveness and wide availability. However, achieving defect-free GaN epilayers on silicon substrates is challenging due to significant lattice and thermal expansion coefficient mismatches with GaN [68]. The incorporation of dopants into undoped silicon hosts inevitably increases mass variance, leading to a reduction in thermal conductivity. Consequently, undoped silicon exhibits the highest thermal conductivity, which diminishes with greater differences between dopant and host masses [46]. These challenges show the importance of understanding the role of doping and impurities in silicon substrates utilized for GaN devices.

Silicon wafers doped with elements like phosphorus, aluminium, boron, or arsenic are commonly utilized in electronics. High levels of doping can substantially reduce the thermal conductivity of silicon, impacting the performance of GaN-based devices. Additionally, unintentional impurities may have previously impacted reported thermal conductivity values in bulk silicon samples for which impurity concentrations were determined from the electrical resistivity [57]. The selection of dopants and the management of impurities become critical factors in optimizing the thermal properties of silicon substrates for GaN applications.

Heavily doped silicon substrates are extensively employed in the manufacturing of discrete power devices [78], [79], [80]. These substrates typically consist of an epitaxial layer grown atop a heavily doped silicon substrate, with the dopant type and resistivity tailored to meet specific device requirements [70]. The demand for silicon substrates with extremely low resistivity ranges is increasing, driving innovation in substrate design and fabrication processes. This trend highlights the importance of considering both the electrical and thermal characteristics of silicon substrates in GaN device engineering.

Silicon substrates, both high-resistivity (HRS) and low-resistivity (LRS), are explored for their scalability and cost advantages. HRS silicon substrates are preferred for RF GaN devices due to lower substrate loss, while LRS substrates dominate in GaN power HEMTs owing to their cost-effectiveness and larger wafer sizes [69]. The choice between HRS and LRS substrates depends on the specific requirements of the GaN device and the intended application, underscoring the need for comprehensive substrate characterization and selection processes.

Additionally, several studies provide insights into the thermal conductivity of silicon. Thomas Gerrer [4] in his dissertation reports a thermal conductivity (k) value of 148 W/mK for silicon at room temperature.

Rüdiger Quay, referring to S. Selberherr's work, cites a k value of 125 W/mK with $\alpha = -1.65$ [49].

Shanks *et al*. (1963) [53] determined the thermal conductivity of pure silicon within the temperature range of 300 to 1400 °C by calculating the product of thermal diffusivity, specific heat, and density. At 300 K, the calculated thermal conductivity value stands at 142 W/mK.

Some additional values of thermal conductivity for pure silicon are provided in table 7.

The earliest recorded thermal conductivity data for an impure sample of silicon was reported by Koenigsberger and Weiss in 1911, who found a value of 84 W/mK at 290 K [52].

M. Ashegi *et al*. [57]conducted measurements on the thermal conductivities of free-standing silicon layers doped with boron and phosphorus at concentrations ranging from $1 \cdot 10^{17}$ to $3 \cdot 10^{19}$ cm $^{-3}$ over temperatures from 15 to 300 K. At 300 K, bulk silicon doped with $3 \cdot 10^{19}$ cm $^{-3}$ phosphorus atoms and $1 \cdot 10^{19}$ cm $^{-3}$ boron atoms yielded a thermal conductivity value of approximately 80 W/mK.

Konstanze Hahn *et al*. [58] reported a similar value of 80 W/mK for silicon doped with 10^{20} cm $^{-3}$ gallium atoms at 300 K, calculated using density functional perturbation theory and the phonon Boltzmann transport equation.

Clemens [59] reported thermal conductivity values of 122 W/mK for n-type doped silicon and 125 W/mK for p-type doped silicon at room temperature, both with dopant concentrations of $2 \cdot 10^{19}$ cm^{-3}.

Table 7 Pure Si thermal conductivity values from literature.

***k* (@ 300 K) (W/mK)**	**Thickness (µm)**	**Reference**
148	N/A	[4]
150	100	[49]
142	N/A	[53]
145	N/A	[55]
156	N/A	[53]
130	N/A	[56]
160	N/A	[44]

Yongjin Lee *et al*. [60] investigated the thermal conductivity of crystalline silicon by doping it with various elements such as boron, aluminum, phosphorus, and arsenic. They found that at a dopant concentration of approximately $5 \cdot 10^{20}$ cm^{-3}, the thermal conductivity of silicon decreased from 137 W/mK at 300 K in undoped silicon to 18/39/57/78 W/mK in arsenic/boron/phosphorus/aluminum-doped silicon.

Andriyevsky *et al*. [61] employed a theoretical approach to calculate the thermal conductivity of crystals based on first principles molecular dynamics. Applying this method to silicon and phosphorus-doped silicon crystals at room temperature, they found a thermal conductivity value of approximately 75 W/mK for silicon doped with 10^{20} cm^{-3} phosphorus atoms.

Table 8 offers further data on the thermal conductivity of silicon doped with various elements.

Table 8 Doped Si thermal conductivity values from literature.

***k* (@ 300 K) (W/mK)**	**Doping conc. (cm^{-3})**	**Reference**
125	p [$2 \cdot 10^{19}$]	[59]
122	n [$2 \cdot 10^{19}$]	[59]
84	N/A	[57]
80	B [$1 \cdot 10^{19}$], P [$3 \cdot 10^{19}$]	[58]
80	Ga [$1 \cdot 10^{20}$]	[57]
78	Al [$5 \cdot 10^{20}$]	[60]
75	P [10^{20}]	[61]

Single crystal silicon is isotropic, meaning there is no preferred direction or crystal axis for the propagation of thermal energy throughout the bulk material [6]. The non-linear temperature behavior described by equation (3.1) is presented in the accompanying table 9.

Table 9 Si model parameters from literature.

k (@ 300 K) (W/mK)	α/n	Reference
148	-1.35	[49]
148	-1.65	[4]

3.1.4.2 Silicon Carbide

Silicon carbide possesses a unique set of properties, including excellent thermal and electrical such as a wide band gap, high thermal conductivity, high critical breakdown electric field, high carrier saturation velocity. Consequently, SiC devices can withstand harsh operating conditions, including high temperature, high power, high voltage, high frequency, and strong radiation. This versatility makes SiC suitable for a wide range of applications including automotive electronics, radar communication, high-voltage power transmission etc [62]. The high thermal conductivity

Table 10 SiC Bulk thermal conductivity values from literature.

k (@ 300 K) (W/mK)	Thickness (µm)	Orientation/Doping	Reference
490	N/A	6H	[49]
390	N/A	6H	[65]
334	N/A	6H	[63]
330	N/A	4H	[49]
280	N/A	4H	[62]
330-370	N/A	V-doped	[49]
330	350	V-doped	[50]
330-408	100	N/A	[29]
370	100	N/A	[49]

(*k*) of SiC is particularly crucial for thermal management in these electronic and optoelectronic devices, especially for high-power applications [71].

The thermal conductivity of SiC exhibits anisotropic behavior, with a 20 % - 30 % difference between the thermal conductivity along the a-axis and the c-axis of the crystal. To address this anisotropy, a common approach involves measuring an average (or equivalent isotropic) thermal conductivity and treating SiC as an isotropic material [29]

Moreover, various investigations have shed light on the thermal conductivity of SiC concerning orientation and doping effects. Kevin Bagnall [3] in his dissertation, observed orthotropic thermal conductivity values for SiC, with variations in both the cross-plane (c-axis) and in-plane directions. He reported thermal conductivity values of 390 W/mK and 490 W/mK for the cross-plane and in-plane directions, respectively. For his model, with a SiC substrate thickness of 100 μm, he adopted a thermal conductivity value of 400 W/mK.

Rusheng Wei *et al*. [62] conducted experiments to measure the thermal conductivity of 4H - SiC crystals as a function of temperature. They observed different trends for N-type SiC normal to the c-axis and V-doped semi-insulating SiC crystals, which were proportional to $T^{-1.26}$ and $T^{-1.256}$. At room temperature, they reported thermal conductivity values of 280 W/mK and 347 W/mK, respectively.

Perevislov *et al*. [63] investigated the effect of B_4C concentration on the thermal conductivity of SiC. They reported a thermal conductivity value of 334 W/mK for single-crystalline 6H-SiC at room temperature.

Xin Qian *et al*. [64] investigated the anisotropic thermal conductivity of three SiC samples, including n-type 4H-SiC (N-doped 1×10^{19} cm^{-3}), unintentionally doped (UID) semi-insulating (SI) 4H-SiC, and SI 6H-SiC (V-doped 1×10^{17} cm^{-3}) measured using TDTR method. At 300 K, the thermal conductivity values in the in-plane direction were approximately 450, 490, and 390 W/mK, respectively, while in the cross-plane direction, the values were around 280, 330, and 270 W/mK, respectively.

The thermal conductivity of bulk SiC shows a steady decrease with temperature, particularly noticeable at and beyond 300 K, exhibiting an approximate $T^{-\alpha}$ functional form with $1 < \alpha < 2$. This reduction in thermal conductivity has significant implications for device performance, particularly in high-voltage operations, where device self-heating can lead to internal temperature rise, performance degradation, instability, and even device failure under high bias conditions [62]. The non-linear temperature behavior described by equation (3.1) is detailed in the accompanying table 11.

Table 11 SiC model parameters from literature.

k **(@ 300 K) (W/mK)**	**α/n**	**Reference**
390	-1.5	[49]
280	-1.26	[62]
347	-1.256	[62]
390/490	1.3	[3]

3.1.4.3 Sapphire/Diamond/QST

Sapphire substrates, readily available in diameters exceeding 4 inches at low cost, suffer from inefficient heat removal due to their low thermal conductivity [67].

Weili Liu *et al*. [23] observed a slight difference in thermal conductivity between the c-parallel and c-perpendicular directions of sapphire, with values of 25 W/mK at 299 K and 23 W/mK at 296 K, respectively. They averaged these values to account for the small directional anisotropy.

Thermal conductivity values for sapphire typically range from 23 to 35 W/mK [23][29][66][67].

In contrast, diamond stands out as the optimal choice for heat spreaders in electrical components, boasting unparalleled thermal conductivity compared to any other substrate.

According to Thomas Gerrer [4], a single-crystalline diamond exhibits a remarkable thermal conductivity value of 2200 W/mK, while the value slightly decreases to 1500 W/mK for polycrystalline diamond, with an α value of -1.85.

The Qromis Substrate Technology (QST) introduces a ceramic poly-aluminum nitride (AlN) layer with the aim of delivering exceptional performance at a low cost, thereby unlocking new applications by providing access to advanced semiconductor process and device technologies for GaN circuit structures.

Designed to match the coefficient of thermal expansion (CTE) of GaN, the QST substrate effectively mitigates warpage and cracking of the GaN epitaxial layer. This feature enables the growth of large-diameter (6-inch, 8-inch, 12-inch), high-quality thick GaN epitaxial layers. As a result, it is anticipated that QST substrates will find applications in power devices [75].

Table 12 Sapphire/Diamond/QST thermal conductivity values from literature.

Material	*k* (@ 300 K) (W/mK)	Reference
Sapphire	23-25	[23]
	30	[67]
	33	[66]
	35	[29]
Diamond	2200	[4]
	1500	[4]
QST	170-220	[76]

3.2 Summary & Discussion

This chapter gave an exhaustive review of the thermal conductivity characteristics of key materials vital for GaN-based devices, such as GaN, Si, SiC, AlN, and emerging substrates like sapphire and QST. The review explored different ways of growing materials and their properties, showing how they interact with each other and affect thermal behavior. Notably, the non-linear temperature behavior described by equation (3.1) highlighted the dynamic nature of thermal conductivity, with significant implications for device operation, particularly under high-voltage conditions where self-heating effects are pronounced. Looking forward, the insights discovered from this review will play a pivotal role in thermal simulations in later section. By using accurate thermal parameters that match specific materials and operating conditions, these simulations will help create strong and dependable GaN-based devices for different uses.

Table 13 Summary of thermal conductivity values used for thermal simulation of GaN power switch HEMTs.

Material	***k* (@ 300 K) (W/mK)**	**Reference**
GaN film	127	[25]
AlN (NL)	25	[25]
SL	10	[4]
Step-graded AlGaN	14	
Si Bulk	80	[57]
GaN Bulk	130	Supplier
SiC	330	[50]
Sapphire	35	[29]
Contacts	315	[4]

4. Thermal Characterization on GaN Power Switch HEMTs

This chapter explores the thermal characterization of GaN power switch HEMT devices. Given the thermal challenges these devices pose, precise measurement techniques are necessary to ensure optimal performance. The methodology centers on a high-voltage GaN-based power switch HEMT equipped with a highly linear, monolithically integrated temperature sensor [8]. Known for its precision, the chosen measurement method offers accurate insights into the device's junction temperature. Expanding on this methodology, the chapter explores GaN power HEMT devices with diverse substrate materials, with the goal of extracting crucial thermal resistance data. These efforts are pivotal for power electronics applications and ensuring the efficiency and reliability of GaN-based devices under demanding operating conditions.

4.1 Integrated Temperature Sensor Method

Thermal characterization is crucial for understanding the performance of GaN HEMT devices, and the integrated temperature sensor method provides a robust approach in this regard. The method focuses on the linear region within the HEMT's output characteristic and utilizes an integrated temperature sensor positioned as a metal meander near the gate. Figure 4 illustrates the measurement circuit [8], which enables meticulous data collection and analysis to determine the thermal resistance (R_{TH}).

Data acquisition is conducted using an Agilent B1500a impedance analyzer operating in continuous IV mode, with a high-power source measurement unit (HPSMU) facilitating precise measurements. The experimental setup utilizes six needle probers from Cascade, equipped with

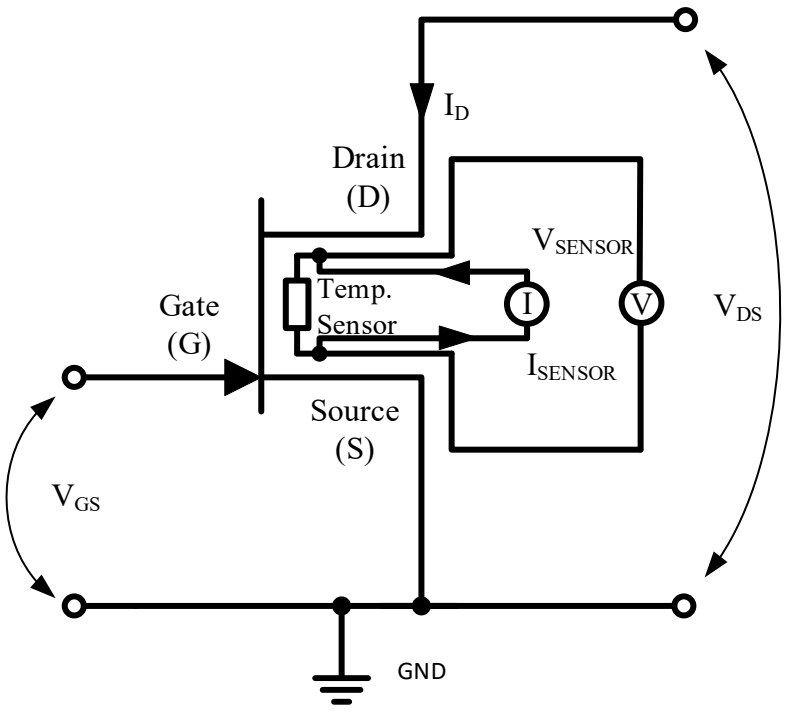
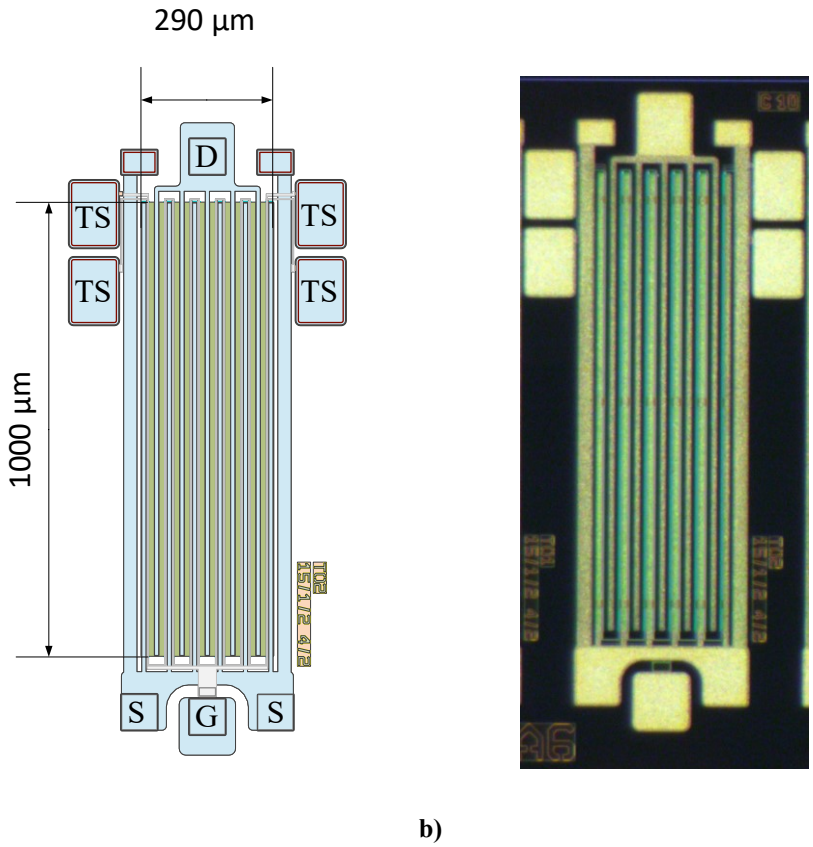


Figure 4 Circuit of the GaN HEMT with integrated temperature sensor.

a temperature unit to ensure accurate control of the backside temperature. Measurements are performed at distinct chuck temperatures (T_C) ranging from 20°C to 80°C.

The measurement setup allocates four needles to temperature pads for a four-point measurement, enabling precise determination of sensor current (I_{SENSOR}) and voltage (V_{SENSOR}). The remaining needles measure drain current (I_D) and drain-source voltage (V_{DS}) values. The drain-source voltage (V_{DS}) is swept from 0 to 2°V, while the sensor voltage ranges from 0 to 1 V with 51 steps.

In HPSMU mode, the drain current is limited to 1 A with a power compliance of 20 W. The



a) **b)**

Figure 5 a) Layout 1 of GaN power switch HEMT with temperature sensor with an active channel area A = 0.29 mm² b) Microscopic view of the measured device layout 1.

temperature-dependent resistance (R_{SENSOR}) of the sensor is characterized on a hot plate, revealing a linear increase in resistance with temperature due to gold metallization. These sensor values contribute to characterizing in-chip temperature as a function of the dissipated power in the GaN HEMT. Additionally, they aid in determining the thermal resistance of the device using equation (4.1) where R_{TH} represents thermal resistance, T_J denotes junction temperature, T_C signifies backside temperature (chuck) and P represents the power dissipated in watts.

$$R_{TH} = \frac{T_J - T_C}{P} \text{ K/W} \tag{4.1}$$

Thermal resistance can also be determined using the equation (4.2)

$$R_{TH} = \frac{l}{k \cdot A} \text{ K/W} \tag{4.2}$$

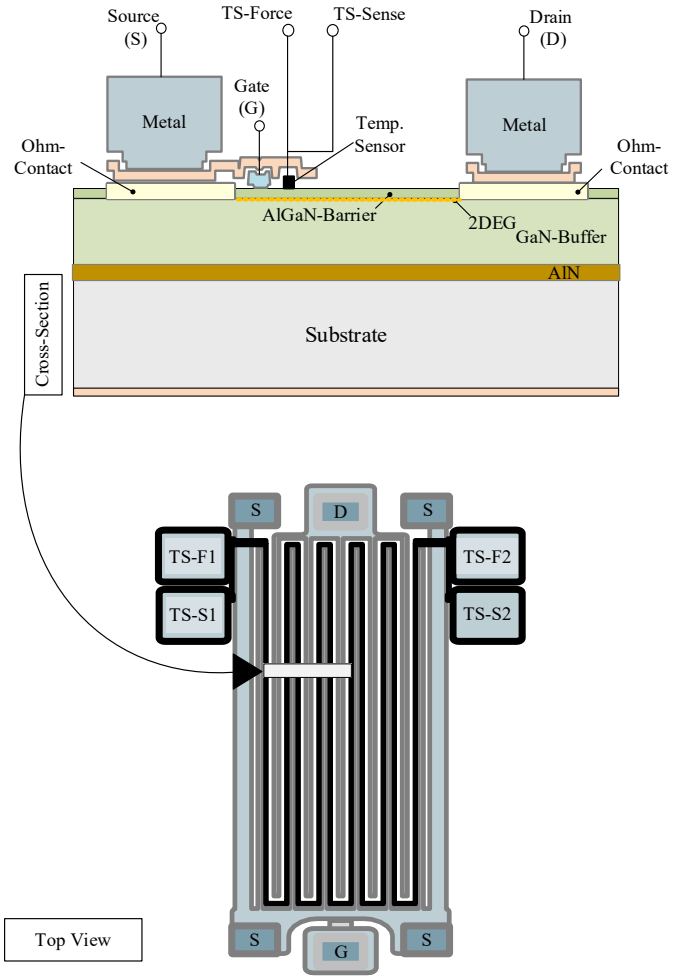


Figure 6 Cross-section and top view of a GaN HEMT with temperature sensor.

Here l represents the thickness of the material, k denotes the thermal conductivity, and A signifies the effective area.

The schematic layout of the device is depicted in figure 6 , illustrating both cross-sectional and top views. The 600 V HEMT structure features a typical gate length of L_G = 1°µm and a gate-drain and gate-source spacing ratio of L_{GD}/L_{GS} = 15/2°µm. The gate structure comprises 10 fingers, each with a gate width of 1 mm, totaling a gate width of W = 10 mm. The device

area measures $A = 0.29$ mm². Notably, from the top view, the metal meander is positioned in close proximity to the gate.

The subsequent section delves into the utilization of the device with Si and GaN substrates, focusing on the extraction of their respective thermal resistances.

4.1.1 GaN-on-Si

Given the widespread use of silicon, it becomes essential to accurately measure the thermal resistance in GaN-on-Si HEMT devices. This ensures that the thermal properties are not overestimated, providing precise values for enhanced device performance. This thesis addresses this need by investigating two distinct buffers grown via MOCVD: the AlN/GaN superlattice (SL) buffer and the step-graded AlGaN/GaN buffer [7]. The goal is to assess the influence of these buffers on thermal resistance values, with the aim of identifying the most suitable option for thermal applications. This inquiry is essential not only for enhancing our understanding of GaN-on-Si devices but also for optimizing their performance in practical applications.

4.1.1.1 Super Lattice Buffer

The AlN/GaN SL buffer is known for its exceptional vertical isolation and reduced substrate biasing effects. As depicted in figure 7, the GaN-on-Si HEMT configuration features an integrated sensor and the vertical layer stacks of the AlN/GaN superlattice buffer. The layer

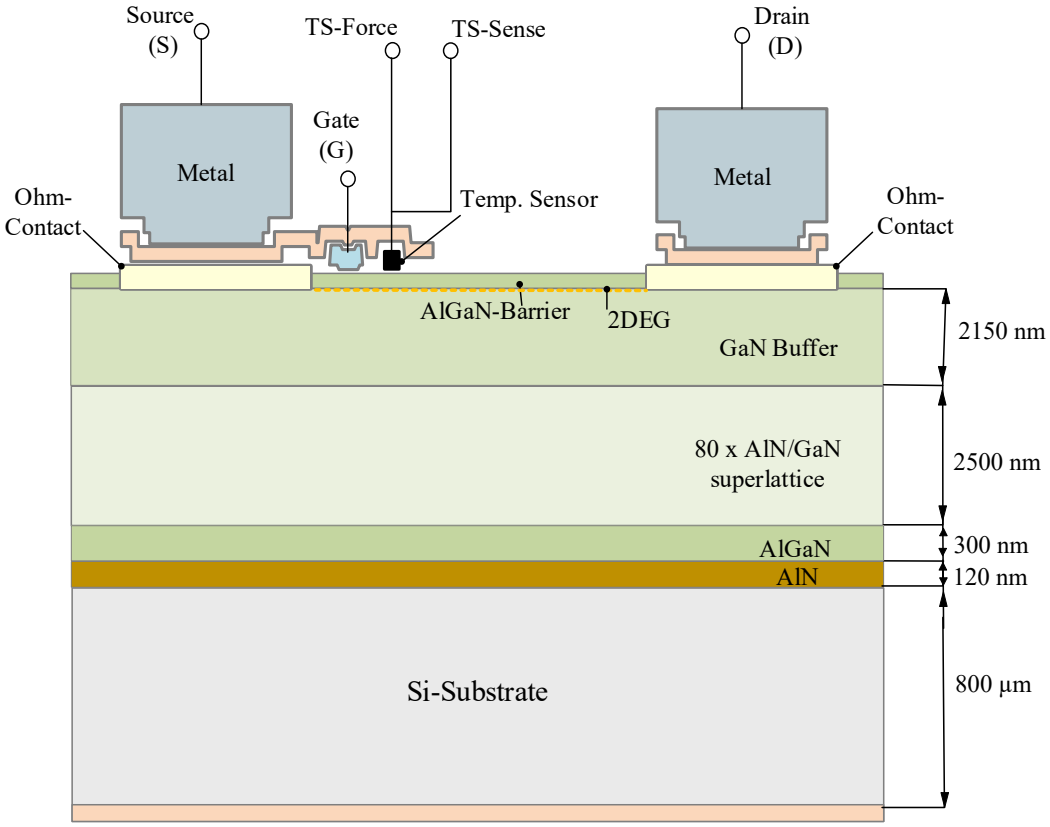


Figure 7 GaN-on-Si HEMT with an integrated sensor and AlN/GaN super lattice buffer.

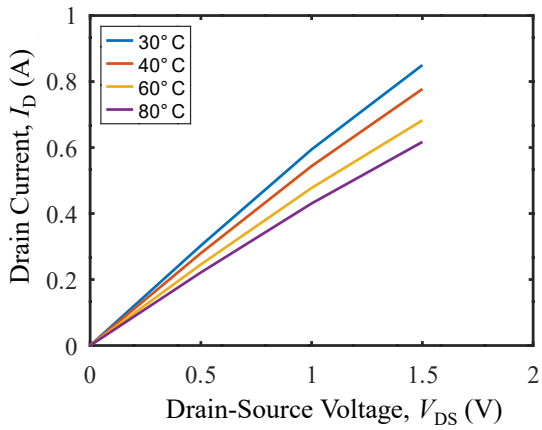


Figure 8 Drain current vs Drain-Source voltage for different chuck-temperatures of the GaN-on-Si HEMT with SL buffer at 0 V Gate-Source.

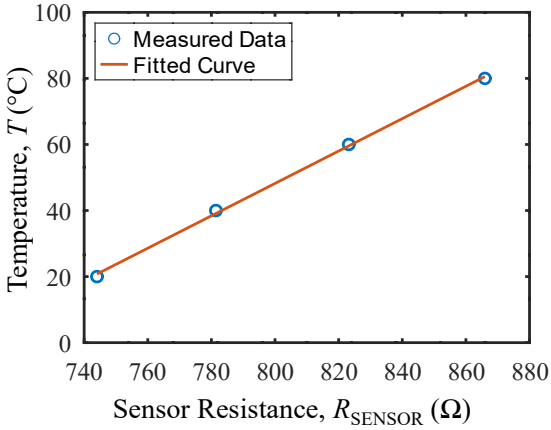


Figure 9 Sensor resistance characterized v/s in chip temperature for HEMT device with SL buffer.

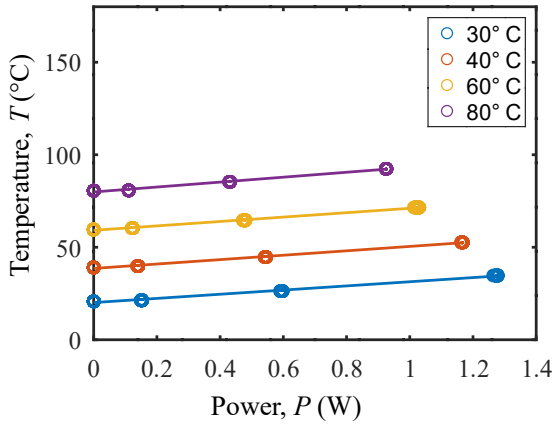


Figure 10 Power vs Temperature graph for SL, showing a common scale for easy comparison with other devices.

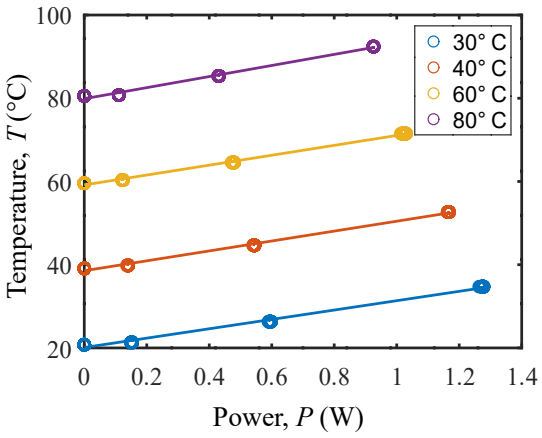


Figure 11 Power vs Temperature graph for SL displaying a different scale to accommodate more data points for detailed analysis.

thicknesses are as follows: the superlattice buffer is 2500 nm thick, with a GaN buffer thickness of 2150 nm. The AlN nucleation layer has a thickness of 120 nm, while the Si substrate measures 800 µm in thickness [4].

Measurements were conducted on the device, with the drain-source voltage (V_{DS}), swept from 0 to 2 V in 500 mV increments for chuck temperatures ranging from 20 °C to 80 °C in 20 °C increments. For HPSMU measurements, the current is limited to 1 A. With increasing temperature, there is a drop in drain current (I_D) due to self-heating of the device channel. An on-state resistance of R_{ON} = 2 Ω was determined for the device, resulting in a maximum power dissipation of around 2 W in the channel. Figure 8 illustrates the maximal drain currents as function of the drain source voltage of the HEMT for different chuck temperatures. Figure 9 shows the characteristics of the temperature sensor. The resistance R_{SENSOR} is increasing with the chuck temperature. Again, is assumed, that chuck temperature is equal to the in-chip

Table 14 Thermal resistance values of HEMT with SL buffer at different temperatures for a channel area, A = 0.29 mm².

Temperature	20°C	40°C	60°C	80°C
R_{TH} (K/W)	11.3	12.4	12.8	13.7
$R_{TH} \cdot A$ (K mm²/W)	3.3	3.6	3.7	4

temperature at the sensor, in case that there is now power dissipated in the HEMT. Sensor resistances were calculated from V_{SENSOR} and I_{SENSOR} values, revealing a linear relationship with temperature as shown in figure 9. Across temperatures ranging from 20 °C to 80 °C, sensor resistance values fell within the range of 740 Ω to 870 Ω.

Figure 10 depicts the channel temperature versus the power generated in the channel for different backside temperatures. It is assumed, that for minimum V_{DS} values the power P is very low, and the effect of self-heating can be neglected. Thus, the junction temperature can be assumed to be equivalent to the chuck temperature. As the power P in the HEMT is increased by increasing $V_{DS,}$ the junction temperature increases as well.

According to equation (4.1), the slope of the power versus temperature graph provides the thermal resistance values. Table 14 lists the R_{TH} values of the HEMT device with SL buffer for different chuck temperature values, ranging from 11.31 to 13.7 K/W and also the area specific R_{TH} in K mm²/W for a channel area, A = 0.29 mm².

4.1.1.2 Graded Buffer

Figure 12 illustrates the GaN-on-Si HEMT featuring an integrated sensor and the fabricated layer stacks of the step-graded AlGaN/GaN buffer. Measurements were conducted following the same procedure as for the superlattice buffer, and thermal resistance values were extracted accordingly. The graded AlGaN/GaN thickness is 730 nm, while the GaN buffer thickness measures 3290 nm. The nucleation layer has a thickness of 120 nm, and the Si substrate is 800 µm thick.

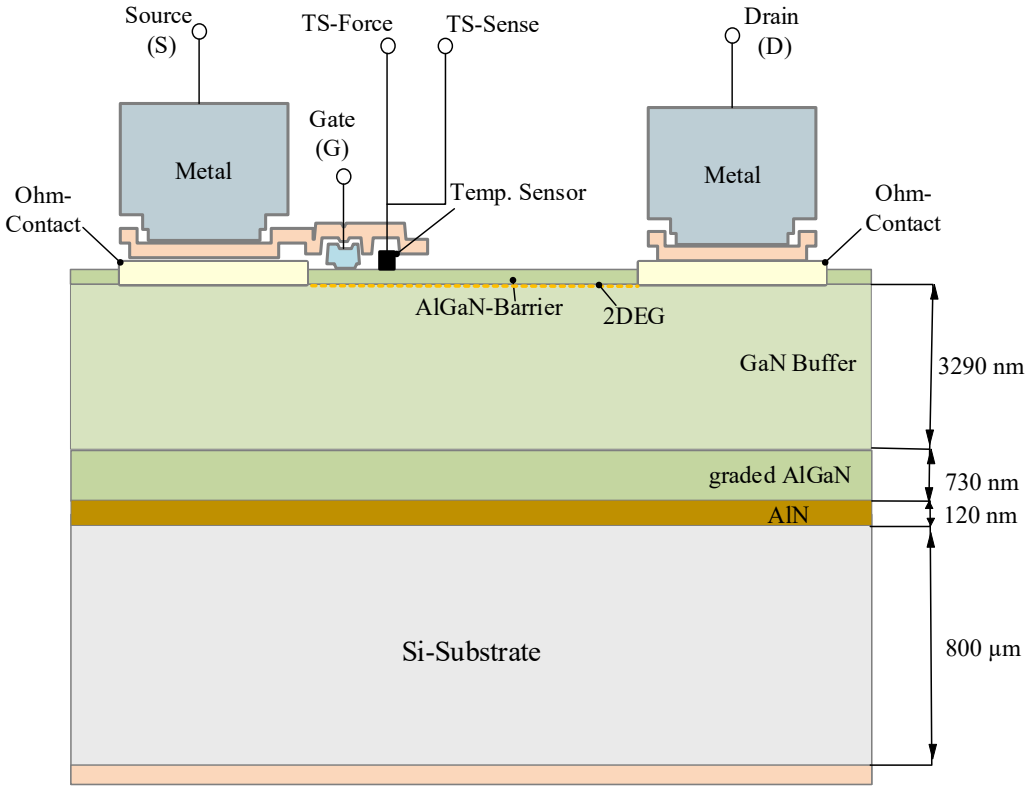


Figure 12 GaN-on-Si HEMT with an integrated sensor and step-graded AlGaN/GaN buffer.

Measurements were performed for chuck temperatures ranging from 30 °C to 80 °C, mirroring the procedure for the device with the SL buffer. The output characteristics and sensor resistance, characterized by temperature, are depicted in figure 13 and figure 14 respectively. The on-state resistance closely resembles that of the device with the SL buffer, and the sensor resistance falls within a similar range. Power was characterized against the channel temperature at different backside temperatures, as shown in figure 15 R_{TH} values were extracted from the slope of the graph. The calculated R_{TH} values are presented in table 15 for the HEMT device with the step-graded buffer.

Comparing the R_{TH} values for the HEMT devices characterized with the SL buffer and step-graded buffer, it is evident that they exhibit similar values. At first glance, there appears to be minimal effect of the buffer on the junction temperature of the device.

Characterizing GaN-on-Si with the SL and step-graded buffers was attempted to investigate the potential impact of using thin substrates with a thickness of 125 µm. However, due to the bow-shaped nature of the wafers and their inability to adhere properly to the chuck, reliable data from these devices could not be obtained.

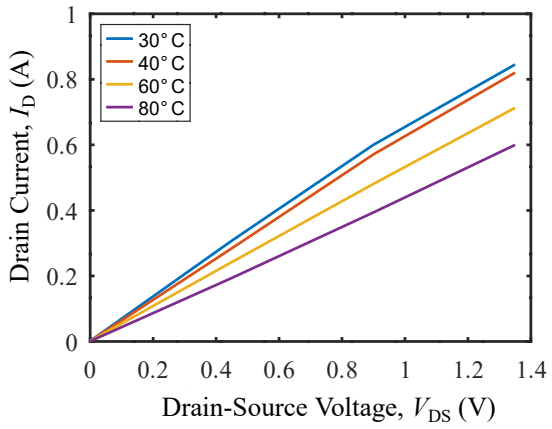


Figure 13 Drain current vs Drain-Source voltage for different chuck-temperatures of the GaN-on-Si HEMT with step-graded buffer at 0 V Gate-Source.

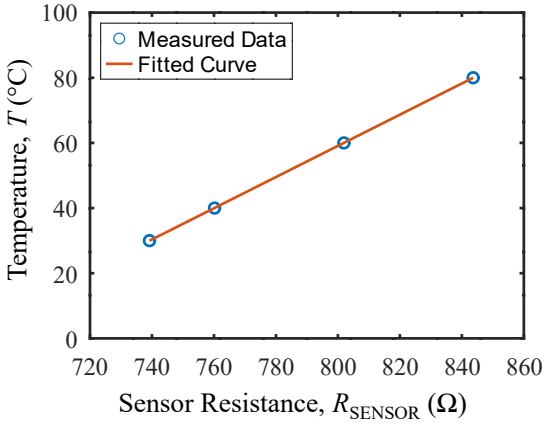


Figure 14 Sensor resistance characterized v/s in chip temperature for HEMT device with step-graded buffer.

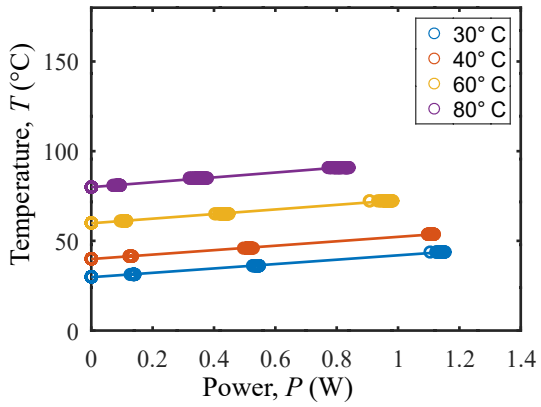


Figure 15 Power vs Temperature graph for step-graded, showing a common scale for easy comparison with other devices.

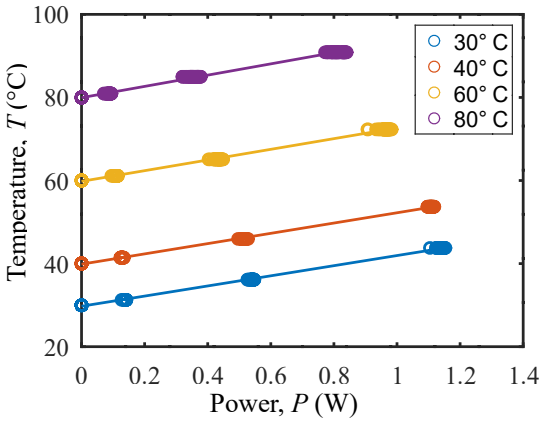


Figure 16 Power vs Temperature graph for step-graded displaying a different scale to accommodate more data points for detailed analysis.

Table 15 Thermal resistance values of HEMT with step-graded buffer at different temperatures for a channel area, A = 0.29 mm².

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	11.7	12.1	12.9	13.5
$R_{TH} \cdot A$ (K mm²/W)	3.4	3.5	3.75	3.9

4.1.2 GaN-on-GaN

A GaN-on-GaN HEMT equipped with an integrated temperature sensor was characterized for thermal resistance extraction. Figure 17 illustrates the layer stacks of the device with GaN as the substrate, featuring a thickness of 500 µm. The GaN buffer thickness measures only 900 nm.

The on-state resistance of the device is notably lower than that of the GaN-on-Si device, with a value of R_{ON} = 1.4 Ω. Given the current limit of 1 A for the setup, the drain-source voltage (V_{DS}), was swept from 0 to 1.6 V in 400 mV increments for chuck temperatures of 30 °C, 40 °C, 60 °C, and 80 °C. Figure 18 displays the output characteristics of the device. Since the device structure is identical, the temperature sensor resistance also falls within the same range, approximately 750 to 870 Ω, as illustrated in figure 19.

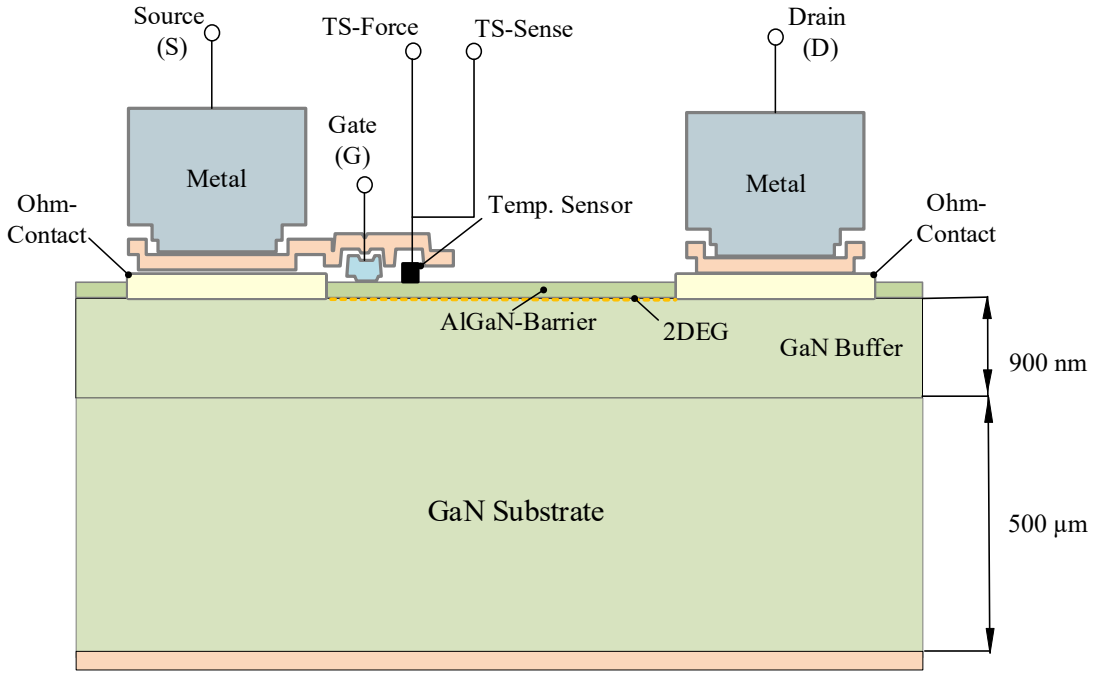


Figure 17 GaN-on-GaN lateral HEMT with an integrated sensor.

The maximum power generated in the channel ranges up to 1.6 W for different chuck temperatures, as depicted in figure 21. The R_{TH} calculated was then calculated from the slope of the graph. The calculated R_{TH} values for the GaN-on-GaN HEMT device are presented in table 16 below.

Notably, the calculated R_{TH} values for the GaN-on-GaN HEMT device are approximately half that of the GaN-on-Si device, indicating superior thermal performance. Moreover, the deviation in the values as temperature increases is less pronounced compared to the Si device.

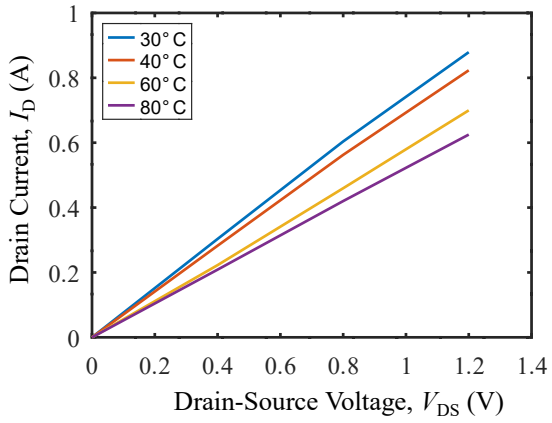


Figure 18 Drain current vs Drain-Source voltage for different chuck-temperatures of the GaN-on-GaN HEMT at 0 V Gate-Source.

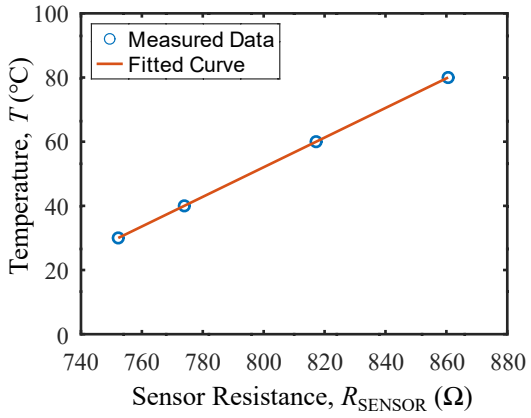


Figure 19 Sensor resistance characterized v/s in chip temperature for GaN-on-GaN HEMT.

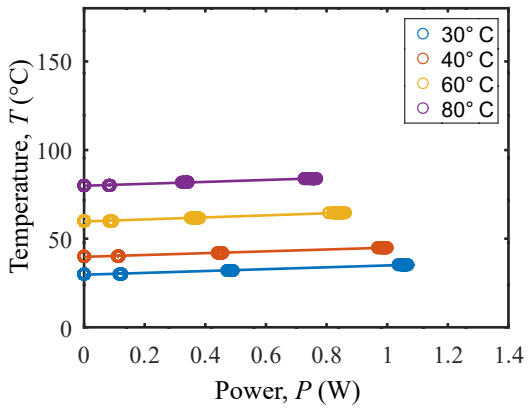


Figure 20 Power vs Temperature graph for GaN-on-GaN HEMT, showing a common scale for easy comparison with other devices.

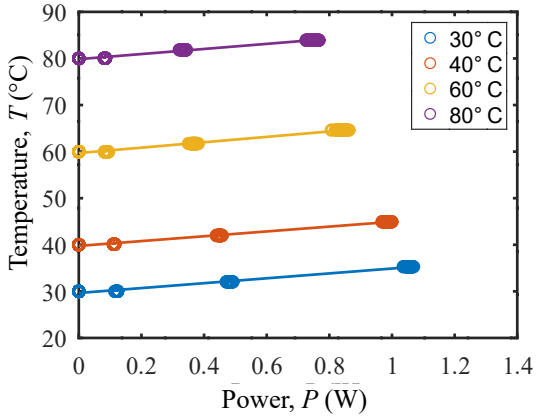


Figure 21 Power vs Temperature graph for GaN-on-GaN HEMT displaying a different scale to accommodate more data points for detailed analysis.

Table 16 Thermal resistance values of GaN-on-GaN HEMT for different chuck temperatures for a channel area, A = 0.29 mm².

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	5.2	5.5	5.8	6.5
$R_{TH} \cdot A$ (K mm²/W)	1.5	1.6	1.7	1.9

Alternative Power Switch Device with Integrated Temperature Sensor

Incorporating an additional power device equipped with an integrated temperature sensor allowed for the thermal characterization of GaN-on-SiC. This method was chosen due to the absence of the layout 1 device structure depicted in Figure 6 for this specific substrate. Given the well-established thermal properties of SiC, conducting comprehensive characterization of GaN-on-SiC devices becomes necessary. Figure 22 presents the cross-section and top view of this device, a 4×4 mm² chip with a cumulative gate width (W_G) of 337 mm across 14 separate comb cells, each with a gate width of 24 mm [8]. Each individual device occupies an area of

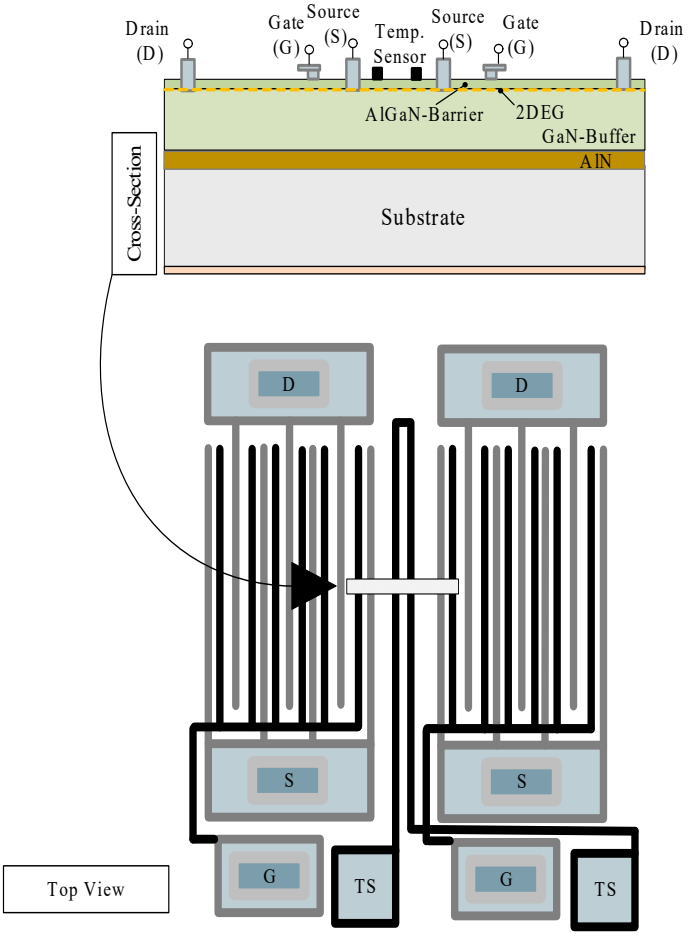
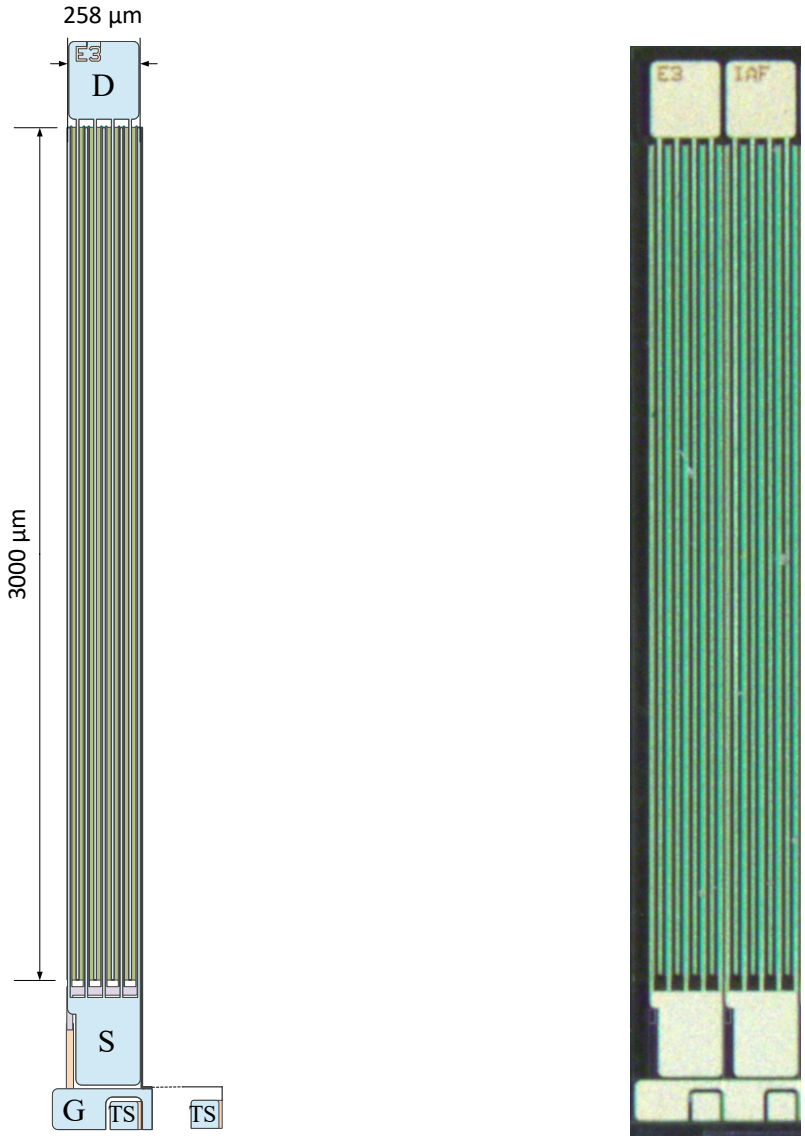


Figure 22 Cross-section and top view of a GaN-on-Si HEMT with temperature sensor.

0.78 mm². Positioned between the two passivation layers within the gap among the HEMT cells, the temperature sensor comprises loops that can be accessed individually at each cell or end-to-end to capture the total chip temperature. Temperature is accurately measured as voltage at the sensor pads by applying sense currents through the sensor turns.



a) **b)**

Figure 23 a) Layout 2 of GaN power switch HEMT with temperature sensor with an active channel area A = 0.78 mm². b) Microscopic view of the measured device layout 2.

The power device is initially characterized on GaN-on-Si to establish a basis for comparison with layout 1. This comparison aims to assess the reliability of the results obtained for GaN-on-SiC. According to equation (4.2), R_{TH} is inversely proportional to area of the device. Therefore, a relation for an area specific resistance in K mm^2/W can be calculated as follows:

$$R_{TH,Layout2} \cdot A_{Layout2} \approx R_{TH,Layout1} \cdot A_{Layout1}\ (\mathrm{K} \cdot mm^2/\mathrm{W}) \quad \text{‘on the same wafer’} \tag{4.3}$$

where $A_{Layout1}$ and $R_{TH,Layout1}$ represent the respective area and thermal resistance values of the GaN-on-Si device for layout 1 in figure 6 and $A_{Layout2}$ and $R_{TH,Layout2}$ represent the respective area and thermal resistance values of the GaN-on-Si device for layout 2 in figure 23. The power

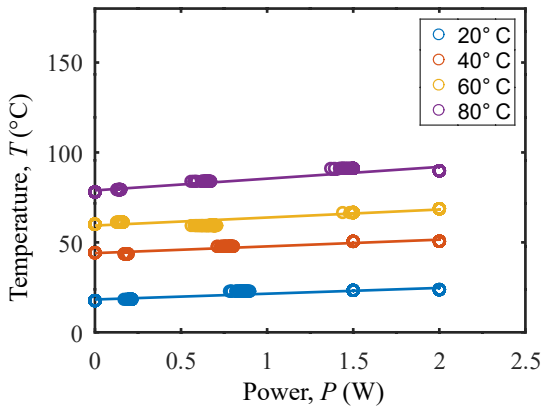


Figure 24 Power vs Temperature graph for GaN-on-Si HEMT for Layout 2 device, showing a common scale for easy comparison with other devices.

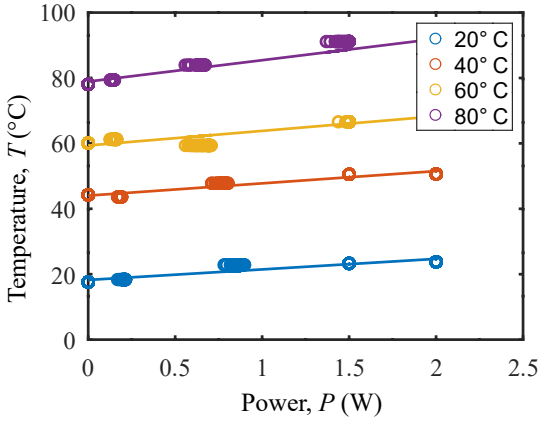


Figure 25 Power vs Temperature graph for GaN-on-Si HEMT for Layout 2 device, displaying a different scale to accommodate more data points for detailed analysis.

device is characterized on GaN-on-Si against the channel temperature at different backside temperatures, as illustrated in figure 24, and the R_{TH} values are then extracted from the slope of the graph.

The thermal resistance values thus calculated for different temperatures are presented in table 17 below and also the area specific R_{TH} in K mm^2/W for a channel area, A = 0.78 mm^2.

Table 17 Thermal resistance values of GaN-on-Si HEMT for different chuck temperatures for a channel area, A = 0.78 mm².

Temperature	20°C	40°C	60°C	80°C
R_{TH} **(K/W)**	3.2	3.7	4.5	6.5
$R_{TH} \cdot A$ **(K mm²/W)**	2.5	2.9	3.5	5.1

It is worth noting that the area specific resistance values for both layout 1 and layout 2 yields a similar result. Any small deviation observed could be attributed to the temperature sensor winding being situated just outside the channel for layout 2 and not as closely integrated into the structure as depicted in figure 6 for layout 1.

4.1.3 GaN-on-SiC

Now that a relationship has been established between the GaN-on-Si devices with the two structures, we can proceed to characterize GaN-on-SiC with the alternative structure with layout 2.The power device is fabricated using high-voltage AlGaN/GaN-on-SiC technology, as illustrated in figure 22, with the layer stacks depicted in figure 26.

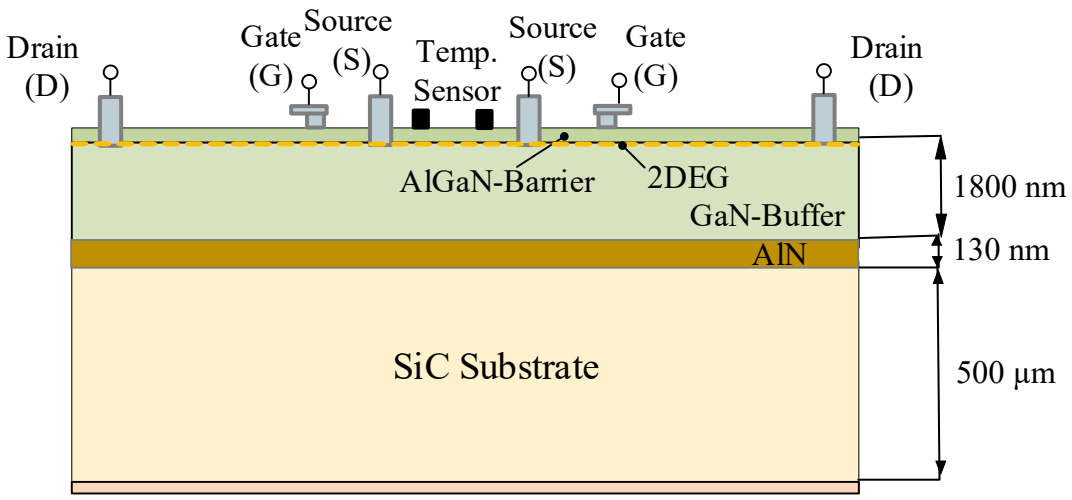


Figure 26 Cross-section and top view of a GaN-on-SiC HEMT with temperature sensor.

The resistance of the sensor, which is temperature-dependent, is characterized for chuck temperatures ranging from 20 °C to 80 °C in 20 °C steps, as shown in figure 28. The sensor resistance increases from 235 Ω at 20 °C to 275 Ω at 80 °C, demonstrating a linear relationship.

Characterizing the in-chip temperature as a function of the dissipated GaN-HEMT power, as plotted in figure 29, enables the determination of the junction temperature, which, in turn, provides the thermal resistance values. The thermal resistance values calculated for GaN-on-SiC at different chuck temperatures are presented in table 18 and also the area specific R_{TH} in K mm^2/W for a channel area, A = 0.78 mm².

Figure 30 illustrates that the plots are nearly parallel to the x-axis, indicating minimal rise in junction temperature with an increase in channel power.

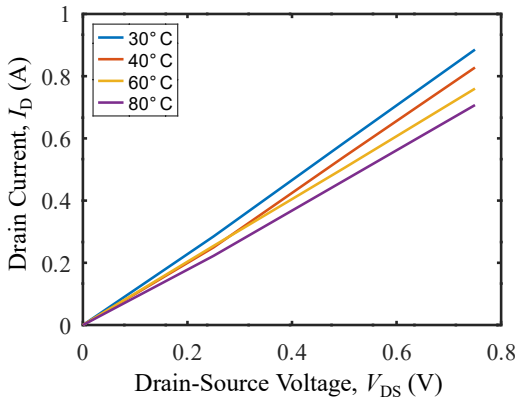


Figure 27 Drain current vs. Drain-Source voltage for different chuck-temperatures of the GaN-on-SiC HEMT for layout 2 device at 0 V Gate-Source.

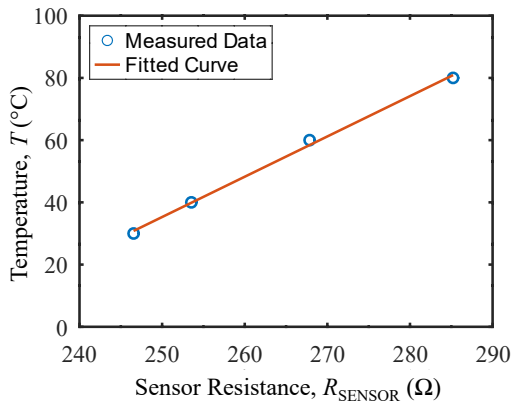


Figure 28 Sensor resistance characterized v/s in chip temperature for GaN-on-SiC HEMT for layout 2 device.

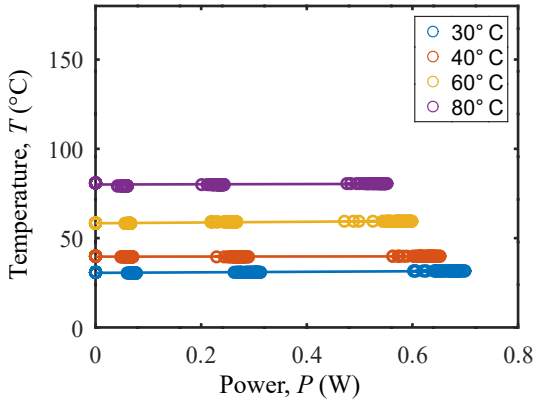


Figure 29 Power vs Temperature graph for GaN-on-SiC HEMT for layout 2 device, showing a common scale for easy comparison with other devices.

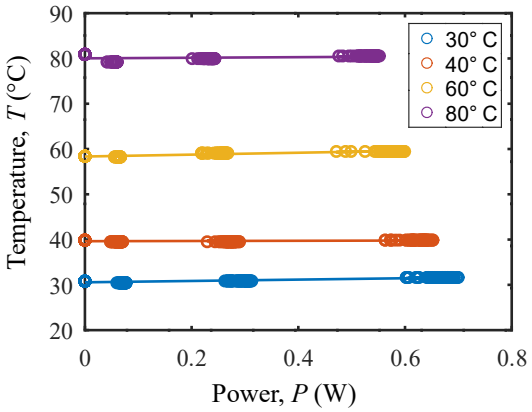


Figure 30 Power vs Temperature graph for GaN-on-SiC HEMT for layout 2 device displaying a different scale to accommodate more data points for detailed analysis.

Table 18 Thermal resistance values of GaN-on-SiC HEMT for different chuck temperatures for a channel area, A = 0.78 mm².

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	0.6	0.7	0.8	0.86
$R_{TH} \cdot A$ (K mm²/W)	0.5	0.55	0.6	0.7

4.2 Summary & Discussion

The chapter aimed to analyze the thermal resistance values of various devices under consideration and provided area-specific thermal resistance, as summarized in the table below. Utilizing an integrated temperature sensor on the device, measurements of junction temperature were conducted at different backside temperatures, with specific voltage settings for drain-source and temperature sensor while keeping the gate source voltage zero. The results indicate that the GaN-on-SiC device exhibits the lowest thermal resistance, followed by GaN-on-GaN and GaN-on-Si devices which display higher values. The investigation sought to discern the impact of different substrate materials on the device's junction temperature, with the intention of optimizing design parameters. There wasn't a significant observable difference in GaN-on-Si devices when employing different buffers (SL and step-graded). This could possibly be attributed to the substantial thickness of the Si substrate. However, when attempting to use a thinner Si substrate, the bow-shaped wafers failed to adhere to the chuck properly, resulting in unreliable results. For GaN-on-SiC, measurements had to be made on an alternative structure while the other structure was not readily available and therefore calculation was made for the other structure to have an understandable comparison. GaN-on-Sapphire devices were not fully

processed and therefore measurements couldn't be made. In conclusion, this analysis has produced promising results that are expected to guide future endeavors in device design and optimization. The devices that couldn't be measured will be further analyzed in the next chapter on thermal simulation.

Table 19 Measured and Calculated thermal resistance values of different structures.

Structure	Area Specific R_{TH} (K mm²/W)					Remark	
	20°C	30°C	40°C	60°C	80°C		
GaN-on-Si (SL)	3.3		3.6	3.7	4	Measured	Layout 1 (A = 0.29 mm²)
GaN-on-Si (Graded)		3.4	3.5	3.75	3.9	Measured	
GaN-on-GaN		1.5	1.6	1.7	1.9	Measured	
GaN-on-Si	2.5		2.9	3.5	5.1	Measured	Layout 2 (A = 0.78 mm²)
GaN-on-SiC		0.5	0.55	0.6	0.7	Measured	

5. Thermal Simulation of GaN Power Switch HEMTs

In this chapter, the thermal simulation of GaN power HEMT devices is explored to better understand their thermal properties and analyze devices that couldn't be characterized experimentally.

Utilizing CST Studio Suite software, a precise model of the target device was modelled. The process involved importing the GDS file containing the device structure into CST Studio Suite as shown in figure 31, followed by generating a corresponding TEC file to represent different elevations and thicknesses of individual layers, as discussed in the previous chapter. This model specifically integrates the metallization, ohmic layers, AlGaN/GaN heterojunction, buffer layers, and substrates, while excluding other passivation layers. This exclusion is based on the assumption that passivation layers have a negligible impact on the device's junction temperature due to their thinness and very low thermal resistances. Each layer was assigned its respective material properties sourced from the material library. Background properties for the materials were established, and thermal boundary conditions were uniformly set to adiabatic in all directions.

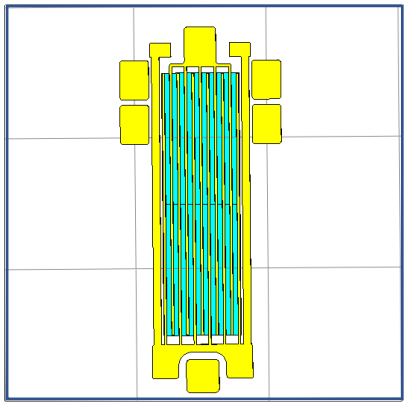


Figure 31 GaN power switch HEMT device structure used for simulation (Layout 1).

Drawing from the comprehensive literature review conducted in Chapter 3.1 on thermal properties, values that best fit the model were selected. Bulk thermal conductivities were allocated for the substrate materials, accounting for the reduction in conductivity in the thin film.

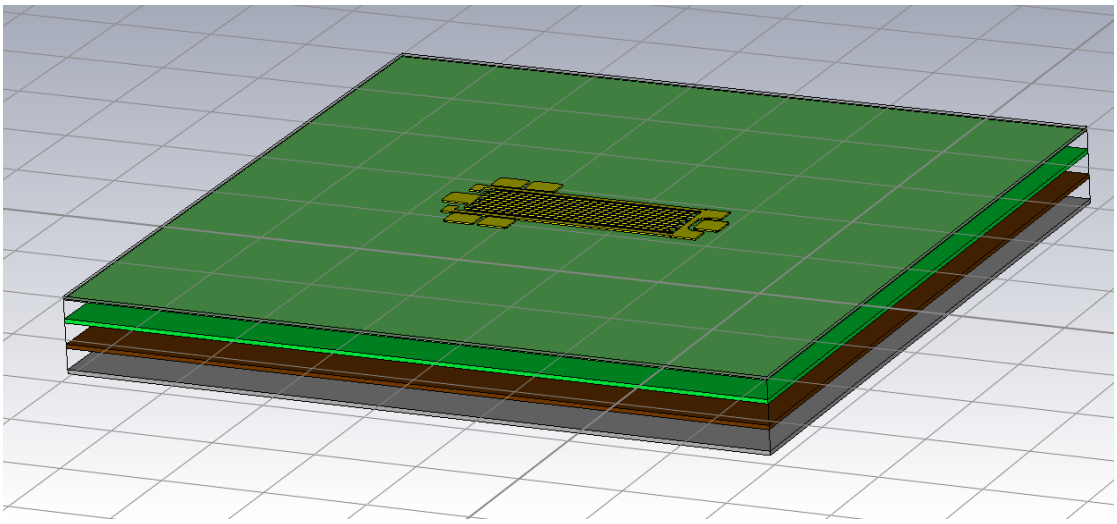


Figure 32 Schematic representation of the layer stacking for thermal simulation. Each layer corresponds to a specific material and thickness, forming the device structure used for thermal analysis in the simulation process.

The layer stacks are visually represented in figure 32. For power switching DC HEMTs, the focus was on the linear region of operation. Unlike RF devices, where the drain side of the gate is considered the heat source, here a uniform distribution of heat was assumed. The peak near the gate is negligible compared to RF devices for a voltage range up to 2 V, so the 2DEG was considered the primary heat source. Therefore, a volume heat with a power of 1 W was applied to the channel. Backside temperatures were set at values of 20, 40, 60, and 80 °C, following which the simulation was executed.

5.1 GaN-on-Si

In this section, thermal simulations were performed for GaN-on-Si devices utilizing both a superlattice (SL) buffer and a step-graded buffer. The aim was to compare the thermal resistance values obtained from simulation with those acquired from characterization and to deduce the thermal conductivity values of each layer accordingly. Below, the simulated model of GaN-on-Si with an SL buffer is illustrated in figure 33.

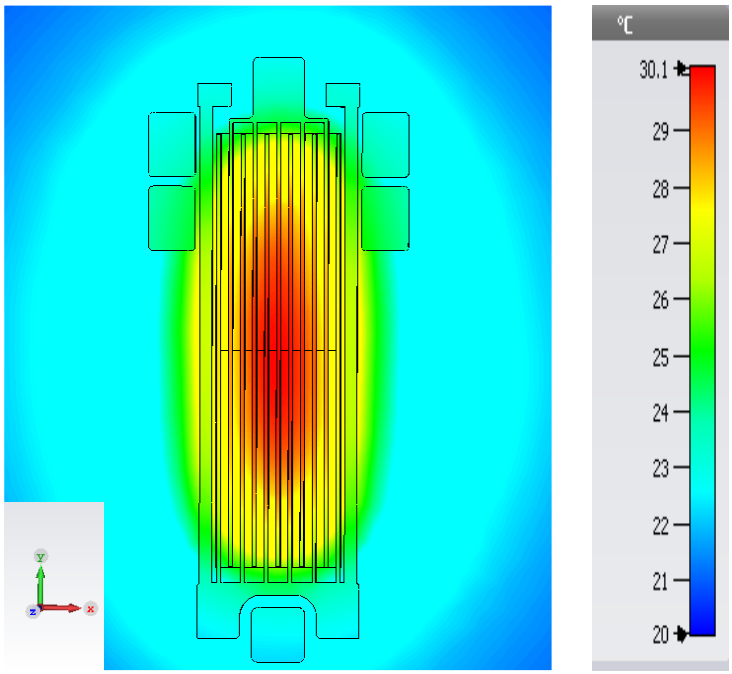


Figure 33 Top view of the simulated model structure for GaN-on-Si with a superlattice (SL) buffer, corresponding to a backside temperature of 20 °C, illustrating the distribution of heat at the junction.

5.1.1 Superlattice buffer

The simulated device structure comprises of an 800 µm Si substrate, succeeded by a 120 nm AlN nucleation layer, a 300 nm AlGaN layer, a 2500 nm AlN/GaN superlattice (SL) buffer, a 2150 nm GaN buffer layer, a 25 nm AlGaN barrier (with 29 % Al content), a 25 nm ohmic layer,

Table 20 Thermal conductivity values utilized for the SL structure in thermal simulation.

Material	***k* (@ 300 K) (W/mK)**
GaN	$127 \cdot (300/T)^{1.4}$
SL	10
AlGaN	25
AlN	$25 \cdot (300/T)^{0.9}$
Si	$80 \cdot (T/300)^{-1.65}$
Contacts	314

and finally, a 7 µm metallization layer. The thermal conductivity values utilized for each layer are provided in the table 20 below.

Simulating the device, the channel temperature and thermal resistance were extracted using equation (4.1).

Figure 34 illustrates the device's cross-section, with emphasis on the region exhibiting the highest heat concentration, allowing visualization of heat dispersion across the layers. The temperature distribution through the layer thicknesses is further plotted in figure 35, providing

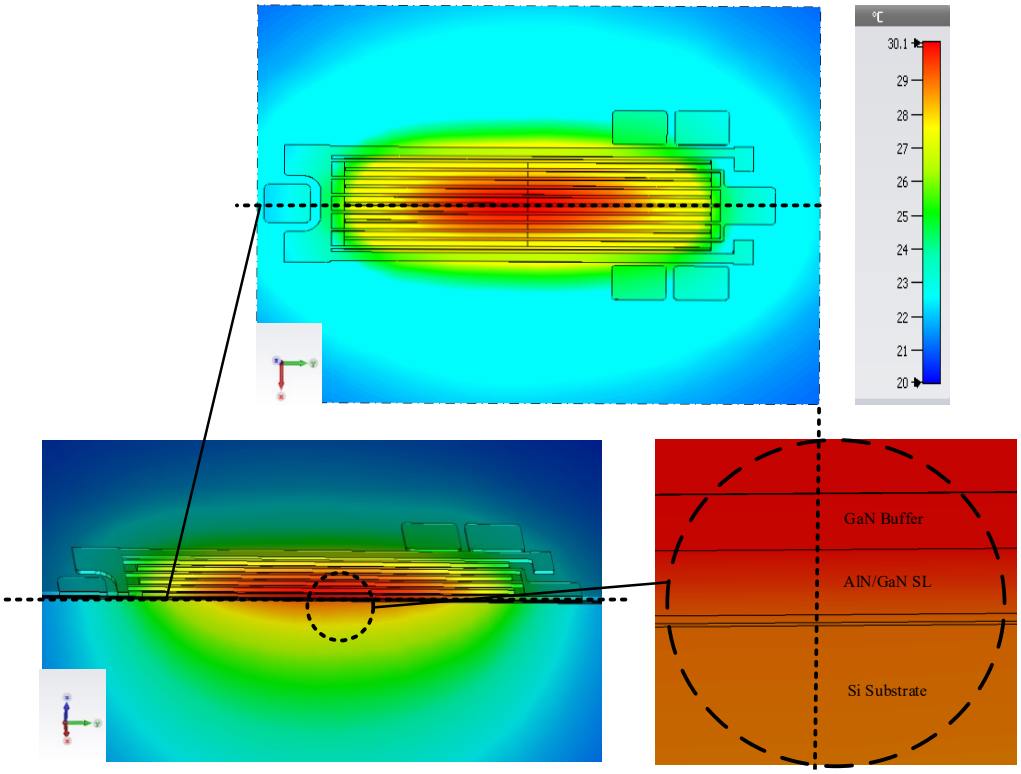


Figure 34 Visualization of the simulated GaN-on-Si device structure, comprising three panels. Panel 1 displays a top view of the device, while Panel 2 presents a cross-section through the middle, providing a detailed insight into the internal composition. Panel 3 zooms in on a specific area exhibiting maximum temperature, elucidating the localized thermal behaviour. Additionally, Panel 3 illustrates the distribution of heat across the various device layers, offering a comprehensive understanding of thermal dissipation within the structure.

insights into temperature variations at each layer and their corresponding thermal resistances. Particularly, in cases of thick substrates with suboptimal thermal properties, heat primarily dissipates along the substrate, with minimal influence from the buffer on junction temperature. Notably, the SL buffer exhibits higher heat levels compared to other buffer layers, potentially attributed to its thickness and relatively lower thermal conductivity.

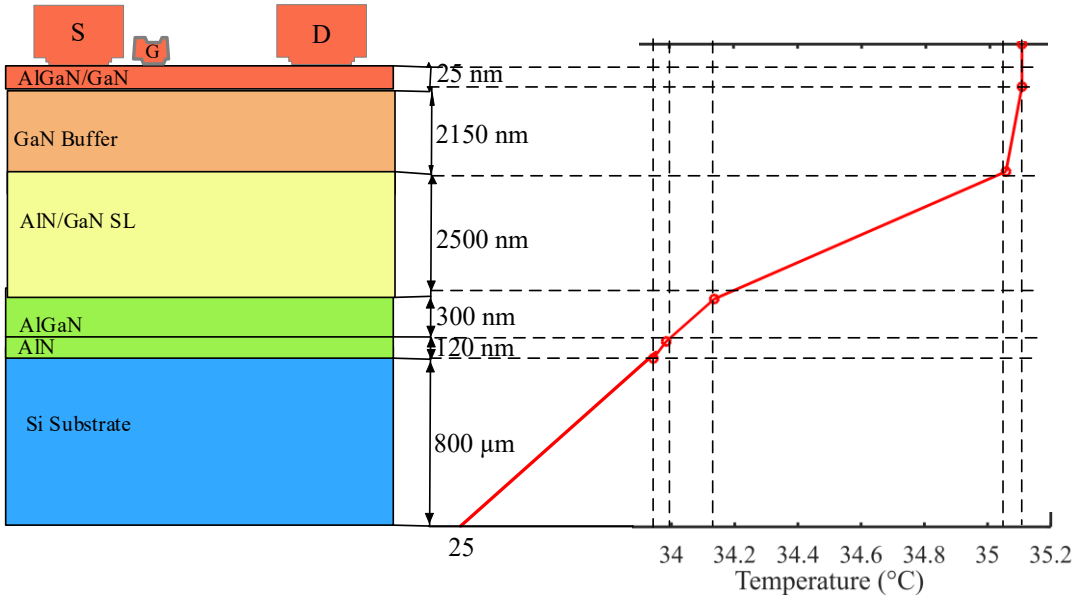


Figure 35 Cross-sectional representation of the GaN-on-Si device structure with SL buffer, highlighting the individual layers and their respective thicknesses. Additionally, the accompanying graph illustrates the temperature distribution along the thicknesses of the device, with temperature plotted on the x-axis.

The calculated thermal resistance values, derived from the obtained junction temperature, and also the area specific R_{TH} in K mm²/W for a channel area, A = 0.29 mm², are presented in the table 21 below. Comparison between the measured and simulated thermal resistance values for the device with an SL buffer is depicted in figure 36, revealing close alignment between measurement and simulation results.

Subsequently, by maintaining all other layer thicknesses constant and reducing the substrate thickness to 125 µm, simulations were conducted to examine and enhance the comprehension of temperature distribution across the layers.

Table 21 Calculated thermal resistance values obtained from simulated junction temperatures for GaN-on-Si devices with a superlattice (SL) buffer, considering various backside temperatures and for a channel area, A = 0.29 mm² (Layout 1).

Temperature	20°C	40°C	60°C	80°C
R_{TH} **(K/W)**	10.1	11.1	12.1	13.3
$R_{TH} \cdot A$ **(K mm²/W)**	2.9	3.2	3.5	3.9

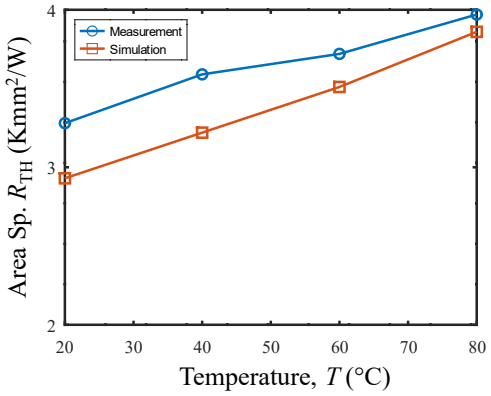


Figure 36 Comparison plot illustrating the thermal resistance values obtained from both measured data and simulation for GaN-on-Si devices with SL buffer for an active channel area, A = 0.29 mm²

Thermal resistance calculations are provided in the table 22 below. The heat distribution pattern is illustrated in the accompanying figure 37.

Table 22 Thermal resistance values calculated from simulated junction temperatures for GaN-on-Si devices with SL buffer, utilizing a thinner substrate and for a channel area, A = 0.29 mm².

Temperature	20°C	40°C	60°C	80°C
R_{TH} **(K/W)**	5.1	5.6	6	6.5
$R_{TH} \cdot A$ **(K mm²/W)**	1.5	1.6	1.7	1.9

At a backside temperature of 25 °C, the maximum junction temperature reached 30.3 °C. Despite the Si substrate absorbing most of the heat up to 29.2 °C, the SL buffer exhibited temperature ranges between 29.27 °C and 30.18 °C, indicating minimal influence on the junction temperature relative to the substrate.

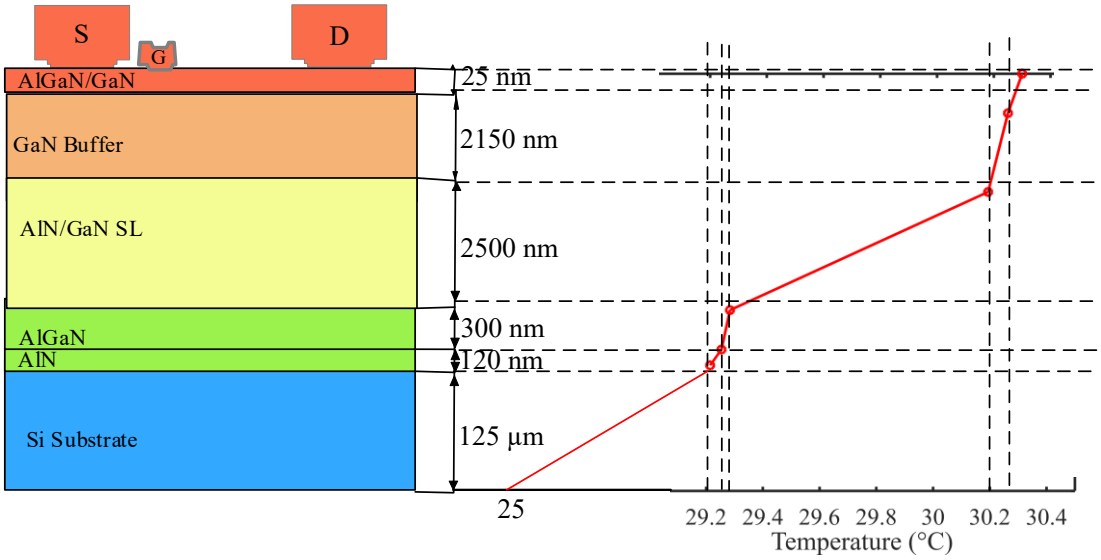


Figure 37 Cross-sectional view of the GaN-on-Si device structure with an SL buffer and a thinner substrate, illustrating the individual layers and their respective thicknesses. The accompanying graph depicts the temperature distribution along the layer thicknesses, with temperature values represented on the x-axis.

5.1.2 Graded Buffer

In the configuration with a graded buffer, the ohmic layers maintain a thickness of 25 nm, while the metallization layer measures 7 µm thick. Positioned between the graded buffer and the AlGaN/GaN heterojunction, the GaN buffer layer has a thickness of 3290 nm, while the graded buffer itself spans 730 nm. Following the graded buffer, there is a nucleation layer, succeeded by the substrate with a thin layer measuring 120 nm. Notably, the Si substrate for this particular

Table 23 Thermal conductivity values utilized for the step-graded structure in thermal simulation.

Material	***k* (@ 300 K) (W/mK)**
GaN film	$127 \cdot (300/T)^{1.4}$
Step-graded	14
AlN	$25 \cdot (300/T)^{0.9}$
Si	$80 \cdot (T/300)^{-1.65}$
Contacts	315

Table 24 Thermal resistance values calculated from simulated junction temperatures for GaN-on-Si devices with step-graded buffer and for a channel area, A = 0.29 mm².

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	10.2	10.8	11.8	13.1
$R_{TH} \cdot A$ (K mm²/W)	3	3.1	3.4	3.8

device is substantially thicker, measuring 800 µm, in stark contrast to the other layers. The thermal conductivity values used for the structure are detailed in table 23.

Similarly, to the SL device, here the cross-section follows a similar pattern as depicted in Figure 34 to observe the heat distribution, subsequently plotted below in figure 38. As illustrated in the figure, for a junction temperature of 30 °C, the Si substrate itself reaches 29.6 °C, indicating that the buffer has minimal impact compared to SL.

The calculated thermal resistance from the simulation and also the area specific R_{TH} in K mm²/W for a channel area, A = 0.29 mm² is provided in table 24 below.

Comparing the measured and simulated thermal resistance values for the device with the graded buffer reveals similar trends to those observed with the SL buffer. To further explore this, the substrate thickness for the graded buffer is reduced to 125 µm and then simulated to observe the temperature distribution through the layers.

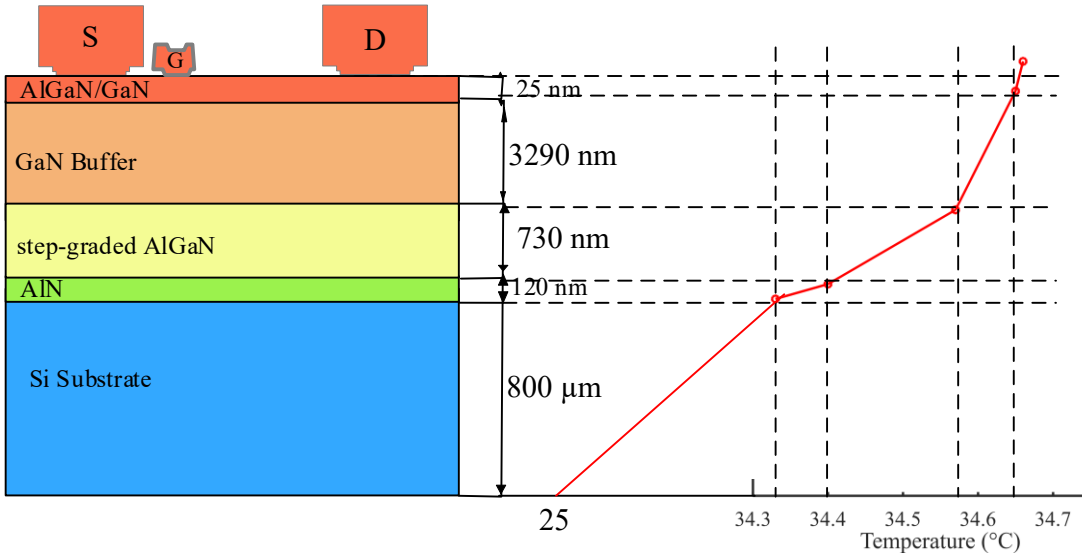


Figure 38 Cross-section of the GaN-on-Si device structure with step-graded buffer, depicting layer thicknesses. The accompanying graph shows temperature distribution along the layers.

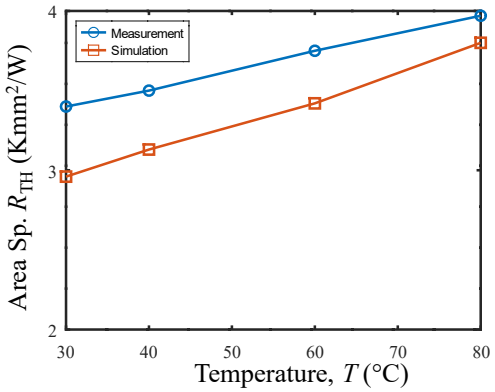


Figure 39 Comparison plot illustrating the area specific thermal resistance values obtained from both measured data and simulation for GaN-on-Si device for an active area, A = 0.29 mm² with step-graded buffer.

The resulting thermal resistance values for different backside temperatures, along with their respective area specific thermal resistance values, are presented in table 25 below.

Table 25 Thermal resistance values calculated from simulated junction temperatures for GaN-on-Si devices with step-graded buffer, utilizing a thinner substrate.

Temperature	30°C	40°C	60°C	80°C
R_{TH} **(K/W)**	4.9	5.4	5.7	6.35
$R_{TH} \cdot A$ **(K mm²/W)**	1.4	1.6	1.7	1.8

The temperature distribution through the layers is depicted as well in figure 40. From the plot, it is evident that the graded buffer has even less of an impact on the junction temperature of the device compared to the SL buffer. This observation may be attributed to the fact that, while SL and graded AlGaN have comparable thermal conductivity values, the lesser thickness of the graded buffer results in lower thermal resistance.

In conclusion, for GaN-on-Si, the substantial thickness and poor thermal conductivity of the Si substrate contribute significantly to the overall thermal resistance of the device. The results indicate that neither the SL nor the graded buffer layers exert a substantial influence on the junction temperature. However, the graded buffer, being thinner, overall yields lower thermal resistance for the device.

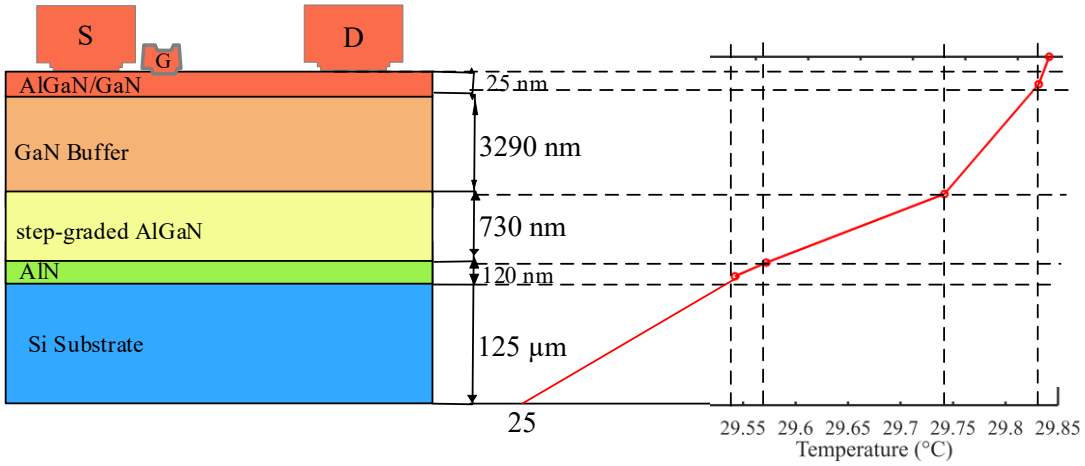


Figure 40 Cross-section of the GaN-on-Si device structure with step-graded buffer and thinner substrate, depicting layer thicknesses. The accompanying graph shows temperature distribution along the layers.

5.2 GaN-on-GaN

GaN-on-GaN devices were previously characterized in the previous chapter, and a model is now created and simulated to compare the results and ascertain reliable thermal conductivity values.

Table 26 Thermal conductivity values utilized for the GaN-on-GaN structure in thermal simulation

Material	***k* (@ 300 K) (W/mK)**
GaN film	$127 \cdot (300/T)^{1.4}$
GaN substrate	$130 \cdot (300/T)^{1.4}$
Contacts	315

The layer structures and thicknesses align with those provided in figure 17, with the ohmic layers measuring 25 nm in thickness and the metallization layer 7 µm thick. The GaN buffer utilized is 900 nm thick, while the GaN substrate measures 500 µm in thickness. Given the GaN-on-GaN configuration, it is assumed that the AlN nucleation layer could be disregarded. The thermal conductivity values used for the structure are detailed in table 26. Additionally, the thermal conductivity value of the GaN substrate was provided by the supplier.

Junction temperature values for different backside temperatures were then simulated, and the resulting thermal resistance values are presented in table 27 below.

Table 27 Thermal resistance values calculated from simulated junction temperatures for GaN-on-GaN device for a channel area, A = 0.29 mm² (Layout 1).

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	5.6	5.8	6.4	6.9
$R_{TH} \cdot A$ (K mm²/W)	1.6	1.7	1.85	2

The thermal resistance values obtained from measurement and simulation for the device are plotted in figure 41, revealing a close alignment between the two sets of data. This consistency lends credibility to the simulation model, suggesting its reliability for further analysis and application.

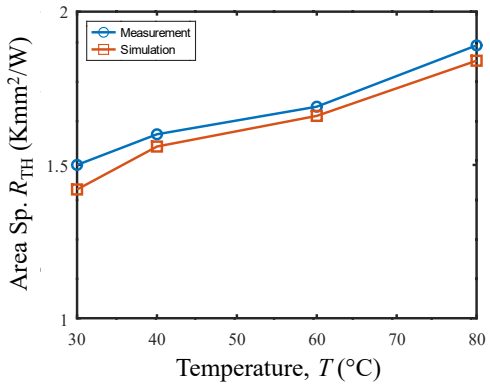


Figure 41 Comparison plot illustrating the area specific thermal resistance values obtained from both measured data and simulation for GaN-on-GaN device.

Utilizing this simulation model, we can examine the impact of a thin GaN substrate on the junction temperature. Given that the devices with thin substrates have a thickness of 125 µm, this parameter is incorporated into the model and simulated accordingly. The resultant values for various chuck temperatures with the thin GaN substrate are detailed in table 28 below.

Table 28 Thermal resistance values calculated from simulated junction temperatures for GaN-on-GaN device, utilizing a thinner substrate for a channel area, A = 0.29 mm² (Layout 1).

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	3.1	3.2	3.5	3.8
$R_{TH} \cdot A$ (K mm²/W)	0.88	0.92	1	1.1

A reduction in GaN substrate thickness correlates with lower thermal resistance values, resulting in lower temperatures at the junction of the device.

5.3 GaN-on-SiC

In the previous chapter, the layer definition for GaN-on-SiC was outlined, featuring a GaN buffer with a thickness of 1800 nm, a 130 nm thick AlN nucleation layer, and a SiC substrate measuring 500 µm in thickness.

The thermal conductivity values utilized for this structure are provided in table 29 below.

The GaN-on-SiC device was initially measured using layout 2, thus simulations were conducted based on the parameters of layout 2 structure. Subsequently, simulations were performed on layout 1 structure for comparison purposes. The obtained results were then evaluated against the area-specific thermal resistance value.

Table 29 Thermal conductivity values used for the GaN-on-SiC structure in thermal simulation.

Material	***k* (@ 300 K) (W/mK)**
GaN film	$127 \cdot (300/T)^{1.4}$
AlN (NL)	$25 \cdot (300/T)^{0.9}$
SiC	$330 \cdot (T/300)^{-1.26}$
Contacts	315

Simulation with an Alternative Power Switch Device (Layout 2)

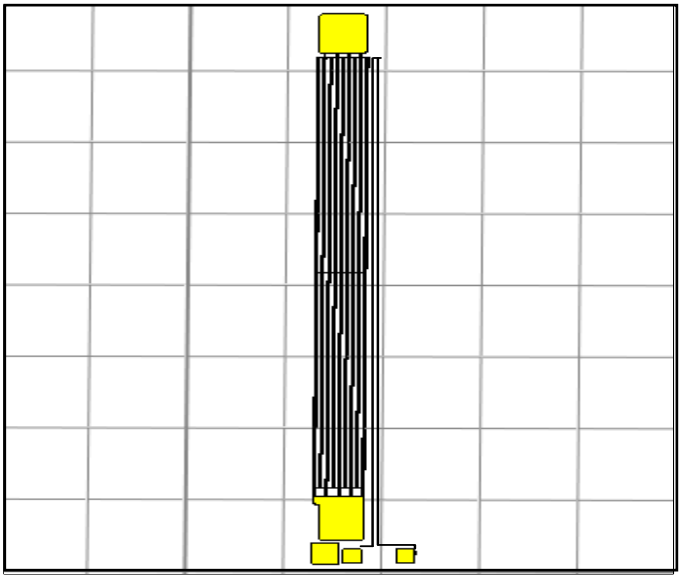


Figure 42 GaN alternative power switch HEMT device structure with temperature pads used for thermal simulation (Layout 2).

Initially, simulations were conducted for GaN-on-Si and compared with the characterized values, yielding similar thermal resistance results. Subsequently, simulations were performed for GaN-on-SiC using the thermal conductivity values from the provided table 29 for different temperatures, and the corresponding thermal resistance values were calculated, as presented in the table 30 below.

Leveraging the simulation model, junction temperatures for the GaN-on-SiC device layout 1 structure were simulated and compared with the area specific thermal resistance values measured from the previous chapter. Consistent thermal conductivity values were employed, with only the device structure being altered while keeping material compositions and layer thicknesses constant. The calculated thermal resistance values obtained after simulation are detailed in the table 31 below.

Table 30 Thermal resistance values of GaN-on-SiC with alternate structure after thermal simulation for different chuck temperatures for a channel area, A = 0.78 mm² (Layout 2).

Temperature	30°C	40°C	60°C	80°C
R_{TH} **(K/W)**	0.7	0.8	0.85	0.9
$R_{TH} \cdot A$ **(K mm²/W)**	0.57	0.62	0.66	0.71

Table 31 Thermal resistance values of GaN-on-SiC device structure after thermal simulation for different chuck temperatures for a channel area, A = 0.29 mm² (Layout 1).

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	2.2	2.4	2.6	2.8
$R_{TH} \cdot A$ (K mm²/W)	0.64	0.69	0.75	0.8

A plot comparing the measured values versus simulated thermal resistance for layout 1 and layout 2 is depicted in figure 43 , demonstrating a close alignment between the results. The values exhibit a remarkable coherence, providing a solid foundation for future analyses aimed at determining junction temperatures across various device structures.

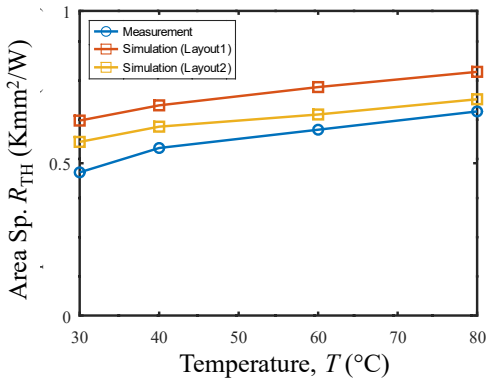


Figure 43 Comparison plot depicting the thermal resistance values of the GaN-on-SiC device, contrasting the calculated values with those obtained from simulation.

For a SiC substrate thickness of 125 µm, simulations were conducted, and the resulting thermal resistance values are presented below in table 32. It is observed that the values are reduced compared to the case with a thick substrate.

Table 32 Thermal resistance values calculated from simulated junction temperatures for GaN-on-SiC device, utilizing a thinner substrate for a channel area, A = 0.29 mm² (Layout 1).

Temperature	30°C	40°C	60°C	80°C
R_{TH} (K/W)	1.2	1.3	1.4	1.5
$R_{TH} \cdot A$ (K mm²/W)	0.35	0.37	0.4	0.44

5.4 GaN-on-Sapphire

For GaN-on-Sapphire, which couldn't be characterized directly, a model was created for thermal simulation to extract thermal resistances. The layer structure comprises a sapphire substrate with a thickness of 650 µm and a GaN buffer layer of 900 nm thickness as shown in figure 44.

The thermal conductivity values used for simulation are provided in table 33 below. The relation for Sapphire at different temperatures is referenced from [77], and the thermal resistance calculated for various backside temperatures is presented in table 34.

Notably, the device exhibits significantly high thermal resistance compared to devices with other substrate materials due to the poor thermal conductivity of sapphire.

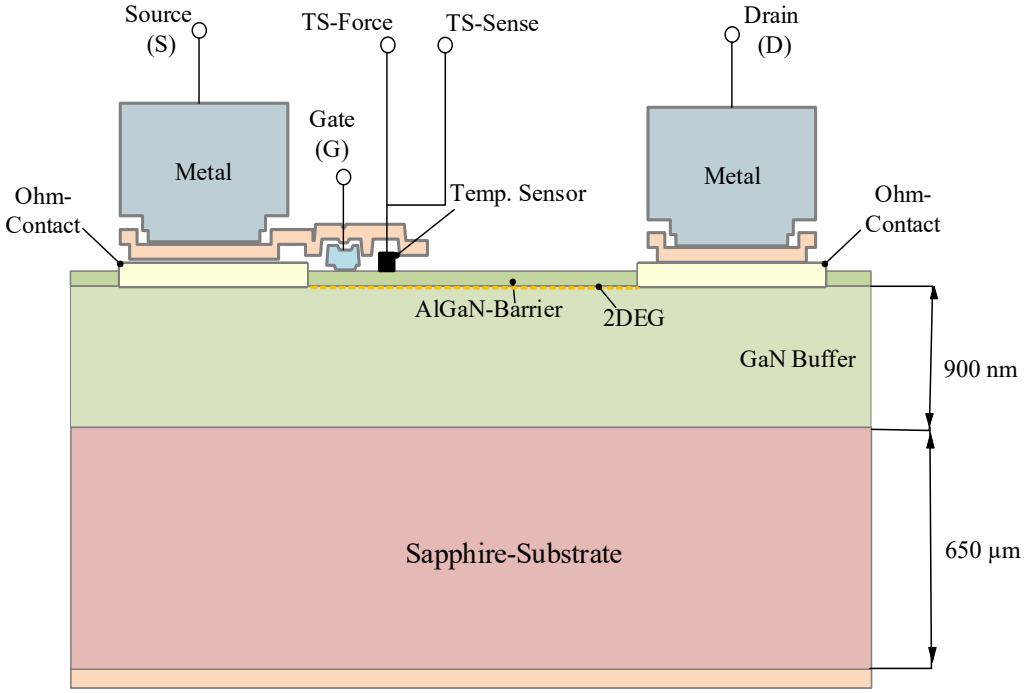


Figure 44 Cross-section and top view of a GaN-on-Sapphire HEMT with temperature sensor.

Table 33 Thermal conductivity values used for the GaN-on-Sapphire structure in thermal simulation.

Material	***k* (@ 300 K) (W/mK)**
GaN film	$127 \cdot (300/T)^{1.4}$
Sapphire	35
Contacts	315

Table 34 Thermal resistance values calculated from simulated junction temperatures for GaN-on-Sapphire device at various backside temperatures for a channel area, A = 0.29 mm² (Layout 1).

Temperature	20°C	40°C	60°C	80°C
R_{TH} (K/W)	20.2	23.7	25.1	27.6
$R_{TH} \cdot A$ (K mm²/W)	5.9	6.9	7.2	8

To explore potential solutions, the sapphire substrate thickness was reduced to 125 µm, and simulations were conducted to assess its impact on reducing thermal resistance. The thermal resistance values calculated after simulation are shown below in table 35.

Table 35 Thermal resistance values calculated from simulated junction temperatures for GaN-on-Sapphire device, utilizing a thinner substrate for a channel area, A = 0.29 mm² (Layout 1).

Temperature	20°C	40°C	60°C	80°C
R_{TH} (K/W)	13.9	16.3	17.2	18.9
$R_{TH} \cdot A$ (K mm²/W)	4	4.7	5	5.5

While a reduction in values compared to thick substrates is observed, these devices still demonstrate high junction temperatures. However, it's noteworthy that the thin substrate exhibits comparable values when compared to the thick substrate GaN-on-Si device.

5.5 Summary & Discussion

In this chapter, thermal simulations were conducted for various GaN HEMT devices on different substrates, including GaN-on-Si, GaN-on-GaN, GaN-on-SiC, and GaN-on-Sapphire. The simulations aimed to evaluate the thermal behavior of these devices and compare the results with experimental characterization data. By utilizing sophisticated simulation software and accurately defining the device structures and material properties, thermal resistance values were extracted for different backside temperatures. The main objective of this chapter was twofold: to establish a reliable simulation model that accurately aligns with measured data and to summarize the thermal conductivity values of each material utilized in the GaN HEMT devices.

Table 36 Summary of Thermal Conductivity Values for GaN Power Switch Transistors.

Material	*k* (@ 300 K) (W/mK)	Reference
GaN film	127	[25]
AlN (NL)	25	[25]
SL	10	[4]
Step-graded AlGaN	14	
Si Bulk	80	[57]
GaN Bulk	130	Supplier
SiC	330	[50]
Sapphire	35	[29]
Contacts	315	[4]

By achieving these objectives, the aim was to avoid overestimating the junction temperature and to provide a foundation for future measurements and optimizations. Additionally, the chapter sought to analyze the results of the calculations and offer a valid comparison, enabling the assessment of devices with different structures using the established model. Furthermore, a key goal was to develop a trustworthy model capable of predicting junction temperatures for devices with sapphire substrates and potentially for other future materials. Through these efforts, this study contributes to advancing the understanding of thermal behavior in GaN-based devices, facilitating informed design decisions and improvements in thermal management strategies.

The table below presents a summary of the area-specific thermal resistance in K mm²/W for GaN power switch HEMTs with thin substrates obtained from simulation.

Table 37 Summary of the area-specific thermal resistance in K mm²/W for GaN power switch HEMTs with thin substrates (t_{SUB} = 125 µm) obtained from simulation.

Structure Layout 1 (A = 0.29 mm²)	R_{TH} A (K mm²/W)				
	20°C	**30°C**	**40°C**	**60°C**	**80°C**
GaN-on-Si (SL)	1.5		1.6	1.7	1.9
GaN-on-Si (Graded)		1.4	1.6	1.7	1.8
GaN-on-GaN		0.88	0.92	1	1.1
GaN-on-SiC		0.35	0.37	0.4	0.44
GaN-on-Sapphire	4		4.7	5	5.5

6. Cross-Validation using Infrared method

To enhance the reliability of the thermal characterization and simulation results, cross-validation was conducted using the Infrared (IR) method. This step of cross-validation aims to bolster the reliability of the study's findings, adding further assurance to the conclusions drawn from the characterization and simulation processes.

6.1 IR on GaN Power Switch HEMTs

In the IR method, measurements were conducted on the same devices characterized in Chapter 4. Needles were positioned on drain and source pads, with the gate-source voltage set to 0 V. By varying the drain-source voltage to generate power in the channel, resulting heat was captured using an IR camera. Throughout the measurements, the backside temperature was consistently set to 40 °C, and the camera was calibrated before each session.

Figure 45 illustrates the heat produced in the device captured by an IR camera.

For GaN-on-Si devices, both superlattice (SL) and step-graded buffers were used to cross-verify the results obtained from characterization.

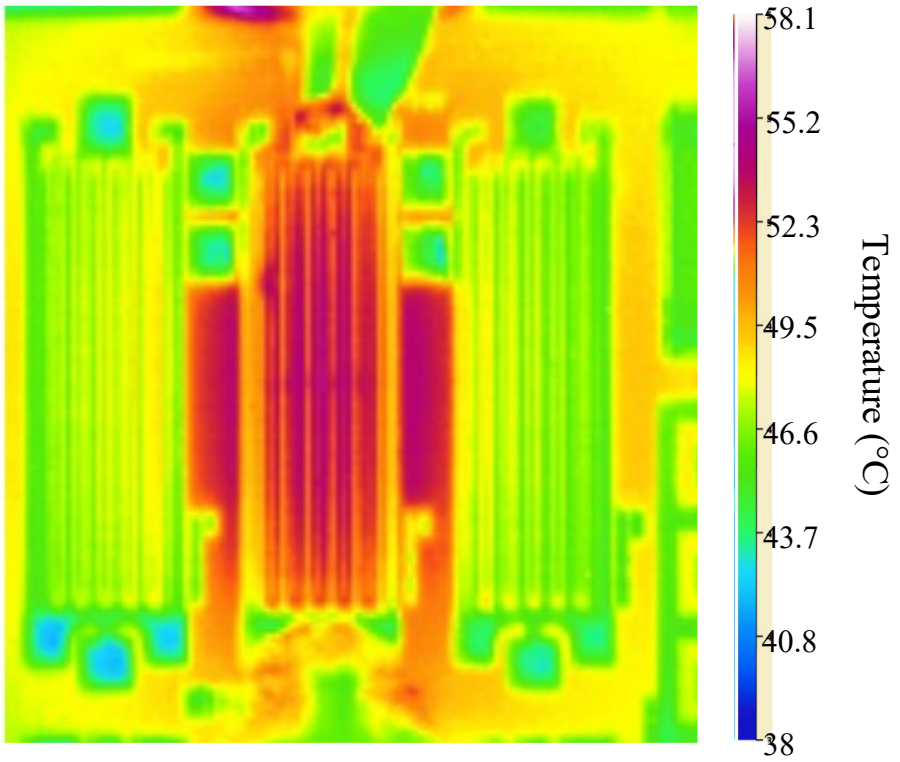
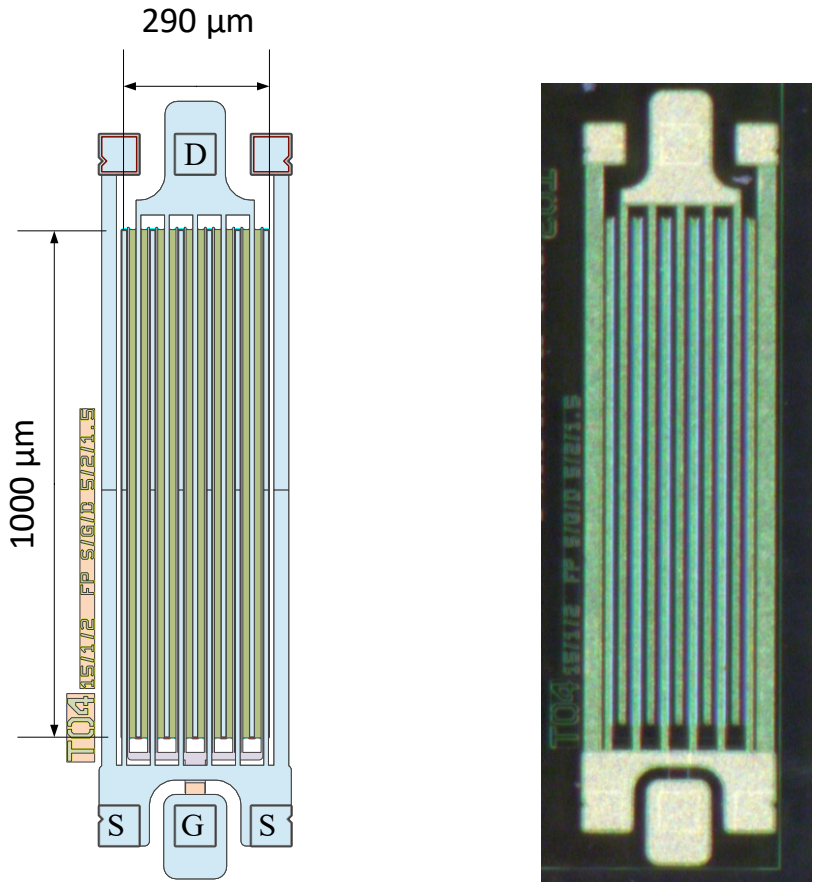


Figure 45 Infrared (IR) Thermal Imaging of GaN-on-Si power HEMT device in the middle with step-graded buffer: Channel power 1°W, Chuck temperature 40 °C.

Additionally, to ensure a comprehensive comparison for GaN-on-SiC, a similar structure (layout 3) with a channel area of A = 0.29 mm^2 as shown in figure 46 and similar R_{ON} to that of layout 1 was employed.

Figure 47 presents the plot of junction temperature at different channel powers for the SL, step-graded, GaN-on-GaN, and GaN-on-SiC devices at a backside temperature of 40 °C.

The slope of the plot aids in calculating the thermal resistance of each device. The table below summarizes the calculated thermal resistance values for each device at a backside temperature of 40 °C.



a) **b)**

Figure 46 a) Layout 3 of GaN power switch HEMT with an active channel area, A = 0.29 mm² b) Microscopic view of the measured device layout 3.

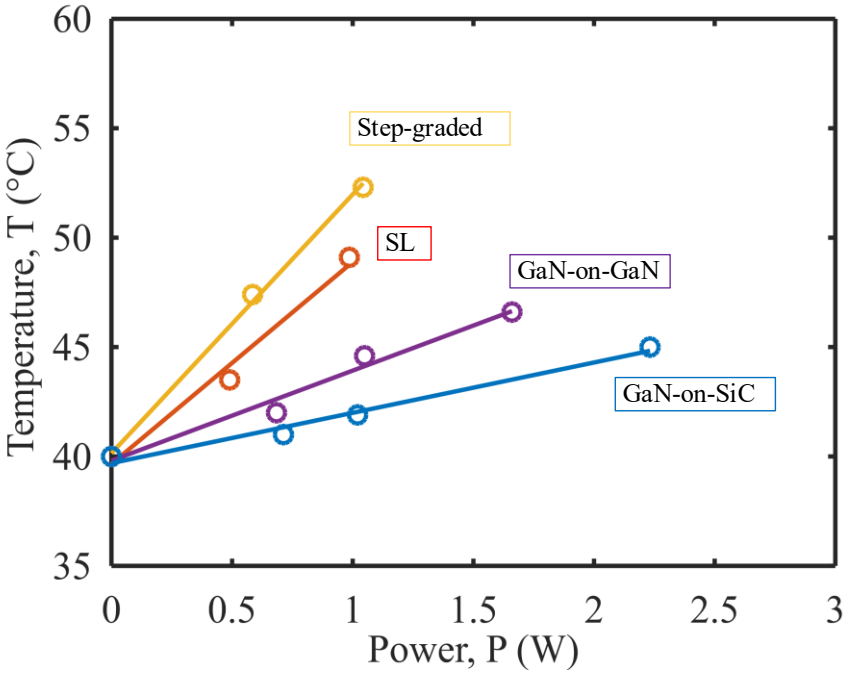


Figure 47 Junction Temperature vs. Channel Power for Various GaN Power HEMT Devices after IR Thermal Imaging.

6.2 Summary & Discussion

Table 38 Summary of Calculated Thermal Resistance Values for GaN Power HEMT Devices with IR at 40 °C Backside Temperature.

Power Device	$R_{TH \cdot A}$ (@ 40 °C) (K mm²/W)
Step-graded	3.4
SL	2.7
GaN-on-GaN	1.2
GaN-on-SiC	0.7

The utilization of the Infrared (IR) method for cross-validation purposes has provided valuable insights into the thermal behavior of GaN power switch HEMT devices across various substrates. Through meticulous measurements conducted on the same devices previously characterized, the IR method enabled an independent assessment of the devices' thermal characteristics. By positioning needles on drain and source pads and setting the gate-source voltage to 0 V, the resulting heat generated in the channel was captured using an IR camera.

Maintaining a consistent backside temperature of 40 °C and calibrating the camera before each session ensured the accuracy of the measurements.

In conclusion, the IR method serves as a valuable tool for corroborating thermal characterization data and validating simulation models.

7. Summary, Results, and Conclusion

Summary

The thesis investigates the area-specific thermal resistance of GaN power switch HEMTs with various substrates, employing an integrated temperature sensor on the devices at different backside temperatures. Analyzing the impact of different substrate materials on the device's junction temperature, the study aims to optimize design parameters.

As expected, GaN-on-SiC demonstrated the lowest R_{TH} giving a value of 0.55 K mm^2/W at 40 °C backside temperature and a substrate thickness of 500 µm (see chapter 4.1.3). GaN-on-GaN for a substrate thickness of 500 µm (1.6 K mm^2/W at 40 °C) devices exhibited high thermal conductance (see chapter 4.1.2) compared to GaN-on-Si for a substrate thickness of 800 µm (3.5 K mm^2/W at 40 °C), with the thermal resistance nearly half the value of that for GaN-on-Si devices (see chapter 4.2).

A lack of a significant observable difference in the impact of different buffer layers (SL & step-graded) on GaN-on-Si devices was observed (see chapter 4.2) and presumably attributed to the substantial thickness and poor thermal conductivity (80 W/m K @RT) of the Si substrate (see chapter 3.1.4.1 & chapter 5.1).

When attempting to use a thinner Si substrate to study the effect of buffer layers, reliable results couldn't be produced. Despite the on-state resistance of the device being within the expected range, and a linear relation between the sensor resistance and temperature being observed, it is likely that the bow-shaped wafers for the thin substrate failed to adhere properly to the chuck.

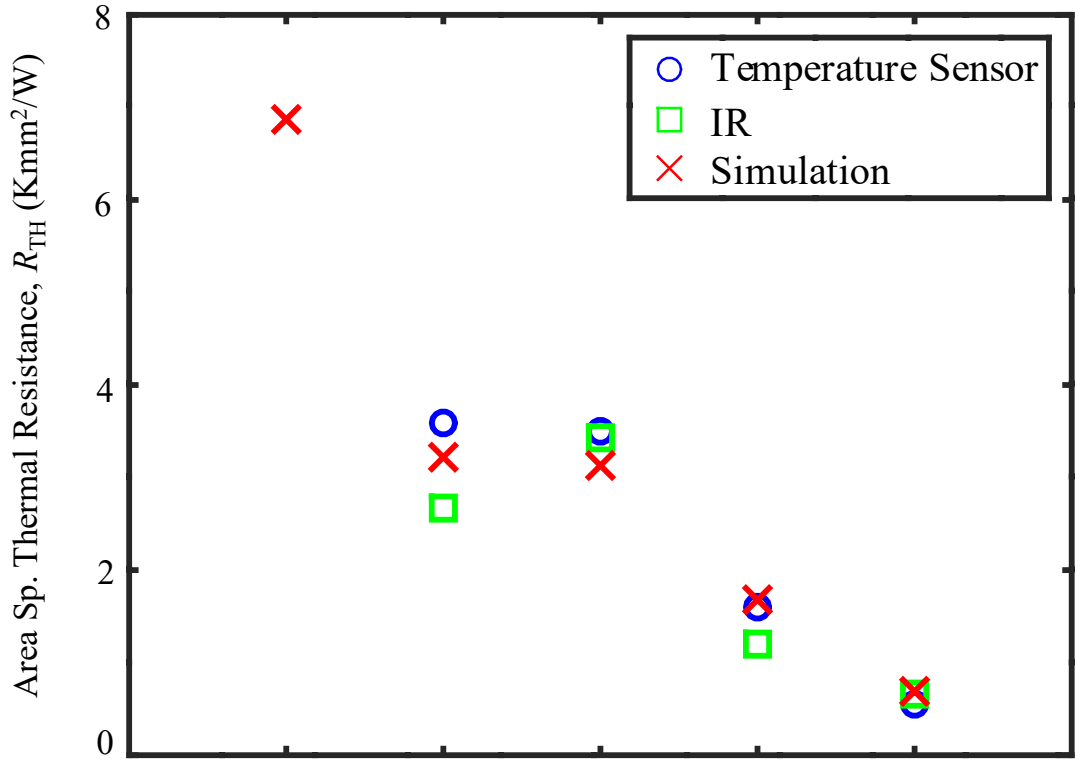
The simulations aimed to assess the thermal behavior of these devices and compare the results with experimental characterization data. Additionally, devices that couldn't be characterized were modeled and simulated including the upcoming GaN-on-sapphire (6.87 K mm^2/W & 4.73 K mm^2/W for a thin sapphire substrate at 40 °C) devices (see chapter 5.4). Simulation was also made on thin substrates to study the role of substrate thickness in the junction temperature (see figure 49). Since the devices with various substrates had a comparable layout, comparison and relevant thermal parameters of the materials could be extracted precisely.

The objective was to establish a reliable simulation model accurately aligning with measured data and summarizing the thermal conductivity values of each material utilized in the GaN HEMT devices, thereby avoiding overestimating junction temperature.

Meticulous measurements conducted through the IR method on previously characterized devices provided an independent assessment of thermal characteristics (see chapter 6.1). This comparative analysis strengthens confidence in the study's findings by corroborating consistency across different measurement techniques. Ultimately, the IR method serves as a valuable tool for corroborating thermal characterization data and validating simulation models.

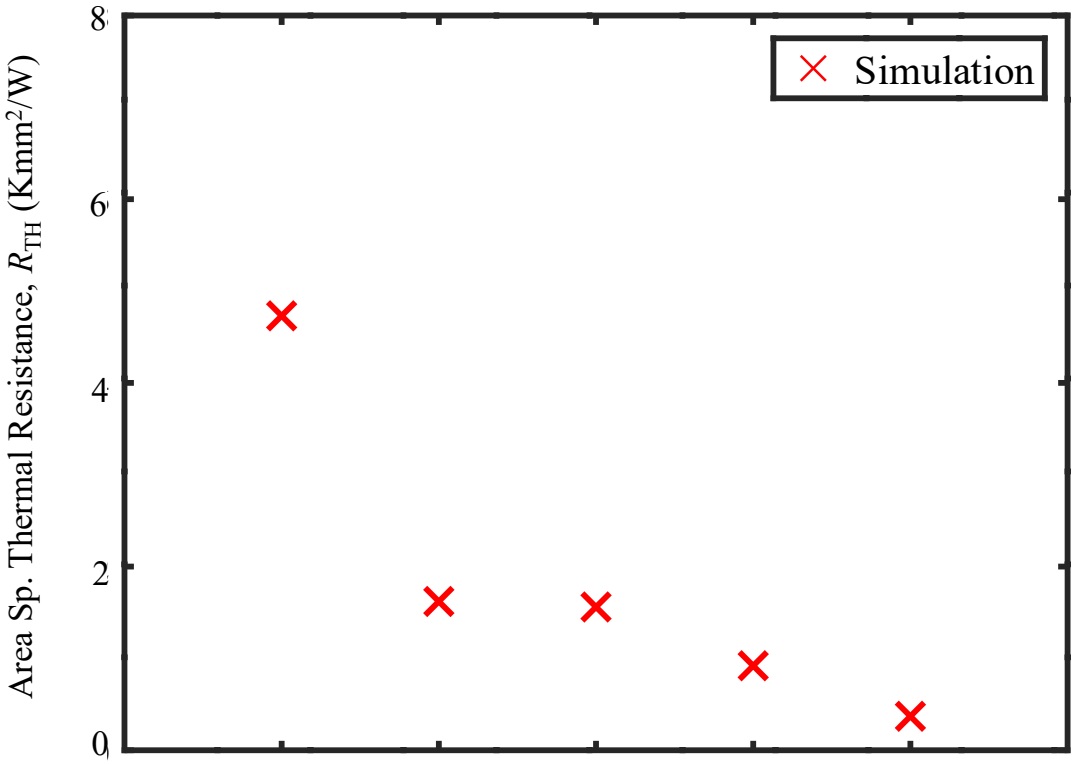
Furthermore, a plot comparing the results obtained from characterization using temperature sensor method, simulation, and IR measurements as shown in figure 48 offers a comprehensive view of the devices' thermal behaviour. For sapphire, only simulation results could be obtained. However, it's evident from the plot that the simulation results align well with other characterization methods. This comparative analysis enhances the confidence in the study's findings by corroborating the consistency across different measurement techniques.

Figure 49 below provides a summary of simulation results for GaN power switch HEMTs with thin substrates at a backside temperature of 40°C. The plot illustrates the thermal resistance values obtained through simulation for various device configurations and substrate materials.



Technology	t_{GaN} [µm]	t_{SUB} [µm]
GaN-on-Sapphire	0.9	650
GaN(SL)-on-Si	2.15	800
GaN(Graded)-on-Si	3.29	800
GaN-on-GaN	0.9	500
GaN-on-SiC	1.8	500

Figure 48 Comparison of temperature sensor method, IR and simulation results for GaN power switch HEMTs: Chuck temperature 40 °C. On the x-axis shows the technology with the GaN buffer thickness and the substrate thickness in µm.



Technology	t_{GaN} [µm]	t_{SUB} [µm]
GaN-on-Sapphire	0.9	125
GaN(SL)-on-Si	2.15	125
GaN(Graded)-on-Si	3.29	125
GaN-on-GaN	0.9	125
GaN-on-SiC	1.8	125

Figure 49 Comparison of simulation results for GaN power switch HEMTs with thin substrates (tSUB = 125 µm): Chuck temperature 40 °C. On the x-axis shows the technology with the GaN buffer thickness and the substrate thickness in µm.

Findings of the Thesis

The findings of the thesis address the scientific questions posed at the outset of the research (see chapter 1.2). It shed light on the significant influence of carrier substrate material on the thermal behavior of GaN power switch HEMTs. Through comprehensive measurements and analysis, it was observed that different substrates, including GaN-on-Si, GaN-on-SiC, and GaN-on-GaN, exhibit varying thermal characteristics. Consistent with existing literature, SiC emerged as the most efficient substrate in terms of thermal behavior, with a thermal resistance of 0.55 Kmm²/W at 40°C (see chapter 4.2).

Notably, the investigation into GaN-on-GaN devices, which is relatively scarce in literature, yielded intriguing results. GaN-on-GaN devices demonstrated remarkably superior thermal performance compared to GaN-on-Si, with the thermal resistance being nearly half that of GaN-on-Si devices. This notable difference can likely be attributed to the higher thermal conductivity of GaN compared to Si (see chapter 3.1, chapter 5.2), as well as the lower substrate thickness and fewer buffer layers in GaN-on-GaN configurations compared to GaN-on-Si setups (see chapter 4.1). This discovery underscores the significance of considering GaN-on-GaN configurations for enhanced thermal management in lateral HEMTs. Overall, the findings suggest a clear hierarchy in area-specific thermal resistance values, with GaN-on-SiC < GaN-on-GaN < GaN-on-Si (see chapter 4.2), emphasizing the crucial role of substrate material in optimizing thermal performance in GaN-based power switch HEMTs.

The thickness of the carrier substrate emerged as a critical factor influencing the junction temperature of the device. GaN-on-Si devices exhibited a higher number of buffer layers (also with poor thermal conductivity) compared to GaN-on-SiC and GaN-on-GaN configurations (see chapter 3.1), contributing to variations in thermal behavior. Additionally, the measured thickness of the Si substrate exceeded that of GaN-on-GaN and GaN-on-SiC substrates, further influencing thermal performance.

These differences in substrate thickness and buffer layer composition indeed played a role in determining junction temperature. However, the specific influence of these factors could be better understood through measurements and comparisons with devices featuring thinner substrates. Unfortunately, attempts to measure devices with thin substrates yielded unreliable results, possibly due to the bow-shaped wafer's inadequate adherence to the chuck. However, the cause of the measurement inaccuracies with thinned wafers could not be conclusively clarified. Despite this challenge, the findings underscore the importance of considering substrate thickness in optimizing thermal performance and highlight the need for further investigation to fully elucidate its impact on GaN power switch HEMTs.

Thermal simulations proved instrumental in gaining deeper insights into the role of substrates in GaN power switch HEMTs (see chapter 5). Notably, the thermal conductivity value for the Si substrate in GaN-on-Si configurations was found to be lower than values reported in many literature sources, likely due to the relationship between doping concentration and material resistivity. Unlike RF devices, which often utilize pure Si substrates, GaN power HEMTs employ doped Si substrates (see chapter 3.1.4.1), significantly impacting the device's junction temperature, especially given the comparatively greater thickness of the substrates relative to other epitaxial layers.

Similarly, both GaN and SiC substrates exhibited lower thermal conductivity values, with the thermal conductivity value for the GaN substrate provided by the supplier aiding in validating the values used for the model (see chapter 5.2). Simulations were also crucial in investigating the influence of thin substrates on junction temperature (see chapter 6.2, figure 49). For

instance, in GaN-on-Si devices, even with a 125 µm Si substrate thickness, minimal influence on the buffer layers was observed. However, for GaN-on-SiC configurations, where SiC possesses higher thermal conductivity, the influence of buffer layers became more pronounced, emphasizing the need for measurement data to accurately determine the thermal conductivity values of buffer layers in thin substrate devices.

Moreover, simulations extended to include devices that could not be characterized, such as upcoming GaN-on-sapphire configurations (see chapter 5.4). Given sapphire's markedly low thermal conductivity compared to other materials, devices featuring this substrate exhibited higher junction temperatures. While the absence of measurement data precluded an accurate prediction of sapphire substrate's thermal conductivity, it is reasonable to infer that buffer layers would have a less significant impact on junction temperature in such devices. These findings underscore the importance of combining simulation insights with measurement data to comprehensively understand the thermal behavior of GaN power switch HEMTs across various substrate configurations.

Cross-validation with IR thermography served as a crucial step in independently assessing the junction temperature of the measured devices (see chapter 6). By utilizing the same wafers for both measurements, the closely matched results not only validated the effectiveness of the integrated sensor method but also provided confidence in the accuracy of the obtained junction temperature readings. Additionally, measurements were conducted on device structures without temperature sensors but with comparable areas (compare layout 1, figure 6 vs layout 2, figure 22), facilitating direct comparisons with other device configurations and enhancing the overall reliability of the study's findings.

The thermal characterization method utilizing an integrated sensor proved to be suitable for understanding the thermal behavior of GaN power switch HEMTs. Placing the sensor close to the channel enabled precise estimation of the junction temperature (see figure 6), while observing a linear relationship between sensor resistance and temperature provided reliable data. Access to GaN wafers with various substrates and buffer layers, each with comparable layouts, facilitated effective comparisons between different device configurations. However, there are some disadvantages to consider with the use of HEMTs with integrated temperature sensors. One such limitation is the necessity for calibration of each device, which can be a time-consuming process. As a result, these sensors are typically reserved for characterization purposes in research settings and may not be widely available for practical applications.

While cross-validation with IR measurements yielded close results, IR measurements are simpler and do not require additional needles for temperature pads. However, not all laboratories may have access to IR measurement setups, whereas impedance analyzers are more common. Furthermore, IR measurements are typically conducted at a single backside temperature, limiting their effectiveness in capturing temperature variations.

Despite these drawbacks, the integrated sensor method offers a better understanding of temperature variations within the device, which is crucial considering the non-linear relationship between temperature and materials. Overall, the method provides valuable insights into the thermal behavior of GaN power switch HEMTs and serves as a reliable tool for characterization.

Conclusion

In conclusion, this thesis thoroughly explores the efficiency of power electronics by studying GaN-based power switch HEMTs, particularly focusing on understanding thermal resistance through characterization and simulation. By examining different epitaxy and substrate technologies and their impact on junction temperature, the study provides valuable insights for improving device performance. Notably, GaN-on-GaN devices exhibit superior thermal capabilities compared to GaN-on-Si devices, suggesting potential avenues for better thermal management in lateral HEMTs. Additionally, the research emphasizes the importance of precise parameterization in thermal simulations and validates the reliability of integrated sensor methods through cross-validation with IR thermography. Overall, this work significantly advances our knowledge of GaN-based power electronics and offers practical guidance for optimizing thermal management strategies.

8. Acknowledgements

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Literature

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