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Two-terminal III–V//Si triple-junction solar cell with power conversion efficiency of 35.9 % at AM1.5g

Patrick Schygulla | Ralph Müller | David Lackner | Oliver Höhn | Hubert Hauser | Benedikt Bläsi | Felix Predan | Jan Benick | Martin Hermle | Stefan W. Glunz | Frank Dimroth

Division Photovoltaics, Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, Germany

Correspondence
Patrick Schygulla, Division Photovoltaics, Fraunhofer Institute for Solar Energy Systems ISE, Heidenhofstr. 2, 79110 Freiburg, Germany.
Email: patrick.schygulla@ise.fraunhofer.de

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Abstract

III–V//Si multijunction solar cells offer a pathway to increase the power conversion efficiency beyond the fundamental Auger limit of silicon single-junctions. In this work, we demonstrate how the efficiency of a two-terminal wafer-bonded III–V//Si triple-junction solar cell is increased from 34.1 % to 35.9 % under an AM1.5g spectrum, by optimising the III–V top structure. This is the highest reported efficiency to date for silicon-based multijunction solar cell technologies. This improvement was accomplished by two main factors. First, the integration of a GaInAsP absorber in the middle cell increased the open-circuit voltage by 51 mV. Second, a better current matching of all subcells enhanced the short-circuit current by 0.7 mA/cm^2. Two different growth directions, upright and inverted, were investigated. The highest cell efficiency of 35.9 % ($V_{oc} = 3.248$ V, $j_{sc} = 13.1$ mA/cm^2, $FF = 84.3$ %) was achieved with an upright grown structure. Processing of upright structures requires additional bonding steps, which results in a reduced homogeneity of cell performance across the wafer. A detailed comparison with the currently best triple-junction solar cell reveals future improvement opportunities and limits, considering voltage and current, respectively.

KEYWORDS
III–V semiconductors, III–V//Si, MOVPE, multijunction solar cells, record efficiency, silicon-based tandem solar cells, two-terminal solar cells, wafer bonding

1 | INTRODUCTION

Single-junction crystalline silicon solar cells have a theoretical efficiency limit between 29.4 % and 29.5 %.[1,2] To make better use of limited areas and to continue reducing levelised costs of electricity in terrestrial applications, it is vital to explore new solar cell concepts that can exceed this limit. In multijunction solar cells, thermalisation and nonabsorption losses are reduced, and thus, the efficiency limit is enhanced. The current record efficiency of all solar cell concepts under 1-sun AM1.5g illumination was demonstrated for an inverted metamorphic sextuple-junction solar cell and amounted to 39.2 %.[3]

Such multijunction solar cells are based on III–V compound semiconductors that are grown by epitaxial deposition for example on germanium (Ge), gallium arsenide (GaAs) or indium phosphide (InP) substrates. The need of rare elements for wafers and precursors, the expensive facilities that are required for epitaxial growth and cell processing and the low numbers of produced units result in large cell

costs of around 60 $/W$_{DC}$[4] which is more than two orders of magnitude larger compared to single-junction silicon (Si) cells. Strong efforts are being undertaken to reduce the cost of III–V solar cell fabrication. One important breakthrough towards this goal are demonstrated growth rates above 120 μm/h.[5,6] The substrate costs amount to around a third of the total costs for III–V multijunction solar cells. Substrate removal and reuse approaches can help to reduce these costs.[7] Here, the expensive substrate is used for epitaxial growth, and then, the solar cell is transferred to a carrier wafer consisting of a cheaper material.

Another possibility is to use a less-expensive substrate material, for instance, silicon, as the bottom cell of a multijunction architecture. The III–V cell layer stack can be grown directly on the Si cell using a metamorphic buffer structure[8,9] to overcome the mismatch in lattice constants between Si and the III–V cells, for example, 4 % for the case of GaAs on Si. The highest power conversion efficiency was reported for a triple-junction GaInP/GaAs/Si solar cell with a value of 25.9 %.[10] This cell suffers from a voltage loss due to nonradiative recombination at the threading dislocation defects introduced by the metamorphic buffer growth. This loss mechanism can be avoided if the III–V top structure is grown lattice matched on GaAs and then either mechanically stacked on the Si cell (four-terminal configuration)[11] or monolithically connected to the Si cell (two-terminal configuration). The latter can be achieved by using either a direct wafer bond[12,13] or a transparent conductive adhesive.[14–16]

The four-terminal configuration does not require balanced current densities between the top and the bottom junctions. Consequently, though, the electrical interconnections of cells on a module level become more challenging. With a four-terminal design, the maximum conversion efficiency demonstrated amounted to 35.9 % for a triple-junction GaInP/GaAs/Si solar cell.[11] This has so far been the highest conversion efficiency of any silicon-based multijunction solar cell.[17] The two-terminal configuration allows for a direct integration into modules and the exploitation of existing technology for Si solar panels. The previous wafer-bonded triple-junction GaInP/AlGaAs//Si champion device, however, achieved a lower maximum conversion efficiency of 34.1 %.[18] Other promising developments for cost reduction in multijunction solar cells include the combination of a perovskite/Si dual-junction. This technology has recently obtained a record conversion efficiency of 29.1 %.[19]

Hence, combining the high-efficiency multijunction concept with the mature and cost-effective silicon technology is a promising route for redefining the practical solar cell efficiency limit. In this work, we explore the experimental efficiency potential of monolithic wafer-bonded III–V//Si triple-junction solar cells in a two-terminal configuration. Although in this work the employed GaAs substrates were etched away, in future, epitaxial lift-off techniques could be used for recycling of the substrate. By employing a new absorber material in the middle cell, we were able to demonstrate a new record conversion efficiency of 35.9 % under an AM1.5g spectrum making the monolithic two-terminal device as efficient as the current record four-terminal device.[11]

2 | EXPERIMENTAL METHODS

2.1 | Solar cell design

Given a bottom absorber with a fixed bandgap of 1.12 eV, the losses due to nonabsorbed photons in the multijunction device are constant. Hence, the incremental efficiency gain with increasing number of junctions is not as high for the case of a silicon bottom cell as for an absorber with the respective ideal bottom cell bandgap. In order to reduce nonabsorption losses, the bottom cell bandgap in an ideal scenario would have to be reduced to 0.93 eV (for three junctions) or 0.72 eV (for four junctions). In Figure 1, the theoretical efficiency limit under standard test conditions (AM1.5g) is shown for multijunction solar cells with and without bandgap constraint as a function of the number of junctions. A triple-junction solar cell with ideal bandgap energies of 1.90, 1.37, and 0.93 eV results in a power conversion efficiency of 51.8 % in the radiative limit. With the constraint of a bottom cell absorber bandgap of $E_g = 1.12\,\text{eV} = E_{g,Si}$, the maximum obtainable conversion efficiency is reduced to 49.6 %. The indirect nature of the silicon bandgap makes Auger recombination the dominant intrinsic recombination channel. Considering additionally a voltage drop of 112 mV compared to the radiative limit,[1] the maximum efficiency can be estimated to further decrease to 48.1 %. The efficiency of multijunction solar cells with a silicon bottom subcell

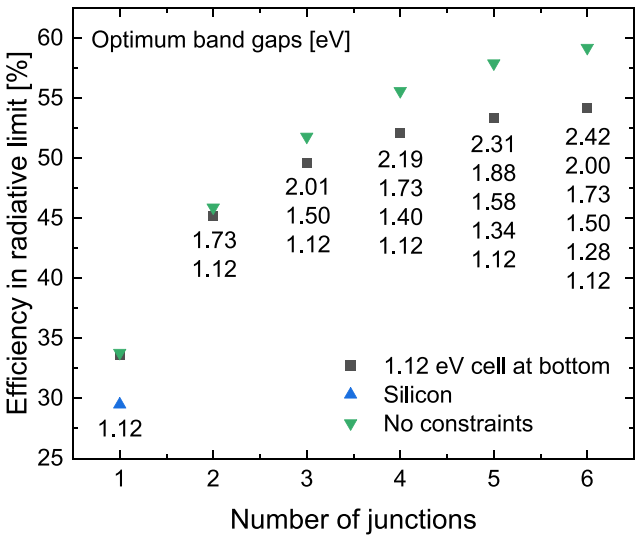

FIGURE 1 The theoretical efficiency in the radiative limit is shown as a function of the number of junctions in a multijunction solar cell. In green, the ideal scenario without constraints of bandgaps is shown. In blue, the value of a silicon single-junction device is plotted. The ultimate efficiency is lower compared to a single-junction solar cell of a direct semiconductor due to Auger recombination. In black, the efficiencies for a direct semiconductor with a bandgap of 1.12 eV as the bottom cell is shown. The numbers give the optimum bandgap combinations for the latter case for highest possible conversion efficiency under AM1.5g. The values were calculated using the software EtaOpt[20]

increases only slightly for more than three junctions, and this theoretical benefit may not even be seen in real devices due to additional losses, for example, in tunnel diodes or by internal resistances. This especially holds when considering the energy yield outdoors under realistic environmental conditions which include spectral and temperature changes throughout the day and year. Here, the sensitivity of multijunction solar cells increases with the number of junctions. Considering the availability of III–V semiconductor bandgaps, a triple-junction solar cell was identified as a promising compromise between efficiency potential and spectral sensitivity.

The ideal bandgap combination of the upper two junctions, which maximise the power conversion efficiency of the triple-junction device under an AM1.5g spectrum at 298 K, was calculated in the radiative limit to be 2.01 and 1.50 eV.[20] For the top junction only aluminium–gallium–indium–phosphide (AlGaInP) or aluminium–gallium–arsenide (AlGaAs) can reach the required bandgap lattice matched to GaAs. Both exhibit severe disadvantages, though. $Al_{0.55}Ga_{0.45}As$ is an indirect semiconductor and hence unsuitable for maximising the voltage. $Al_{0.11}Ga_{0.40}In_{0.49}P$ is known to have a rather low carrier mobility and an increased incorporation probability for parasitic oxygen resulting in reduced diffusion lengths, reduced open-circuit voltage, and increased sheet resistance, which is detrimental for the uppermost junction.[21] Choosing GaInP with a direct bandgap of 1.90 eV, our group can at present reach higher absolute voltages in practice. The theoretical efficiency potential, however, decreases with the lower bandgap absorber material to 46.8 %. Because of a higher minority carrier lifetime and reduced recombination in the depletion region resulting in higher voltages and a higher filling factor, a rear-heterojunction cell architecture with a thin $Al_{0.18}Ga_{0.33}In_{0.49}P$ base was implemented.[22] Choosing a lower bandgap top junction absorber does not alter the ideal middle cell bandgap, though, which remains at 1.50 eV. This bandgap can be realised either by $Al_{0.06}Ga_{0.94}As$[23] or $Ga_{0.93}In_{0.07}As_{0.87}P_{0.13}$[24] as shown in Figure 2. Previous studies have revealed that single-junction component cells with an $Ga_{0.93}In_{0.07}As_{0.87}P_{0.13}$ absorber layer reach higher open-circuit voltages than cells with an $Al_{0.06}Ga_{0.94}As$ absorber layer after respective optimisation of growth conditions.[25] With a higher In- and P-concentration, this quaternary material has also been shown to be a promising candidate for applications in a bandgap range of 1.6–1.8 eV.[26–28] From the theoretically ideal bandgap combination, we have calculated the actually required subcell thicknesses and bandgaps with an optical model of measured quantum efficiency results of previous III–V//Si batches.[29] The resulting layer structure of the triple-junction solar cell is presented in Figure 3.

2.2 | Epitaxial growth of the III–V top structure

The III–V top junction solar cells were grown using metalorganic vapour-phase epitaxy (MOVPE) in a commercial AIXTRON AIX2800G4-TM reactor. GaAs wafers of 4″ size with a 6° miscut of the (001) surface towards the (111)-B direction were employed as substrates. The precursors for the group-III elements were trimethylgallium (TMGa), trimethylindium (TMIn) and trimethylaluminium (TMAl). For the group-V elements, phosphine (PH_3) and arsine (AsH_3) were used. The doping agent precursor for n-type absorber layers was silane (SiH_4). For p-type material, dimethylzinc (DMZn) was used. Epitaxial growth was performed at standard wafer surface temperatures ranging from 550 °C to 680 °C with a preference for lower temperatures where possible to reduce the thermal load and interdiffusion effects. The V/III ratios were set between 20 and 40 for arsenide-based layers and between 60 and 140 for phosphide-based layers. For the top and middle junction absorber layers, the V/III ratio has been optimised in terms of the

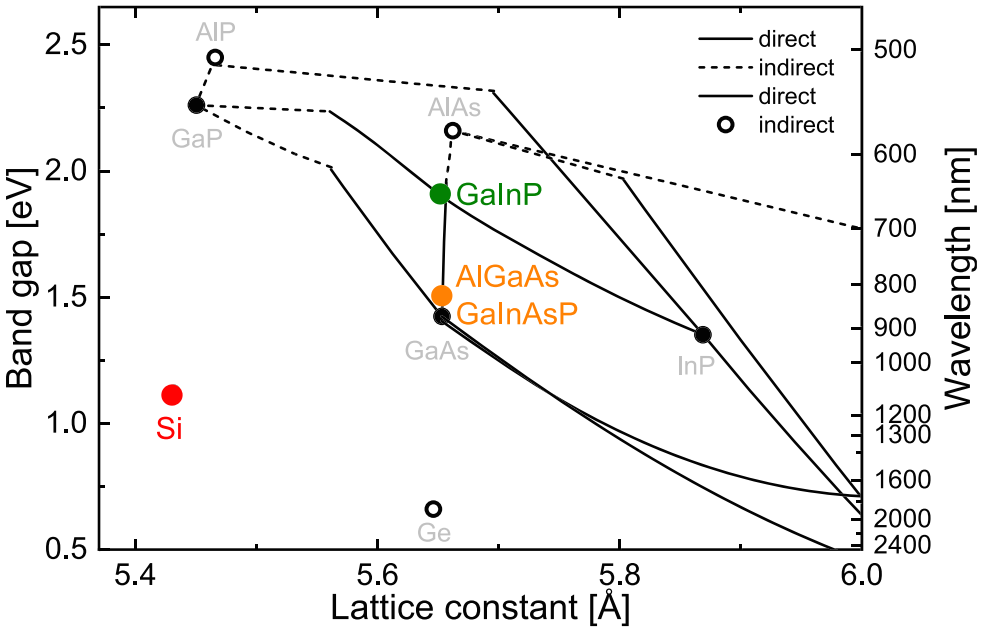

FIGURE 2 The target bandgaps for the top III–V dual junction at 1.90 and 1.50 eV can be realised by GaInP and GaInAsP or AlGaAs. To overcome the large lattice mismatch between the III–V semiconductors and silicon, a direct wafer bond is used

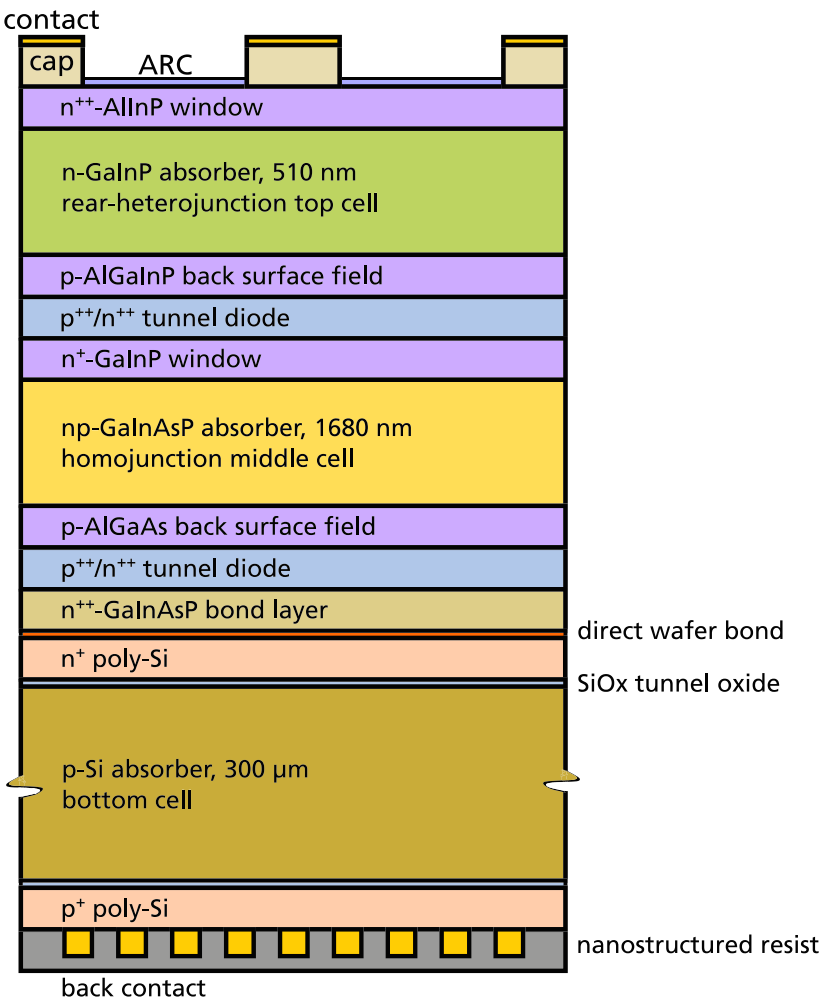

FIGURE 3 Schematic layer stack of the III–V//Si triple-junction solar cell design including a double-layer antireflection coating (ARC), a highly doped n-GaAs cap layer below the contacts, a GaInP-rear-heterojunction top cell, a GaInAsP homojunction middle cell, a silicon bottom cell with tunnel-oxide passivating contacts (TOPCon) and a nanostructured diffractive rear-side grating for light path enhancement

open-circuit voltage of single-junction component cells. Hydrogen was used as the carrier gas for the precursors. More details on the epitaxial growth are reported elsewhere.[12]

The III–V dual-junction subcells were grown in two different growth directions, upright and inverted. For both cases, the growth started with a GaInP etch stop layer to allow for selective chemical etching of the substrate. Then, for the upright grown samples, the bond layer was grown first followed by the middle junction, the top junction and the cap layer. In the case of inverted growth, the top junction was grown before the middle junction, and the bond layer was grown last as the uppermost layer.

2.3 | Silicon bottom cell

Float zone-grown p-type silicon wafers with a bulk resistivity of 4 Ω cm and a thickness of 280 µm, which had been polished on both sides, were used for the fabrication of the silicon bottom cells. Tunnel-oxide passivating contacts (TOPCon)[30] were formed on the n-type front and p-type back side. These layers passivate the surface very well and thus allow for a high voltage. A thin oxide was grown in HNO_3. A 100 nm thick intrinsic amorphous silicon was deposited by low-pressure chemical vapour deposition (LPCVD) on both sides. This layer was then doped by ion implantation of phosphorus at the front and of boron monofluoride at the back side. The amorphous layer was eventually annealed to polysilicon at 850 °C. Last, the samples were exposed to a remote hydrogen plasma at 425 °C. The front side was polished by chemical–mechanical polishing (CMP) to remove particles and thin the poly-Si layer to around half its thickness. No optimisation of the silicon bottom cell was performed as the largest potential was expected from the III–V top structure improvement. More details of the silicon subcell can be found elsewhere.[12]

2.4 | Solar cell processing

The two sets of samples were processed differently according to their respective growth direction. In Figure 4, the processing chains for upright and inverted grown samples are illustrated. The upright grown samples were first temporarily bonded to a sapphire carrier wafer. Then, the GaAs substrate was etched away, and the uncovered bond surface was smoothened by CMP. Next, a direct wafer bond between the III–V layer stack and the silicon bottom cell was performed in an Ayumi SAB100 high vacuum direct wafer bonder. The native oxides

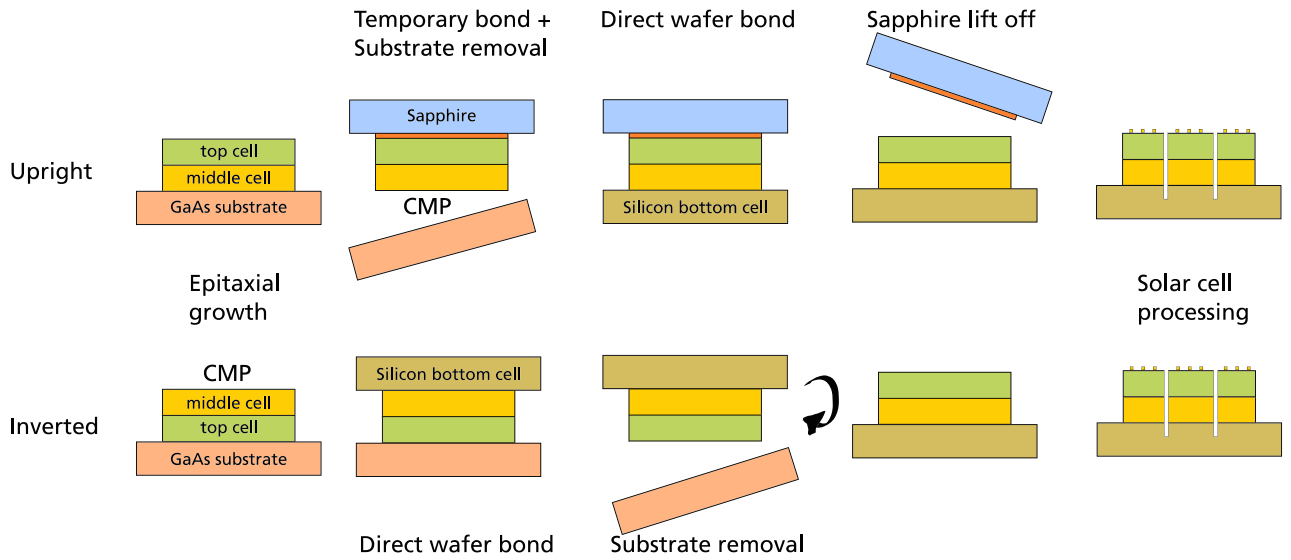

FIGURE 4 Process flow of upright (top) and inverted (bottom) grown solar cell structures. Both routes have some steps in common, such as the chemical–mechanical polishing (CMP), the direct wafer bond and the GaAs substrate removal. The upright processing route requires additionally a temporary bond to a sapphire plate and the corresponding lift-off

of the surfaces were first removed by argon ion sputtering at an energy of 0.3–0.4 keV. Then, the wafers were pressed together with a force of 2.4–10 kN for 5 min. Further details on the wafer bonding process are described elsewhere.[12,31] The sapphire carrier wafer was removed by thermal slide at 190 °C. At this point, the process chains of the upright and inverted route join again. The inverted route does not require the temporary bond. Here, the direct wafer bond can be performed directly before GaAs substrate removal.

The front contacts were deposited with the help of photolithography and metal evaporation. The cell area of 4.028 cm^2 was defined by wet chemical mesa etching. A Ta_2O_5/MgF_2 antireflection coating (ARC) was deposited on the front side by evaporation. On the rear side, an optical grating for light path enhancement in the silicon cell was implemented by nanoimprint lithography of a SU-8 photo resist.[32] Finally, a 1 µm thick silver contact layer was deposited on the nanostructured grating.

2.5 | Solar cell characterisation

The triple-junction solar cells were characterised in the Fraunhofer ISE CalLab under calibrated conditions. The external quantum efficiency (*EQE*) was measured with a grating monochromator and adjustable bias illumination in lock-in mode. Current–voltage (*IV*) characteristics were acquired for 1-sun conditions using the AM1.5g spectrum (IEC90604-3, ed. 2 with 1000 W/m^2). A spectrally adjustable sun simulator with one xenon and two halogen lamp fields at a cell temperature of 25 °C was used to set the correct illumination conditions.[33] A mask with a 3.987 cm^2 large aperture was put on the cells during the measurements to avoid generation of charge carriers in the Si wafer outside the active cell area. For the analysis of the current–voltage data, the two-diode model including resistances was employed.[34]

Electroluminescence (EL) spectra $I_{EL}(\lambda)$ were acquired under different injection conditions. Applying the reciprocity relations,[35]

$$I_{EL}(\lambda) = EQE(\lambda)\, I_{bb}(\lambda)\left(\exp\left(\frac{qV}{k_B T}\right) - 1\right),$$

the *EQE* and EL could be combined to calculate the contribution of each junction to the overall open-circuit voltage as a function of the short-circuit current density.[36] Here, $I_{bb}(\lambda)$, q, k_B, and T denote the black body emission spectrum at a photon wavelength λ, the elementary charge, Boltzmann's constant and the temperature, respectively. The forward bias current density and corresponding voltage are interpreted as the equivalent of the short-circuit current density and open-circuit voltage pair of an illuminated *IV* curve. Voltage calibration was done using *IV* curves at four different injection conditions. The bandgaps of the III–V semiconductors were determined from the intersection of two exponential fits to the *EQE*.[37]

3 | RESULTS AND DISCUSSION

3.1 | Performance of upright grown structures under 1-sun illumination

The *EQE*s of the three subcells of a triple-junction solar cell with upright grown top cell structure and their sum are shown in Figure 5. Integrating the AM1.5g spectrum under consideration of the quantum efficiency of each junction, one obtains the photocurrent beyond which the respective junction becomes limiting. The GaInP top

junction is slightly too thick for a perfect current match, and the Si bottom cell limits the total current density that is produced by the triple-junction. An additional solar resource of 0.67 or 0.22 mA/cm^2 per subcell could still be distributed by adjusting the absorber layer thicknesses. Note that the sum of the *EQE*s is constant at a high level ranging between 95 % and 98 % in the wavelength interval from 470 to 910 nm.

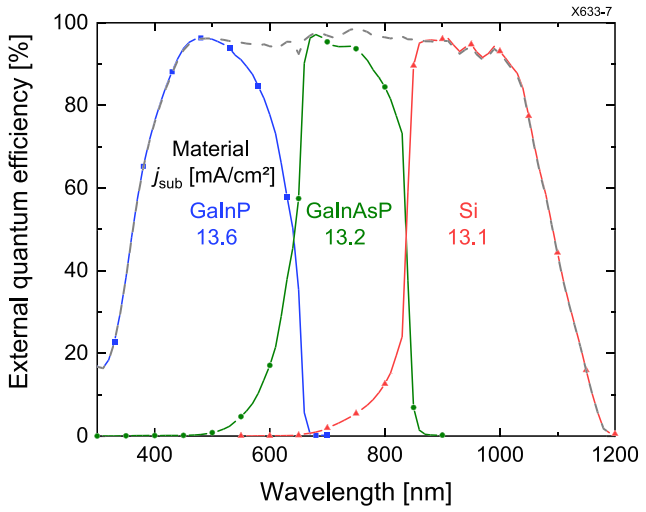

FIGURE 5 External quantum efficiencies of the top (blue, squares), middle (green, circles), bottom (red, triangles) subcells and the overall sum (grey, dashed) in the two-terminal record III–V//Si solar cell X633-7. The current density that each subcell could contribute to the photocurrent is given below the absorber material for each junction. The external quantum efficiencies were calibrated using the short-circuit current density of the triple-junction solar cell

The current–voltage characteristics of the champion cell are presented in Figure 6. Compared to the previous III–V//Si record device with a conversion efficiency of 34.1 %, the performance could be improved by 5.3 %$_{rel}$ or 1.8 %$_{abs}$. The two main reasons for this improvement were an increase in the voltage and in the current density. The open-circuit voltage (V_{oc}) was improved by 2.2 % or 71 mV. The origin of this voltage gain will be discussed in more detail in the following section. The current density could be enhanced by 5 % or 0.7 mA/cm^2. The previous cell was strongly current limited by the second junction with an AlGaAs absorber layer with a maximum difference in subcell current of $\Delta j_{sub} = 1.2$ mA/cm^2.[18] This imbalance could be reduced to $\Delta j_{sub} = 0.6$ mA/cm^2 in the current champion device thanks to an increased quantum efficiency and thus current generation in the GaInAsP-based middle junction.

From fitting the *IV* curve with a two-diode model, the series resistance was found to be around 1 Ω cm^2. Since the solar cell is designed to work under 1-sun condition, this results in a rather low voltage and filling factor loss. The low series resistance is a confirmation of the electrical functionality of the wafer bond and of a sufficiently high conductivity in the n-GaInP top layer. No impact of a finite parallel resistance could be observed in the modelling.

3.2 | Voltage gain by improved subcell absorber material

The improvement in open-circuit voltage compared to the previous champion device[18] can be understood from the subcell voltages shown in Figure 7. The voltage increases logarithmically with increasing injection current density because of the higher resulting charge carrier density. At injection conditions that correspond to AM1.5g

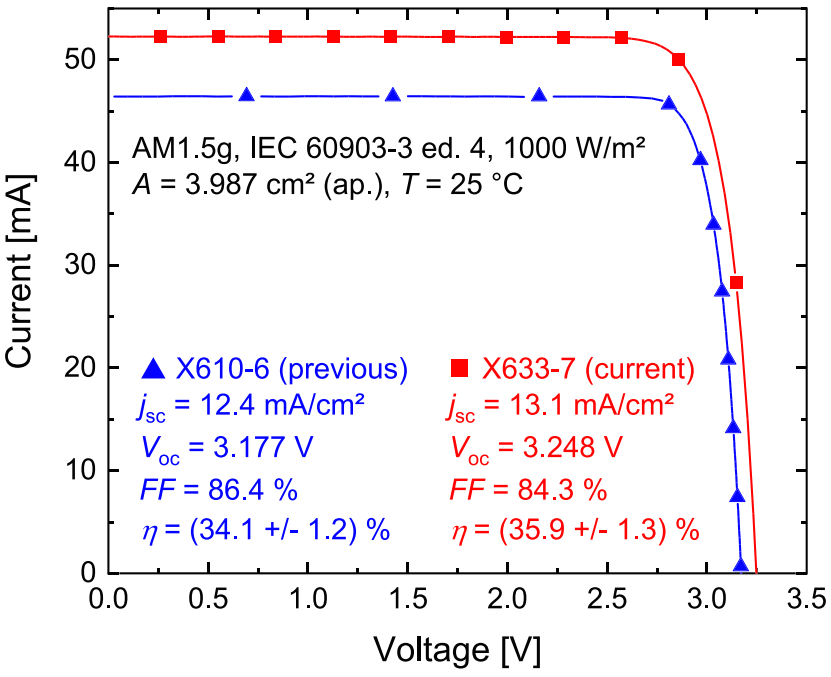

FIGURE 6 Current–voltage characteristics of the current two-terminal record III–V//Si solar cell X633-7 (red, squares) compared to the previous champion device X610-6 (blue, triangles) under the AM1.5g spectrum

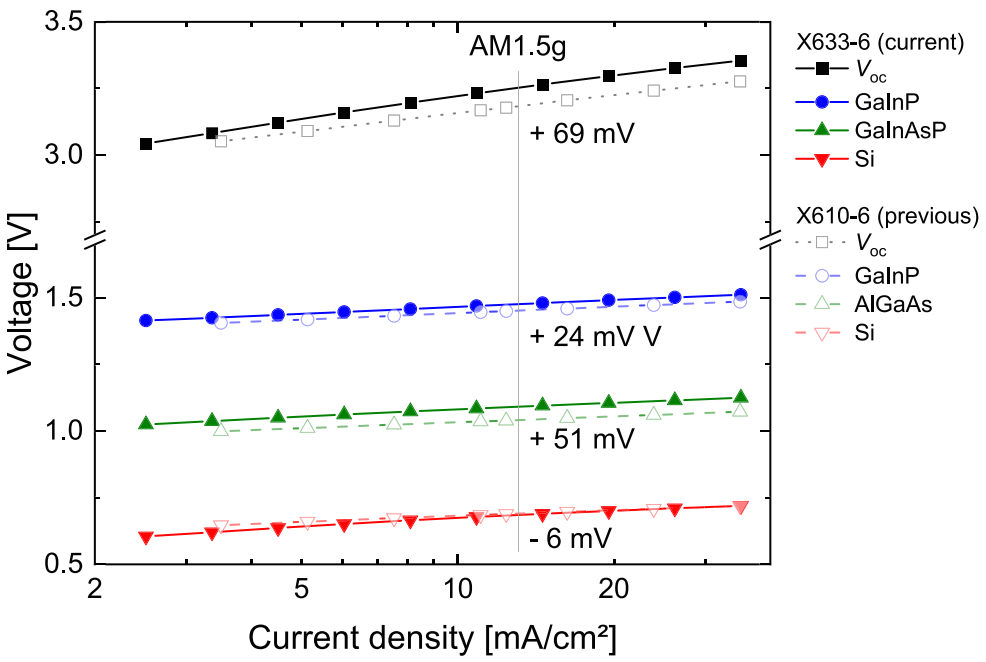

FIGURE 7 Open-circuit voltages (black, squares) and subcell voltages (coloured, squares, triangles) of the cell X633-6 from the current record III–V//Si wafer (solid, filled symbols) and of the previous champion device X610-6 (dotted, open symbols) at different injection current densities

illumination, 13.1 mA/cm^2 in this case, the open-circuit voltage can be broken down into a contribution of the three subcells. Comparing these subcell voltages to the ones of the previous champion device X610-6, the improvements can mostly be attributed to one development step. It has to be noted that for the previous champion device X610-6, the AM1.5g injection current amounted to only 12.4 mA/cm^2 so the total voltage improvement is even higher than indicated in Figure 7.

The biggest voltage gain resulted from replacing the AlGaAs absorber by a GaInAsP absorber in the middle junction as shown in Figure 7. As both materials had a similar bandgap to within 10 meV, the gain is due to an increased minority carrier lifetime resulting in a lower loss to the radiative limit on substrate of 55 mV, or 125 mV for a design with perfect rear-side reflector. This corresponds to an external radiative efficiency on substrate $\eta_{ext,rad} = \exp\left(-\frac{q\Delta V_{rad}}{k_B T}\right)$ of 11.1 %. Given that this is a value of a junction inside a multilayer structure, this compares well to the highest performing GaAs single-junction solar cell which has a rear-side mirror and exhibits an external radiative efficiency on mirror of 35.7 %.[38] A second smaller voltage gain originates in the GaInP top cell. Possible reasons for this increase could be fluctuations in the solar cell processing which damage the top cell most, for example, from the ARC deposition or cap etching inhomogeneities that generate local shunts.

The small voltage difference in the Si bottom cell, which was nominally the same for both devices, might be explained by a small scratch on the rear side of the cell and by measuring uncertainty. The subcell voltage analysis was performed on another cell of the record wafer, X633-6, which exhibited the same open-circuit voltage as the record device, X633-7, in order to save the record device from potential damage during the EL measurement process.

3.3 | Comparison between upright and inverted grown solar cells

It was shown above that the improved middle cell absorber material of the upright grown triple-junction solar cell was the key factor to push the efficiency to 35.9 %. As for the inverted grown structure with the same layer stack, the maximum obtained efficiency amounted to only 34.5 % despite of a higher fill factor of 86.3 % compared to 84.3 % for the upright grown device. The main reason for the weaker performance of the inverted grown device is the increased thermal load that the top junction experiences. In previous experiments with rear-heterojunction GaInP component cells, a decrease in open-circuit voltage and in short-circuit current density were observed if the cell was kept for another 45 min at growth temperature inside the MOVPE reactor. This deterioration is related to diffusion processes of Zn atoms from the higher doped back-surface field into the space-charge region as secondary ion mass spectroscopy (SIMS) profiles have revealed experimentally. Layers with a higher phosphide content are more strongly affected by this process.[39] Therefore, if the growth direction is reversed and the GaInP junction is grown last, the detrimental effect of the temperature-induced diffusion processes is less severe.

Due to the more complex processing chain of the upright route, which included additional steps such as the temporary bond to a sapphire wafer, the demands on the homogeneity of each process step are higher. As can be seen in the lower part of Figure 8, the distribution of open-circuit voltages of all 12 large solar cells on the wafer has a wider spread for the upright grown structure, yet with a 70 mV higher median value, than for the inverted grown structure. Subcell voltage measurements suggest 35 mV of the voltage loss to the GaInP top cell as expected from the single-junction experiments.

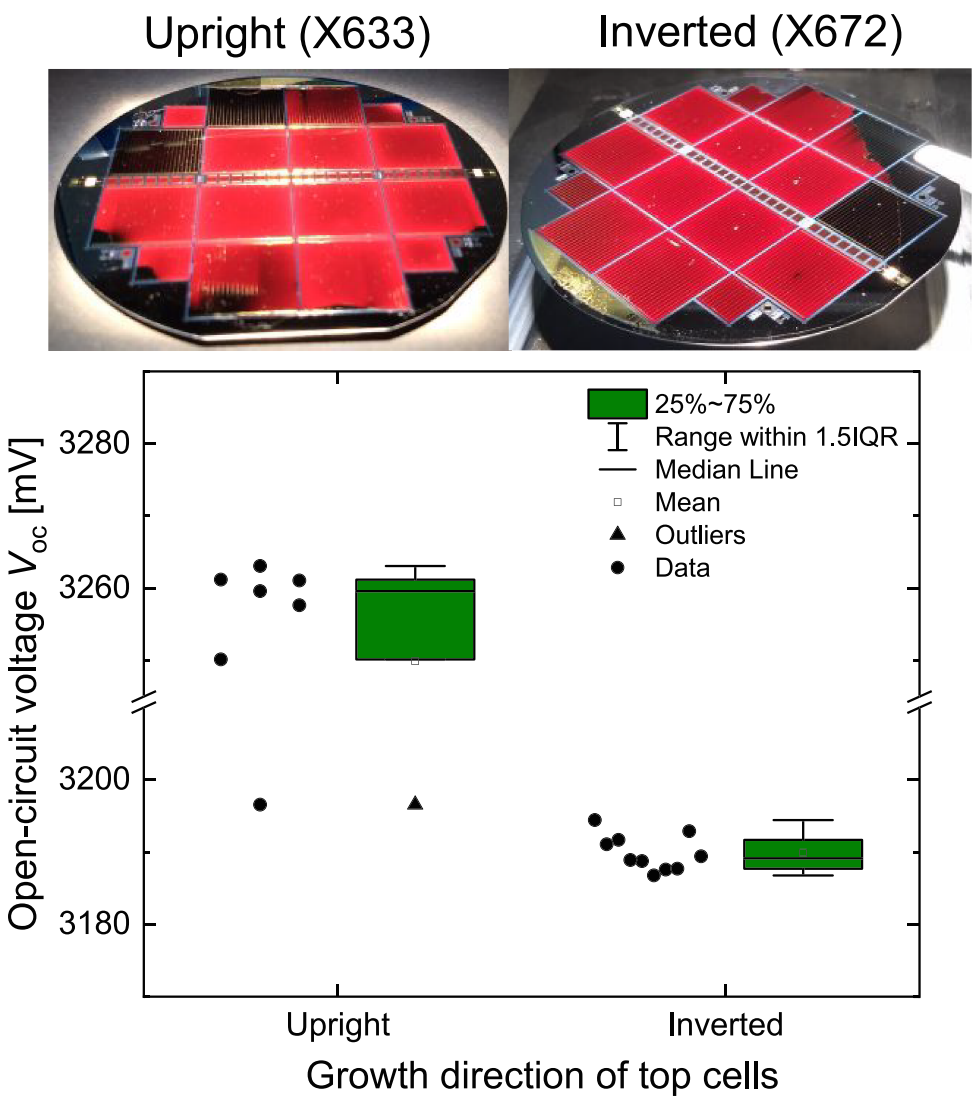

FIGURE 8 Top: Photograph of the wafer X633 with the upright grown record cell structure (left) and of the wafer X672 with the inverted grown cell structure (right). Under white light illumination, the GaInP top junction emits visible red light where the wafer was not harmed during the processing. This is a sign of high external radiative efficiency and thus high material quality. Bottom: Open-circuit voltage of all working cells on the wafers. This measurement was conducted under an uncalibrated AM1.5g spectrum resulting in slightly higher voltages for all cells than for the calibrated measurement shown in Figure 6. The box plots next to the data points indicate the mean (open point), the median (horizontal line), the central quartiles (green box), the 1.5 interquartile range (IQR, whiskers) and outliers (triangle)

The other 35 mV are caused by a decreased subcell voltage in the GaInAsP middle junction whose origin requires further investigation. Two possible reasons could be an epitaxial interface problem inside the GaInAsP layer structure, which is sensitive to the growth direction, or process fluctuations of the MOVPE reactor. Besides, the additional bonding and debonding steps increase the risk of complete destruction of single cells on the wafer, especially around the edges. This manifests itself in the dark cell areas that can be seen in the photographs of illuminated wafers in the upper part of Figure 8. Only seven cells (58 %) for the case of upright growth while 11 cells (92 %) for the case of inverted growth exhibited a measurable open-circuit voltage. Hence, the achieved efficiencies are higher for the upright route but at the cost of a reduced yield of functioning cells per wafer.

3.4 | Comparison to other champion devices

The presented III–V//Si triple-junction device is limited in its performance by the bandgap constraint of the Si bottom cell. In Figure 9, the consequences of this constraint are shown by a comparison of the device performance to an inverted metamorphic GaInP/GaAs/InGaAs triple-junction (IMM3J) solar cell from SHARP Corporation.[40] This cell exhibits the highest conversion efficiency of all triple-junction solar cell concepts under AM1.5g, that is, without concentration. Thanks to the flexibility in choosing the bottom cell absorber material freely, the optimum bandgap combination could be implemented to within 50 meV for each subcell. This enabled a better utilisation of the solar spectrum. As a consequence, the short-circuit current density is higher by 1.2 mA/cm^2. The lower bandgap bottom cell absorber requires to also reduce the bandgaps of the top and middle junction and to make these absorbers thicker. This, however, reduces the potential energies of the generated charge carriers. What is more, the metamorphic buffer between the GaAs middle cell and the InGaAs bottom cell introduces threading dislocation defects. These act as nonradiative recombination centres reducing the voltage. On the other hand, the difference between the sum of the bandgaps and the open-circuit voltage $W_{oc,tot} = \sum_i E_{g,i} - V_{oc}$ is higher by 30 mV for the wafer-bonded case. In the radiative limit the bandgap-voltage

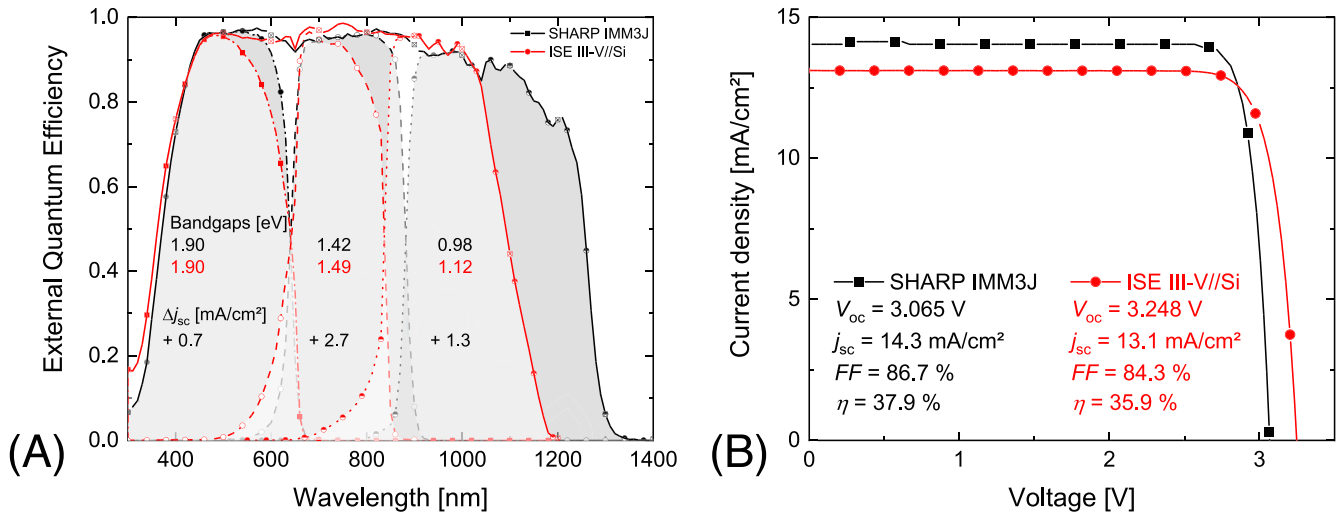

FIGURE 9 (A) External quantum efficiency and (B) current–voltage characteristics of the record inverted metamorphic triple junction (IMM3J) by SHARP[40] (black, squares) compared to the presented III–V//Si solar cell (red, circles). In the insets of the left diagram, the bandgaps and the difference in short-circuit current density of each subcell are given. The grey shaded areas indicate the advantage in photocurrent generation. The sum of the subcell EQEs is shown with a solid line. The external quantum efficiencies of the subcells were scaled according to the calibrated AM1.5g short-circuit current density from the *IV* characteristics

offset $W_{oc,rad}$ increases by 11 meV between 0.98 and 1.12 eV and by 5 meV between 1.42 and 1.49 eV. Due to the high minority carrier diffusion length in the indirect semiconductor silicon, recombination at the edge of the cell is nonnegligible. Simulations have shown that mesa trench passivation could improve the open-circuit voltage by around 40 meV.[41] Hence, the effective material and interface quality and thus the voltage potential are slightly higher in the GaInP/GaInAsP//Si device. In total, the open-circuit voltage is higher by 183 mV compared to the IMM3J.

Given the agreement of the absolute height of the EQE in the areas without absorption limitation, that is, in the short-wavelength part of each junction peak, there is little opportunity for improvement of the III–V//Si device in terms of current. However, the voltage benefit could still be further exploited if the loss to the radiative limit in each subcell is further reduced, the top cell bandgap is increased, and additionally, the mesa trenches are passivated which will be implemented in a future batch. If a constant current density and the fill factor of the IMM3J are assumed, then a voltage increase of 86 mV would suffice for equal efficiency as the IMM3J, which is realistic with the improvements mentioned above.

4 | CONCLUSION

We have shown how the efficiency potential of silicon-based multijunction solar cells can be further exploited. By choosing III–V semiconductor materials that can be deposited with a high crystal quality at the right bandgap and by improving the MOVPE growth conditions for these materials, we were able to present a two-terminal wafer-bonded triple-junction solar cell which sets a new efficiency record with 35.9 % under an AM1.5g spectrum. In particular, the employment of a GaInAsP middle junction resulted in a significant voltage gain. Two growth directions, upright and inverted, were evaluated. High efficiencies of 34.5 % along with a reliably high yield of equally well-performing cells per wafer can be achieved with inverted grown top cells that are directly bonded to a silicon bottom cell. The highest efficiencies with a slightly less uniform performance on a wafer could be realised with upright grown top cells that had to be processed with an additional temporary bonding step. If the degradation of the top cell can be solved, for instance, by lower growth temperatures or different p-type doping agents, the inverted route would be the preferred alternative due to the simpler processing and the higher yield.

It was demonstrated that a monolithic, two-terminal silicon-based multijunction can achieve at least the same efficiency as the currently best performing four-terminal device with 35.9 %.[11] No separate interconnection of the mechanically stacked subcells is required for the two-terminal configuration as it is the case for the four-terminal configuration. Hence, installation costs of modules made from such cells are lower. If the costs can be reduced in the future, the presented results may therefore increase the market entrance chances for III–V//Si solar cells. Life-cycle analyses have shown that the III–V//Si technology has the potential to be comparable or even superior in environmental impact compared to single-junction silicon solar cells of today.[42]

From comparing this cell to the currently best triple-junction device, we found that despite the nonoptimum bandgap combination, the silicon-based cell compares well with the best-in-class device in terms of voltage even after the different bandgaps are considered. The current can likely not be improved much further with a Si bottom cell because of the constant transmission losses at photon energies below 1.12 eV. There is still some room for improving the subcell

absorbers, though, for example, by increasing the top cell bandgap and thus voltage with the use of AlGaInP, integrating a rear-heterojunction into the middle cell, and passivating the mesa trenches to reduce edge recombination losses in the silicon bottom cell.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

ORCID

Patrick Schygulla https://orcid.org/0000-0001-9103-1045
Ralph Müller https://orcid.org/0000-0001-6248-3659
David Lackner https://orcid.org/0000-0001-8170-0874
Oliver Höhn https://orcid.org/0000-0002-5991-2878
Benedikt Bläsi https://orcid.org/0000-0003-1624-1530
Felix Predan https://orcid.org/0000-0002-8735-9109
Jan Benick https://orcid.org/0000-0002-9433-1171
Stefan W. Glunz https://orcid.org/0000-0002-9877-2097
Frank Dimroth https://orcid.org/0000-0002-3615-4437

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