Failure Mechanism Detection Algorithm with MOSFET Body Diode

Mohamad El Khatib, Sven Reitz, Jens Warmuth
Fraunhofer Institute for Integrated Circuits IIS
Division Engineering of Adaptive Systems EAS, Zeunerstraße 38, 01069 Dresden
mohamad.el-khatib@eas.iis.fraunhofer.de

Abstract

Autonomous driving is playing a big role in the automotive industry and defines the future of mobility on a big scale. However, autonomous driving faces several challenges, such as the performance of artificial intelligence and hardware reliability. To ensure safe functionality, the reliability of the electronic components plays an essential role and must be taken into consideration. One aspect of studies that analyze the electronics reliability is the observation of the system's thermal impedance and deriving a correlation between the failure mechanisms and thermal impedance behavior. In recent times, several new approaches have been suggested to improve the electronics reliability. Many studies were carried out to determine the effect of solder voiding on the thermal impedance of chip-level packages. In this paper, a defect diagnosis and physical damage detection method for electronic packaging are studied by measuring the thermal impedance through the body diode of the device under test (DUT). The detection method uses MOSFET body diode temperature measurements to investigate different failure mechanisms at different locations in the electronic packaging system.

1. Introduction

Power MOSFETs are used in various automotive medium and high voltage applications. Nevertheless, robustness and reliability remain a main issue for MOSFET application and much research has been published to find methods for improving the electronics reliability. Generally, electronic components experience thermal cycles and other stresses during service. This reduces the lifetime of the components and leads to electrical malfunctions and physical damages that can affect the performance of the electronic and cause failures. So far research investigates the effect of the failure mechanisms on the mechanical, thermal and electrical properties [1]. The thermal impedance Zth in the MOSFET is determined using a temperature sensitive parameter. It can be obtained by measuring the voltage of the body diode between drain and source or the drain-source on-state resistance (RDSon) or the threshold voltage when the MOSFET starts to conduct [2]. This paper uses the body diode forward voltage to investigate the damages that occur frequently in the system like die attach voids, cracking mold and solder fatigue [5]. The aim of this research is firstly to check if the investigated failure mechanism in the package can be detected by the MOSFET body diode temperature measurement. Secondly, to introduce a detection algorithm able to analyze the thermal impedance and detect damage if it occurs. The first part of the study is measuring the cooling curve of the system using the body diode. For this purpose, test boards equipped with multiple discretely packaged transistors are tested. The experimental measurement in this study investigates the thermal impedance of packages with solder damages. Other failure mechanisms are simulated using the Finite Element Method (FEM). The simulation results designating the thermal impedance Zth of the package are used to develop the detection algorithm based on the structure-function. The detection method at the end is tested with the experimental body diode measurement data.

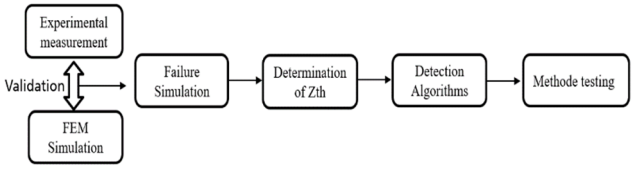

Figure 1: Progressive sequence steps of the study

2. Methodology

The work flow starts in this paper by measuring the thermal impedance Zth experimentally using the body diode of the transistor. The second part presents the simulation results of the Zth for the same model including different failure mechanism at different location. Finally, the developed detection method is tested based on the simulation data. The investigated modules in this paper on the test board are identical and contain the same transistor. The only difference is the soldering between PCB and the chip carrier. Figure 2 shows a computed tomography (CT) scan image of the solder layer for different modules on the same test board. The module A is designated as reference module with no damages. The area inside the red rectangle in Figure 2 shows where the solder voids are located. Module B and C refer to module with solder void damages. Module B has four soldering pads uncoated. Module C has three pads uncoated at the right side. This image allows to check the real solder partition in the solder layer as well as the solder thickness and copper via filling.

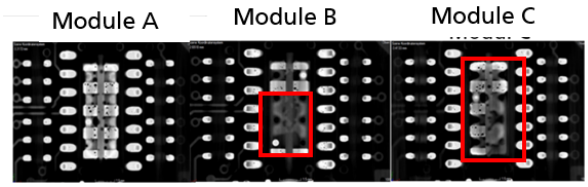

Figure 2: CT scan of the solder layer for different modules on the same test board (Source: HELLA GmbH & Co. KGaA)

The investigated MOSFET on each module is an N-channel smart power switch with 60 mΩ RDSon value, embedded in an exposed pad package. It is specially designed to drive valve applications in the automotive environment. In order to determine the temperature measurement of the body diode, the K-factor which relates temperature to the measured voltage needs to be determined. Therefore, the transistor is placed in a climatic test chamber and the body diode voltage is measured by applying a negative drain current of 100 µA. Figure 3 shows the voltage measurement of the body diode in module A at different temperatures. The K-factor of -2.10 mV/K.

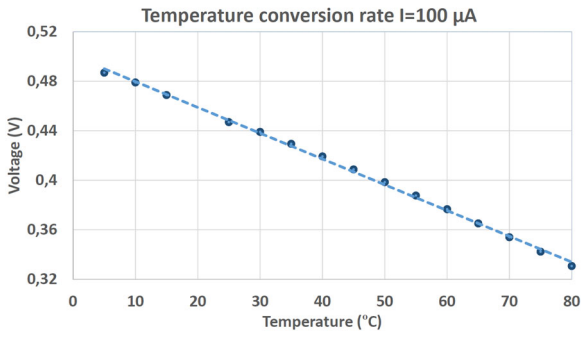

Figure 3: Body diode temperature conversion curve

With respect to MOSFET structure, the body diode is formed by the PN junction between the source and drain polarized toward the drain as indicated in Figure 4. In order to activate the body diode of the MOSFET it needs to be operated with a reverse low current from source port to the drain port of the transistor while no gate voltage is applied. In this case, the transistor channel does not conduct, and the body diode is the only part that can conduct. Figure 4 shows that at the time when the body diode conducts the gate voltage is switched off. In consequence, the body diode is only able to track the temperature of the system by measuring the "cooling curve" of the device after switching off the transistor.

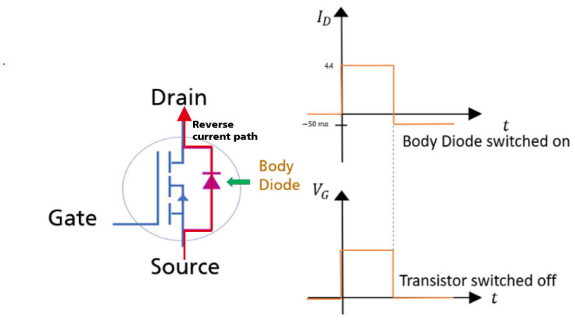

Figure 4: Body diode of a transistor

In order to perform the measurement, the transistor is operated in the saturated region with a constant drain current flow for 100 s. This operating time is sufficient to ensure that steady state is reached. After reaching the steady state in the heating phase, the transistor is switched off and the body diode measurement is activated for 1000 s until the cooling temperature reaches the steady state at room temperature. The following Figure 5 shows the experimental result of the body diode measurement in logarithmic time scale for module A presented in Figure 2.

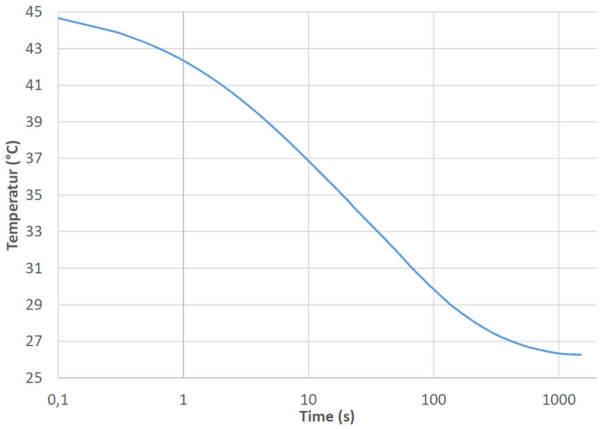

Figure 5: Experimental measurement of the cooling curve by the body diode

The following section introduces the FE simulation. The FE model computes transient thermal simulation for the damages at different locations in the same module of the test board. To ensure accurate and reliable results, the FE model is a geometrical model based on the nominal design and modified to correspond with CT images regarding the solder layer thickness and void size which enhances the accuracy of the simulation result. The test board contains 6 modules in total. The FE model does not include the whole test board but includes only the actual module, i.e. chip, package and the board directly beneath it, with 20 mm x 20 mm dimension as presented in Figure 6.

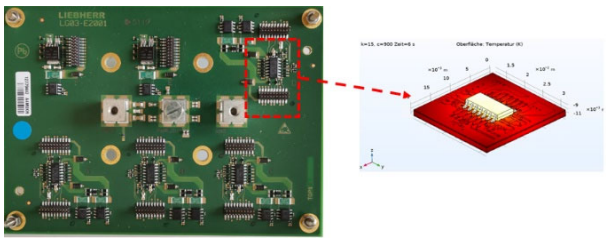

Figure 6: Test board and package in FEM modeling

The simulation shows the heat transfer behavior of the overall system. The temperature is measured in the middle of the active layer on the die top surface as shown in Figure 7 and the simulation's boundary conditions are set up to be the same as in the experimental measurement.

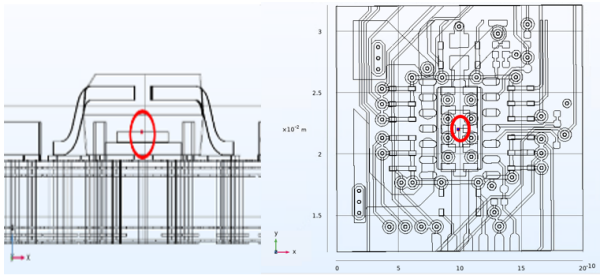

Figure 7: Body diode position inside the package

The thermal step-response, known as "transient response", reveals the junction temperature modification after a sudden step-change in internal power dissipation. The thermal step response is defined as the "cooling curve" when the step-change is switching off the internal power dissipation till it reaches the steady-state at the ambient temperature.

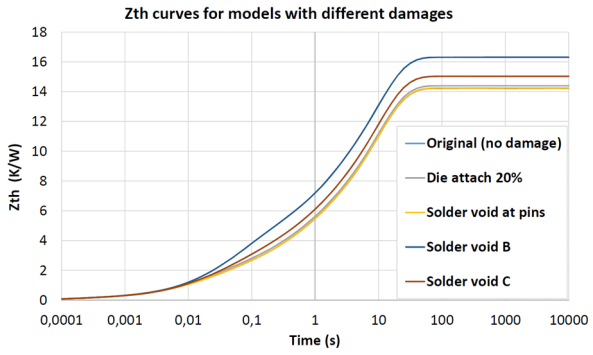

Figure 8: Zth curves for models with different damages

Figure 8 shows the FEM thermal transient simulation result for models with investigated damages. The package model is simulated with logarithmic time steps with constant power loss of 1 Watt until it reaches the steady state at 100 seconds. The simulation shows differences between curves in the steady state region. Model B and C, containing the solder voids corresponding to module B and C (see Figure 2), are the most remarkable and the curves deviate from the no damage model with 2.2 K/W and 0.9 K/W at steady state respectively. The Zth curves for the die attach voids model and the model with solder damage at the pins do not deviate much (barely visible in the figure) from the original curve since the damage location at the pins is far from the active area of the die and not in the main heat flow path. The die attach void is not large enough to be detected in the Zth curve. In the next section, these results are implemented in the detection method and the damages are detected using the structure function method described.

Thermal resistance, junction-to-case (JC), by definition is the thermal resistance from the operating portion of a semiconductor device to the outside surface of the package (case) [3]. The most common method to represent the Zth-JC is the structure function of one-dimensional heat-flow through a layered structure. The thermal impedance of a semiconductor device shall be defined as [3]:

$$Z_{th} = \frac{T_J - T_C}{P} \quad (1)$$

where T_J is the junction temperature, T_C is the reference or case temperature and P is the power loss. By setting the power loss to 1 Watt, Zth is equal to the difference between junction temperature and case (in this instance the same as ambient) temperature.

The next section of the study introduces the cumulative structure function method used for detection. In the early paper of Protonotarios and Wing [6] the structure function is introduced to describe non-uniform RC line. This function presents the cumulative thermal capacitance C as the function of the cumulative thermal resistance R. Therefore it is necessary to generate the RC networks known as Foster and Cauer Model. The thermal impedance (Zth curve) is also called unit step response a(t) mentioned by V. Székely [4] and equal to:

$$a(t) = \int_0^\infty R(\tau)(1 - \exp(-t/\tau))\, d\tau \quad (2)$$

where R(τ) is the time-constant spectrum, t is the time in logarithmic scale and τ=RC is the time constant where R represents the thermal resistance and C the thermal capacitance of the unit step response at time t. It is proved in a previous paper from V. Székely [5] that the R(z) time-constant spectrum and the unit-step thermal response function (the Zth curve) can be written as the following:

$$\frac{d}{dz}a(z) = R(z) \otimes w(z) \quad (3)$$

With $\frac{d}{dz}a(z)$ is the derivative of the unit step response where z=ln(t) and R(z) is the time constant spectrum and "⊗" is the convolution operator and w(z) is the weighting function defined as:

$$w(z) = \exp(z - \exp(z)) \quad (4)$$

From equation 3 the time-constant spectrum R(z) can be computed by deconvolution of the time derivative $\frac{d}{dz}a(z)$ with the function w(z) and can be written as

$$R(z) = [\frac{d}{dz}a(z)] \otimes^{-1} w(z) \quad (5)$$

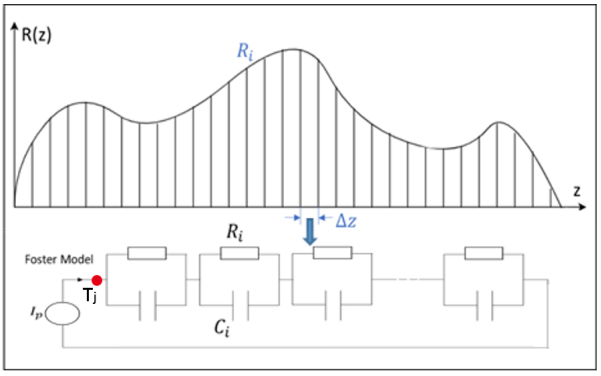

Figure 9: The time constant spectrum and the equivalent Foster model

The discretization of the time-constant spectrum R(z) with Δz obtains a thermal equivalent Foster model [3] is shown in Figure 9. The higher the number of Δz in the discretization is the better the resolution of the structure function becomes. The R(z) function is split into a number of segments having Δz width. Each RC stage in the circuit corresponds to one Δz segment of the time-constant spectrum.

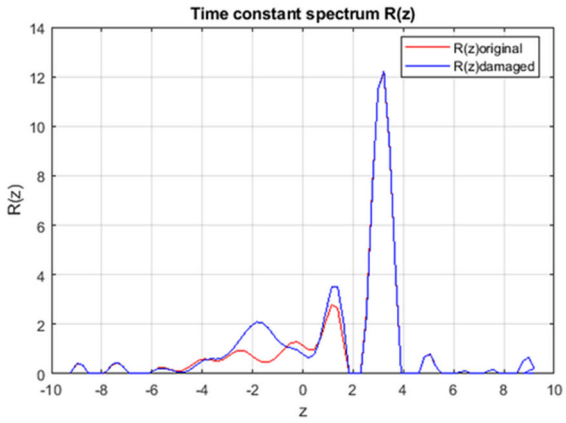

Figure 10: Time constant spectrum for 2 models

Figure 10 shows the time constant spectrum for two models based on the Zth of the simulation results. The red curve corresponds to module A with no damage and the blue curve corresponds to module B with solder void damage. From the graph in Figure 10, there is some difference between the two curves of the R(z) which leads by discretization of the R(z) to different value of RC stages in Foster models. In this paper the number of Δz is set to 80 which yields to 80 numbers of RC stages in the Foster model. The resulting Foster model must be validated with the simulation result before applying the Cauer transformation and later the cumulative structure function. Henceforward the Foster model is simulated in LTspice for electrical circuit simulation and the result is compared with the Zth curve used as the unit step response in equation 2. Figure 11 shows the result of the validation.

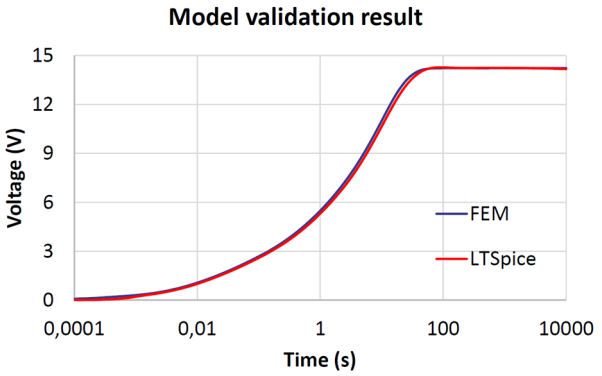

Figure 11: Validation graph for the Zth curve and voltage curve

In order to realize the simulation in LTspice, the Foster circuit is connected to an electrical current source of one Ampere. This current source is analogous to the 1 Watt of power dissipation in thermal simulation. Figure 11 shows the voltage curve analogous to the temperature for the thermal transient simulation. After 100 s of time the voltage remains constant and the steady state is reached. The voltage measured at node T_J (Figure 9) contains the information regarding the junction temperature and can be compared with T_J obtained in the FEM simulation. The voltage curve in LTspice almost fits the Zth curve and reaches the same maximum of 14 V at the steady state region. The Foster model validation confirms that the RC network shows the thermal transient behavior of the system but it's still not ready to give any information about the physical structure of the package. The thermal resistance is related always to the temperature difference between a single RC ladder between two nodes and not to one single node connected to ground. Since the Foster model has node to node capacitance connection as shown in Figure 9, the voltage measurement at a node between two ladders in the circuit cannot be correlated with the T_J of a physical region in the package and the structure function cannot show the thermal characteristics of the structure. Therefore, the Foster model has to be converted to the Cauer model. The Cauer RC model keeps the same thermal device performance of the Foster model but the thermal capacitance are all connected to the thermal ground referring to the ambient temperature. Therefore it can be used for the characterization of the thermal structure. The cumulative structure functions of the models A, B and C are shown in Figure 12.

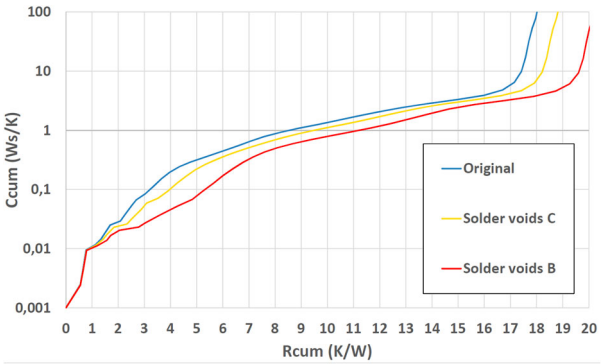

Figure 12: Structure function diagram for the investigated models

It can be seen that the curves for Model C and for Model B respectively start to deviate from the original model A with no damage at 1.2 K/W thermal resistance. The deviation is more significant for module B and shows less thermal capacitance since it has more voids at the solder level. For the other simulated damage models shown in Figure 8, the cumulative structure function is also obtained for each model. Figure 13 shows 2 graphs comparing structure function curves of the models with damage to the original model with no damage.

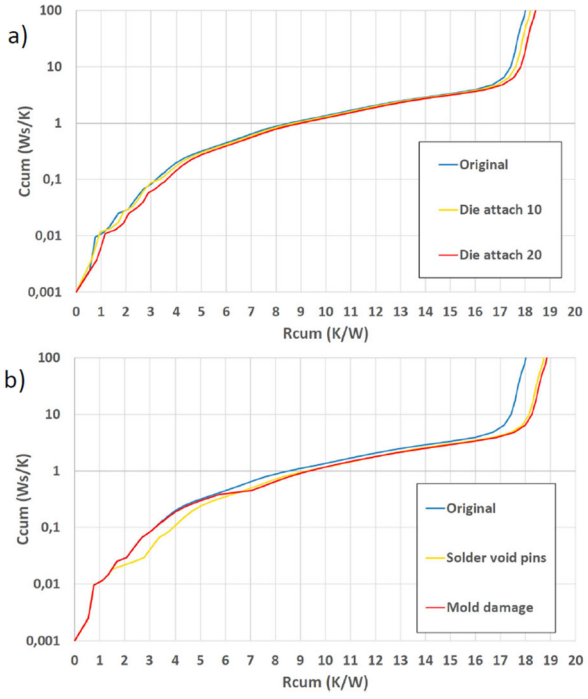

Figure 13: Structure function diagram for the investigated models

The graph (a) corresponds to the model with die attach voids, the blue curve corresponds to the original with no damage. The others curves represent the die attach 10% void in yellow and die attach 20% void in red. The yellow curve deviates at 0.1 K/W thermal resistance but is not well distinguished from the original one. The curve in red deviates almost at the same location but with more significant thermal resistance difference of 0.4 K/W. In graph (b) the yellow curve corresponds to the model with solder damage at pins at both sides of the package. The curve deviates at approximately 1.7 K/W thermal resistance and has a distinct change in slope at 2.2 K/W. This is due to the damage modeling where different damages where placed at different locations for this model. The red curve corresponds to the model with simulated mold damage. It is well detectable with a significant deviation at 7 K/W. The structure function confirms that the simulated damages and the formation of voids at different location in the package is the reason for the curve shifting in the structure function curves.

3. Conclusion

A reliable detection concept based on the transient thermal analysis depends on the accuracy of the body diode measurement and on the applied method's limitations in processing the thermal impedance into the structure function. The body diode as a temperature sensor is able to detect variations in the Zth for solder voids damage experimentally. The detection of damages are so far based on simulation result and laboratory measurements. In order to implement this method on board and in real application, it is necessary to investigate more failure mechanisms experimentally with the body diode measurement under real application conditions. However, it is also necessary to confirm the feasibility of this method with microcontroller performance for integration purposes. The next step in the research will focus on real application testing and investigate the ability of the body diode to experimentally detect different damages in the packaging.

Acknowledgments

This work was partly funded by the German Federal Ministry of Education and Research within the project *Thermische On-Board Spektroskopie für autonome Elektrofahrzeuge* (ThermOBS/16EMO0367K).

References

1. P. Singh, "Power MOSFET failure mechanisms," INTELEC 2004. 26th Annual International Telecommunications Energy Conference, Chicago, IL, USA, 2004, pp. 499-502, 10.1109/INTLEC.2004.1401515.
2. F. Kato, S. Sato, K. Koui, H. Tanisawa, H. Hozoji and H. Yamaguchi, "Study of Gate Bias Voltage for Preventing Threshold Shift of SiC–MOSFET Body Diode during Transient Temperature Measurements," 2019

International Conference on Electronics Packaging (ICEP), Niigata, Japan, 2019, pp. 88-91,

3. “Transient Dual Interface Test method or the measurement of the thermal Resistance Junction to Case of Semiconductor Devices with heat flow through a Single Path”, EIA / JEDEC Standard, JESD51-14, updated at 10.2010 [www.jedec.org].
4. V. Székely, Tran van Bien: "Fine structure of heat flow path in semiconductor devices: measurement and identification method", Solid-State Electronics 31(9): 1363-1368 (1988)
5. V. Székely: "Distributed RC networks" In: Wai-Kai Chen (ed.): The Circuits and Filters Handbook, Boca Raton: CRC Press Inc., 2003. pp. 1201-1222. (The electrical engineering handbook series) ISBN:0-8493-0912-3
6. E. N. Protonotarios and O. Wing, "Theory of Nonuniform RC Lines, Part II: Analytic Properties in the Time Domain," in IEEE Transactions on Circuit Theory, vol. 14, no. 1, pp. 13-20, March 1967.