Dielectric layers suitable for high voltage integrated trench capacitors

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In this work, two different dielectric stacks consisting of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) are analyzed regarding their suitability as dielectrics in a high voltage trench capacitor. The processing of the dielectric layers and the resulting edge-coverage in the trench holes are described. Voltage and temperature dependence of the trench capacitance are analyzed and compared with planar capacitors for reference. The leakage currents are measured and the current transport mechanisms are analyzed. The outstanding properties of the devices are a high capacitance per area (1.25 nF/mm^2 for SiO_2 and 1.5 nF/mm^2 for Si_3N_4), a low temperature coefficient (SiO_2: 18 ppm/K; Si_3N_4: 85 ppm/K from 25–100 °C), and a low leakage current ($<1\times10^{-6}$ A) for voltages up to 400 V for Si_3N_4. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3525283]

I. INTRODUCTION

For the realization of future smart power modules and systems, it becomes more and more important to integrate passive devices that can cope with the additional requirements of advanced power systems. Especially, the reduction in geometric dimensions and the capability to cover a wide temperature range are important aspects for those devices.[1] Additionally, the passive devices have to be applicable for high voltages, too. Nowadays, passive high power devices like capacitors are typically implemented as discrete components. Integrated solutions, which have to achieve high capacitance per area, such as trench capacitors used as integrated rf-capacitors[2] or dynamic random access memory cell capacitors,[3] are only implemented for logic-type voltage levels (approximately 5 V). Integrated solutions for applications in the voltage range of several hundred volts are not available. In this work, the processing and the electrical behavior of dielectric layers suitable for high voltage integrated trench capacitors are discussed.

II. DEVICE AND PROCESS DESCRIPTION

A. Device structure

There are three possibilities to maximize the capacitance per required silicon area. One is to reduce the thickness of the dielectric layer, the second is to use high-k dielectric layers, and the third is to enlarge the capacitor area via three-dimensional structuring of the silicon surface while keeping the required silicon area constant. For power device applications, besides a high capacitance per area, the endurance under high voltages is an important characteristic. Therefore, the minimum thickness of the dielectric layer is restricted by the requirement to withstand high voltages. To fulfill the demands for high capacitance per area, the enlargement of the capacitor area by circular trench holes, which are formed by anisotropic dry etching, has been pursued in this work.

The schematic device structure of a trench capacitor applicable for high voltages is depicted in Fig. 1(a). The dielectric layer is situated directly underneath the top electrode covering the surface of the silicon. The silicon surface and, therefore, the capacitor area are enlarged by regularly arranged deep trench holes. The patterned silicon wafer surface forms the bottom electrode of the capacitor. The bottom contact of the device is located at the backside of the silicon wafer, and, therefore, the silicon substrate is the dominant factor that defines the serial resistance of the capacitor. Figure 1(b) shows a top view of the trench capacitor mask, which was used to form the trenches. A hexagonal arrangement of the circular trench holes is used, and the essential geometry parameters are diameter d and distance a. In this work, capacitors with trench hole diameters d from 2 to 2.5 μm and distances a between the trench holes of 3 and 3.5 μm have been formed. The characterized device types and the corresponding labeling for the various types are shown in Table I. The required silicon wafer area A_{Si} of the devices are 1, 12.5, and 25 mm^2. Planar capacitors with identical silicon wafer areas were produced in addition to the trench hole capacitors.

B. Process technology

Manufacturing of the trench capacitors was done based on complementary metal-oxide semiconductor processing. A simplified process flow is depicted in Figs. 2(a)–2(h). First, a 20 nm silicon dioxide (SiO_2) layer is thermally grown on the cleaned 150 mm p-doped ($N_A\approx1.3\times10^{-15}$ cm^{-3}) silicon

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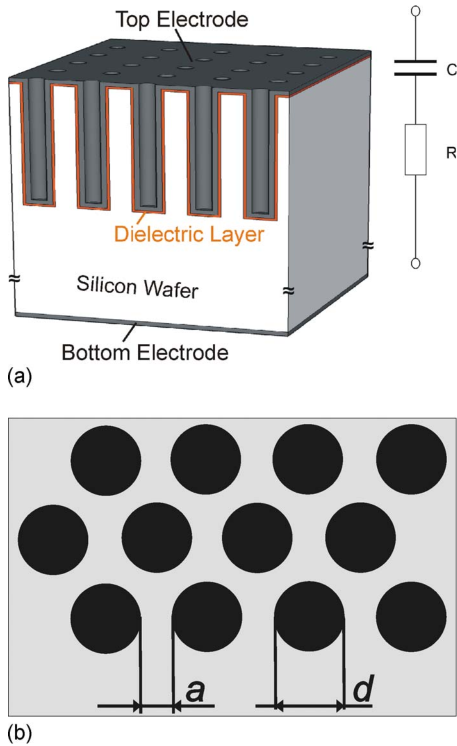


FIG. 1. (Color online) (a) Schematic device structure of the integrated trench capacitor suitable for high voltages and (b) top view sector of the hexagonal arranged circular trench holes of the mask.

TABLE I. Geometrical parameters of characterized device types and labeling.

Nominal hole diameter (μm)	Nominal distance	
	3 μm	3.5 μm
2	d2a3	d2a3.5
2.25	d2.25a3	d2.25a3.5
2.5	d2.5a3	d2.5a3.5

wafer, and the backside is highly *p*-doped by ion implantation to form a good Ohmic contact [Fig. 2(a)]. Then, the trench hole positions are defined by lithography [Fig. 2(b)]. Next, the trench holes are etched with a depth of about 31 μm using the advanced silicon etch process, which is a derivate of the Bosch process[4] [Fig. 2(c)]. Subsequently, the photoresist and the 20 nm SiO_2 layer are removed [Fig. 2(d)]. Next, the insulators for the metal insulator semiconductor capacitors are formed. For one part of the wafers (split A), the dielectric stack consists of 400 nm of SiO_2 grown by wet thermal oxidation. The other part of the wafers (split B) received a dielectric stack consisting of 20 nm thick SiO_2 grown by dry thermal oxidation and a 500 nm thick layer of silicon nitride (Si_3N_4), which is deposited by low pressure chemical vapor deposition (LPCVD) [Fig. 2(e)]. The top electrode is formed by deposition of polysilicon using LPCVD and subsequent doping by a thermal treatment in phosphoryl chloride ($POCl_3$) atmosphere. On top of this, aluminum is deposited and the whole top electrode is patterned by a second mask layer that defines the area of the devices [Fig. 2(f)]. Next, the processed layers are removed from the backside of the wafer to expose the highly *p*-doped silicon [Fig. 2(g)], and the bottom electrode metallization is deposited by physical vapor deposition [Fig. 2(h)]. Finally, the wafers were forming gas annealed (FGA) at 430 °C for 30 min.

In Figs. 3(a)–3(d), scanning electron microscope (SEM) images of cross sections of manufactured devices for the two process splits (A and B) are depicted. Figures 3(a) and 3(c) show the thermal oxide thickness at the top and at the bottom of a trench hole. At the top, the layer thickness of the SiO_2 is higher than the nominal 400 nm. Particularly, at the edges, however, the layer thickness is reduced down to 300 nm. The thinnest spot is located at the lower concave edge of the trench hole. The conformity for the SiO_2 layer is 70%. The origin of the layer thickness reduction especially at concave edges can be explained by a retardation of the oxidation, which is caused by a geometry effect and stress caused by a

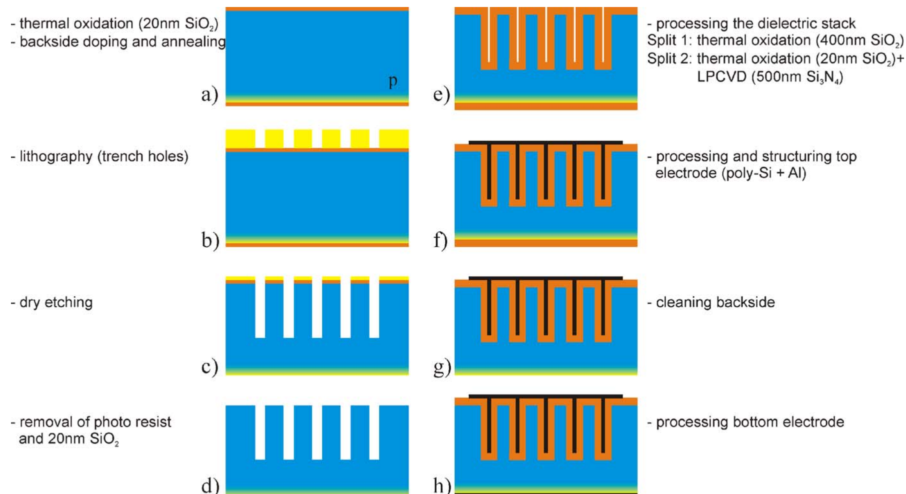


FIG. 2. (Color online) Simplified process flow for a trench capacitor.

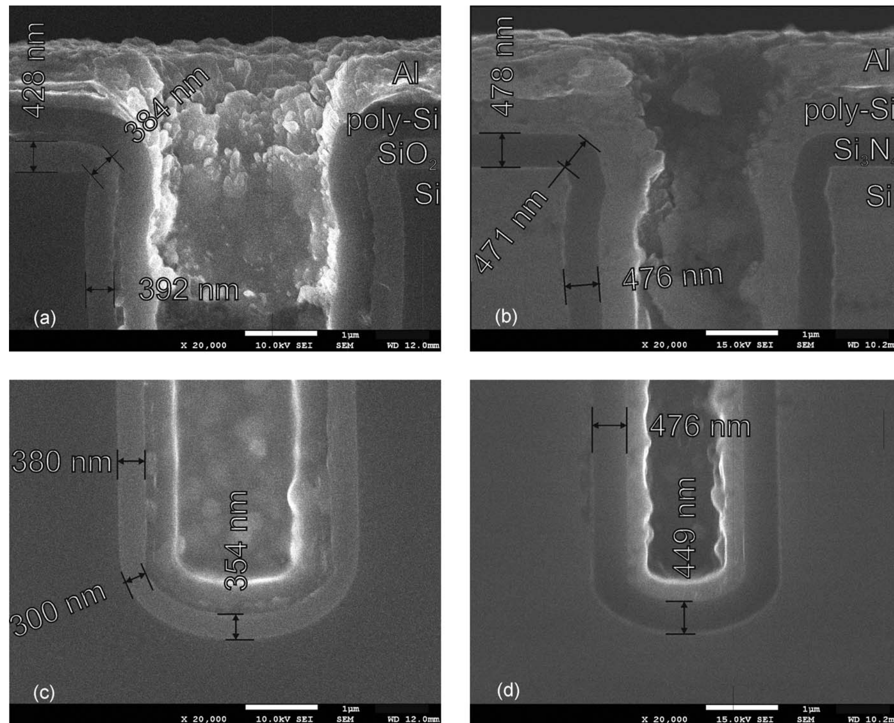


FIG. 3. SEM image of (a) thermal oxide in trench at the top, (b) LPCVD deposition of Si_3N_4 in trench at the top, (c) thermal oxide in trench at the bottom, and (d) LPCVD deposition of Si_3N_4 in trench at the bottom.

volume expansion in elastic SiO_2 during the thermal oxidation. Similar results for oxidation in circular trenches were reported and described by Kao *et al.*[5,6] and Xu *et al.*[7] Figures 3(b) and 3(d) show the deposited Si_3N_4 at the top and at the bottom of the trench hole. The conformity of the deposited Si_3N_4 is 93% and therefore significantly better than that of the SiO_2. Especially, the coverage of the concave edges at the bottom of the trench holes for the deposited Si_3N_4 is clearly better than that for the thermally grown SiO_2.

III. DEVICE CHARACTERISTICS

A. Capacitance-voltage measurements

To analyze the impact of the voltage on the capacitance, capacitance-voltage (C-V) measurements were performed using an HP 4277 LCZ-meter at a frequency of 1 MHz and a test signal level of 1 V_{rms} (root mean square, effective value of the oscillation voltage) applying a dc voltage from −40 to 40 V at room temperature. Figure 4(a) shows the results of the C-V-measurements for SiO_2 capacitors with trench hole diameters d from 2 to 2.5 μm, a hole distance a of 3 and 3.5 μm and a needed silicon area A of 25 mm^2. It can be seen that the capacitors with a trench hole diameter of 2.5 μm and a hole distance of 3 μm show the highest capacitance. The flatband voltage V_{fb} is approximately −2.6 to −2.1 V for all analyzed geometries. In Fig. 4(b), the results of C-V-measurements on Si_3N_4 capacitors with geometry variations identical to the SiO_2 capacitors described above are depicted. Again, the capacitor with the largest diameter (d=2.5 μm) and the smallest distance between the holes (a=3 μm) exhibits the highest capacitance. The flatband

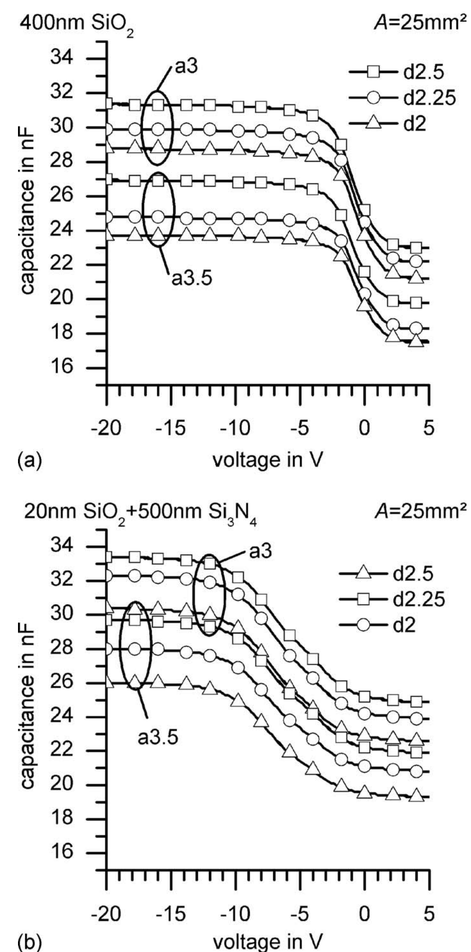


FIG. 4. C-V-curves (a) for SiO_2 capacitors and (b) for Si_3N_4 capacitors with various geometry parameters.

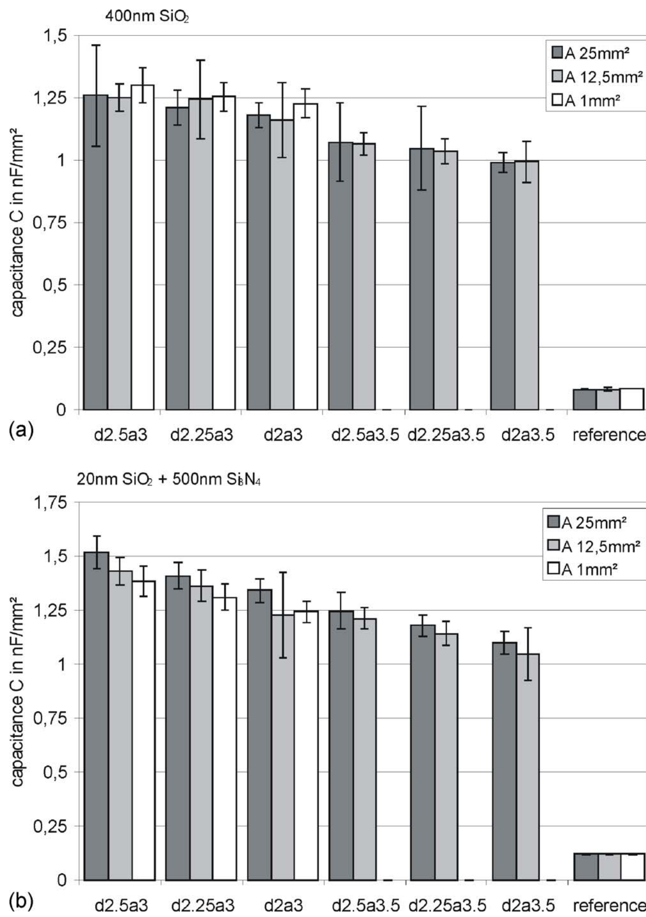


FIG. 5. (Color online) (a) Capacitance per area for SiO_2 capacitors and (b) for Si_3N_4 capacitors with various geometry parameters. Enlargement of the capacitance for the trench devices compared with the planar references can be seen.

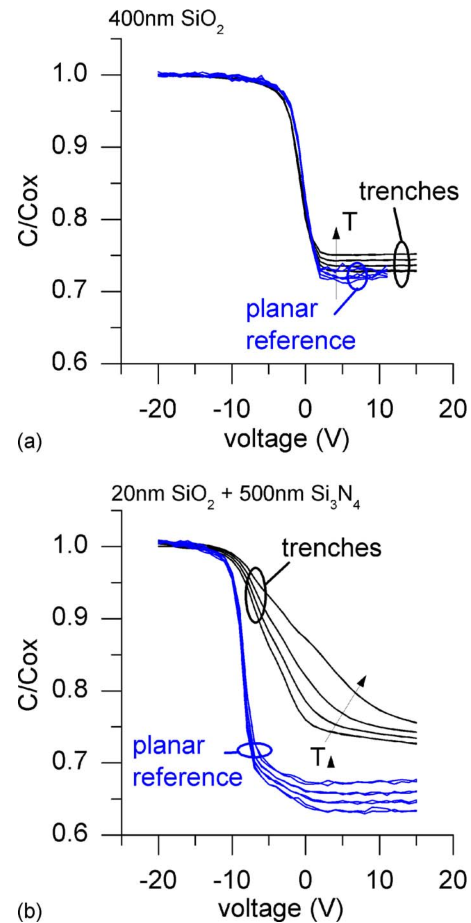


FIG. 6. (Color online) (a) *C*-*V*-measurements at temperatures from RT to 373 K for SiO_2 capacitors and (b) for Si_3N_4 capacitors.

voltage for these capacitors is approximately −10.1 V to −9.3 V. In comparison to the *C*-*V*-curves of the SiO_2 capacitors, the Si_3N_4 capacitors show a significantly higher interface state density, which is reflected in the stretch-out of the *C*-*V*-curves.

To analyze deviations in capacitance of the capacitors across the wafer, capacitance measurements of 34 devices for each geometry version (d2-2.5, a3-a3.5, planar references; A1-A25) and for both dielectric stacks (SiO_2, Si_3N_4) are conducted at −40 V. The results of the measurements are depicted in Figs. 5(a) and 5(b), which indicate the capacitance per mm^2 of the required silicon area. It can be seen that the Si_3N_4 capacitors have a significantly higher capacitance per area than the SiO_2 capacitors. The maximum enlargement of the capacitance for the trench compared to the planar reference capacitors is about 15.7 for the SiO_2 stack and about 12.7 for the Si_3N_4 stack. The greater enlargement of the capacitance for the SiO_2 stack is due to two effects. First, during thermal oxidation, silicon is consumed, and the diameter of the trench hole increases. Therefore, the effective area of the SiO_2 stack is greater compared to the smaller diameter of the trench holes for the Si_3N_4 stack. Second, the SiO_2 layer thickness in the trench holes is reduced, as shown in Figs. 3(a) and 3(c).

B. Temperature dependent capacitance-voltage measurements

Figure 6(a) shows the result of *C*-*V*-measurements at temperatures between 298 and 373 K for a SiO_2 capacitor, and Fig. 6(b) shows the result for a Si_3N_4 capacitor, respectively. The temperature coefficient for the capacitance value in accumulation for the SiO_2 capacitor is calculated to be 18 ppm/K, and for the Si_3N_4 capacitor, the value is 85 ppm/K. The temperature coefficient for the capacitance in depletion is significantly higher for both dielectric layers and is calculated to be approximately 450 ppm/K for the SiO_2 capacitor and approximately 500 ppm/K for the Si_3N_4 capacitor. Ceramic capacitors, which are used in similar applications, show temperature coefficients of up to ±1500 ppm/K.

Furthermore, for Si_3N_4 as dielectric, the interface state density is higher in trench devices compared to planar devices for the Si_3N_4 capacitor, as can be seen in the flat slope of the *C*-*V*-curves in Fig. 6(b). The deposition of the dielectric layers in the trench holes results in high stress at the interface between SiO_2 and Si. Therefore, the saturation of

the interface states during FGA is not as effective in the trench holes due to the stress, as in the planar devices, which show a significant decrease in the interface state density after FGA.

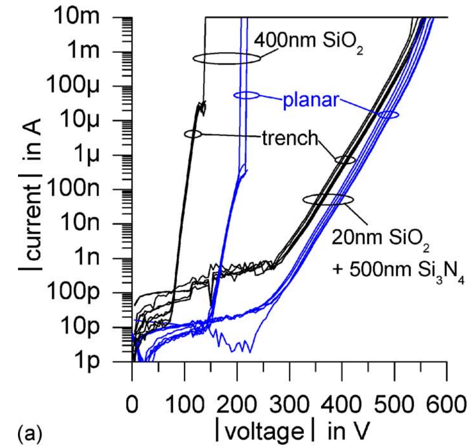
The temperature coefficient α_C for the capacitance value can be theoretically described according to Eq. (1), which consists of three terms.[8] The first term reflects the change in capacitance for a capacitor area A and insulator thickness of t_I due to thermal expansion. The second term represents the temperature dependence of space charge capacitance C_{Si}, and the third term represents the temperature dependence of the dielectric constant ε_I of the insulator,

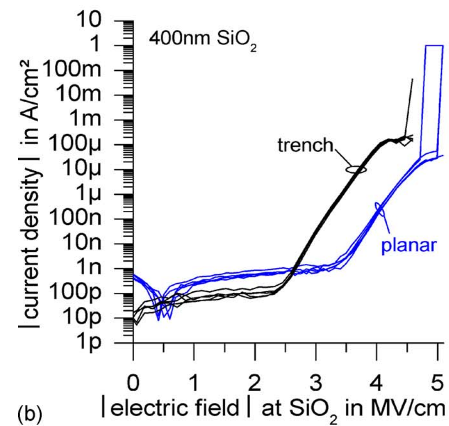
$$\alpha_C = \left(\frac{1}{A}\frac{dA}{dT} - \frac{1}{t_I}\frac{dt_I}{dT}\right) + \left(\frac{C_I}{C_{\mathrm{Si}}}\frac{dC_{\mathrm{Si}}}{dT}\right) + \left(\frac{1}{\varepsilon_I}\frac{d\varepsilon_I}{dT}\right). \quad (1)$$

The first term can be simplified by neglecting the deviation of the insulator thickness change due to thermal expansion $[dt_I/(t_I \times dT)=0]$ and the assumption that the thickness of the substrate is large compared to that of the insulator. This allows the silicon substrate to expand freely, carrying the thin film along with it. Hence, the first term is equal to two times the linear thermal expansion coefficient of silicon L_{Si} (2.8 ppm/K), which is about 5.6 ppm/K. In the case of accumulation, which is the typical operation condition for this capacitor, the second term can be neglected. In the literature, values of 15–21 ppm/K can be found as the temperature coefficient for the permittivity of SiO_2. Therefore, the measured values of the temperature coefficient for the capacitance for the SiO_2 capacitors are similar to the theoretical values reported in literature. No values of the temperature coefficient for the permittivity of Si_3N_4 can be found in the literature to the best of our knowledge.

C. Current-voltage measurements

To analyze the current transport mechanisms and the leakage current of the different dielectric layers, current-voltage (*I-V*) measurements were performed using a Keithley 237 source measurement unit. Figure 7(a) shows *I-V*-curves in accumulation of the two dielectric stacks (400 nm SiO_2, 20 nm SiO_2+500 nm Si_3N_4) for planar devices as well as for trench devices with a needed silicon area A_{Si} of 1 mm^2. For each type, the *I-V*-curves of five devices are shown. The *I-V*-measurements show no significant dependence on the trench geometry parameters (d, a). The SiO_2 trench devices show a significant rise in the leakage current at −75 V, and the planar devices show a rise only at −150 V. Conversely, all Si_3N_4 types show a rise in the leakage current at −260 V. Breakdown of the dielectric occurs at −130 V for the trench SiO_2 capacitors, at −200 V for the planar SiO_2 capacitors, and beyond −530 V for the trench as well as the planar Si_3N_4 capacitors. For both dielectric stacks, the trench devices show significantly higher leakage currents than the planar devices. This has two reasons: The effective area is higher due to the trench structure, and the thickness of the dielectric layer, especially for the SiO_2 devices, is, especially at the bottom of the trench, smaller in the trench structure, as shown in Figs. 3(a)–3(d). Therefore, in Fig. 7(b) the current





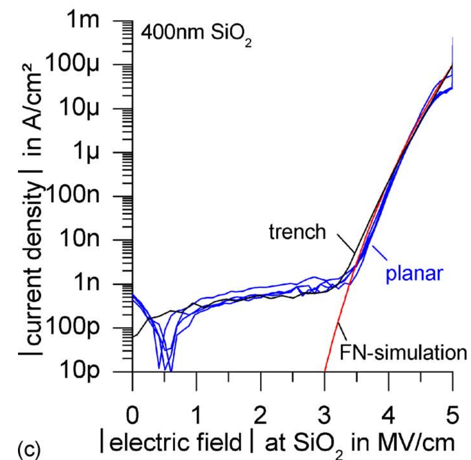


FIG. 7. (Color online) (a) *I-V* curves of SiO_2 capacitors and Si_3N_4 capacitors, (b) *J-E* curves of planar and trench SiO_2 capacitors, and (c) area and dielectric thickness corrected *J-E* curves of planar and trench SiO_2 capacitors.

density J versus the electric field E_{SiO_2} in the SiO_2 layer is depicted for the SiO_2 capacitors. For the calculation of the electric field, a SiO_2 thickness of 428 nm for the planar devices and of 300 nm for the trench devices and a flatband voltage of −2.35 V were taken into account. The current density was calculated, assuming an effective area of 1 mm^2 for the planar devices and an area of 15.7 mm^2 for the trench devices, which was determined by the *C-V*-measurements. This indicates a capacitance enlargement by a factor of 15.7.

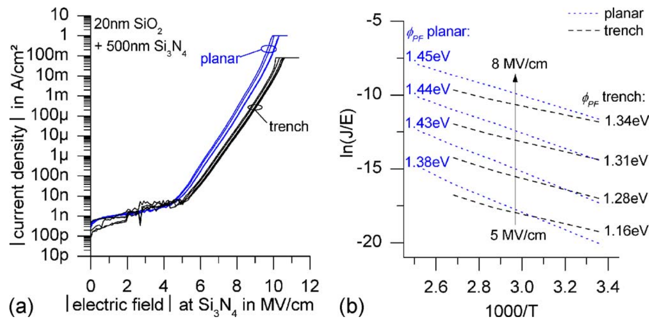


FIG. 8. (Color online) (a) *J-E* curves of planar and trench Si_3N_4 capacitors and (b) Poole–Frenkel Plot of planar and trench Si_3N_4 capacitors.

It can be seen that the current density for the trench devices is lower compared to the planar devices until an electric field of 2.5 MV/cm. At an electric field of 2.5 MV/cm, the current density of the trench devices starts to rise rapidly, whereas the current density of the planar devices only increases significantly at an electric field above 3.5 MV/cm. This mismatch might have three reasons. First, the electric field in the trench devices might be higher than the calculated value due to even lower dielectric thickness in the trenches compared to the depicted thickness in Fig. 3. A second reason can be an increase in the electric field at the trench structures due to edge effects, especially in the concave corner at the bottom of the trench. Third, the effective area for the current transport through the trench devices could be lower than calculated from *C-V*-measurements. Most of the current in the case of the trench structure flows through a small area, where the dielectric thickness is the thinnest.

Recalculating the current density and the electric field for a trench structure with an effective area of 4.5 mm^2 instead of 15.7 mm^2 and an effective dielectric thickness of 230 nm instead of 300 nm, the *J-E*-curves of a trench structure and the planar devices are almost identical, as depicted in Fig. 7(c). Figure 7(c) also shows the result of a Fowler–Nordheim tunneling current[9] simulation of J vs E_{SiO_2}, which matches very well with the measurement results with 230 nm oxide thickness and 4.5 mm^2 area as parameters. The contribution of tunneling currents through areas of thicker oxide appears to be negligible due to the exponential dependence of the electric field. Therefore, Fowler–Nordheim tunneling is likely to be the dominant current transport mechanism for the SiO_2 capacitors in a range of the electrical field from 3.5 to 5 MV/cm.

In Fig. 8(a), the current density J versus the electric field $E_{Si_3N_4}$ for the Si_3N_4 capacitors is depicted. For the calculation of the electric field, an equivalent oxide thickness of 285 nm for both the planar and the trench devices and a flatband voltage of -9.7 V are taken into account. The current density is calculated with an effective area of 1 mm^2 for the planar devices and an area of 12.7 mm^2 for the trench devices, which was determined by the result of the *C-V*-measurements. It can be seen that in contrast to the SiO_2 capacitors, there is a good correlation between the planar and the trench devices, even when the same equivalent oxide thickness is taken into account for the planar as well as for the trench devices, and the enlargement of the capacitor area of the trench devices is extracted from the *C-V*-measurements. This verifies the uniform coverage of the Si_3N_4 dielectric layer in the trench devices, which is also observed in the SEM-images in Figs. 3(b) and 3(d). To further analyze the current transport mechanism in the Si_3N_4 capacitors, temperature dependent *I-V*-measurements were performed. The results are shown in a Poole–Frenkel plot in Fig. 8(b). In the range of the electrical field $E_{Si_3N_4}$ from 5 to 8 MV/cm, a Poole–Frenkel current conduction with trap depths of 1.16–1.34 eV for the trench capacitors and of 1.38–1.45 eV for the planar devices can be calculated. In the literature, values between 0.9 and 1.5 eV have been reported for Si_3N_4, so that our values are plausible.[10,11]

IV. CONCLUSION

In summary, high voltage trench capacitors were successfully manufactured utilizing thermally grown SiO_2 and Si_3N_4 deposited by LPCVD. The capacitance enlargement per required silicon area amounts up to 15.7 for the SiO_2 capacitor and up to 12.7 for the Si_3N_4 capacitor. Good temperature stability of the capacitance was observed. The breakdown electrical field and the leakage current density of the devices using Si_3N_4 are not influenced from the device geometry. Trench capacitors using a Si_3N_4 layer as a dielectric offer the most promising route to realize high voltage trench capacitors especially for automotive applications.

ACKNOWLEDGMENT

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