Managing Complexity And A Left Shift: Reconfigurable Mixed-Signal Circuits For Complex Integrated Systems

Strategies to tackle the long development times and high costs involved in designing and verifying analog components.

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The chip market is growing worldwide; it's projected to nearly double by 2030 to over one trillion dollars. Most of this market is made up of digital functions in the form of logic, microprocessors, and memory. Although analog ICs account for only around 15% of the total, they are key components for overall systems and are therefore almost always present. In particular, they provide power management and enable special functions in the communications, automotive, and industrial sectors, among others. This article takes a closer look at the role of analog or mixed-signal circuits. One trend that leaps to the eye is how value creation takes place at the system level: the relatively small analog IP market contrasts with a much larger market for analog ICs. The reasons for this can be found in digitalization itself: analog signal processing is the basis for digital sensors and actuators, and it always forms the bridge between physical signals and the digital world. Rising demand for chips goes hand in hand with increasing requirements for performance and complexity per unit.

But let's move on to design. While designers of digital ICs can draw on a wide array of automation options (i.e., electronic design automation, or EDA), analog circuits are still designed largely by hand. Although much progress has been made in analog EDA in recent years, it's still mostly "just" successive support of manual design. As a result, productivity in analog circuit design lags several orders of magnitude behind digital. This means that even small analog parts in microchips incur long development times and high costs, which often exceed those of digital components. At the same time, the number of young designers is continuing to fall due to declining numbers of graduates in the relevant degree programs, and so fewer and fewer designers are available to create increasingly complex chips. This trend is likely to intensify in the coming years – as will the pressure to find solutions.

There are multiple ways to tackle this challenge. One is to step up use of systems engineering to handle growing complexity through a systematic top-down approach. Although this increases the effort required in the first step – due to the development of the system itself, and to the initial increase in verification effort of various methods and models at higher levels of abstraction – in the long run, it cuts down on verification time. This is because the only way to sufficiently verify complex systems is through fast and comprehensive system simulations. The entire periphery and application of the IC must also play a role here: the external electrical circuitry (e.g. power supply), electronics packaging technology, firmware, even software environments of the target applications – a host of details must be covered across all the needed levels of abstraction. This quality of verification at the system level provides a much better overview and thus forms the basis for greater coordination and parallelization of component design tasks. In turn, it ultimately saves design time and increases system robustness. And likely, new ML methods will even help to reduce related initial efforts.

Methodically breaking down a system into individual components also makes it possible to reuse components sustainably. With fewer and fewer experts available for design, the reusability of individual system components is essential and strategic. However, it faces two challenges.

One is that a single IP block can't cover all conceivable specification parameters for different systems (bottom-up). For example, some parameters – such as the sample rate in combination with the resolution of an ADC, or a buffer's input voltage range – are constantly adjusted depending on the application. The individual block must therefore be able to be quickly adapted to its diverse range of applications (within certain limits). One possible solution is to design reconfigurability into the analog parts of the circuit. This can either be done in the design phase using analog EDA or realized using a suitable implementation that keeps the circuit configurable during operation, e.g., through configuration using digital registers.

The second challenge to reuse is the migration to new technologies, which opens up options to benefit from scaling or dual/multiple sourcing. If an IP works for just one or a few semiconductor technologies, then it is possible to address only this small number of technology nodes and manufacturers. To increase the addressable market, porting needs to be made as uncomplicated as possible, especially for layouts, in order to keep design effort to a minimum. As the design process has to be run through again, new EDA methods for reuse and design acceleration are required. Ideally, these EDA methods should be conceived and implemented in combination with the design process and the new IP – or even the IP family.

Ultimately, a combination of measures – such as reconfigurable and modular IP architectures, flexible design concepts, and increased use of EDA – is the only way to meet the growing demand for analog circuit components as well as the rise in system complexity, both now and in the future.