An Approach to Generate Test Signals for Analog Circuits – A Control-Theoretic Perspective

Wolfgang Vermeiren, Fabian Hopsch, Roland Jancke
Fraunhofer IIS/EAS Dresden, Germany

Abstract—This paper presents a control-theoretic driven approach to the automatic generation of test signals for analog circuits or systems. It is based on the adaption of a tracking control structure for the task of generating test signals aimed at manufacturing test for a finished circuit design. The approach will be derived and its functionality is demonstrated using circuit examples. The integration of the proposed approach within a more general test development procedure for improving the fault coverage is explained.

Keywords—Automatic test signal generation, analog circuit, fault-model based test approach, fault detection, structural test, control-theoretic derivation, tracking control principle, network simulator, analog fault simulation, test development procedure, improvement of fault coverage, analog ATPG

I. INTRODUCTION

The analog part of integrated circuits comprises in general a relatively small section of the complete circuit. However, it needs due to the mainly applied specification-oriented tests a significantly higher effort for testing than the digital circuit part. This constellation will be exacerbated even further with continued increasing circuit complexity. Therefore, a better test efficiency is of vital significance for analog and mixed-signal circuits and components. This can be achieved by the creation of efficient and cost-optimized test signals. An approach for surmounting this analog test effort problem consists of using a fault-model based (structural) test approach rather than a specification-oriented one.

There are two main issues why a fault-model based test approach has not been established. On the one hand, there is a lack of standard fault models [1], on the other hand, metrics are missing for comparing results of the different methods [2]. Therefore, especially a constructive, automatic generation of test signals for analog circuits is difficult. Comprehensive surveys to this topic have been presented in [3][4][5]. They include, but are not limited to: usage of signal flow graphs and other graphs, construction of testability transfer factors, sensitivity-based ATPG, application of principles for solving optimal control problems, alternative test approaches, and methods of automatic test parameter selection. However, no single methodology and test signal waveform, respectively, have become prevalent. Their performance capabilities are circuit specific and application dependent, so that they complement each other. Thus, the test signal generation for analog circuits is a still incomplete and open research topic.

In this paper a control-theoretic approach for test signal generation is suggested as contribution to that topic. This approach represents on the one hand a generalization of the test generation task to a more abstract point of view. On the other hand it is a simple applicable method to generate test signals, which are designed to be utilized within a manufacturing test. The proposed approach is based on adapting the structure of a tracking control for the purpose of generating test signals. The functionality of the approach is proven in control-theoretic manner as well as experimentally with examples. The approach is intended to be used within the phase of test development after the circuit design had been completed. Furthermore, it is integrated within a test development scheme whose main purpose is the improvement of the fault detectability for achieving a high fault coverage.

The introduction into the approach and its control-theoretic derivation as well as the validation of its technical feasibility by means of a network simulator is presented in Section II. In Section III the integration within a test development scheme is described. Thereafter, the functionality of the approach is demonstrated with two circuit examples in Section IV. Finally, a discussion of the presented concept and an outlook is given.

II. TEST SIGNAL GENERATION BY TRACKING CONTROL

In [6] a methodology has been presented for applying a predefined input signal to a terminal of an analog circuit which is embedded in a System on Chip (SoC). For doing that, a tracking control structure is used (see Fig. 1).

In that tracking control structure of [6] a PID-controller\(^1\) is applied as controller. The module which is upstream of the embedded analog circuit is used as controlled system. The input variable \(w\) corresponds to the signal which shall be applied to the embedded analog circuit. By means of the PID-controller the stimulus at the primary SoC input \(u\) is adjusted in such a manner that the variable \(y\) which should be set follows the input variable \(w\). In this way, the predefined input signal can be provided to the terminal of the embedded analog circuit.

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\(^1\) Proportional-plus-integral-plus-derivative controller
Such a tracking control principle can be correspondingly applied to the task of the test signal generation for an individual analog circuit or unit. This is feasible when the controlled system consists of the model of a test process. The test process model is composed of a comparison structure of the faulty circuit or system (Unit Under Test—UUT) and the fault-free nominal one (Reference Module). The concept is shown in Fig. 2.

This modified tracking control structure adopts the concept presented in [7][8] which had been developed from a circuit’s point of view and combines it with the idea described in [6]. In relation to [7][8] the approach from Fig. 2 represents a generalization with respect to the following points:

- no fix specification of test signal waveforms whose parameter have to be optimized
- free choice of the kind of the used controller rather than limitation to a simple amplification which extends the design versatility of the test signals to be generated
- possibility of freely selectable waveforms for the deviation behavior between faulty and fault-free circuit
- no limitation to electrical circuits, but simple extension capabilities to systems described at functional or behavioral level

Generally, a fault is assumed to be detected if the deviation between UUT and reference exceeds a predefined threshold. This is equal to saying that a specific behavior of the deviation between UUT and reference must exist. In the tracking control principle that deviation is the input information, which is applied as requested reference variable \( \Delta y_{\text{Ref}} \). The control loop structure is such that the controlled variable \( \Delta y_{\text{Tar}} \), which is the calculated target behavior of the deviation between UUT and reference, follows the reference variable \( \Delta y_{\text{Ref}} \). Here, the control signal \( u \) is just the test signal, which effects the deviation behavior \( \Delta y_{\text{Tar}} \). This test signal is concurrently and automatically generated during the control process for \( \Delta y_{\text{Tar}} \). It is the output information of the test generation procedure.

Subsequently, the control-theoretic derivation of such a test signal generation and its execution for a simple faulty lowpass filter is presented. The analytic solution of the control-theoretic approach and the results obtained by means of a network simulator are presented as well.

### A. Control-Theoretic Derivation

The transfer function of the single control loop structure according to Fig. 2 is

\[
G(s) = \frac{Y(s)}{W(s)} = \frac{G_F(s) \cdot G_R(s)}{1 + G_F(s) \cdot G_R(s)}. \tag{1}
\]

where \( s \) is the complex frequency variable. \( W(s) \) and \( Y(s) \) are the Laplace-transforms of reference and controlled variable as well as \( G_F(s) \) and \( G_R(s) \) are the transfer functions of the controlled system and the controller (regulator).

Thus, the transfer behavior between reference variable \( w \) and controlled variable \( y \) results in

\[
Y(s) = \frac{G_R(s)}{1 + G_F(s) \cdot G_R(s)} \cdot W(s). \tag{2}
\]

And with \( Y(s) = G_F(s) \cdot U(s) \) the transfer behavior between reference variable \( w \) and actuating variable, i.e. the control signal, as test signal \( u \) results in

\[
U(s) = \frac{G_R(s)}{1 + G_F(s) \cdot G_R(s)} \cdot W(s). \tag{3}
\]

With \( w \sim \Delta y_{\text{Ref}} \) and \( y \sim \Delta y_{\text{Tar}} \) (Fig. 2) the test signal \( u \) results in

\[
U(s) = \frac{G_R(s)}{1 + G_F(s) \cdot G_R(s)} \cdot \Delta Y_{\text{Ref}}(s). \tag{4}
\]

and using \( G_F(s) = G_{\text{Faulty}}(s) - G_{\text{Gold}}(s) \) it yields

\[
U(s) = \frac{G_R(s)}{1 + (G_{\text{Faulty}}(s) - G_{\text{Gold}}(s)) \cdot G_R(s)} \cdot \Delta Y_{\text{Ref}}(s). \tag{5}
\]

### B. Test Signal Reconstruction

The validation of the functionality of the proposed approach can be performed by reconstructing a known test signal.

A passive lowpass filter which is implemented as RC-network is used as example system (Fig. 3). It has the time constant \( T = R \cdot C \) and the transfer function \( G_{TP}(s) \).

\[
G_{TP}(s) = \frac{1}{1 + s \cdot T}.
\]

The components of a fault-free nominal circuit (Reference Module) are assumed to have the parameters \( R_g = 110 \, \Omega \) and \( C = 20 \, nF \), and the faulty circuit (UUT) is supposed to have the parameters \( R_f = 1.1 \, k\Omega \) and \( C = 20 \, nF \). This represents a parametric fault on the resistance \( R \). Consequently, the time constants \( T_g = 2.2 \, ms \) and \( T_f = 0.022 \, ms \) and the transfer behavior from the reference variable \( \Delta y_{\text{Ref}} \) to the actuating variable \( u \) results in

\[
U(s) = \frac{G_R(s)}{1 + \left( \frac{1}{1 + sT_g} \cdot \frac{1}{1 + sT_f} \right) \cdot G_R(s)} \cdot \Delta Y_{\text{Ref}}(s). \tag{6}
\]

A unit step function applied at the input \( u_a \) acts as known test signal. Fig. 4 (next page) depicts the deviation behavior between the faulty lowpass filter and the fault-free nominal circuit, which is used now as the reference signal \( \Delta y_{\text{Ref}} \).
Fig. 4: Behavior of the deviation $\Delta y_{ref}$ between faulty UUT and reference for a unit step function as known test signal.

1) Analytical Solution

The analytical descriptions of the deviation behavior in the complex variable domain and the time domain are

$$\Delta Y_{ref}(s) = \frac{1}{1+Ts_g} - \frac{1}{1+Ts_f} \cdot \frac{1}{s}$$  \hspace{1cm} (7)

$$\Delta Y_{ref}(t) = -e^{-\frac{t}{T_f}} \cdot \left(-1 + e^{\frac{t}{T_f}} \frac{T_f}{T_g} \right) \cdot 1.$$  \hspace{1cm} (8)

Using the formulas (6), (7) the description of the generated test signal in the complex variable domain results in

$$U(s) = \frac{G_R(s)}{1+G_R(s)} \left( \frac{1}{1+Ts_f} - \frac{1}{1+Ts_g} \right) \cdot \frac{1}{s}.$$  \hspace{1cm} (9)

After applying the parameter values for the time constants $T_g$ und $T_f$ as well as with the help of a proportional controller $G_R(s) = K_{Prop}(s) = 10000$ the formula of the test signal waveform in the time domain $u(t)$ results, e.g. by using Mathematica [9], in

$$u(t) = 10000 \cdot \left( -99.9898 \cdot 10^{-6} \cdot e^{-4.5909 \cdot 10^{-2} \cdot t} + 99.9898 \cdot 10^{-6} \cdot e^{-4.5909 \cdot 10^{-2} \cdot t} \right) \cdot 1,$$  \hspace{1cm} (10)

which represents a unit step function.

2) Simulative Solution

The unit step function as known test signal is also reconstructed if the approach for generating the test signal (Fig. 2) is formulated as an electrical circuit description and a transient simulation with a network simulator is performed. The simulation with Spectre [10] yields the result depicted in Fig. 5.

III. IMPROVING THE FAULT COVERAGE OF CIRCUITS

In Section II, the control-theoretic approach for generating test signals according to Fig. 2 has been derived and its functionality has been demonstrated. Moreover, the approach is integrated within a test development framework. After determining an initial fault coverage $FC_0$ as well as a set of remaining non-detected faults $FL_{nd}$; have remained, yet are non-detected by the already preexisting standard tests. This contributes to improve the prior fault coverage.

Based on the previous explanations the test development procedure for an analog circuit depicted in Fig. 6 is suggested.

The procedure contains the following flow:

1) Fault simulation for already preexisting tests and a defined fault set for determining an initial fault coverage $FC_0$ as well as a set of remaining non-detected faults $FL_{nd}$;

2) Heuristic choice of a yet non-detected fault from the set $FL_{nd}$ which should be used for generating tests, if the set $FL_{nd}$ is empty ($FL_{nd} = \emptyset$) jump to END;

3) Test signal generation for the selected fault via the control-theoretic methodology (Fig. 2); if no test generation is possible (fail) then update the set $FL_{nd}$ of remaining non-detected faults by dropping the just handled fault $F_1$ from the outgoing set $FL_{nd}$ and jump to (2);

4) Fault simulation for all of the faults of the remaining fault set $FL_{nd}$ just using the generated test signal, updating the set $FL_{nd}$ of remaining non-detected faults by dropping all new detected faults from the set $FL_{nd}$, if the updated set is not empty jump to (2), else ($FL_{nd} = \emptyset$) jump to END;

5) Termination if all faults have been detected or if a test signal generation had been carried out for all faults according to (3).

Fig. 5: Reconstruction of the unit step function as known test signal via a network simulation.

Fig. 6: Flow chart of the test development procedure for improving the fault coverage of circuits.

2 The application of the proportional controller has been done only for purposes of presentability of the waveform expression of the test signal.
IV. APPLICATION EXAMPLES

A. Continuous-Time State-Variable Filter (CT-Filter)

The procedure for the test development according to Section III will first be illustrated via the continuous-time state-variable filter (CT-Filter) from [11] (Fig. 7).

1) The fault set comprises 162 short and open circuit faults. That fault set consists of 90 shorts represented by a resistance of 20 $\Omega$, and 72 opens represented by a resistance of 10 M$\Omega$. Here, a fault is assumed to be detected if the deviation between UUT and reference exceeds the threshold of 1.1 V. Determinations of fault detections are achieved by running fault simulations using aFSIM [12]. Here, within the DC$^3$-, AC$^4$-, and transient$^5$ domain via the evaluation of all of the three filter outputs 122 faults have been detected. This implies that the set of the non-detected faults consists of 40 faults.

2) For selecting a non-detected fault, which should be used for generating tests the following heuristic is used: Choose that fault, which is indeed non-detected with the already used tests, but which delivers of all the other non-detected faults the largest deviations from the fault free circuit. Thus, from the set of yet non-detected faults a short circuit fault within the operational amplifier A1 has been chosen for the test signal generation.

3) A transient behavior of the deviation signal on the high pass output has been chosen for the generation of a new test signal, namely a ramp-wise waveform from 0.0 V to 5.0 V during a period of 20 ms (Fig. 8). This deviation signal behavior aims on the one hand for a dependable fault detecting above the permissible tolerances of 1.1 V and allows on the other hand a stable operation of the tracking structure from Fig. 2. The application of the test signal generation approach for the selected fault results in the test signal to the CT-filter, which is depicted in Fig. 9. This test signal has been generated using a PID-controller with moderate control performance.

4) Using this generated test signal additionally 10 faults could be detected of the non-detected 40 faults by fault simulations on the evaluation of all three filter outputs (HP, BP, LP). Thus a reduction of the number of non-detected faults by 25% could be achieved, i.e. the fault coverage increases from 75% to 81%.

5) The proposed approach with the selected controller parameters did not generate any further test signals, which would have been valid within the specified domain of the filter.

B. Active Bandpass Filter

As another system for applying the test development procedure with the included tracking control test generation approach an active bandpass filter from [13] is used. Its implementation is shown in Fig. 10.

At first, for this circuit on the basis of deviation signals between a faulty UUT and the nominal reference circuit which had been given in [14] the corresponding test signals have been reconstructed.

Then, the procedure for the test development according to Section III has been applied, however with a slightly extended choice of the deviation behavior $\Delta y_{ref}$ used for generating a test signal. Additionally, the allowed voltage values of the resulting test signal have been limited.

1) The fault set comprises 50 short and open circuit faults. That fault set consists of 21 shorts represented by a resistance of 20 $\Omega$, and 29 opens represented by a resistance of 10 M$\Omega$. Here, a fault is assumed to be detected if the deviation between

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3 DC-Sweep from -5 V to +5 V
4 AC-Sweep from 0.1 Hz to 5000 Hz
5 sine-signal with an amplitude of 5 V and frequency of 795 Hz

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Fig. 7: Continuous-time state-variable filter (CT-Filter) from [11].

Fig. 8: Required behavior of the deviation $\Delta y_{ref}$ between faulty UUT and reference.

Fig. 9: Generated test signal and the resulting outputs of reference and faulty UUT.

Fig. 10: Bandpass filter circuit for implementing the functionality given in [13].
UUT and reference exceeds the threshold of 0.1 V. Determinations of fault detections are achieved by running fault simulations using the aFSIM tool. Thereby, within the DC\(^{-}\), AC\(^{+}\), and transient\(^{8}\) domain via the evaluation of the filter output 36 faults have been detected. This implies that the set of the yet non-detected faults consists of 14 faults.

(2) For selecting a non-detected fault, which should be used for generating tests the heuristic begins as above: Choose that fault, which is indeed non-detected with the already used tests, but which delivers of all the other non-detected faults the largest deviations from the fault free circuit. Thus, from the set of yet non-detected faults an open circuit fault within the operational amplifier has been chosen for the test signal generation. But, additionally the original deviation signal has been enlarged by a factor of 10.

(3) The deviation behavior used for generating a test signal via the approach is depicted in Fig. 11. This deviation signal behavior aims on the one hand for a dependable fault detection above the permissible tolerances of 0.1 V and allows on the other hand a stable operation of the tracking structure from Fig. 2. The application of the test signal generation approach for the selected fault results in the test signal to the bandpass filter which is depicted in Fig. 12. This test signal has been generated using a PID-controller with moderate control performance. Furthermore, the capability of the network simulator has been used to constrain the resulting test signal.

(4) Using this generated test signal additionally 2 faults could be detected of the non-detected 12 faults by fault simulations. Thus a reduction by about 17% of the number of non-detected faults could be achieved, i.e. the comprehensive fault coverage improves from 76% to 80%.

(5) The proposed approach with the selected controller parameters did not generate any further test signals, which would have been valid within the specified domain of the filter.

V. DISCUSSION OF THE CONCEPT AND OUTLOOK

An approach for an automatic test signal generation for analog circuits from a control-theoretic perspective was presented. The functionality of the approach was demonstrated in control-theoretic manner as well as with circuit examples. By integrating the proposed approach within a more general test development scheme, by means of the additional generated test signals, the fault coverage can be improved with respect to preceding standard tests.

However, investigations into the approach are not yet completed. Especially, issues relating to its further applicability still have to be explored. Also, comparisons with other methodologies for generating test signals are still open.

Thus, the choice of a proper waveform regarding the signal behavior of the reference variable to be predefined is an aspect which has to be investigated. Or in other words: How to find a deviation behavior \( \Delta y_{\text{ref}} \) between the faulty circuit or system (UUT) and the fault-free nominal one (Reference Module) to generate test signals that are valid according to the circuit and system specifications, respectively.

Challenges with the suggested approach to be solved are e.g.

- balancing the high number of degrees of freedom which involves the relation between the kind and parameters of the used controller and the predefined waveform of the deviation behavior between UUT and reference,
- choice of the order of the non-detected faults for which the test signal generation is to be performed,
- convergence problems which can result in unwanted termination of the test signal generation process.

Additional work will consist in automating the methodology as a whole (especially for selecting the controller parameters).

Future research has to validate the proposed approach with further circuits and systems, respectively. The presented control-theoretic approach is not only a method limited to electrical circuits, but also a more generally one, which is also appropriate to structures described at functional or behavioral level. For that reason, the authors see a large prospective within the applicability of the tracking control based test signal generation on system level. Hence, recommendations from ISO 26262 [15] for carrying out fault simulations for ensuring functional safety can be supported. Therefore, investigations are intended regarding a proof of concept for applying the approach to systems which are described with SystemC-AMS.

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6 DC-Sweep from -5 V to +5 V

7 AC-Sweep from 0.1 Hz to 100 Hz

8 sine-signal with an amplitude of 1 V and frequency of 0.2905 Hz
This will be done via the SystemC-AMS simulator COSIDE [16]. The objective of such investigations is to generate tests which are particularly capable to detect above all faults whose detectability has to be proven. The development of a concept for such a feasibility study is a work in progress.

In this sense, the investigations done so far can be considered as preparatory work.

REFERENCES


