

Reliability of Silver Sintering on DBC and DBA Substrates for Power Electronic Applications

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Summary / Abstract

In terms of reliability standard power electronic modules are at their limit regarding robustness aspects. As a high reliable alternative for assembly processes such as Sn-based soldering and aluminum wire bonding, the assembly with nano silver sintering technology on different substrate materials has been investigated in this work. The reliability of silver sintered top and bottom side interconnects has been determined by end-of-life active power cycling testing with 50 mm² commercial diodes from Infineon sintered on DBC (direct bonded copper) and DBA (direct bonded aluminum) substrates with a sintered silver ribbon for the top side connect. The setup with DBC substrate showed a 17 times, the one with DBA substrates a 2.7 times higher statistical lifetime than the soldered and wire bonded reference. Delamination of the sintered layers and with a progressing aging in active temperature cycles also showed oxidized cracks in the Cu metallization of the substrate as new failure mechanisms of the DBC samples with double sided sinter technology. For DBA assemblies a formation of hillocks on the Al surface underneath the diode could be detected next to delamination of the sinter layer.

1 Motivation

Due to higher integration levels standard packaging of power electronic modules is more and more approaching its limitations. One possible alternative for common solder and bond wire interconnects is the silver sintering technology, first published by Schwarzbauer and Kuhnert [1] in 1990.

Micro scale sintering processes take place at a pressure of 30 MPa to 50 MPa, sintering times of 60 s to 180 s and temperatures between 200 °C and 300 °C. For nano scale sintering, much lower pressures in the range of about 5 MPa together with typical sintering times of 60 s and temperatures of 275 °C can be used [2], due to the higher surface energy at a smaller particle size in nano scale sintering pastes.

The use of sinter paste instead of solder paste leads to much lower mechanical stresses inside the device and substrate during sintering and subsequent operation of the module, therefore cracking and delamination can be reduced remarkably.

Previous passive accelerated lifetime tests showed promising results of silver sintered samples compared to soldered and wire bonded ones. Up to 646 thermal cycles from -55 °C to 175 °C were achieved with a soldered diode on a copper (Cu) substrate, whereas the lead-free soldered samples only survived 51 cycles [3].

Lei et al. [4] found that direct bonded aluminum (DBA) substrates can withstand 1500 cycles from -55 °C to 250 °C without any delamination of the aluminum layers, but with a roughening of the surface. DBA substrates with

an aluminum nitride (AlN) ceramic layer have also been subjected to passive temperature cycling in previous tests at the Fraunhofer IISB [5]. The samples reached 575 cycles from -40 °C to +230 °C without any delamination. It was also shown that direct bonded copper (DBC) substrates with the same ceramic material and substrate layout survived one number of cycles less until 20 % of the contact area is delaminated.

In this work, both techniques silver sintering as well as DBA substrates have been combined for a high reliable module. Power cycling tests have been carried out for the evaluation of these techniques.

2 Experimental

For active temperature cycling tests, the anode sides of diodes type SIDC50D60C6 from Infineon have been coated by evaporating chromium, nickel and silver to build a sinterable and solderable surface. Four kinds of assemblies have been mounted which are shown in **Figure 1** and described in **Table 1**: Sample type A comprises a double sided sintered sample with an silver (Ag) ribbon on a DBA substrate with AlN ceramic (first row, left). Sample type B is a soldered and wire bonded sample on a DBC substrate with alumina (Al₂O₃) ceramic (first row, right). The other two types of samples are double sided sintered assemblies with DBC substrates again with Al₂O₃ ceramic and a silver ribbon as the topside interconnect, further called sample type C (second row, left) and a double sided soldered assembly with DBA substrates with

AlN ceramic and a silver ribbon on top named D (second row, right).

The DBC substrates consist of an Al₂O₃ layer with a thickness of 630 μm and two Cu layers each with a thickness of 300 μm on both sides of the ceramic, provided by Curamik electronics GmbH. The DBA has an AlN ceramic, also with 630 μm thickness, and two 300 μm thick aluminium (Al) metallization. DBA substrates have been delivered by DENKA Chemicals GmbH. All substrates are coated with Ni/flash Au. For the sintered sample types, the metal pads below the diodes have been coated with a galvanic Ag layer for adhesion reasons.

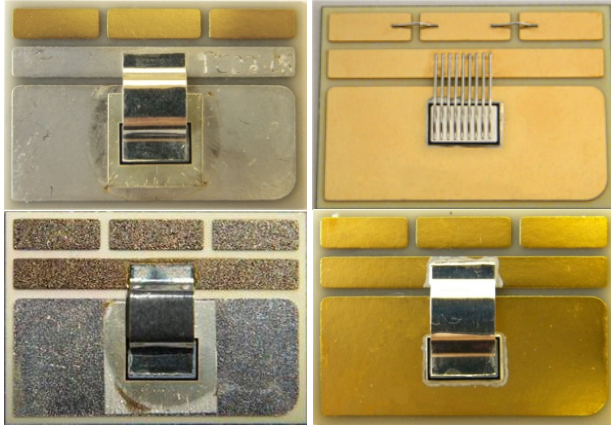


Figure 1 Test devices for power cycling, first row from left right: sample type A and B, second row from left to right: sample type C and D

2.1 Mounting of the samples

The silver sinter paste nanoTach, K-series from NBE Tech LCC is used to mount the semiconductor device as well as the Ag ribbon for sample types A and C. The paste consists of nano scaled Ag particles with a high surface energy. To inhibit the sintering of the paste at room temperature, the paste is encapsulated with an organic material. Additionally, the encapsulated nanoparticles are stirred in a solvent which provides a good printability of the paste during a screen or stencil printing step.

The nano silver paste has been applied in a screen printing process. The printed thickness of the paste is between 60 μm and 80 μm. During a subsequent drying step, the solvents are removed from the paste, and the thickness of the layer is reduced to 30 μm to 40 μm. After the drying step, the metallized diode is placed on the Ag sinter layer and the setup is sintered in a pneumatic press (23-100 from Schmidt Technology) with 5 MPa and 275 °C for 60 s. An evenly distributed pressure is realized by a silicone layer with a thickness of 2 mm on top of the semiconductor. The screen printing and drying steps are repeated on top of the diode and substrate and a 100 μm thick Ag ribbon is sintered on top.

The soldered samples for reference (types B and D) have been mounted in a process oven SRO-704 from ATV with eutectic SnAgCu solder preforms. The oven was supplied with a formic acid atmosphere to achieve a reductive at-

mosphere during the soldering process. For sample type B, the top side connection was realised with the help of ultrasonic wire bonding with Al thick wires with a diameter of 375 μm.

Sample type	A	B	C	D
Chip top metallization	AlSiCu/ Cr/ Ni/ Ag	AlSiCu	AlSiCu/ Cr/ Ni/ Ag	AlSiCu/ Cr/ Ni/ Ag
Top side connect	100 μm Ag ribbon	375 μm Al bond wires	100 μm Ag ribbon	100 μm Ag ribbon
Top side mounting	20 μm Ag sinter layer	Ultra- sonic wire bonding	20 μm Ag sinter layer	100 μm SnAgCu solder layer
semiconductor device	Diode SIDC50D60C6 from Infineon			
Bottom side mounting	20 μm Ag sinter layer	100 μm SnAgCu solder layer	20 μm Ag sinter layer	100 μm SnAgCu solder layer
Substrate	AlN- DBA	Al ₂ O ₃ - DBC	Al ₂ O ₃ - DBC	AlN- DBA
Substrate metallization	Ni/ flash Au/ Ag	Ni/ flash Au	Ni/ flash Au/ Ag	Ni/ flash Au

Table 1 Test devices for power cycling

2.2 Accelerating lifetime testing with active power cycling tests

All samples were mounted on a cold plate by clamping. To enhance the thermal performance of the indirectly cooled substrates, the thermal interface material Keratherm from Kerafol Keramische Folien GmbH with a thickness of 225 μm was used. With a cycling time of 30 s, the samples were heated up to +175 °C by applying current and cooled down again to +45 °C with the help of a liquid coolant inside of the cold plate, whereat the heating time is the same as the cooling time. The residual temperature change, therefore, amounts to 130 K.

3 Results and Discussion

The end-of-life in accelerating lifetime testing was defined to be at either 20 % increase of the forward voltage in operation (heating) or 20 % increase of temperature difference.

The temperature difference in active temperature cycling is shown in Figure 2 for sample types A and D with DBA substrates. The blue line shows the raise of the temperature difference up to 200 °C, followed by the end of life. For this sample, the contact area at the silver sinter layers starts to degrade at about 16,500 cycles and shows 20 %

of increase of temperature difference at about 18,000 cycles. The electric contact is completely open at 19,000 cycles.

3.1 Weibull statistics of power cycles

With the help of Weibull statistics, the characteristic lifetime β of the soldered and wire bonded samples on DBC substrates could be determined to 11,970 cycles with a narrow distribution (Weibull modulus α : 4.3). Silver sintering on the same substrate increased β by a factor of 17 up to 208,000 cycles [3]. The samples mounted on DBA substrates showed a lower statistic lifetime in power cycling with a β of 4,047 for the double sided soldered DBA sample and a β of 31,998 for the double sided sintering on DBA sample.

The probability functions $F(N_f)$ versus the number of cycles N_f of the four samples are shown in **Figure 3**.

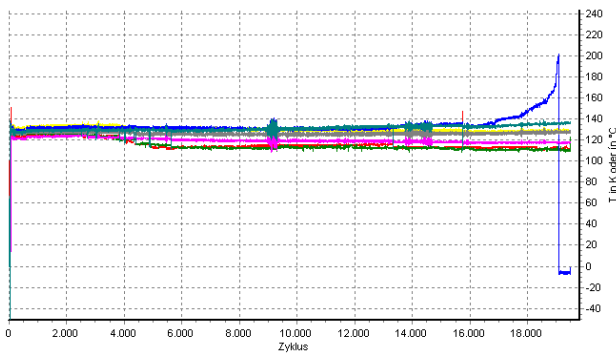


Figure 2 Temperature difference measured in accelerated lifetime tests of sample types A and D samples

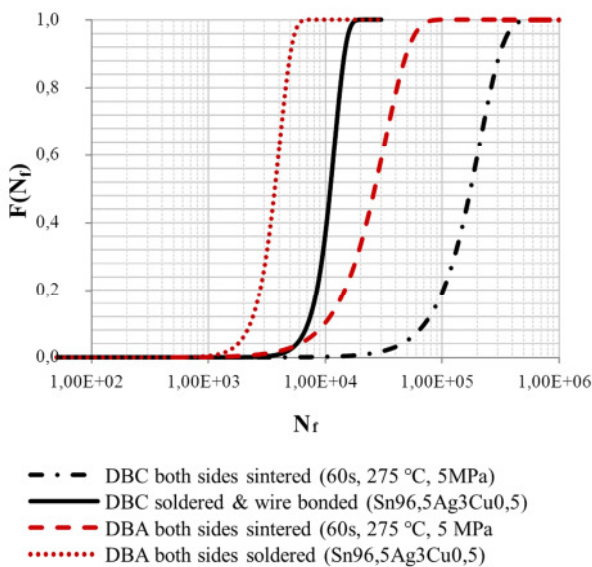


Figure 3 Weibull analysis of active temperature cycling tests from +45 to +175 °C

3.2 Classification of the results with the help of Coffin-Manson approach

Suhir's model [6] was used to calculate the shear and normal strength as well as the von-Mises stress, as described in [3]. The material data used for this calculation is listed in **Table 2**.

	Ag layer	Diode	DBC	DBA
Thickness [m]	20 10^{-6}	90 10^{-6}	0.98e ⁻³	1.33 10^{-3}
Young's Modulus [GPa]	15,0	16,7	145	70
CTE [$10^{-6}K^{-1}$]	20.0	3.0	7.1	4.2
Poisson's ratio	0.37	0.17	0.34	0.34
Edge length [m]		7.5576 10^{-3}		
Yield strength [N/mm ²]	26.6			
ΔT [K]	130			

Table 2 Data for the determination of the maximal resulting von-Mises stress using Suhir's model [7]

The characteristic lifetime β of the four sample types is plotted as cycles to failure against the plastic strain in a Coffin Manson plot in **Figure 4**. Existing values from previous tests [3] are added to the graph.

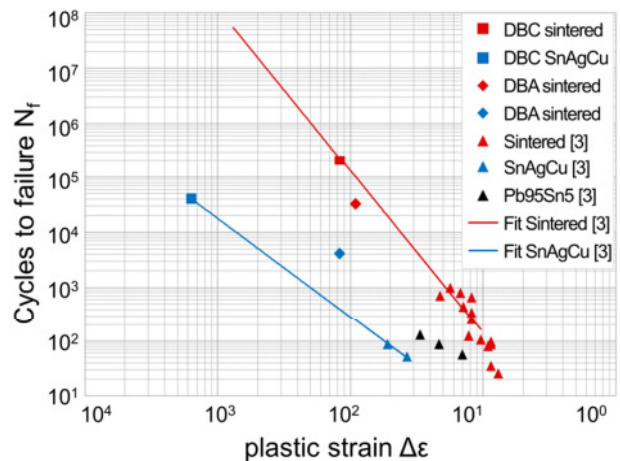


Figure 4 Coffin Manson fits of the four sample types in comparison with previous tests at Fraunhofer IISB [3]

It can be seen that by using the silver sintering technique instead of soldering and Al wired bonding, the lifetime of the samples can be increased by about 17 times. The samples with sinter technology used together with DBA sub-

strates did not reach the number of cycles to failure of the substrates with sinter technology on DBC substrates. There seems to be an additional effect that reduces the lifetime.

The samples with a complete solder mounting on DBA substrates showed a higher lifetime than the soldered and wire bonded samples on DBC substrates. This may be due to the better and more evenly heat dissipation by the Ag ribbon that replaces the Al wire bonds.

3.3 Failure modes and mechanisms

Samples of the type B failed due to bond wire lift-off, as shown in **Figure 5**. Also cracks started to grow from the edges of the SnAgCu solder layer.

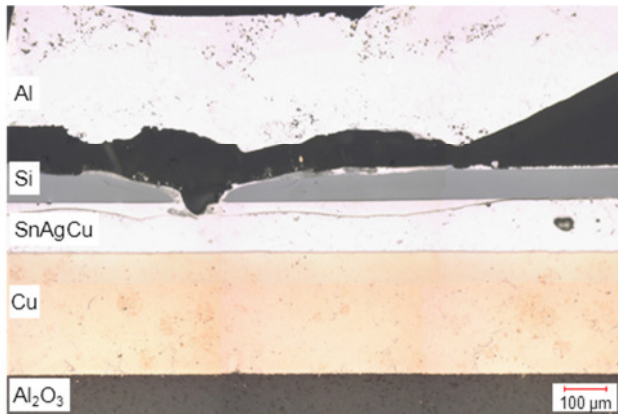


Figure 5 Bond wire lift-off as the lifetime distinguishing failure mode for sample type B at active temperature cycling tests

DBC samples with double sided sintering (sample type C) failed because of a lift-off of the Ag ribbon due to delamination of the nano silver paste, mostly followed by a local melting of the Ag ribbon and the silicon diode. The sinter layer below the diode exhibits some few big pores in the layer after sintering, whereas the sinter layer on the silver ribbon still contains finely distributed pores with an average pore size of a few micrometers, as shown in **Figure 6**. This is because the chip backside sinter layer passed two times the sintering process, whereas the upper sinter layer only has been sintered once. The pores of the lower sinter layer do not only grow during the second sintering step, but also during the following active temperature cycling.

Starting at some bigger pores, cracks grow several 100 μm into the copper of the DBC surrounded by a grey phase at their borders. With the help of EDX analysis, these regions could be identified as Cu_2O with small amounts of carbon. The oxygen and carbon is supposed to origin from leftovers by the solvents of the sinter paste.

The origin of the crack is supposed to be the combination of. Due to the Suhir's model, the maximum stress from the mismatch of the thermal expansions of the single material layers in the module is located in the sinter layer under the edges of the semiconductor device. From these edges crack growth starts. If the edges of the DCB sub-

strate itself are bended downwards at the same time, crack growth also progresses downwards into the Cu metallization.

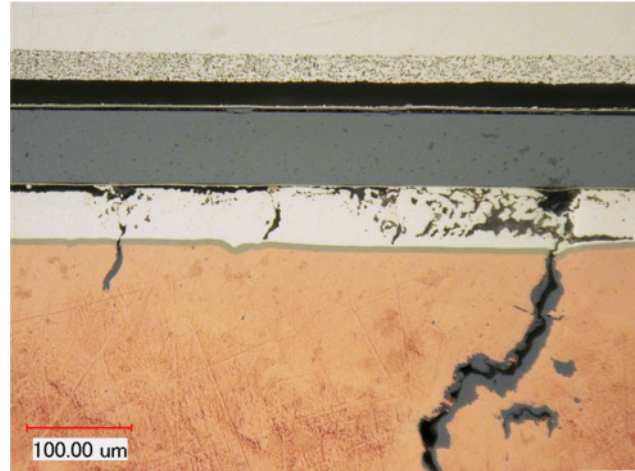


Figure 6 Delamination and cracking in silver sintered sample typ C with DBC substrate after 200,000 cycles

The failure modes of the DBA samples were similar to the DBC samples, but accompanied by the recrystallization of the aluminum of the DBA below the diode due to the locally elevated temperatures. This results in a corrugating of the aluminum surface and a smaller contact area between the diode and the substrate and, therefore, a worse cooling and short lifetime. A formation of hillocks on the surface of the DBA substrates with a diode soldered on top after active temperature cycles can be seen in **Figure 7**. This phenomenon was also observed by Gardner et al. [8] in thin films used for interconnections in integrated circuits described as hillocks appearing in these films as a result of compressive plastic deformation.

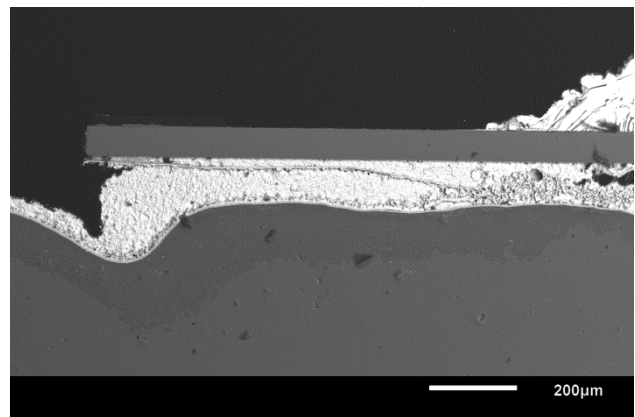


Figure 7 SEM picture of hillocks at the edges of the diode soldered on DBA substrate after active temperature cycling

Above a temperature of 0.3 times the melting temperature T_m , plastic deformation in the shape of creep processes starts in metallic materials [9]. For a temperature higher than 0.4 T_m , recrystallization does begin in materials [10]. This means that creep processes can take place at room temperature in aluminum with a melting

temperature of about 933 K and recrystallization starts at 100 °C. For copper, the starting temperatures for plastic deformation are much higher due to its high melting temperature of about 1358 K. Creeping may start at 135 °C, recrystallization at around 270 °C or higher, depending on purity.

The amount of deformation of a material also depends on the degree of pre-deformation. In the case of DBA and DBC substrates, a relatively low degree of deformation does exist. During the DBA respectively DBC process, the material is heated up close to the melting temperature at which the material softens and almost all of the stress are relaxed. Only a low amount of stress is frozen into the material during the subsequent cooling down. At a higher degree of pre-deformation in the material, recrystallization can take place, too. During recrystallization, new grains are forming in the microstructure which are growing at the expense of grains with lots of dislocations and, therefore, with a high pre-load [11]. In only slightly pre-deformed materials, strain induced grain boundary motion (SIBM) takes place and no new grains are formed, but grains with a low dislocation density grow into grains with a higher ones [11]. Therefore, it can be assumed that SIBM or even recrystallization takes place in the DBA substrates during active temperature cycling. At the same time, the grains grow and they do form a round shape to achieve a low Gibb's energy of the crystal lattice [11] resulting into a generation of hillocks on the surface.

The observed hillock formation of the DBA substrates is assumed to be the reason for the shorter lifetime in active temperature cycling tests. Due to the corrugation, the semiconductor device and the substrates are only in contact at the top of the formed hillocks which result in less contact points of the semiconductor device and the substrate and, therefore, in an inferior thermal interface.

In addition the DBA samples with a double sided soldered diode showed this corrugating effect. Here the results of the active temperature cycles are a strong disruption of the eutectic SnAgCu solder layer, as shown in **Figure 8**.

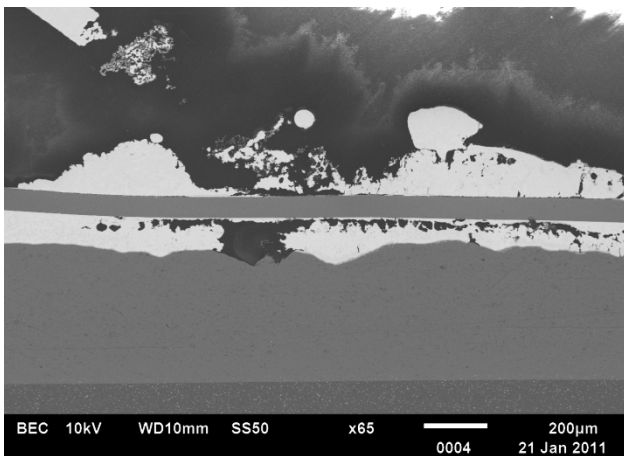


Figure 8 SEM picture of hillocks underneath the diode soldered on DBA substrate after active temperature cycles with a strong disruption of the solder under as well as on top of the diode

4 Conclusions

Power cycling with top and bottom side silver sintering on DBC substrates from +45 °C to +175 °C with 30 s cycling time showed a 17 times higher lifetime than soldered and wire bonded DBC samples. As new failure mode, delamination of the solder layer together with oxidized cracks in the Cu metallization of the DBC have been detected. DBA samples with double sided sintering survived 2.7 times longer than the soldered and wire bonded DBC samples. On DBA, the formation of hillocks on the surface of the Al layer below the diode and delamination of the sinter layer were the main failure mechanisms. With the help of double sided soldering of the semiconductor devices on DBA substrates, it was possible to show a higher lifetime compared to soldered and wire bonded DBC samples.

Further work should be carried out for power cycles of DBA substrates for lower temperature ranges to analyze the initial temperature for Al recrystallization effects or to improve the substrate in order to minimize these effects.

Independent of the investigated samples, the bottleneck of power modules lifetime is no longer the semiconductor bonding but the insulating substrate.

5 Outlook

The effect of plastic deformation of the substrate's aluminum is the lifetime increasing factor of DBAs for the passive temperature cycling test. For the active temperature cycling, this mechanic behavior is a disadvantage resulting in a lower number of cycles compared to copper metallization.

To suppress this failure mechanism, approaches based on enhancing the strength of the surface layer are considerable. The DBA substrate metal will be local hardened at the semiconductor positions and still soft at all other areas. The result should be still excellent passive temperature cycling capability and a high number of power cycles at the same time. This can either be done by a coating of the Al with Ti or W, possibly in several layers [8, 12] or ion implantation into the first surface layer to generate dislocations and, therefore, cause hardening of the surface [8]. Diffusion of partial Ag by a simple tempering process is favored.

Acknowledgements

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6 References

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