SINTO EWT SILICON SOLAR CELLS

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ABSTRACT: In this work we combine the SiNTO cell process with the EWT cell concept. All masking steps are performed by inkjet printing technology. The via-holes and laser-fired contacts are created by high-speed laser drilling. A new polishing process, which is suitable for inkjet masking, to pattern the interdigitated grid on the rear side is developed. For passivation purposes a thermal silicon oxide is used for the rear surface and a silicon nitride antireflection coating for the front surface. An e-gun evaporated aluminium/titanium/silver stack is used for the metallization, where the silver acts as a seed layer for a subsequent electro-plating step. Conversion efficiencies up to 16.9% on FZ material are obtained.
The emitter is additionally analyzed on symmetric lifetime samples. Two different emitter diffusion processes, a 35 and a 65 Ω/sq. $POCl_3$ diffusion process are regarded. An emitter diffused from a phosphorus doped silicon oxide layer in the same diffusion process as the 35 Ω/sq. emitter is analyzed as well. Emitter saturation current densities as low as 286 fA/cm^2 are reached for an oxidized emitter.
Keywords: Solar cell, lifetime, SiO_2

1 INTRODUCTION

The emitter wrap-through (EWT) cell concept first published by Gee et al [1] has the potential to reach high efficiencies using relatively moderate and low material qualities and offers a reduction of module assembly costs due to easier cell interconnection of back-contacted solar cells [2, 3]. In this work the EWT concept is combined with the silicon nitride thermal oxidation (SiNTO) process which already demonstrated high efficiencies exceeding 18% [4] on Cz material for silicon solar cells with conventional screen printed front contacts and local laser-fired rear contacts (LFC) [5].

The conventional SiNTO process features a silicon nitride which is first used as an etch mask on the front surface during the emitter removal and levelling of the texture and afterwards used as an oxidation mask during the wet thermal oxidation process. To apply the EWT process the SiNTO process has to be slightly modified.

2 EXPERIMENTAL

As a baseline process is still to be established, FZ as-cut material with 0.5 Ω*cm resistivity for the fabrication of the EWT silicon solar cells is used. The symmetric lifetime samples are processed on 1 Ω*cm FZ as-cut material. For secondary ion mass spectroscopy (SIMS) shiny etched wafers with 1 Ω*cm resistivity are used.

On each wafer three small EWT solar cells corresponding to a symmetry element of a 125x125 mm² design with two busbar pairs as proposed by Kress et al. [6] were fabricated. The process sequence starts with a saw damage removal, followed by the laser drilling of the via-holes, the laser damage removal and the texturization process.

Subsequently three different emitter profiles were applied. First a 35 Ω/sq. emitter is diffused from a liquid $POCl_3$ source in a tube furnace process. This emitter will be referred to as POCl-35. Secondly a side selective emitter is diffused as already described in [7]. Therefore a phosphosilicate glass (PSG) is deposited on the front surface prior to the tube furnace diffusion process by means of plasma enhanced chemical vapor deposition (PECVD). The PSG layer acts as a finite diffusion source. The tube furnace process is the same as for the POCl-35 emitter, which enables a moderately doped emitter on the front side and a heavly doped emitter in the via-holes and on the rear side. This process is referred to as PECVD-PSG. The third diffusion process is a 65 Ω/sq. emitter, again diffused from a liquid $POCl_3$ source. It is referred to as POCl-65.

After the emitter formation the SiNTO process sequence can be applied but with a slight modification. As the emitter on the rear surface has to be patterned to form the interdigitated grid, it is not possible to use potassium hydroxide for the emitter removal and levelling of the texture. The inkjet hotmelt ink, which is used for all patterning steps, is not stable against potassium hydroxide. A different etching process had to be developed.

Therefore in a pre-examination different solutions consisting of nitric and hydrofluoric acid were analyzed on test samples. The test samples have a textured surface and a diffused emitter. The area of the samples is 3*3 cm^2. Some of the test samples had inkjet printed structures, like the ones which are later used for the pattern of the interdigitated grid, on one side. The purpose of this examination was to find a process that can remove the emitter, level the texture and at the same time does not affect the printed inkjet mask. As the stability of the hotmelt ink is dependent on its melting point, which is around 70°C, the etching solution is not allowed to heat up. The reaction in the nitric-hydrofluoric acid solution is strongly exothermic, consequently the solution is cooled down to 8°C.

After etching the samples in the solution, a short etching step in lowly concentrated potassium hydroxide at room temperature is applied to remove the porous silicon which forms during the process. As a first hint how even the texture is, the reflection after the etching process has been measured. The reflection is increasing with the etching time until the weighted reflection reaches a value close to 34%. This value corresponds to a damage-etched surface which is a sufficient condition for the rear surface. To get a visual impression of the surface scanning electron microscope images have been taken.

The first image on the left side of Figure 1 shows the texture before the etching step. The random pyramid structure can be clearly identified. In the second picture in the middle 5 µm of silicon have been removed. Mainly the top of the pyramids have been rounded, which raises the reflection but is still not a plain surface. The last image on the right hand side shows the texture after 10 µm have been taken off. The pyramid structure cannot be seen anymore and the surface appears to be hilly. To conclude this pre-examination 10 µm abrasion seems to be sufficient to remove the emitter and level the texture in the cell process.

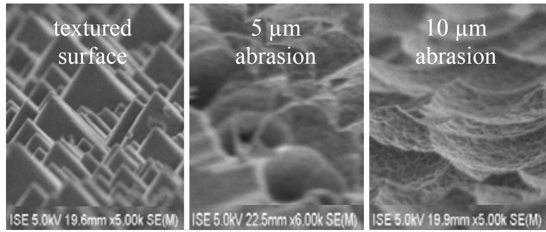

Figure 1: Surface of test samples before, after 5 µm and after 10 µm abrasion. The emitter is etched back in a nitric-hydrofluoric acid solution, followed by a short dip in 3% potassium hydroxide at room temperature to remove porous silicon which is built during the etching process.

Afterwards the process has been transferred to an industrial scale equipment. The concentration had to be adapted as the ratio of silicon to etching solution and the cooling efficiency is different. This led to a higher concentration in the industrial scale equipment but also to a faster process. The etching time could be reduced from 20 to 4 minutes.

In the EWT cell process the silicon nitride antireflection coating (ARC) has been deposited prior to the patterning of the rear emitter. This proves disadvantageous because another etching step has to be applied to create emitter windows on the front side. First the silicon nitride has to be removed from the front surface in hydrofluoric acid and afterwards the emitter removal and texture leveling can be applied. This is only relevant for a small cell area as used in this work, as for a full 125*125 mm^2 cell area no emitter windows are needed. After removal of the inkjet hotmelt ink and a cleaning step, the samples are oxidized in dichloroethene (DCE) environment. Subsequently the thermal oxide is thickened by a PECVD oxide of 90 nm thickness to improve the internal reflection.

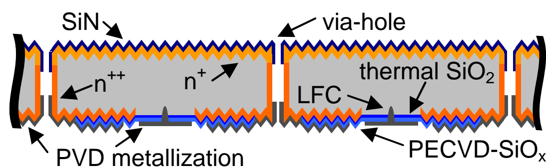

Figure 2: Cross section of the final EWT solar cell structure with a side selective emitter.

For the backend of the EWT solar cells, the oxide on the emitter has to be locally removed to contact the emitter. This is done by means of inkjet masking. A 300 µm wide line opening is created in the middle of the emitter which also includes the via-holes. Then the metallization stack is evaporated onto the rear surface by e-gun. The metallization stack consists of an aluminium layer, which is needed for the subsequently laser-fired contact formation, and a thin layer of titanium and silver. The titanium increases the adhesion between the silver and the aluminium, whereas the silver is needed as a seed layer for the following electro-plating step.

A cross section of the final cell structure can be seen in Figure 2. The image implies that silicon nitride and the metallization also reside inside the via-holes.

3 EXPERIMENTAL RESULTS

3.1 Emitter analysis by symmetric lifetime samples

To evaluate the emitter quality as well as the passivation quality of the base, symmetric lifetime samples were fabricated on 1 Ω*cm FZ as-cut material. All samples were simultaneously processed with the EWT solar cells. The seven groups, as shown in Figure 3, represent the different surface regions of the EWT solar cell with different emitter profiles and the undoped base surface, where the emitter is etched back. Group 1 represents the PECVD-PSG emitter on the front side. Group 2-4 represent the 3 different surface regions of the EWT solar cell with the POCl-35 emitter. Group 2 incorporates the front emitter surface, group 3 the rear emitter surface and group 4 the rear base surface of the EWT solar cell. Group 5-7 represent the same surfaces with a 65 Ω/sq. emitter respectively. After each step which affects the surface, lifetime measurements were done by means of quasi-steady-state photoconductance measurements (QSSPC) [8]. Measurements are evaluated at an injection level of $\Delta n = 1*10^{15}\,cm^{-3}$.

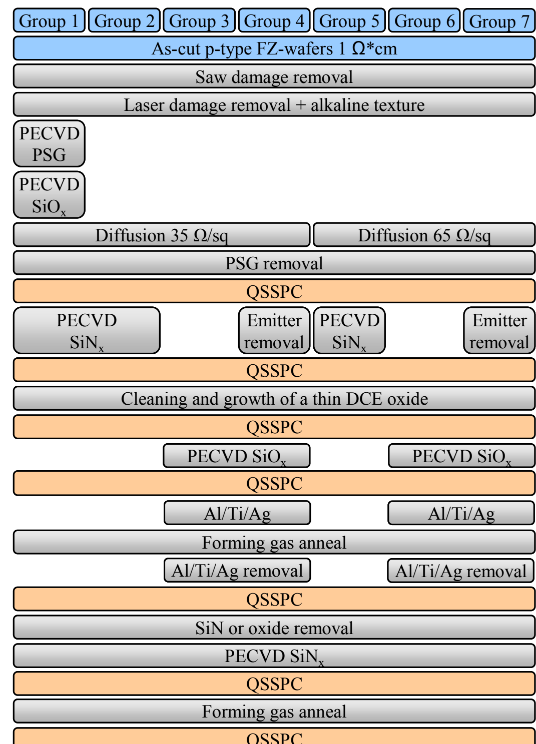

Figure 3: Process flow for the symmetric J_{0e} samples.

Under low injection the emitter saturation current density J_{0e} can be calculated by [9, 10]

$$J_{0e} = \frac{qn_i^2 W}{2(N_A + \Delta n) \cdot \left(\frac{1}{\tau_{eff}^{-1} - \tau_{Aug}^{-1} - \tau_{Rad}^{-1} - \tau_{SRH}^{-1}} - \frac{W^2}{D_n \pi^2} \right)} \quad (1)$$

where q is the elementary charge, n_i = 9.14*10^9 cm^{-3} the intrinsic charge carrier concentration, W the thickness of the sample, N_A = 1.49*10^{16} cm^{-3} the bulk doping concentration and D_n = 27.05 cm^2/s the diffusion constant.

The radiative recombination τ_{Rad} can be neglected under low injection conditions. For the Shockley-Read-Hall recombination it is assumed that it does not affect the bulk recombination significantly, which is a suitable assumption due to the use of high quality material. This means the effective lifetime τ_{eff} is only diminished by the auger recombination τ_{Aug} which can be calculated as in [11], yielding ~2 ms for the bulk lifetime (1 Ω*cm, Δn = 1*10^{15} cm^{-3}). This leaves two parameters for determination. First, the wafer resistivity is needed to deduce the bulk doping N_A and with that the diffusion constant D_n. Second, the wafer thickness W is needed. More details about the determination of J_{0e} under low and high injection conditions can be found in [9].

As can be seen in Figure 4 a high effective lifetime for the bulk material can be achieved after a post metal anneal (PMA) at 400°C for 5 minutes. This indicates that a good surface passivation quality can be achieved on the levelled rear surface. For all samples the surface recombination velocity S_0 is below 60 cm/s. It also indicates that the passivation quality is not dependent on the prior diffused emitter.

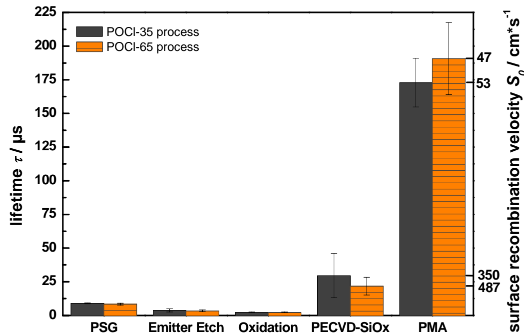

Figure 4: Effective minority carrier lifetime τ_{eff} on symmetric lifetime samples in different stadiums during the cell fabrication process. The QSSPC measurement is evaluated at an injection level Δn of 1*10^{15} cm^{-3}.

For the analysis of the different emitters the sheet resistance shown in Table 1 is regarded. As can be seen the sheet resistance R_{sh} is influenced by the oxidation process. The PECVD-PSG emitter, which has about the same sheet resistance as the POCl-65 emitter after the removal of the PSG, is less influenced by the DCE oxidation. This is due to the fact that the PECVD-PSG emitter was diffused at a temperature of 850°C, whereas the POCl-65 was diffused at 820°C. The DCE oxidation is done at a plateau temperature of 850°C. Thus, in case of the POCl-65 emitter previously inactive phosphorus is activated which leads to a lower sheet resistance. The amount of inactive phosphorus within the PECVD-PSG emitter is much smaller, causing less impact on the sheet resistance.

Table 1: Inductively measured sheet resistance of the emitter [12] after certain process steps. FS denotes the front side and RS the rear side.

Emitter	R_{sh} after PSG [Ω/sq.]	R_{sh} after DCE oxidation (FS) [Ω/sq.]	R_{sh} after DCE oxidation (RS) [Ω/sq.]
PECVD-PSG	66 (±27.21)	59 (±8.11)	
POCl-35	38 (±0.36)	28 (±0.16)	30 (±0.49)
POCl-65	65 (±0.42)	43 (±0.36)	46 (±2.45)

This can also be seen in the measured doping profiles in Figure 5. In the first image (a) the doping profiles of the PECVD-PSG emitter before and after oxidation are shown. It has to be noted that the two profiles originate from two different samples. Unfortunately the sheet resistance of the oxidized emitter is much higher, which makes a comparison of these two profiles impossible. The surface concentration is already pretty low after the diffusion. If the doping profiles are compared to the POCl-65 emitter profile after oxidation in the third image (c), it is striking that the kink part of the POCl-65 emitter profile is at higher phosphorus concentration levels, which coincides with lower the sheet resistance. The maximum electrical active phosphorus concentration n_e according to Solmi [13] is 2.84*10^{20} cm^{-3} at 850°C (dashed line in Figure 5). This means that most of the phosphorus in the PECVD-PSG and the POCl-65 emitter is electrical active after the oxidation. The POCl-35 emitter profile, which is shown in the second image (b), has a higher amount of phosphorus concentration as well as a deeper profile overall. As this emitter is also diffused at 850°C with an infinite diffusion source this is an expected result. The fraction of the electrical inactive phosphorus is much larger compared to the other two emitters. The saturation concentration of phosphorus in silicon C_{sat} lies at 4.05*10^{20} cm^{-3} (dotted line in Figure 5 b) for a diffusion process at 850°C. Above this phosphorus concentration, the phosphorus exists as SiP precipitates [13, 14] which causes lower lifetime and consequently higher saturation currents [15]. In the first 70 nm of the POCl-35 emitter the concentration is above this saturation limit. Interestingly the emitter profile seems to be deeper if no silicon nitride is deposited before the oxidation process. Although the profile is deeper the sheet resistance R_{sh} is slightly higher. This may be mainly due to the cleaning step before the oxidation which removes a few nanometer of highly doped silicon resulting in slightly smaller highly doped region. Similar trends are observed for emitter POCL-65 (see Figure 6c)

If the extracted emitter saturation current densities J_{0e} in Figure 6 are regarded, it can be seen that the PECVD-PSG emitter reaches the lowest values for the front surface and the POCl-65 emitter for the rear surface. The POCl-35 emitter has high J_{0e} values above 800 fA/cm^2 for all surfaces, which will lead to a low open-circuit

voltage V_{oc}. These results correspond well with the measured doping profiles, showing the high surface doping concentration which increases the J_{0e}. Regarding the front surfaces with SiN present during the oxidation, the PECVD-PSG emitter reaches the lowest values of about 377 fA/cm^2 after a forming gas anneal (FGA) at 400°C for 5 minutes. This seems to be reasonable as this emitter has the highest R_{sh}. Thus this emitter yields the lowest active phosphorus concentration, which will lead to less Auger recombination. For the rear side where an oxide layer passivates the surfaces, J_{0e} reaches the lowest values on the samples with a POCl-65 emitter. The oxide layer received a post metal anneal (Alneal) in a forming gas environment as a final step. For this emitter a J_{0e} of 286 fA/cm^2 could be reached.

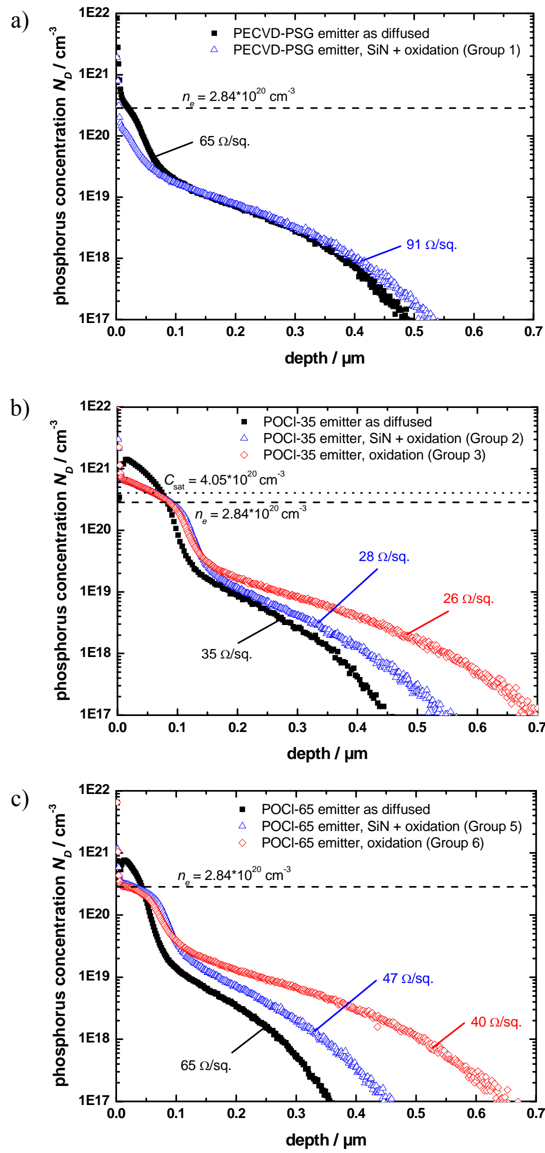

Figure 5: SIMS profiles on shiny etched samples with PECVD-PSG (a), POCl-35 (b) and POCl-65 emitter (c) after diffusion and oxidation. The maximum active carrier concentration n_e is 2.84*10^{20} cm^{-3} (dashed line) after the oxidation process at 850 °C. The saturation concentration of phosphorus is C_{sat} is 4.05*10^{20} cm^{-3} (dotted line).

On a few samples from each group, the SiN or the SiO_2 respectively was removed, and SiN was deposited on both sides (ARC New) and it was annealed for a second time at 400°C for 5 minutes. The J_{0e} could be further reduced for the front surfaces and is about the same for the rear surfaces. It is known that the hydrogen content, which could passivate dangling bonds at the Si-SiN interface, is reduced during the oxidation process. This affects the passivation quality of silicon nitride layer. An oxidation without a masking SiN_x for the front emitter is beneficial for the reduction of J_{0e}. This can be applied in a cell process without any extra process steps. As the oxide on the rear side has to be patterned for the metallization, the oxide on the front could be removed in the same process step. This would even save one inkjet printing step, which has to be applied to protect the SiN antireflection coating during the oxide removal.

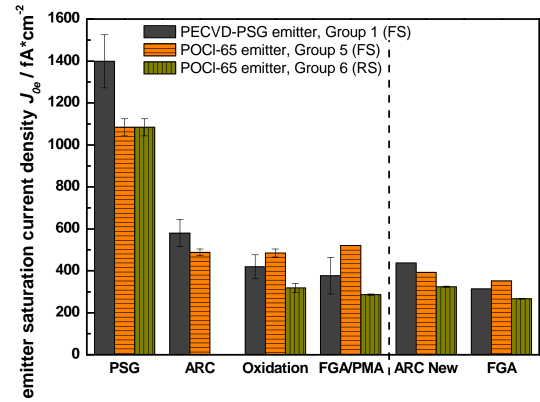

Figure 6: J_{0e} values on symmetric lifetime samples in different stadiums during the cell fabrication process.

The V_{oc}-limit is an important parameter to estimate the potential of the cell process. It can be calculated by

$$V_{oc,\max} = V_{th} \ln\left(\frac{J_{sc}}{J_{0e}} - 1\right) \tag{2}$$

where V_{th} = 25.7 mV is the thermal voltage and J_{sc} is the short circuit current density of the cell.

Assuming a J_{sc} of 38 mA/cm^2, an oxide passivation inside the via-holes, no metallization area on the rear surface and no base recombination results in a V_{oc}-limit of about 636 mV for the POCl-65 emitter. The J_{0e} values of the different surfaces are added area-weighted. If we further assume no SiN present during the oxidation the V_{oc}-limit could be pushed to 647 mV. An even higher level might be achieved by using the side selective emitter approach in the POCl-65 process, but it has to be taken into account that at some point the series resistance of the emitter will limit the cell efficiency. In practice, the base saturation current density J_{0b} and the metallization area reduce the V_{oc} of the EWT solar cells.

To summarize this chapter, the POCl-35 emitter has not the potential to reach high efficiencies. The phosphorus surface concentration is well above the saturation concentration limit, which reduces the lifetime additionally to the larger Auger recombination. This reduces the V_{oc}-limit to 615 mV of the EWT cell. With the PECVD-PSG process the V_{oc}-limit can be enhanced to 631 mV, but it still suffers from the high surface

concentration of the POCl-35 emitter inside the via-holes and on the rear side. The POCl-65 emitter process has the highest efficiency potential with a V_{oc}-limit of 636 mV due to a low J_{0e}. The V_{oc}-limit can be further enhanced to 647 mV by performing the oxidation process without the SiN antireflection coating present during the oxidation.

3.2 SiNTO EWT cell results

To analyze the EWT solar cells, they have been split up into groups. In total 4 different groups as shown in Table 2 are compared.

Table 2: Different groups of EWT solar cells.

Group Number	Emitter Process	Rear Surface Emitter Area	Rear Surface Base Area
1	POCl-35	textured (A)	polished
2	POCl-65	textured (A)	polished
3	POCl-35	textured (B)	polished
4	POCl-65	textured (B)	polished

The arithmetic mean of the cell parameters is shown in Table 3 for each group. These values were measured after an electro plating step but prior to a FGA. The fill factor *FF* has improved by the electro plating process, as the series resistance R_s of the metal fingers is reduced. On the other hand, on some cells the short circuit current density J_{sc} is slightly reduced due to overplating near the via-holes. A flower like structure can be seen at the front surface at the via-holes.

The POCl-35 emitter features the highest *FF* up to 73% due to less R_s losses on the front side and inside the via-holes. The highest V_{oc}, J_{sc} and η could be reached on the POCl-65 emitter. According to emitter analysis in the previous chapter this could be expected, as this emitter concept features the highest V_{oc}-limit. The cell parameter of the best EWT cell can be found in Table 4 (cell No. 1). The V_{oc} of 608 mV is still not close to the V_{oc}-limit of 636 mV. On the one hand the loss can be contributed to the still large metallized area on the rear emitter and the via-hole surface, as well as additional bulk recombination. On the other hand the cell is not yet annealed which implies an insufficient passivation quality.

The annealing process in a forming gas environment has the potential to raise the short circuit current density J_{sc} and the open-circuit voltage V_{oc}, as the passivation quality of the oxide layer is improved. Therefore it is essential that the annealing process can be performed at 400°C [16]. As the fabricated EWT cells feature a direct contact between aluminium and silicon, a high potential of aluminium spiking is at hand. Silicon has a high diffusivity and solubility in aluminium already at low temperatures. This degrades the cell performance as already shown in [17]. This can be seen for cell No. 2 and 3 in Table 4 in a reduction of the *pFF* and *FF* after a forming gas anneal (below dashed line) at 350°C for 5 minutes. Although the V_{oc} and J_{sc} are improved, the reduction of the *FF* diminishes the gain in efficiency (cell No. 3) or in most cases eliminates it totally (cell No.2). The values of the *pFF* clearly show that the *FF* reduction is due to a lower shunt resistance or higher recombination in the space charge region, which hints to aluminium spiking. These cells all feature a 65 Ω/sq. emitter, but the same effect is observed for all other emitters.

Table 3: Arithmetic mean of the cell parameters V_{oc}, J_{sc}, *FF*, *pFF* and η after electro plating and before annealing.

Group Number	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	*pFF* [%]	η [%]
1	593.4	35.0	71.8	76.7	14.9
2	607.2	37.7	71.7	77.2	16.4
3	596.2	34.6	73.2	78.2	15.1
4	610.7	36.9	72.4	79.1	16.3

After the forming gas anneal the V_{oc} is increased up to 620 mV, which still leaves 16 mV missing to reach the V_{oc}-limit. This missing voltage can be attributed to the base recombination as well as the highly recombinative metallized area.

Table 4: Cell parameters of three EWT cells with POCl-65 emitter. The cell below the dashed line received a FGA at 350°C for 5 minutes.

Cell No.	Group No.	FGA	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	*pFF* [%]	η [%]
1	2	no	608.1	37.9	73.6	78.9	16.9
2	2	no	607.5	37.6	71.0	76.2	16.2
3	4	no	609.3	36.9	71.3	78.1	16.0
2	2	yes	619.3	38.0	64.0	69.2	15.0
3	4	yes	617.8	38.3	69.3	76.6	16.4

To exploit the full potential of this cell concept, the main focus of further research will be set on avoiding the aluminium spiking. Therefore several possible solutions will be investigated. To get to higher efficiencies, silicon nitride will be deposited after the oxidation and the metallization area will be reduced.

4 CONCLUSIONS

It has been shown that the SiNTO process can be combined with the EWT solar cell process with some slight modifications. Therefore an inkjet feasible fast emitter etching process has been developed which can be used in an industrial scale equipment. The etching process removes the emitter and levels the texture in a single step. On such a surface high lifetimes can be achieved.

Three different emitters have been analyzed in respect to the emitter saturation current density and the doping profile. For the SiNTO process the lowest J_{0e} of 377 fA/cm^2 for the front side could be obtained with the PECVD-PSG emitter. For the rear side the POCl-65 emitter reached a J_{0e} of 286 fA/cm^2. It proves beneficial to perform the oxidation of the front surface without SiN, as lower values of J_{0e} of 268 fA/cm^2 can be reached. The emitter profiles of the PECVD-PSG and the POCl-65 emitter feature a very low inactive phosphorus concentration which enables a low J_{0e}.

The fabricated EWT solar cells can reach a V_{oc} around 620 mV and a J_{sc} around 38 mA/cm^2 after a forming gas anneal. The forming gas anneal reduces the *FF* due to a reduction of the *pFF*. The reason for this behaviour is probably aluminium spiking. The best cell reaches an efficiency of 16.9% prior to a FGA.

The main advantages of the SiNTO cell process for solar cells with front metallization, the masking ability of the SiN layer for etching and oxidation processes, are of reduced value in the SiNTO EWT cell process due to the complexity of the EWT solar cell fabrication process. The current cells are limited by a *pFF* reduction inhibiting the annealing process to yield full benefit. In future work this aspect will be addressed. As the V_{oc} limited of the SiNTO EWT cells is reduced, it might be beneficial to apply the passivation layer before the deposition of the ARC.

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