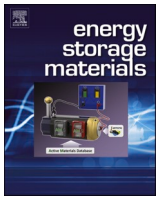
Energy Storage Materials 81 (2025) 104535

Contents lists available at ScienceDirect

Energy Storage Materials

journal homepage: www.elsevier.com/locate/ensm



Gate controlled EDL-based capacitor-diodes (G-CAPode) for switchable signal filters with logic gate functionality

Christin Gellrich [a], Przemyslaw Galek [a,*], Leonid Shupletsov [a], Julia Grothe [a], Stefan Kaskel [a,b,*]

[a] Inorganic Chemistry I, Technische Universität Dresden, Bergstraße 66, 01069 Dresden, Germany
[b] Fraunhofer Institute for Material and Beam Technology (IWS), Winterbergstraße 28, 01277 Dresden, Germany

ARTICLE INFO

Keywords:
G-CAPode
Ionic transistor, Ionic diode
3D printing
Varactor
Signal filtering, Iontronics

ABSTRACT

This work explores a novel application of the G-CAPode – a previously developed, 3D-printed gate-controlled electrochemical capacitor-diode – by demonstrating its ability to perform logic operations in ionic circuits. The G-CAPode integrates diode-like rectification, voltage-controlled switching via a gate electrode, and dynamically tunable capacitance within a single architecture. While prior studies demonstrated G-CAPodes to function as tunable capacitors – a varactor – in high-pass filters, this study extends its use toward logic operations. Specifically, frequency-dependent OR and AND logic behaviors are realized by connecting two G-CAPodes in parallel and series, respectively. In these configurations, logic output is determined by the impedance state of each device, which is dynamically controlled via gate bias. The OR-gate circuit yields a high output when at least one G-CAPode is in the ON (low-impedance) state, while the AND-gate setup requires both devices to be ON for signal transmission, consistent with Boolean logic. The switching behavior is controlled by applying specific gate biases, which modulate the impedance of each G-CAPode in real-time and therefore enables analog logic functionality using purely ionic components. The results underline the potential of the printed G-CAPode as a multifunctional platform for adaptive signal processing, offering a compact and silicon-free solution for emerging iontronic applications such as neuromorphic computing, adaptive filtering, and analog signal processing.

1. Introduction

The development of iontronic devices, electronic components that operate via ion transport instead of electron flow, has gained increasing attention in recent years, again after their initial discovery mid last century, [1] due to their unique advantages over conventional semiconductor-based electronics [2–5]. Ion-based systems can mimic biological signaling, offering new possibilities for bioelectronics, neuromorphic computing, and energy-efficient logic circuits. Unlike traditional electronics, which rely on rigid binary switching (ON/OFF states), iontronic devices can process and store information in an analog manner, leveraging the diverse properties of ions, such as size, charge, and mobility [6,7]. Therefore, iontronic devices present a shift away from the traditional von Neumann computing architecture, which relies on Boolean logic and complex wiring. By utilizing neuromorphic computing components, [8,9] ionic selective gating [10,11] and ionic diodes, [8,12] iontronic circuits can reduce the need for extensive wiring and improve energy efficiency in programmable analog logic. This approach enables simpler, more energy-efficient designs that are well-suited for complex tasks [13,14]. Another key advantage of iontronics is their ability to integrate multiple functionalities into a single device, combining energy storage, current rectification, and dynamic switching in ways that are difficult to achieve with standard electronic components. Iontronic circuits can operate in liquid and soft-matter environments, making them highly compatible with biological systems [5,15,16]. Additionally, due to their low operating voltages and energy-efficient charge transport mechanisms, iontronic devices hold promise for low-power computing applications, including logic gates and frequency-selective filtering [17,18].

One of the most promising developments in iontronics has been the CAPode (capacitor-diode), introduced in 2019, as a capacitive analogue of a semiconductor diode [19]. The original concept of the CAPode exploited ion-sieving effects to achieve unidirectional charge storage, allowing it to function as ionic diode with high rectification ratios. By

* Corresponding authors.
E-mail addresses: przemyslaw.galek@tu-dresden.de (P. Galek), stefan.kaskel@tu-dresden.de (S. Kaskel).

https://doi.org/10.1016/j.ensm.2025.104535
Received 4 June 2025; Received in revised form 6 August 2025; Accepted 11 August 2025
Available online 12 August 2025
2405-8297/© 2025 The Authors. Published by Elsevier B.V. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

carefully selecting carbon electrodes with different pore sizes and an electrolyte with asymmetric ion sizes, the CAPode enables directional charge flow. Effective charging occurs only when the system's electrodes are polarized in a specific way (under "open/chargeable" polarization; analogous to the forward bias of a diode), while charge accumulation is blocked under reverse polarization ("blocked/unchargeable" polarization) (Fig. 1a).

To facilitate miniaturization and integration into microelectronic architectures, 3D-printed in-plane CAPodes have been developed [17]. Their fabrication involves extrusion printing of mesoporous carbon (C_{meso}; omnisorbing) for one electrode, while the ultramicroporous carbon (C_{micro}; sieving) is inkjet printed using a prepolymeric aqueous solution of resorcinol and formaldehyde for second electrode (Fig. 1b). The use of 3D printing enables the automated and precise deposition of active materials onto a substrate, achieving small lateral dimensions while maintaining rectification performance similar to macroscopic CAPodes. These advancements mark an important step toward the miniaturization of iontronic circuits.

Beyond their rectification capabilities, CAPodes have been successfully implemented in basic logic circuits, including OR and AND gates. Furthermore, a switchable high-pass filter based on a CAPode was demonstrated for the first time, underscoring their potential as miniaturized and planar ion-computing elements [17]. Building upon the CAPode concept, a significant advancement was achieved with the development of the G-CAPode (gate-controlled CAPode), a device that additionally integrates transistor-like behavior into a capacitor-diode [20]. The key innovation of this system is the introduction of a third gate electrode (GE), which enables voltage-controlled tuning of capacitance and rectification behavior similar to a field-effect transistor (FET). By applying a positive or negative gate bias between the counter electrode (CE) and the GE, the electrochemical potential of both CAPode electrodes (working electrode (WE) and CE), can be dynamically shifted due to the direct connection between the GE and the CE. This modification alters the cut-off voltage (the voltage at which the system switches from low to high capacitance (impedance) and reverse), rectification properties, and effective capacitance, thereby providing an additional degree of control over charge transport. Consequently, the entire working window of the working capacitor (W-Cap), and therefore of the CAPode, shifts to positive or negative potential values depending on whether the GE is negatively or positively biased (Fig. 1c).

A very recent study introduced a printed ion-sieving-based G-CAPode, building upon previous work on printed CAPodes [18]. In this system, the GE was printed around the CAPode (acting as a W-Cap) using the same mesoporous carbon material as the CE. Alongside a detailed characterization of its switching mechanism and performance, this study also demonstrated the application of the G-CAPode in tunable high-pass filter circuits, where it functions as a varactor enabling real-time tuning of the cut-off frequency (f_C) of the filter – i.e. the threshold frequency above which signals can pass through while lower frequencies are attenuated. These results confirm the ability of the G-CAPode to act as an energy-efficient, dynamically tunable varactor, providing an alternative to traditional semiconductor-based devices. The experimentally obtained f_C values closely matched theoretical predictions, validating the feasibility of the G-CAPode in real-time signal filtering applications.

Until now, however, research has primarily focused on single G-CAPode devices in basic high-pass filter applications and in NOT gate circuits. In this work, we explore a novel application of G-CAPodes in logic circuits, demonstrating their ability to construct OR and AND gates through parallel and series connections of G-CAPodes as gate-bias-dependent filters by using AC signals. By leveraging the gate-tunable properties of the G-CAPode, these configurations enable programmable ionic logic operations, opening up new possibilities for reconfigurable iontronic circuits. This study provides a detailed characterization of the filtering behavior, explores the dependence on gate bias voltage, and demonstrates the feasibility of using G-CAPodes for frequency-based logic operations.

2. Results and discussion

2.1. Construction and mechanism of the in-plane printed G-CAPode

The in-plane printed G-CAPode system used in all studies is the same device previously presented and electrochemically characterized in detail [18]. In brief, the device consists of an asymmetric W-Cap, i.e. a

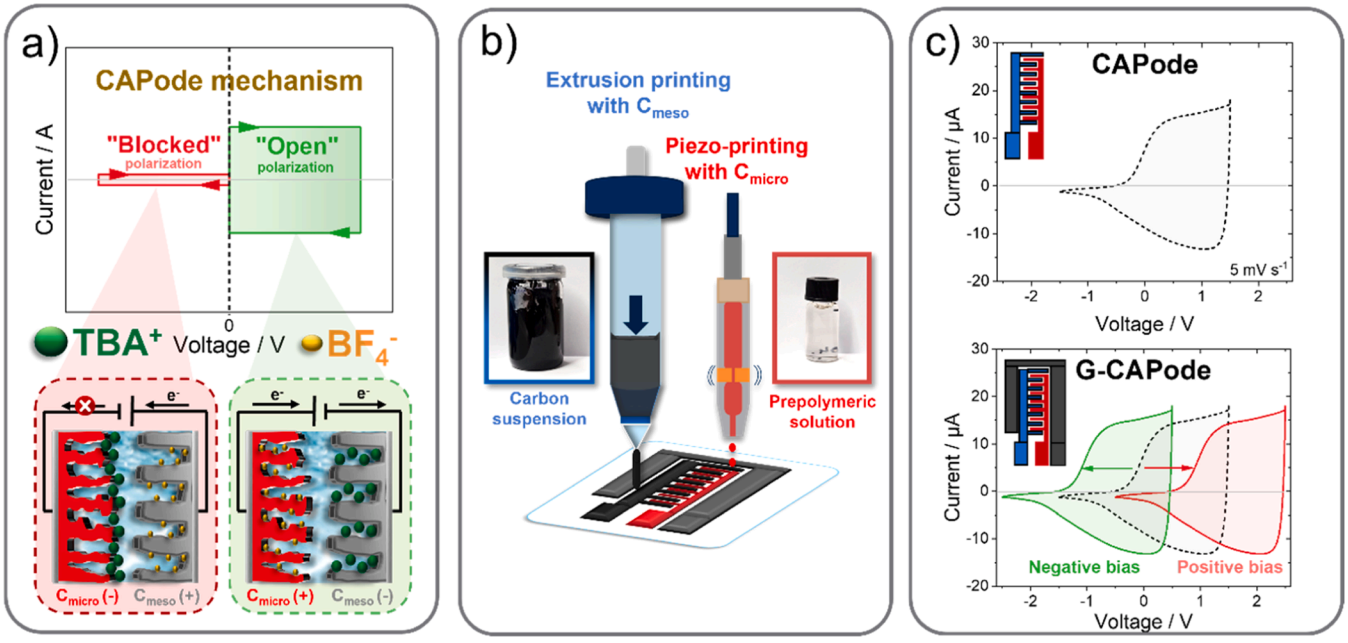


Fig. 1. (**a**) The scheme of an ideal CV curve for the ion-sieving (EDL-based) CAPode together with charge storage mechanism (reproduced with permission, [18] Copyright 2025 from Wiley Company). (**b**) The scheme of printing process of the G-CAPode using extrusion and piezo inkjet printing of the C_{meso} and C_{micro} carbons derived from a carbon suspension and a prepolymeric solution. (**c**) The CV curve registered for CAPode and scheme of working principle of G-CAPode switching the onset-voltage depending on the applied U_{bias} to GE [18].

CAPode based on the ion-sieving effect. In this asymmetric W-Cap the WE comprises an inkjet-printed C_{micro} electrode with an average pore size of 0.69 nm and an extrusion-printed C_{meso} electrode with an average pore size of 3.1 nm. Using an asymmetric electrolyte, 1 mol L^{-1} tetra-n-butylammonium tetrafluoroborate ($TBABF_4$) in acetonitrile (ACN; C_2H_3N), with a bulky cation (TBA^+; d = 1.1 nm) and a small anion (BF_4^-; d = 0.41 nm) results in a highly asymmetric CV shape, characterized by high current/capacitance under "open" polarization ("positive" voltage range) and a low, limited response under "blocked" polarization ("negative" voltage range). A third GE, printed using the same C_{meso} suspension as for the CE, ensures close proximity to both WE and CE. The geometrical dimensions match previous reports and are shown again in **Fig. S1**.

Applying U_{bias} between GE and CE shifts the W-Cap's cut-off voltage and entire working window almost linearly to more "negative" voltage (-0.39 V shift per U_{bias} = -1 V). This behavior is attributed to the potential distribution between the WE, CE, and GE. When a "negative" U_{bias} is applied to GE, its potential shifts negatively, while the CE shifts positively to maintain the applied voltage difference. Since the CE is shared within the W-Cap system, the WE also follows this shift toward more positive potentials. As a result, the entire working window of the W-Cap moves to more positive potentials, cycling more in the "open" direction, leading to a higher capacitance and lower impedance of the device. The magnitude of this shift depends on the applied U_{bias} between GE and CE, which dictates the potential difference and, consequently, the extent of the working window shift. A stepwise increase to "positive" U_{bias} progressively shifts the cut-off voltage and working window toward more positive values. As previously observed, this shift occurs almost linearly with increasing U_{bias} (0.33 V shift per U_{bias} = 1 V). Conversely, when a "positive" U_{bias} is applied to GE, its potential shifts positively, while CE shifts negatively. Consequently, the WE follows the CE's shift to more negative values, resulting in the entire W-Cap working window moving toward more negative potentials, causing the observed CV curve shift. These potential distribution between the electrodes have been investigated in the previous studies to the single printed G-CAPode device using a calculation method proposed by Slesinski et al. [18,21]. These method revealed how the applied U_{bias} modulates the local electrochemical potentials of the WE and CE, thereby shifting their cycling regions and favoring either anion or cation adsorption depending on the polarization state. Additionally, equivalent circuit modeling based on impedance spectroscopy was performed in the context of the G-CAPode's application as a switchable LC filter. The model incorporated EDL capacitances, Warburg elements, and resistive components – all of which vary with U_{bias} . These analyses provided deeper insight into the charge redistribution dynamics and validated the U_{bias}-driven modulation mechanism that governs the system's filtering performance.

2.2. Application of the G-CAPode in a high-pass filter

To rationally operate the G-CAPode in an OR and AND gate circuit using AC signals, firstly the frequency dependent behavior of a single G-CAPode requires further discussion and examination. As in detail explained in our previous study, the G-CAPode can be used as capacitor device showing switchable capacitance and impedances depending on the applied U_{bias} [18]. As already introduced in the introduction, this characteristic was exploited in a tunable high pass filter circuit, where the G-CAPode functions as a switchable varactor with dynamically changing impedances at certain frequencies, enabling real-time control over the cut-off frequency f_C and therefore over the signal attenuation or transmission of the filter at a certain frequency depending on U_{bias}

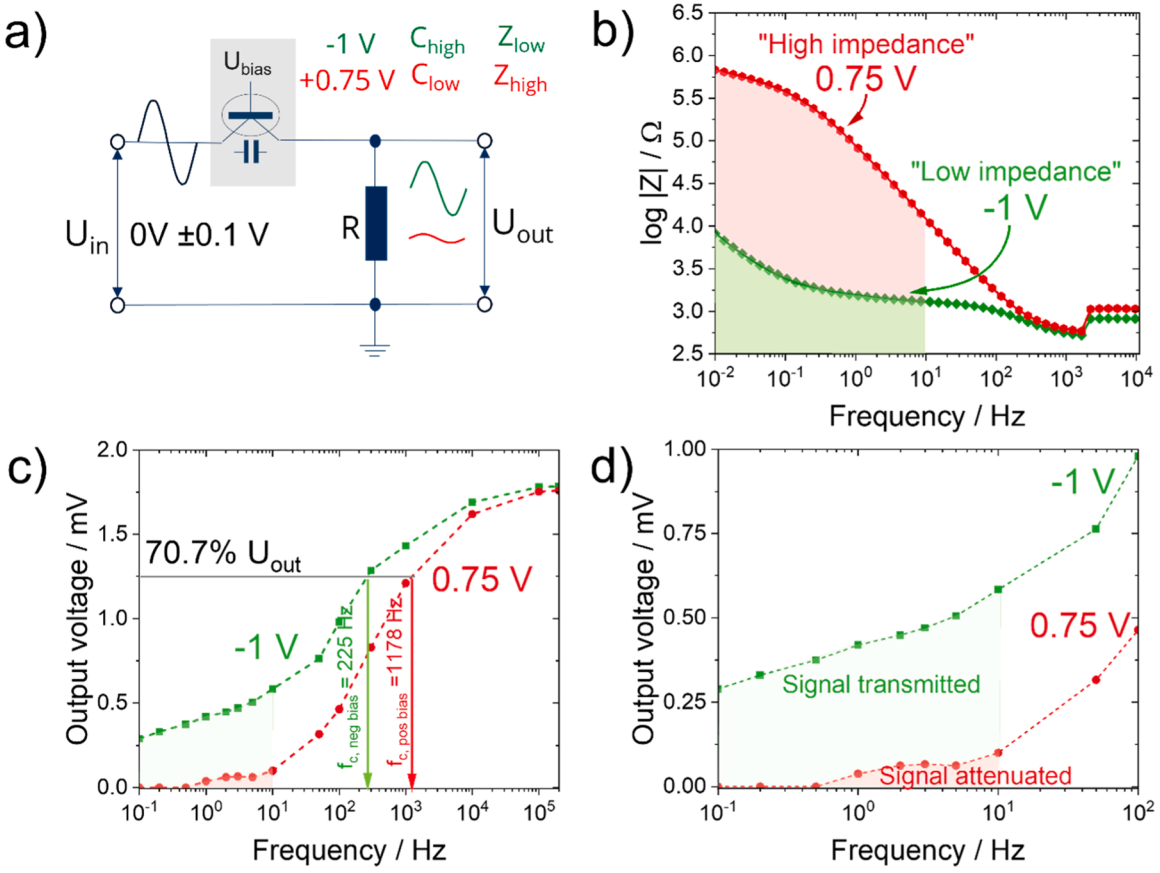


Fig. 2. Application of a printed G-CAPode in a high-pass filter (reproduced with permission [18]. Copyright 2025 from Wiley Company). (**a**) Electrical circuit of a variable high-pass filter using the G-CAPode as the device with variable capacitance. (**b**) Bode plot showing log(|*Z*|) depending on the frequency for U_{bias} = -1 and 0.75 V. (**c, d**) Registered U_{out} = f(*f*) plot for the printed G-CAPode in a high-pass filter with marked f_C exhibiting different signal transmission depending on U_{bias}.

(Fig. 2a). In short, in our former studies we presented a high-pass filter configuration, in which the G-CAPode is connected in series with a resistor (R = 1 Ω), forming a tunable RC circuit, where the f_C is determined by Eq. (1).

$$f_C = \frac{1}{2\pi R C} \quad (1)$$

By applying U_{bias}, the capacitance (C) of the G-CAPode and, therefore, its impedance can be dynamically adjusted especially in the frequency range below 10 Hz, thereby shifting f_C in real time (Fig. 2b). Previous experimental results obtained from printed G-CAPode devices demonstrated a wide range of tunable capacitances, directly influencing the filter's behavior [18]. When U_{bias} = 0.75 V was applied, the G-CAPode exhibited a minimal capacitance of 0.136 mF and a higher impedance. This was attributed to the positive bias shifting the working window into the blocked polarization region, effectively suppressing charge storage and reducing the device's capacitive response. Consequently, the cut-off frequency increased to 1178 Hz, allowing higher-frequency signals to pass while attenuating lower frequencies (Fig. 2c,d). In contrast, when U_{bias} = -1 V was applied, the capacitance increased to 0.814 mF leading to a lower impedance, as the negative bias enhanced charge accumulation in the "open" polarization region, leading to a significantly higher capacitive response. This resulted in a lower cut-off frequency of 225 Hz, meaning a broader range of low-frequency signals was allowed to pass compared to the case with high bias. These measured f_C values, defined as the frequency at which output voltage (U_{out}) is 70.7 % of input voltage (U_{in}), were determined empirically from frequency sweep measurements (Fig. 2c). We emphasize that f_c does not mark a sharp transistion between "blocking" and "non-blocking" states, but instead indicates where signal attenuation becomes significant. While Eq. (1) provides a useful approximation for f_C, it assumes a frequency-independent, ideal capacitance. However, in iontronic systems like the G-CAPode, the capacitance is highly frequency-dependent due to ion transport limitations, pore accessibility and nonlinear charge storage behavior. However, from Fig. 2b one can estimate that below 10 Hz the impedance difference (and therefore capacitance difference) is significant and highly U_{bias}-dependent and tunable. The ability to precisely control the f_C by simply adjusting the U_{bias} demonstrates the versatility and energy efficiency of the G-CAPode for adaptive signal processing and frequency-selective applications.

2.3. The construction of a frequency-depended OR logic gate circuit

Based on our previous findings summarized in chapter 2.2, we aimed to utilize the switchable impedance and capacitance adjustment of the G-CAPode to build more complex circuits for simple logic gate functions. In this section, two G-CAPodes, functioning as switchable high-pass filters are connected in parallel to construct a logic gate circuit with OR behavior (Fig. 3a). The connection to poteniostat/galvanostat is presented in **Fig. S2** and further described in the experimental part.

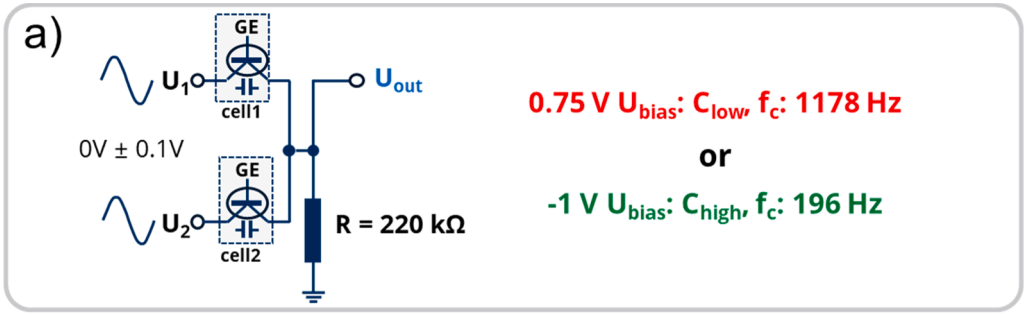
The goal of this setup is to demonstrate frequency-dependent signal transmission, where the U_{out} is measured across a 220 kΩ resistor connected to the ground. The applied input voltages (U_1 and U_2) are synchronized, oscillating at 0 V with 0.1 V amplitude (i.e., a total voltage difference is 0.2 V). The frequency of this AC component is varied between 0.1 Hz and 500 Hz. The switching behavior of each G-CAPode is controlled by applying a constant U_{bias} between GE and CE. Therefore, U_{out} consists of a DC level, determined by the constant U_{bias} applied to the G-CAPodes, modulated with a frequency-dependent AC signal. Only the AC component of U_{out} is analyzed to assess the signal transmission characteristics. Consistent with the previous high-pass filter studies, a U_{bias} = -1 V places the device in the ON state, characterized by a high capacitance and a low f_C, allowing low-frequency signals to pass. Conversely, applying a positive U_{bias} = 0.75 V shifts the G-CAPode into the OFF state, resulting in a low capacitance and a high f_C, thereby blocking lower-frequency signals.

In a parallel circuit, U_{out} is determined by the combined response of both G-CAPodes at a given frequency. In general, the U_{out} of this circuit follows the voltage divider equation (Eq. (2)) for a parallel impedance network.

$$U_{out} = U_1 \cdot \frac{Z_{cell2}}{Z_{cell1} + Z_{cell2}} + U_2 \cdot \frac{Z_{cell1}}{Z_{cell1} + Z_{cell2}} \quad (2)$$

Where U_1 and U_2 are the input voltages applied to the two G-CAPodes, Z_{cell1} and Z_{cell2} are the impedances of the two G-CAPodes and U_{out} is the resulting output voltage across the resistor. By assuming the G-CAPode behaves as an RC element, consisting of a frequency-dependent capacitive impedance and an internal resistive component (R_i). The total impedance (Z_{cell}) of a single G-CAPode can be expressed by Eq. (3).

$$Z_{cell} = R_i + \frac{1}{j\omega C} \quad (3)$$



b)

	U_{bias} = -1 V for cell1 and cell2	U_{bias} = -1 V for cell1 / U_{bias} = 0.75 V for cell2	U_{bias} = 0.75 V for cell1 and cell2
Impedance	$Z_{cell1+2}$ are both low	Z_{cell1} is high, Z_{cell2} is low	$Z_{cell1+2}$ are both high
U_{out} equation	$U_{out} \approx U_{in}$ (no/low residual impedance)	$U_{out} \approx U_{in}$ (no/low residual impedance, perfect blocking effect)	$U_{out} \approx 0$
U_{out}	High U_{out}	High U_{out}	Low U_{out}
Logic gate state	„11" state	„10" or „01" state	„00" state

Fig. 3. (**a**) Circuit diagram of two G-CAPodes connected in parallel (U_1, U_2: 0 V (±0.1 V) and applying U_{bias} = -1 or 0.75 V as input to switch the devices ON/OFF) and (**b**) comparison of the three different logic gate states.

Where R_i is the internal (ohmic) resistance, C the tunable capacitance of the G-CAPode, ω is the angular frequency and j the imaginary unit, representing the phase shift introduced by the capacitor. Therefore, the voltage divider equation describes how U_{out} is a weighted sum of the two U_{in}, with the weighting factors determined by the relative impedances of each G-CAPode.

According to Eq. (2), U_{out} is determined by the combined response (impedance) of both G-CAPodes at a given frequency and is therefore dependent on their individual ON or OFF states. Assuming that the two G-CAPodes are identical and can shift independently from each other without mutual influence, the following three cases can be distinguished:

1. Both G-CAPodes in the ON state (U_{bias} = -1 V for each device applied representing the "11" state; high capacitance; low f_C). In a certain input frequency range, both G-CAPodes allow the signal to pass, leading to a high U_{out}. This corresponds to the logical "11" state in an OR function, where the signal is fully transmitted. Ideally, both G-CAPodes exhibit the same capacitance and therefore the same diminished impedance. Eq. (2) simplifies to Eq. (4) and the full signal should pass without attenuation.

$$U_{out} = \frac{U_1 + U_2}{2} \approx U_{in} \quad (4)$$

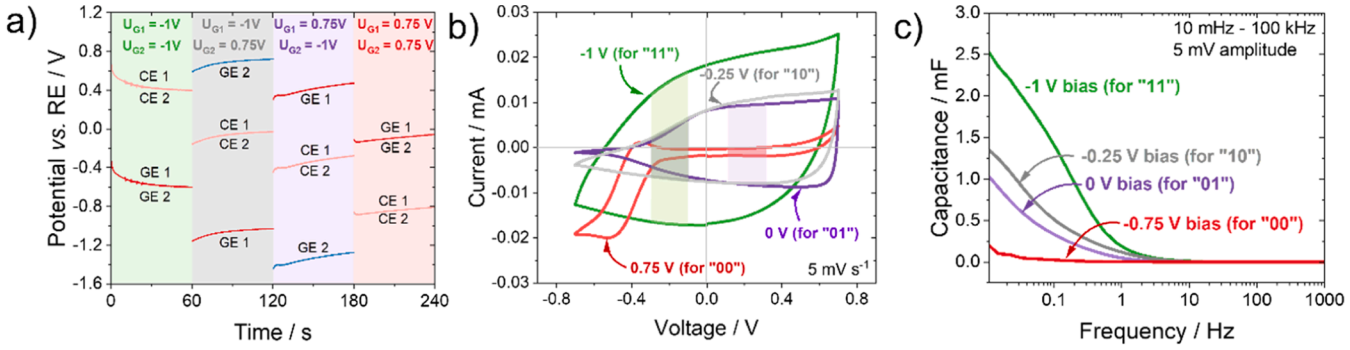
2. One G-CAPode is in ON stage (U_{bias} = -1 V) and one G-CAPode is in OFF stage (U_{bias} = 0.75 V). In this configuration, signal transmission is primarily governed by the G-CAPode in the ON state, as it exhibits a low impedance and thus only a minimal voltage drop. The OFF-state G-CAPode, in contrast, behaves effectively like an open circuit due to its high impedance, resulting in a significant voltage drop across it. Since the two devices are arranged in parallel, U_{out} closely matches the input signal amplitude. This is because the ON-state device provides a path with minimal voltage drop, thereby dominating the output signal, while the OFF-state device does not influence the output significantly. This behavior reflects an OR logic operation: whether the input is "10" or "01", the output remains high and comparable to the "11" case, as at least one conducting (low-impedance) path ensures signal transmission. This approximation holds as long as the ON-state impedance remains sufficiently low relative to the overall system conditions (Eq. (4)).

3. Both G-CAPodes are in the OFF state (U_{bias} = 0.75 V; low capacitance; high f_C). When both G-CAPodes are in the OFF stage, they exhibit low capacitance and a high f_C, meaning that within a certain frequency range, both devices block the signal. In this case, no significant U_{out} is detected (~0), corresponding to the logical "00" state in an OR function.

As explained above and in detail in reference [18,20], the switchability and tunable capacitance of the G-CAPode depends on the GE's ability to shift the CE potential to lower or higher values, therefore shifting the whole W-CAP potential window to higher values (W-CAP cycles under "open" polarization; high capacitance) and lower values (W-CAP cycles under "blocked" polarization; low capacitance). However, this shifting was only explained in one device without any connection to other cells and circuit elements. However, to implement the G-CAPode in logic gate circuits, several G-CAPodes need to be connected by their CE (in parallel) or between CE and WE (in series). In this case, the potential shifts of the two W-CAPs cannot be induced separately from each other anymore.

To verify the hypothesis made above and to understand changes in the shifting ability when two cells are connected, a parallel filter using two G-CAPodes, as shown in Fig. 2a, was first constructed. To gain a more detailed insight into the switching behavior and the potential shifting of the GE and CE in two connected cells upon applying the same or different U_{bias}, a non-aqueous reference electrode (RE; Ag/AgCl/0.01 mol L^{-1} $AgNO_3$ in 0.1 mol L^{-1} TBAP) was used to track the different polarization of the GE and CE (Fig. 4a) of the two G-CAPodes in the circuit (**Fig. S3**).

As input signals, synchronized and equal voltages U_1 and U_2, oscillating between 0 V (±0.1V), were applied at a frequency of 1 Hz to ensure that distinct capacitances in the ON and OFF states could be observed. In the experiment, a 60 s long U_{bias} pulse was applied, starting with both cells at U_{bias} = -1V (both in the ON state; "11"). Then, the U_{bias} of one cell was changed to 0.75 V, while the other remained at -1 V (one cell in the ON state, the other in the OFF state; "10"), followed by switching the states vice versa ("01"). Finally, both cells were set to U_{bias} = 0.75 V (both in the OFF state, "00") (Fig. 4a). For all applied U_{bias} values, it is evident that the potentials of the two CEs of the G-CAPodes are identical due to their direct connection in the circuit. As a result, the individual shifting of each CE is restricted to some extent, as they act as a single, unified electrode rather than independent entities. This behavior



d)

Frequency / Hz	Capacitance for $U_{bias,G1}$ = -1 V $U_{bias,G2}$ = -1 V „11" state	Capacitance for $U_{bias,G1}$ = -1 V $U_{bias,G2}$ = 0.75 V „10" state	Capacitance for $U_{bias,G1}$ = 0.75 V $U_{bias,G2}$ = -1 V „01" state	Capacitance for $U_{bias,G1}$ = 0.75 V $U_{bias,G2}$ = 0.75 V „00" state	Relative difference between „11" and „00" state / %
0.1	1.34 mF	0.51 mF	0.33 mF	0.02 mF	99
1	0.19 mF	0.12 mF	0.05 mF	0.0048 mF	97
10	11.60 µF	7.76 µF	2.84 µF	1.82 µF	84
500	2.90 µF	1.05 µF	1.03 µF	1.34 µF	54

Fig. 4. (**a**) Potential distribution of the CE and GE of the two G-CAPodes connected in parallel for the four different logic gate states, (**b**) CV curves of one G-CAPode when different bias voltages are applied with marked working window of the WE and CE in the final logic gate (0 V (±0.1 V)) corresponding to the potentials gained from (**a**), (**c**) *C(f)* – plot for different applied U_{bias} gained from the impedance spectra measured at CE potentials from (**a**).

directly influences the potential distribution across the system and differs from previous studies where the CE potential was more flexible due to its lower mass and capacitance relative to the larger GE. When both U_{bias} values are set to -1 V, the CE electrodes stabilize at approximately 0.4 V *vs*. RE, while the GE electrodes shift to -0.6 V to maintain the required U_{bias} = -1 V. As a result, both CEs are cycling predominantly under "open" polarization of the CAPode leading to a high capacitance (green region in Fig. 4a, b). Note, that the cycling region (voltage values) marked in Fig. 4b was determined from the potential distribution plot (one example for U_{bias} = -1 V is shown in **Fig. S4**). In cases where the two U_{bias} values differ (e.g. one at -1 V and the other at 0.75 V), the ability to shift the CE potentials compensates for CE1 and CE2, resulting in the CE potentials settling near 0 V (gray or violet region in Fig. 4a, b), whereas the GEs undergo significantly larger potential shift to accommodate the imposed U_{bias} condition (in total the CE potential slightly shifts toward the negative range since the U_{bias} = -1 V slightly overcompensates the U_{bias} = 0.75 V). This behavior contrasts with previous findings, where the CE potential exhibited greater variations due to its lower mass and capacitance, while the larger GE remained relatively stable. In the current circuit configuration, the direct connection of both CEs causes them to function as a single, combined electrode, thereby limiting their individual potential shifts. As a result, the GE potentials, which must shift independently to achieve the required U_{bias} = 1 and 0.75 V, undergo more significant potential adjustments. Due to the uneven U_{bias} values of -1 and 0.75 V applied to cell1 and cell2, the CE potentials in the "10" and "01" states differ slightly (0.031 and -0.28 V *vs.* RE), causing a slight asymmetry in their shifts. When both U_{bias} values are positive, the CE electrodes shift further into the negative potential range, stabilizing at approximately -0.8 V *vs.* RE, while the GE electrodes settle around -0.25 V *vs.* RE. Consequently, both CEs shift to the negative potential range of the CAPode (into the "blocked" direction), resulting in low capacitance.

As it was explained for Fig. 3a, although the CEs of the two G-CAPodes function as a single electrode and consequently shift to the same potential window upon U_{bias} application, resulting in identical capacitance changes for both devices, the overall CE potential can still be tuned to high, middle, or low values. These potential variations correspond to high, middle, and low capacitances, which are fundamental for achieving the desired impedance modulation in the system and, ultimately, the OR-gate behavior (Fig. 3b). However, since the shifting of the two CE is accompanied by a larger shift of the individual GE to meet the desired U_{bias}, the overall CE potential adjustment is more restricted in this configuration compared to a single-device setup. As a result, unlike theoretical expectations described above, the G-CAPodes in the "10" and "01" states do not switch independently between ON and OFF states. Instead, they adopt an intermediate state where the capacitance takes on a moderate value rather than distinctly high or low values.

To prove this and to assess the capacitances obtained in the different cases from one device, impedance measurements were performed at the specific CE potential points. From the imaginary part the capacitance can be calculated according to Eq. (5).

$$C = \frac{1}{2 \cdot -\mathrm{Im}(Z) \cdot f} \quad (5)$$

According to Fig. 4c, d, the capacitance values vary significantly depending on the applied U_{bias}, especially for frequencies below 10 Hz. Therefore, we estimate the "critical" frequency at which the capacitance of the G-CAPodes can be significantly tuned depending on the applied U_{bias} at ≈10 Hz. At 0.1 Hz, for instance, a capacitance of 1.34 mF is achieved, when U_{bias} = -1 V is applied, corresponding to the fully ON state of the device (to obtain the "11" stage). In contrast, if U_{bias} = 0.75 V is applied, representing the fully OFF state, the capacitance drops drastically to only 0.02 mF (corresponding to the input for the "00" stage). For the "10" and "01" logic stages where one device is ON and the other is OFF, as expected intermediate capacitances are reached corresponding to 0.51 mF ("10" stage) and 0.33 mF ("01" stage). The difference between these two values arises from the slightly asymmetric U_{bias} applied (-1 and 0.75 V) leading to asymmetric shifts in the CE potentials and thus slightly different capacitance responses. As expected, because the CE terminals are electrically coupled in the parallel configuration, they float to a shared potential influenced by both gate biases. This coupling limits the independent switching of each device and leads to intermediate capacitance values, which explains why the capacitances in the "10" and "01" states do not reach the values observed in the "11" state. As the frequency increases, these capacitance differences diminish significantly. At 500 Hz, the variations become marginal. This behavior is attributed to the decreasing capacitive reactance at higher frequencies, which reduces the influence of U_{bias} induced changes in capacitance. At such high frequencies, the dominant contributions stem from bias-independent factors such as contact resistances and bulk electrolyte resistance, rather than from the capacitive behavior of the devices.

In the following, firstly low frequencies of 0.1 Hz were tested in the described OR gate circuit using the four possible U_{bias} combinations presenting the 11, 10, 01 and 00 state (Fig. 5a).

The results clearly demonstrate that the "11", "10", and "01" states exhibit a high U_{out} amplitude, with a maximum of 48 mV for the '11' state when both G-CAPodes are in the ON state with a U_{bias} = -1 V (Fig. 5a). When only one device is in the ON state (U_{bias} = -1 V), while the other remains in the OFF state (U_{bias} = 0.75 V), the output amplitudes are 31 and 35 mV, respectively. However, when both devices are in the OFF state, U_{out} amplitude drops significantly to below 1 mV, representing the "00" state. As shown in the output voltage profile the overall position (offset) of U_{out} is influenced by the polarization at the junction point of the circuit and is primarily determined by the applied U_{bias}. When both U_{bias} values are set to -1 V (green region), the entire U_{out} signal shifts toward negative values, whereas when both U_{bias} values are set to 0.75 V (red region), the offset shifts toward positive values. As shown in Fig. 4a, d, adjusting the capacitances via U_{bias} in the different four bias state combinations allows fine-tuning of the capacitance to high, middle, and very low values. This, in turn, directly influences U_{bias} of the logic gate circuit leading to an OR-gate voltage profile.

Each time the bias switches between positive and negative, a steep increase in absolute voltage is observed. This is due to the charging of the GE/CE half-system, which adjusts to establish the desired U_{bias}, thereby temporarily influencing the detected U_{out}. However, after this initial charge redistribution, the voltage rapidly equilibrates within a few seconds, stabilizing at a total voltage determined by the interplay of the U_{bias} voltages modulated by the superimposed alternating signal with distinct high and low outputs amplitudes corresponding to the applied biases (logic gate states). The crucial factor for the logic functionality is not the absolute value of U_{out}, but rather its amplitude. It is this amplitude variation that governs effective signal transmission and enables the differentiation between logical states, ensuring reliable logic gate operation.

To investigate the influence of different input frequencies, higher frequencies were also tested. Similar results to the 0.1 Hz experiment were observed at frequencies ten times higher (1 Hz; Fig. 5b) and 100 times higher (10 Hz; **Fig. S4**). At a frequency of 1 Hz with an input signal of 0 V (±0.1 V), a significant impedance difference remains between the ON (U_{bias} = -1 V) and OFF (U_{bias} = 0.75 V) states. As a result, the '00' state produces a very low U_{out} of only 2 mV, while the "10" and "01" states yield 23 and 24 mV, respectively, approximately half of the U_{out} observed in the "11" state. This confirms an OR-gate behavior, where the output remains high when at least one device is in the ON state. At 10 Hz, the difference between ON and OFF states begins to diminish due to a reduction in the impedance contrast between the G-CAPodes at U_{bias} = -1 and 0.75 V (**Fig. S5**). Consequently, the "00" state no longer remains as low as at 1 Hz and approaches approximately half of the "10" and "01" states, indicating a loss of distinct logical differentiation.

The ability to differentiate between logic states is only feasible within a specific frequency range where the G-CAPodes exhibit distinct

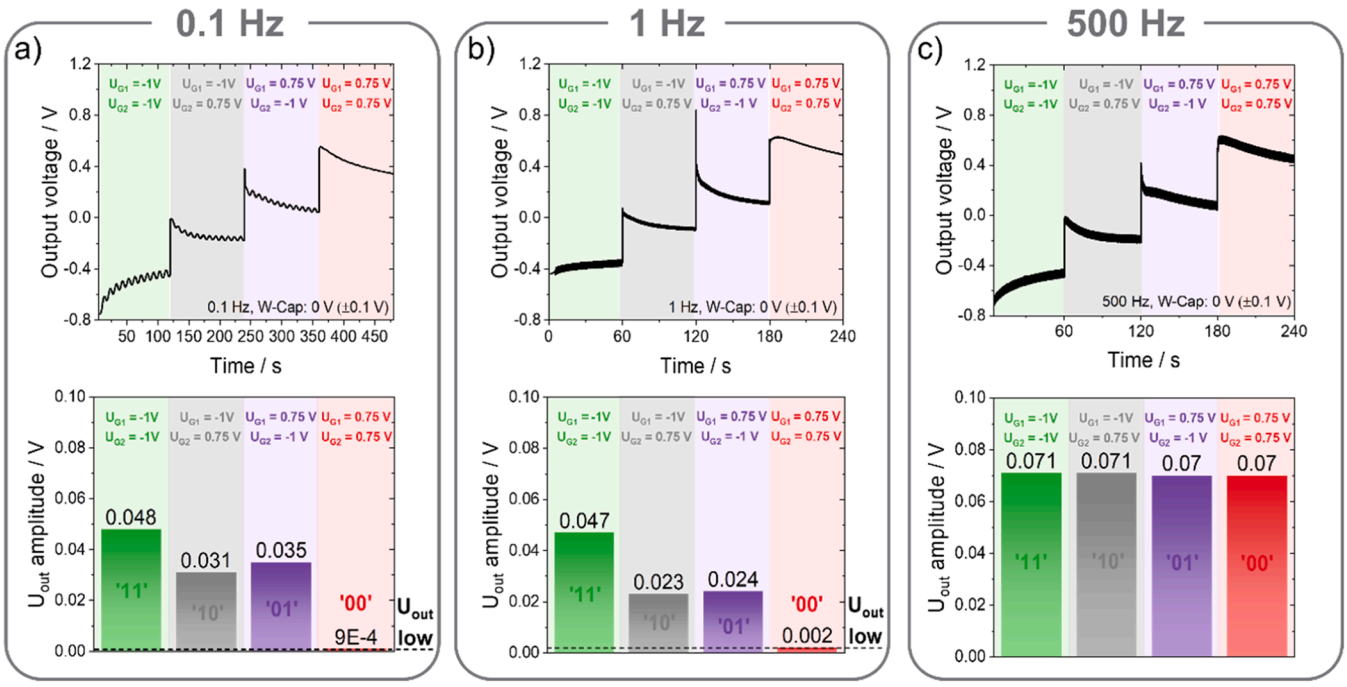


Fig. 5. U_{out} and U_{out} amplitude depending on different U_{bias} in parallel connection using U_{in} = 0 V (±0.1 V) for both cells with a frequency of (**a**) 0.1, (**b**) 1, and (**c**) 500 Hz.

impedance behavior depending on the applied gate bias. Previous studies on high-pass filters have demonstrated that the impedance and phase shift of the G-CAPode are strongly voltage-dependent at low frequencies, particularly below 50 Hz. As frequency increases, these differences gradually diminish, and above 500 Hz, the response is dominated by voltage-independent effects such as electrolyte resistance, cable and contact resistances and other parasitic phenomena. In this regime, the devices behave similarly regardless of the applied U_{bias}, effectively eliminating the distinction between ON and OFF states. At high frequencies, the circuit ceases to function as an OR gate since the filtering properties are no longer tunable via the gate bias. This behavior is evident when the input frequency reaches 500 Hz (Fig. 5c), where the expected differentiation between logic states is lost. At 500 Hz, no significant difference in U_{out} amplitude is observed between the different logic states, as the impedance of the G-CAPodes at such high frequencies becomes nearly identical. This results from the fact that, at higher frequencies, the capacitive reactance decreases significantly, reducing the influence of capacitance variations induced by the applied U_{bias}. Consequently, no clear distinction between ON and OFF states can be tracked, leading to a loss of the gate-tunable filtering effect and the OR-gate function. As the frequency increases, the overall impedance of the G-CAPodes decreases, transitioning from being dominated by ion diffusion resistances to being dominated by contact and electrolyte resistances at higher frequencies. This shift in impedance characteristics leads to an increase in the overall U_{out} amplitude, rising from 48 mV at 1 Hz to 71 mV at 500 Hz. The increase in U_{out} can be attributed to the decreasing capacitive reactance, which allows a greater proportion of the input signal to pass through. However, despite this increase, U_{out} still does not reach the full input voltage U_{in}. This discrepancy arises from several factors. Although 500 Hz is relatively high, the capacitive reactance of the G-CAPodes is not yet negligible and still contributes to the overall impedance. This remaining impedance leads to a voltage drop across the devices, limiting full signal transmission. Moreover, slight differences in the internal resistances of the two G-CAPodes can create an imbalance in the voltage divider network, resulting in an asymmetric voltage distribution. The 220 kΩ output resistor also affects the voltage transfer, as part of the input signal is dropped across the combined impedance of the G-CAPodes. At higher frequencies, additional effects such as phase shifts between voltage and the modulated AC component can further reduce the effective U_{out}.

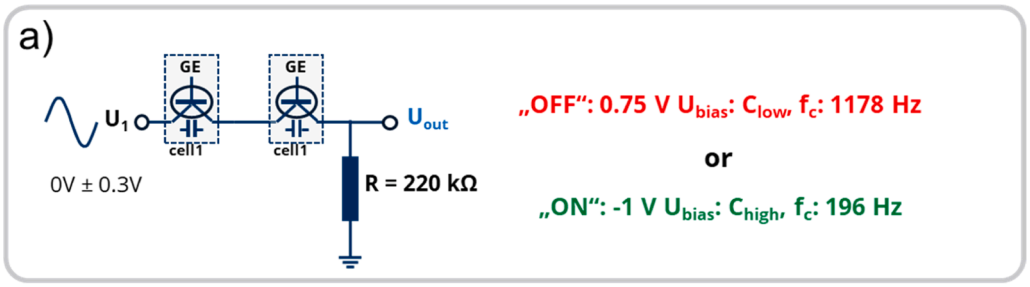
To highlight the difference between the G-CAPode results and a symmetrical reference system, the same experiment was conducted using two symmetrical supercapacitors, consisting of a WE, CE, and GE all printed using the same C_{meso} material with identical structural design like the G-CAPode. Due to the symmetrical W-Cap construction, no blocking or rectifying behavior is observed (symmetrical CV shape) and no switching of capacitance or impedance via U_{bias} is expected (**Fig. S6**). As a result, across all logic gate input states no variation in output voltage amplitude is observed. This underlines that the logic-gate-like behavior and voltage modulation seen in the G-CAPode system arise specifically from its asymmetrical, bias-dependent structure, which enables capacitance switching and selective conduction, features not present in a fully symmetrical system.

Another way to connect G-CAPodes together is by using a serial connection, which, in principle, exhibits behavior similar to that of an AND logic gate. Unlike the parallel connection, where both inputs are applied to each cell, in the serial configuration, only one input is applied to the first G-CAPode (cell1), and the output of cell1 is used as the input to the second G-CAPode (cell2). In this configuration, the CEs are not directly connected to each other; rather, the CE of cell1 is connected to the WE of cell2 (Fig. 6).

As in the previous experiments, the input voltage is an AC signal with a peak value of 0 V (±0.1 V), and the output is measured across a 220 kΩ resistor placed after cell2. The impedance of each cell can be adjusted by varying the applied U_{bias} for the two cells, which alters the capacitance and therefore impedance of each varactor. In a series circuit, the same current flows through both varactors, but the voltage is divided between them according to their respective impedances. The total impedance of the series connection is the sum of the individual impedances of the two cells (Eq. (6)).

$$Z_{total} = Z_{cell1} + Z_{cell2} \quad (6)$$

As described in Eq. (3), the impedance of one cell is determined by the capacitive reactance and the internal (ohmic) resistance.



b)

	U_{bias} = -1 V for cell1 and cell2	U_{bias} = -1 V for cell1 U_{bias} = 0.75 V for cell2	U_{bias} = 0.75 V for cell1 and cell2
Impedance	$Z_{cell1+2}$ Z_{total} are both low, is low	Z_{cell1} is high, Z_{cell2} is low, Z_{total} is high	$Z_{cell1+2}$ Z_{total} are both high, is very high
U_{out} equation	$U_{out} \approx U_{in}$ (no/low residual impedance)	$U_{out} \approx U_{in}$	$U_{out} \approx 0$
U_{out}	High U_{out}	Low U_{out}	Very low U_{out}
Logic gate state	„11“ state	„10“ or „01“ state	„00“ state

Fig. 6. (**a**) Circuit construction of the two G-CAPode connected in series (U_{in}: 0 V (±0.1 V), and applying U_{bias} = -1 or 0.75 V as input to switch the devices ON and OFF) as well as (**b**) comparison of the three different logic gate states.

Since an AC voltage divider is formed between the combined series impedance of the G-CAPodes and the external circuit (with the assumption that the load impedance is much larger and does not significantly influence the voltage drop), the output voltage amplitude at the end of the circuit (after cell2) is given by Eq. (7).

$$U_{out} = U_{in} \cdot \frac{Z_{ext}}{Z_{ext} + Z_{total}} \tag{7}$$

Where Z_{ext} is the impedance of the external circuit, primarily determined by the load resistor, and Z_{total} is the combined impedance of the two varactors in series.

When both varactors are in the ON state (“11”), their capacitance is high, leading to a low total impedance. As a result, in an ideal case, nearly the entire input voltage appears at the output, meaning $U_{out} \approx U_{in}$, assuming no residual impedance (no ohmic resistances in the G-CAPode). This behavior mirrors the expected operation of an AND gate, where the output is high only when both inputs are high. In contrast, when both varactors are in the OFF state (“00”), their capacitance is low, resulting in a high total impedance. Consequently, most of the input voltage drops across the varactors, and only a very small voltage appears at the output. For the intermediate states (“10” and “01”), where one varactor is ON and the other is OFF, the total impedance remains

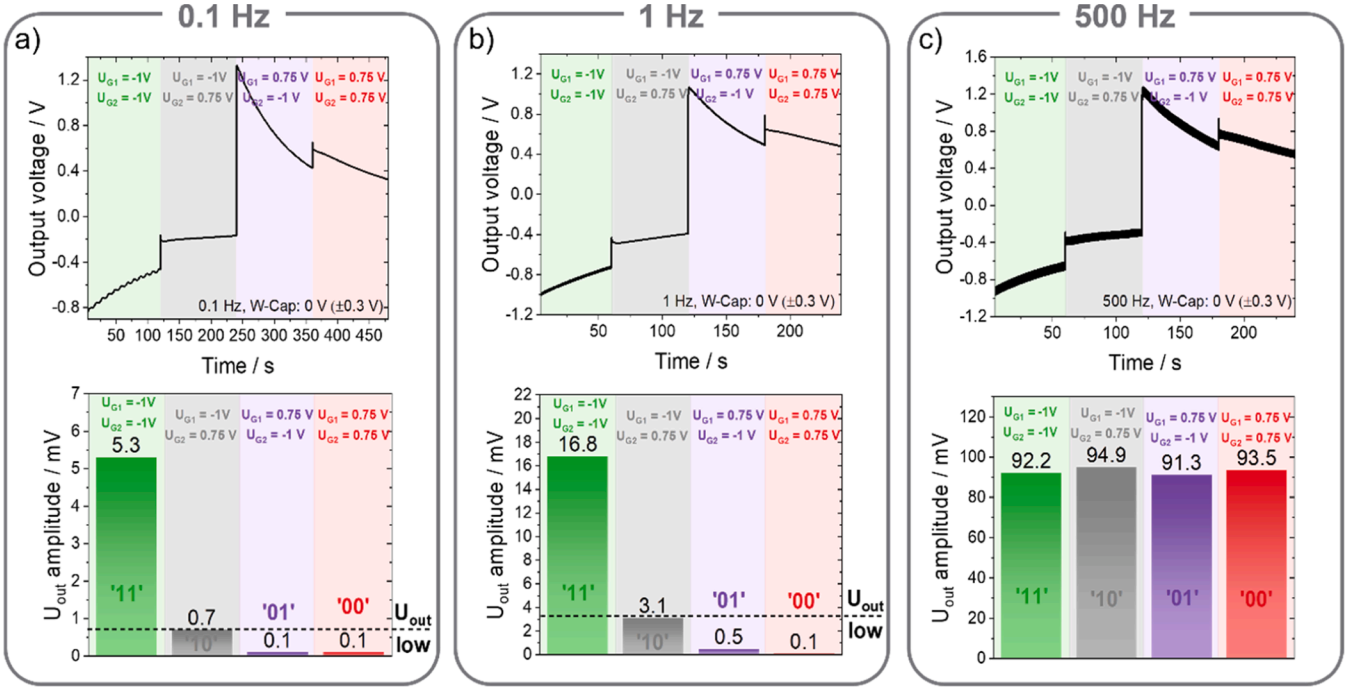


Fig. 7. U_{out} and U_{out} amplitude depending on different U_{bias} in serial connection using U_{in} = 0 V (±0.3 V) for both cells with a frequency of (**a**) 0.1, (**b**) 1, and (**c**) 500 Hz.

relatively high. Since the varactors are connected in series, the total capacitance is dominated by the varactor with the lower capacitance (higher impedance). As a result, the U_{out} remains low. Thus, the circuit successfully implements the AND gate behavior by ensuring that a significant U_{out} only appears when both varactors are in the ON state. This guarantees that the output is high only when both inputs are high, as required by the AND gate logic.

To test the hypothesis the circuit like depicted in Fig. 6a was constructed and various frequencies of 0.1, 1, 10, and 500 Hz were tested (Fig. 7 and **S7**). To overcome the overall impedance of the compound circuit and ensure that a measurable voltage modulation could be observed at the second device, the input amplitude was increased ±0.3 V.

As expected, at low frequencies of 0.1 and 1 Hz, the logic behavior of the serial G-CAPode circuit follows the expected AND-gate response. Therefore, a high U_{out} amplitude can be achieved only when both devices are in the ON state meaning both have an U_{bias} = -1 V applied. In all other cases, ("10", "01", and "00"), at least one device exhibits a high impedance (low capacitance) due to its OFF state, which leads to a large voltage drop across the device and, consequently, a low U_{out}. However, as the frequency of the input signal increases (e.g. to 10 Hz and beyond), this ideal behavior becomes less distinct. In particular, an increase in U_{out} is observed for the "10" and "01" stages, indicating that the blocking effect of the OFF device becomes less effective at higher frequencies. This can be attributed to the decreasing capacitive reactance of the G-CAPodes and the increasing influence of bias independent contact and internal resistances, which make the logic filtering behavior frequency-dependent, as explained above for the parallel circuit.

Interestingly, a notable asymmetry is observed especially at intermediate frequencies (10 Hz; **Fig. S7**): the U_{out} amplitude in the "10" stage is significantly higher than in the "01" stage. While both G-CAPodes are arranged in series and, under ideal and symmetric conditions, should produce a comparable U_{out} behavior for these input states, the observed difference is most likely arising from the fact that the two devices are not perfectly identical in their electrical properties. Slight variations in internal resistance, impedance response, or electrode morphology can lead to unequal voltage division, particularly at intermediate to low frequencies.

At higher frequencies (e.g. 500 Hz), both G-CAPode devices have bias-independent impedances. Due to the significant decrease in capacitive reactance at such high frequencies, the influence of the applied bias on the impedance becomes negligible. As a result, both ON and OFF states exhibit similarly low impedance, leading to minimal contrast between logic states. Consequently, the output voltage is high in all logic configurations, and the distinct switching behavior observed at lower frequencies is effectively lost.

Furthermore, a symmetrical reference system (symmetrical supercapacitors with identical structure design including WE, CE, and GE consisting of the same C_{meso} material) was tested in the serial logic gate circuit (**Fig. S8**). As expected, across all logic gate input states and independently of the applied U_{bias}, no variation in the U_{out} amplitude was observed. This is because the symmetric system exhibits no rectifying or blocking behavior in the CV that could enable an ON or OFF switching state. Consequently, current flows uniformly for all logic states, governed solely by the identical and U_{bias}-independent capacitance of both devices. Once again across all logic gate input states and independent of the applied frequency, no variation in output voltage amplitude is observed for the symmetric system since no blocking effect in the CV is observed which can turn the device ON or OFF. Therefore, for all logic gate states the current is passing through depending on the unified and identical capacitance of the devices at different frequencies. In line with previous observations, a slight difference in U_{out} between the "10" and "01" states is still noticeable. Specifically, U_{out} is slightly higher in the "10" state than in the "01" state. As explained above, this can be attributed to minor differences in the devices such as differences in internal impedance or material properties, which lead to an uneven voltage distribution despite the symmetric configuration.

3. Conclusion

A novel and versatile approach in logic gate design was successfully conceptualized and demonstrated utilizing two G-CAPodes acting as variable filter elements capable of performing logical operations. Unlike conventional semiconductor-based logic gates, such as AND and OR gates constructed using diodes where the logic output is simply a direct function of the input voltages, the approach presented here is based on variable ionic filters that modulate the amplitude of the output signal in response to frequency-dependent filtering characteristics depending on the applied bias. This leads to a logic architecture in which the output is independent of the absolute voltage value propagated from the inputs, but a transformed modulated signal shaped by the intrinsic properties of the filter configuration. Hence, the logic output is encoded in the output amplitude.

By arranging two G-CAPode transistors in series or in parallel, we successfully demonstrated logic gate-like behavior mimicking the AND and OR functions, respectively. Crucially, using AC as input voltage between WE and CE instead of DC enabled a constant charging and discharging of the system's capacitive components. This overcomes the limitation of DC operation, where the capacitive response decays over time and ultimately prevents further signal transmission once the system is fully charged. AC, by continually reversing polarity, maintains charging and discharging cycles, ensuring ongoing current flow and active interaction with the circuit. This dynamic operation enhances the device's responsiveness to frequency and gate bias, which are crucial for logic functions.

The G-CAPode platform uniquely integrates energy storage, rectification behavior, and frequency-dependent switching within a single device architecture, enabling reconfigurable logic operations without the need for complex circuit layouts. In contrast to traditional digital logic gates, which operate based on binary states (high or low, 1 or 0), G-CAPodes respond to a combination of input frequency, voltage amplitude, and applied gate bias. This allows for analog programmability and state-dependent signal shaping, offering a level of dynamic tunability ideal for real-time adaptive systems, such as neuromorphic computing or context-aware circuitry moving beyond rigid logic operations [16, 22]. Their graded switching behavior enables smooth transitions between ON and OFF states, depending on input characteristics. Importantly, G-CAPodes feature two independent control parameters, AC frequency and gate bias, allowing versatile logic responses. Since these devices operate at biologically relevant voltage amplitudes and frequencies (e.g., those corresponding to heartbeat, breathing, or plant signaling), they offer strong potential for applications in bioelectronic interfaces. Moreover, the use of soft, carbon-based electrodes and ion-based signal processing suggests that such systems could be designed for biocompatibility, potentially enabling future development of intelligent, flexible devices for sensing, control, or stimulation in biological environments [23]. For implementation in physiological environments, the electrolyte would need to be replaced by a water-based, biosafe alternative. Identifying suitable biocompatible electrolytes that maintain ion-sieving functionality and high conductivity, such as "water--in-salt" systems, represents an important direction for future work.

To further enhance circuit performance and expand the operational frequency range for U_{bias}-dependent logic switching, improvements in ion transport dynamics could be considered. Equivalent circuit modeling indicates that diffusion-related components, such as Warburg-type elements, become more pronounced in certain operating regimes to reduced switching contrast at higher frequencies [18]. Future developments may benefit from exploring carbon electrode materials that combine narrow pore size distributions with improved connectivity and reduced tortuosity to facilitate faster ion exchange. Additionally, surface functionalization strategies that modulate hydrophilic/hydrophobic balance could promote more efficient ion adsorption and desorption.

Optimizing the electrolyte, particularly by selecting systems with high ionic conductivity and pronounced ion size disparity, could further support faster and more selective charge accumulation. In this regard, reducing internal resistances, such as electrode, contact, and interfacial resistance, through architectural refinement or material engineering may also help mitigate voltage losses, particularly in the high capacitance "11" state. These enhancements could collectively support more pronounced and stable logic responses across a broader frequency range.

At the same time, it should be emphasized that the frequency-selective nature of the logic behavior is not a limitation but a functional feature. The ability to distinguish between frequency ranges, where U_{bias} actively modulates the output (logic operation) and where the signal passes unaffected (transparent transmission), could enable hybrid analog-digital functionality. This opens avenues for advanced applications such as frequency-encoded signaling, adaptive filtering, or circuits that simultaneously perform logic operations and analog signal processing, thereby expanding the utility of G-CAPodes beyond traditional binary systems.

As a next step, performing Fourier transformation of the registered U_{out} signal could allow for the transformation of the AC signal into steady DC voltages. Such an approach would bridge the gap between ionic signal processing and conventional voltage logic levels, further enabling integration into other circuit elements and architectures. Overall, this approach establishes G-CAPodes as flexible and multifunctional components for iontronic logic systems, offering a new take on how logic gates can be designed and operated. By integrating logic and passive filtering in the same material platform the presented approach can offer a multifunctional, compact alternative to complex, multi-component semiconductor designs.

4. Experimental section

Synthesis of ultramicroporous carbon precursor and mesoporous carbon ink

The ultramicroporous carbon precursor was prepared following a procedure previously outlined by our team [17]. In brief, 10 mmol of resorcinol was dissolved in 5 mL of deionized water, after which 2 mmol of imidazole ($C_3H_4N_2$; Sigma Aldrich®), 0.5 mmol of ethylene diamine tetraacetic acid (EDTA; $C_{10}H_{16}N_2O_8$; Sigma Aldrich®), and 2 mmol of zinc chloride ($ZnCl_2$; abcr®) were added to the solution one by one while stirring vigorously. After 10 min of stirring, a formaldehyde (H_2CO; Carl ROTH®) solution (37 wt. %) containing 20 mmol of formaldehyde was rapidly injected into the mixture while stirring quickly, resulting in a solution with a pH of 3.5. This precursor solution remained clear and could be used for inkjet printing for up to 4 days at room temperature (or up to 10 days with additional cooling in a fridge at 2°C). As the synthesis procedure and formulation were followed identically to our previous study, we refer the reader [17] for detailed structural formulas, material characterization, and the rationale behind each component used.

The synthesis and characterization of the mesoporous carbon ink were detailed in a previous publication by our group [24]. In short, 0.17 g of Ketjenblack EC600JD (AkzoNobel®), 0.034 g multi-walled CNTs (length: 4 μm; inner and outer diameter: 4.5 and 10 nm; Sigma Aldrich®) and 0.136 g of ethyl cellulose (viscosity 10 cP; Sigma Aldrich®) were thoroughly mixed and ground together. This mixture was then added to a solution of 25.5 mL (0.335 mol) isopropanol (99.99 %; Sigma Aldrich®) and 4.5 mL (0.044 mol) Cyrene (Sigma Aldrich®). The resulting mixture was ultrasonicated for 30 min using an ultrasonication finger (Labsonic P; Satorius®) while kept in an ice bath. The isopropanol was then removed via rotary evaporation at 60°C (130 mbar) to yield a homogeneous, stable suspension. Before the printing process, the suspension was sonicated for 15 min in a sonication bath. As the synthesis procedure and formulation were followed identically to our previous study, we refer the reader [24] for detailed structural formulas, material characterization, and the rationale behind each component used.

Fabrication of the 3D printed in-plane G-CAPode

Interdigital G-CAPode structures were fabricated using a Bio-Scaffolder 3.2 printer (GeSiM mbH®) equipped with an extrusion module and a Nano-Tip J piezoelectric micropipetting tip (drop volume: 400 pL, chamber volume: 0.7 μL, maximum operating frequency: 1000 Hz). The printing parameters, including frequency, pulse width, and voltage, were fine-tuned with the aid of a stroboscopic camera to generate stable drops (150 Hz; 90 μs; 60 V) before beginning the inkjet printing process of the microporous carbon precursor. For the extrusion printing of the mesoporous carbon, a 15 mL cartridge was loaded with the carbon ink and extruded through a 90 μm nozzle. To achieve successful extrusion, air pressures of 30 to 40 kPa were applied, with the tip moving at speeds of 12 to 18 mm s^{-1}. The structures were printed onto 25 × 25 × 1.1 mm glass substrates (Corning 1737; DELTA Technologies substrates®). Prior to printing, the glass substrates were treated in a piranha solution (one-part 30 % H_2O_2; Fisher Chemicals®; three parts conc. $H_2SO_{4\,\text{Fisher Chemicals}}$) for at least 20 min to enhance adhesion and wettability. After rinsing with deionized water and ethanol, the substrates were dried with a nitrogen stream and placed on a heated substrate holder (60°C) to facilitate rapid curing of the printed lines with high resolution. Once printed, the structures were stored in a drying furnace at 90°C in air to ensure complete curing of the deposited material before pyrolysis.

The printed structures were placed in a tube furnace with a corundum tube and subjected to pyrolysis at 920°C for 2 h under an argon atmosphere (heating rate 300 K h^{-1}, flow rate 30 mL min^{-1}). Before the furnace entered the cooling phase, the structures underwent physical activation using CO_2. To initiate this, the argon supply was shut off and replaced with a carbon dioxide stream at a flow rate 30 mL min^{-1} for 45 min [17].

The pyrolyzed carbon structures were contacted with silver conducting paste (Ferro GmbH®) on the contact pads. Additionally, a specified region of 11 × 10 mm for S1 and 10 × 6 mm for S2 and S3 around the electrodes was enclosed with PDMS (Sylgard 184 elastomer kit; Dow Chemicals®) to create a defined reservoir for the electrolyte. To contain the electrolyte, a 3D-printed polypropylene reservoir was placed on top of the structure and sealed with PDMS. Next, the organic electrolyte, 1 mol L^{-1} tetrabutylammonium tetrafluoroborate in acetonitrile ($TBABF_4$; for electrochemical analysis; Sigma Aldrich®) was injected into the reservoir (∼0.3 mL) and an additional layer of PDMS was applied to seal the setup (**Fig. S2a**).

Electrochemical measurements and characterization

The printed G-CAPodes were electrochemically analyzed with a computer-controlled multichannel potentiostat/galvanostat (VMP300; Biologic®) using a CE-to-ground setup synchronizing two channels with one CE. In this setup, the ground as well as the REF2 cables from channel 1 and 2 are connected to the CE, while the blue cables (CE; REF3) of channel 1 are connected to the WE of the device (**Fig. S2c**). The blue cables from channel 2 represent the second WE of the setup and are connected to the GE. This connection enables the measurement of two working electrodes separately (both connected to one counter electrode) and therefore to control and analyze the W-Cap (channel 1) and the GE-CE system (channel 2) in parallel. In our typical experiments, the W-Cap is cycled using a CV experiment while a constant bias voltage between GE and CE is applied via a CA experiment. To study the potential distribution of WE, CE, and GE the light red cables (REF1 of channel 1 and 2) are connected to the reference electrode (RE). The dark red cables of channel 1 and 2 are interconnected forming the new internal grounding of the system.

In a typical experiment, two G-CAPodes were connected in parallel or in series representing and OR gate or AND gate behavior. To construct a parallel circuit, two CE-to-ground configurations (each consisting of two synchronized channels) are set up and individually connected to cell1 and cell2, respectively. All four channels are synchronized to ensure that the applied AC input voltages are identical in both amplitude and phase (**Fig. S2d, e**). To measure the U_{out} across a resistor, an

additional channel is used in the standard setup, configured to record the voltage drop using the open-circuit voltage (OCV) mode. In a series configuration, only one CE-to-ground setup is used to supply input to cell1. The output of cell1 is then connected to the WE of cell2, effectively serving as its input. Again, a third channel measures U_{out} across the resistor using the OCV mode. For both circuit configurations, the CEs of the channels are connected together at a common point after the resistor, which serves as the ground reference for the entire circuit system. In a typical experiment, an AC voltage of 0 V (±0.1 V), with a frequency range from 0.1 to 500 Hz, is applied to the WEs. Simultaneously, a switching bias voltage U_{bias} between the GE and the CE is applied, alternating between 0.75 and -1 V for 60 s each. This setup enables the investigation of all four possible logic states: 11, 10, 01, and 00.

Electrochemical impedance spectroscopy (EIS) measurements were carried out in a frequency range from 10 mHz – 100 kHz at a certain offset voltage with a voltage amplitude of 5 mV. At the same time a constant U_{bias} = -1, -0.25, 0 or 0.75 V is applied.

Supporting information

Supporting Information is available from the Wiley Online Library or from the author.

CRediT authorship contribution statement

Christin Gellrich: Writing – original draft, Visualization, Methodology, Investigation, Data curation, Conceptualization. **Przemyslaw Galek:** Writing – review & editing, Visualization, Supervision. **Leonid Shupletsov:** Writing – review & editing, Conceptualization. **Julia Grothe:** Writing – review & editing, Supervision. **Stefan Kaskel:** Writing – review & editing, Visualization, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Stefan Kaskel reports financial support was provided by European Research Council. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

The authors acknowledge the funding received from the European Research Council (ERC) under the European Union's Horizon 2020 Research and Innovation Programme (grant agreement no. 101054940; title: Ultracapacitor Logic Gates.

Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.ensm.2025.104535.

Data availability

The data that support the findings of this study are openly available in a public repository that issues datasets with DOIs. The DOI to access the raw data is: https://doi.org/10.5281/zenodo.15736381.

References

[1] N.S. Lidorenko, M.L. Fish, Meas. Tech. 10 (1967) 772–777.
[2] K. Xiao, C. Wan, L. Jiang, X. Chen, M. Antonietti, Adv. Mater. 32 (2020), https://doi.org/10.1002/adma.202000218.
[3] E. Zhang, L. Galle, S. Lochmann, J. Grothe, S. Kaskel, Chem. Eng. J. 420 (2021) 130431.
[4] J. Rivnay, S. Inal, A. Salleo, R.M. Owens, M. Berggren, G.G. Malliaras, Nat. Rev. Mater. 3 (2018), https://doi.org/10.1038/natrevmats.2017.86.
[5] P. Li, P. Galek, J. Grothe, S. Kaskel, Chem. Sci. 16 (2025) 6511–6512.
[6] K. Tybrandt, R. Forchheimer, M. Berggren, Nat. Commun. 3 (2012), https://doi.org/10.1038/ncomms1869.
[7] J.T. Santini, M.J. Cima, R. Langer, Nature 397 (1999) 335–338.
[8] Y. Xing, M. Zhou, Y. Si, C.Y. Yang, L.W. Feng, Q. Wu, F. Wang, X. Wang, W. Huang, Y. Cheng, R. Zhang, X. Duan, J. Liu, P. Song, H. Sun, H. Wang, J. Zhang, S. Jiang, M. Zhu, G. Wang, Nat. Commun. 14 (2023) 1–11.
[9] H.H. Chouhdry, D.H. Lee, A. Bag, N.E. Lee, Nat. Commun. 14 (2023) 1–12.
[10] B.I. Weintrub, Y.L. Hsieh, S. Kovalchuk, J.N. Kirchhof, K. Greben, K.I. Bolotin, Nat. Commun. 13 (2022) 2–7.
[11] Z. He, J. Zhou, X. Lu, B. Corry, ACS Nano 7 (2013) 10148–10157.
[12] Y. Wei, Y. Zhao, Q. Ding, J. Zhao, Y. Yang, Y. Liu, J. Dong, D. Zhang, S. Han, P. Huo, Chem. Eng. J. 498 (2024) 155655.
[13] R. Sarpeshkar, Neural Comput 10 (1998) 1601–1638.
[14] P. Peng, H. Qian, J. Liu, Z. Wang, D. Wei, Int. J. Smart Nano Mater. 15 (2024) 198–221.
[15] T. Arbring Sjöström, M. Berggren, E.O. Gabrielsson, P. Janson, D.J. Poxson, M. Seitanidou, D.T. Simon, Adv. Mater. Technol. 3 (2018), https://doi.org/10.1002/admt.201700360.
[16] S.Z. Bisri, S. Shimizu, M. Nakano, Y. Iwasa, Adv. Mater. 29 (2017) 1–48.
[17] C. Gellrich, L. Shupletsov, P. Galek, A. Bahrawy, J. Grothe, S. Kaskel, Adv. Mater. 36 (2024), https://doi.org/10.1002/adma.202401336.
[18] C. Gellrich, P. Galek, L. Shupletsov, N. Niese, A. Bahrawy, J. Grothe, S. Kaskel, SusMat 5 (2025), https://doi.org/10.1002/sus2.70006.
[19] E. Zhang, N. Fulik, G.P. Hao, H.Y. Zhang, K. Kaneko, L. Borchardt, E. Brunner, S. Kaskel, Angew. Chemie -Int. Ed. 58 (2019) 13060.
[20] A. Bahrawy, P. Galek, C. Gellrich, N. Niese, J. Grothe, S. Kaskel, Energy Storage Mater 74 (2025) 103872.
[21] A. Slesinski, E. Frackowiak, J. Solid State Electrochem. 22 (2018) 2135–2139.
[22] A. Mehonic, A.J. Kenyon, Nature 604 (2022) 255–260.
[23] S. Wang, R. Wang, Y. Cao, X. Ma, H. Wang, Y. Hao, Adv. Electron. Mater. 9 (2023) 2200972.
[24] C. Gellrich, Y. Bräuniger, R. Schmidt, J. Grothe, S. Kaskel, Batter. Supercaps 7 (2024) e202300469.