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# Atomic Force Microscopy Analysis of Aluminum Layer Properties and Correlation to Masking Functionality in Copper Plating Metallization for Solar Cells

Thibaud Hatt,* Tobias Morawietz, Jonas Bartsch, Leonard Tutsch, and Markus Glatthaar

**The native $AlO_x$ grown on a thin sputtered aluminum layer can be used as mask for electroplating copper, e.g., for metallizing silicon heterojunction (SHJ) solar cells. Effects that influence the masking quality for selective electroplating are studied herein. Atomic force microscopy characterization in PeakForce mode highlights the presence of some insulation defects in the native $AlO_x$ due to local contamination, pinholes, or tunneling currents. A focused ion beam/scanning electron microscopy analysis is further conducted to understand some defects in detail. The $AlO_x$ insulation can be improved by adsorbing a self-assembled monolayer, which is mainly required along the process sequence to adjust the surface wetting of the Al for optimal $NaOH_{aq}$ printing. The mask quality and complete metallization sequence for solar cells are demonstrated on industrial SHJ precursors. Inkjet- and FlexTrail-printing of $NaOH_{aq}$ are shown to be suitable to pattern the Al layer. Promising conversion efficiency comparable to screen-printing reference is reached on large area.**

## 1. Introduction

Terawatt (TW) scale photovoltaic (PV) energy conversion is already a reality: in 2022, one TW of installed capacity was reached, which in a few years will be the annual production volume. A sustainable supply chain from silicon feedstock to module manufacturing is a strong concern for multi-TW PV.[1–7] Typically for the leading Si technology, the electrodes on solar cells are metallized by screen-printing of silver pastes. For silicon heterojunction (SHJ) or TOPCon solar cells with silver grid on both sides, 15% of the PV module costs stems from the Ag electrodes.[6] Furthermore, silver is reported to be the main material sustainability issue for the Si solar cells.[7]

Moving to electroplated copper metallization is a sustainable path for multi-TW scale PV manufacturing because it suppresses the need of scarce silver. It is worth noting that electroplating is already a standard process for decades in the integrated circuit industry.[8] Despite its more complex processing sequence, copper plating for solar cells was already successful for large-scale PV production by BP Solar,[9] Tetrasun, Suntech,[10] SunPower,[11] or GS Solar. SHJ solar cells which require the most silver per Watt and suffer from poor conductivity of the low temperature silver pastes would yield the greatest cost savings and efficiency gains with plated copper metallization compared to other Si solar cell technologies. An additional advantage of applying copper plating for SHJ solar cells is the presence of the topmost transparent conductive oxide (TCO) layer which is proved to be an effective barrier to copper migration into the silicon bulk, i.e., no plated nickel barrier is required.[12–14] However, for plating a copper grid, the TCO layer has to be masked to avoid copper deposition on the full wafer area. There, a wide variety of plating approaches adapted to bifacial SHJ solar cells were investigated in the last decade as reviewed in the literature.[15–19] To date, the most advanced sequence for industrial implementation is based on a sacrificial micrometer-thick organic masking layer on top of a sputtered metal seed layer. As summarized in the review articles, several institutes and companies such as Kaneka, CSEM, INES, GS Solar, Hevel, and Sundrive (reduced ITO as seed instead of PVD layer) have reached remarkable cell performance with this approach, lately above 26% conversion efficiency on industrial size SHJ solar cells.[16,18,20,21] However, it seems that the use of a thick organic mask (e.g., photoresist), which produces waste water polluted with organics, is not considered viable for mass production in the PV industry.

In the last years, we aimed at a similar plating approach using an alternative sacrificial masking layer, a nanometer-thick self-passivated aluminum film (i.e., conductive and inorganic), which we patented as the NOBLE (native oxide barrier layer for selective electroplating) approach.[22] Under ambient atmosphere, a native

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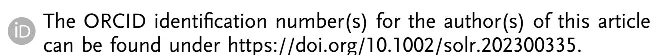
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oxide grows on the conductive Al layer and was shown to be an effective masking layer while selective plating can occur at patterned areas on the exposed metal seed.[23] In this article, a deeper investigation on the insulation quality of the conductive self-passivated Al layer along the NOBLE processing is performed. In addition, *I–V* results of the SHJ solar cells metallized by this approach without parasitic Cu deposition are presented.

## 2. Results and Discussion

### 2.1. Approach

The NOBLE metallization process flow adapted to bifacial SHJ solar cells is detailed in **Figure 1**. The thin PVD metal layers ($\leq$150 nm) are deposited following the TCO coating on both wafer sides in an extended sputtering line without breaking the vacuum. The Al self-passivation occurs rapidly by exposition to ambient atmosphere[24] after unloading the wafers from the sputter tool. Several industrial relevant patterning methods of the thin Al layer were developed: printing of alkaline solutions (e.g., by inkjet- or FlexTrail-printing) or laser ablation.[25,26] Copper electrochemical deposition is then performed selectively on the exposed metal seed layer (e.g., Cu) simultaneously on both sides of the wafer, which is typically vertically oriented within the wet chemical tool. Finally, additional baths are used in the wet tool to remove the PVD metal stack (seed and Al) and to cap the plated Cu grid with Sn or Ag, if required. The NOBLE process for bifacial SHJ solar cells presents many advantages: 1) The sputtered metal seed ensures an extremely low contact resistivity $\rho_c$ and an excellent adhesion of the grid to the TCO.[27] 2) The patterning step of the Al mask only in grid positions ($\leq$5% of wafer area, grid design easily adjustable) is very fast. 3) Full area metal seed and Al layers enable homogeneous plating current distribution on front and rear sides of large wafers using a simple contact on wafer edge. 4) After etching back the sputtered metallic layers (seed and Al), the metal ions can be recycled from the waste water. 5) Low process costs compared to other plating or metallic-paste printing metallization.[27]

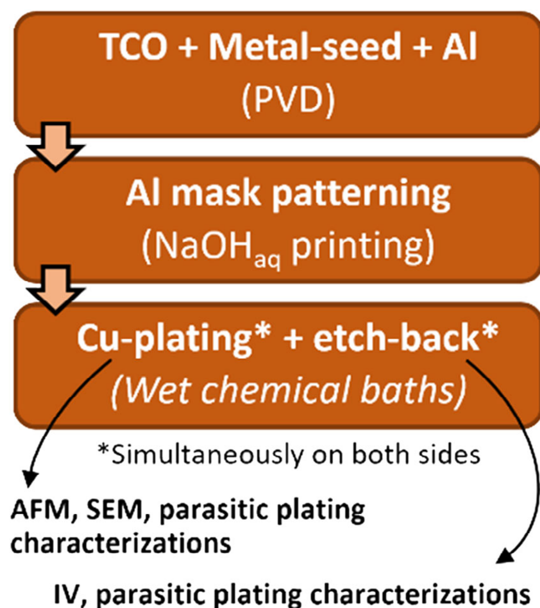


**Figure 1.** Sequence of the NOBLE metallization for bifacial SHJ solar cells and related processing step for the characterizations in this study.

### 2.2. Insulation Ability of the Native $AlO_x$

Achieving a successful selective Cu electrodeposition using the self-passivated Al masking layer depends on several factors. The electrolyte chemistry (e.g., pH, additives, etc.) has to be tuned to avoid potential corrosion of the native $AlO_x$ as shown in ref. [28]. Further, the quality of the Al patterning, with potential Al/$AlO_x$ residues at the grid positions, also impacts the ability of plating Cu selectively.[25] If present, residues in the patterned areas seemed to be responsible for a 3D crystallites copper growth relying on a nucleation–coalescence mechanisms.[19] Finally, the electrical parameters applied for electrodeposition were optimized by implementing a reverse pulsed plated current that includes anodic and cathodic pulses. The anodic pulses prevent parasitic plating by dissolving the adsorbed ions on the native $AlO_x$, which is energetically more favorable than dissolving the ad-ions on the metal seed. The parasitic nuclei potentially formed during the previous cathodic pulse are typically small because the ad-ions first have to diffuse to the rare defective native $AlO_x$ sites. In addition, the anodic pulses may lead to reform the corroded native $AlO_x$ by anodization as typically performed in sulfuric acid milieus.[29] Herein, we investigated by atomic force microscopy (AFM) in conductive tapping (Bruker PeakForce TUNA) mode the insulation quality of the native $AlO_x$ along the NOBLE processing.

A thin PVD metal stack with topmost Al was deposited on a planar polyimide (PI) foil. While being exposed to ambient, the foil was then cut in different samples to enable characterizing by AFM the Al/$AlO_x$ layer along the NOBLE process sequence as depicted in **Figure 2**. The 100 nm-thick sputtered Al layer was patterned by inkjet-printing a low concentration $NaOH_{aq}$ ink as shown in ref. [25]. Prior to inkjet-printing, for some samples a self-assembled monolayer (SAM), octadecyl phosphonic acid (ODPA), was adsorbed on the native $AlO_x$ to enhance the hydrophobicity and the insulation properties. Copper was then selectively electrodeposited on the patterned lines by applying the reverse pulse plating process. AFM was performed under argon atmosphere on the samples after growth of the native $AlO_x$ with/without ODPA adsorption and after the selective Cu plating in the patterned positions. As the inkjet-printing patterning process is performed only locally, no impact on the native $AlO_x$ is expected. In Figure 2, the high-resolution AFM topography mappings show the typical densely packed fibrous grains morphology around 10–30 nm big of PVD metal coatings. It seems that some uncleanliness is present which would explain the higher round structures, probably particles. The morphology of the $AlO_x$ before and after plating seems unchanged. The functionalized $AlO_x$/ODPA surface looked also very similar to the $AlO_x$ (not shown).

The AFM in PF-TUNA mode mapping results on the $AlO_x$ and $AlO_x/C_{18}H_{39}O_3P$ surfaces are presented in **Figure 3**a–d and e–h, respectively. On the left, the topography mappings (a,e) before electroplating are shown for both surfaces. The topography mappings after plating look all very similar and are not shown.


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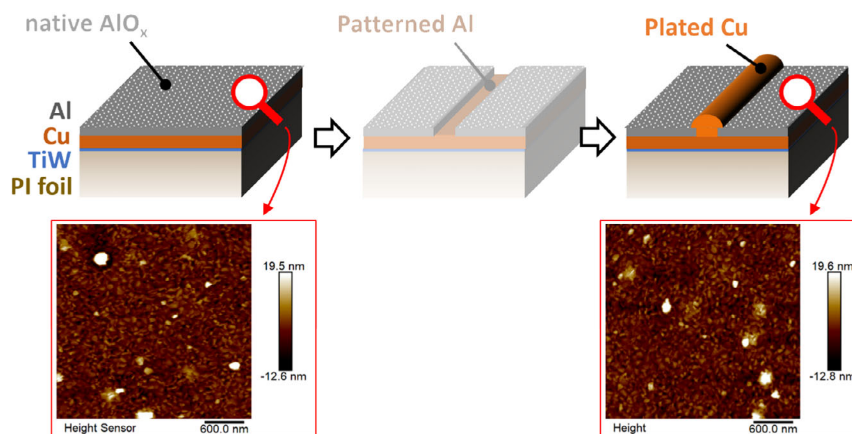


**Figure 2.** Schematic drawing of the layer stack on a planar polyimide foil along the NOBLE processing (after sputtering, patterning of the Al layer and Cu plating) and respective high-resolution AFM mappings of the Al/$AlO_x$ surface topography.

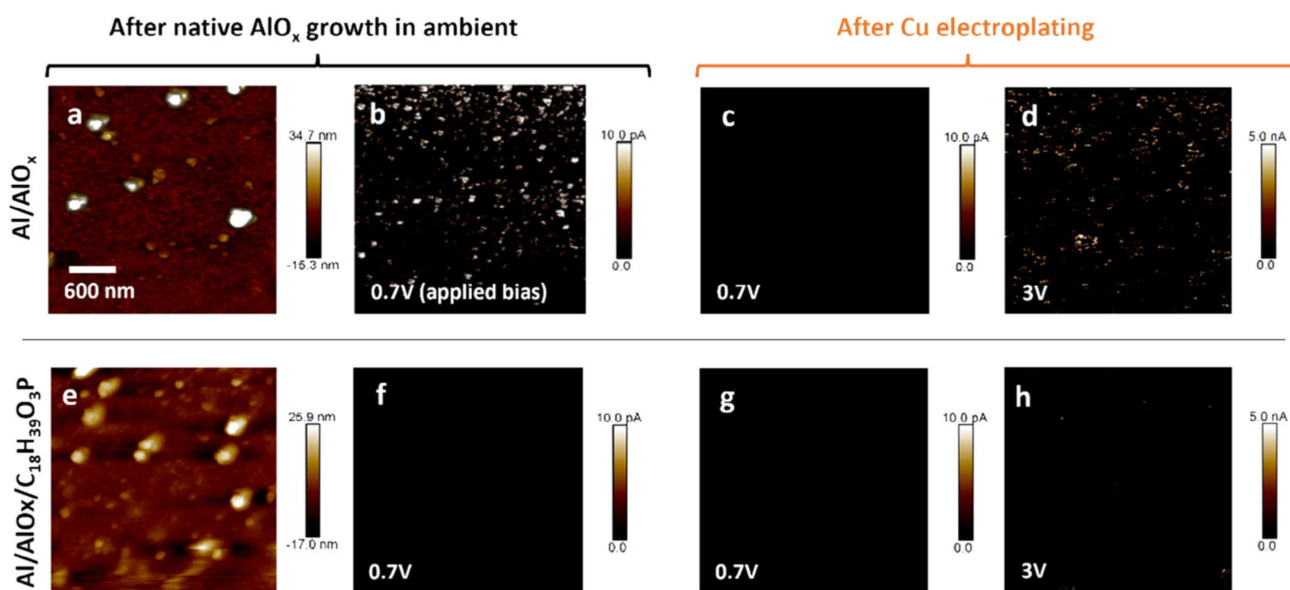


**Figure 3.** AFM mappings of the Al/$AlO_x$ surface: a,e) topography with/without adsorbed ODPA and corresponding electronic current under argon atmosphere for applied bias, b,c,f,g) 0.7 V and d,h) 3.0 V; b,f) before and c,d,g,h) after plating; f,g,h) with and b,c,d) without adsorbed ODPA.

In PF-TUNA mode, 0.7 V bias were applied, which will mostly drop along the insulating $AlO_x$ layer. This corresponds to the voltage which typically arises during our selective Cu electroplating process (at $I_{forward} = 6\ A\ dm^{-2}$) on the patterned solar cells. The mapping of the unpatterned $AlO_x$ surface (b) highlights several positions at 0.7 V where a current in pA range can be measured, meaning that the insulation is not completely impermeable to electric current at this voltage. Besides the positions of the potential particles, several other conductive spots are detected. These may result from pinholes in the native $AlO_x$ or from a too thin $AlO_x$ enabling tunneling currents. In comparison, at 0.7 V the native $AlO_x$/$C_{18}H_{39}O_3P$ surface (f) seems well insulative without current measured. After the typical pulsed reverse plating process, the native $AlO_x$ surface (c) insulation is improved with no current measured at 0.7 V. This result could confirm that besides the $Cu^{2+}$ reduction, an anodization of the Al layer happens. At higher (3 V) applied bias currents up to 5 nA are measured (d) at some spots which shows the insulation limit of the newly formed $AlO_x$. For the native $AlO_x$/$C_{18}H_{39}O_3P$ surface (g,h), no current is measured even for applied bias of 3 V. However, the surface was observed to be impacted by the measurements at 3 V. Further work could be done to investigate if an anodization of the Al layer takes place through the self-assembled monolayer.

### 2.3. Masking Quality on Textured SHJ Solar Cells

The NOBLE processing depicted in Figure 1 was performed on industrial textured M2 SHJ precursors finished with ITO. These precursors were split in three groups depending on the PVD


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metal stack as well as the Al patterning technique (inkjet- or FlexTrail-printing of $NaOH_{aq}$ ink) as described in the Experimental Section. For group 1, a Cu/Al stack (100/50 nm on ITO after wafer shipment) was sputtered in an industrial horizontal tool. Before inkjet-printing patterning, the native $AlO_x$ on surface was functionalized by ODPA which was shown to be required for a homogeneous and narrow patterning by $NaOH_{aq}$ inkjet-printing.[25] After patterning and selective Cu electroplating (wafer vertically immersed in the electrolyte), the parasitic deposition on the native $AlO_x/C_{18}H_{39}O_3P$ surface was characterized. **Figure 4** shows pictures of the solar cell full area after metallization. In (a) and enlarged (b), almost no parasitic copper deposition is observed on the Al masking layer, besides some spots marked by red arrows on the wafer edges. The insulation masking quality of the native $AlO_x$ improved with ODPA is therefore quite effective on the complete (i.e., almost) textured wafer area. This was suggested by the AFM characterization on flat surface and is here achieved with an even thinner Al masking layer (50 nm). However, the parasitic Cu deposition on the edges could result from different effects: 1) scratching of the Al, pinholes or uncleanliness (as for $SiN_x$[30,31]) on the edges typically due to manual handling of the wafers in lab; 2) locally higher current density at the edges and pyramid tops due to more area in contact with the electrolyte and a higher electric field density.[32]

As seen in (c), several parasitic features of the edges are removed by peel-off due to under-etching of the PVD metal layers during the final etch-back step.

The parasitic copper on the edges was further characterized by scanning electron microscopy (SEM). It is observed that the parasitic Cu on the Al mask forms random structures for the larger one (micrometer range) or small spheres on the pyramids summit. To investigate the early reasons for parasitic copper deposition on the Al, the focus was put on the small spheres and a focused ion beam (FIB) tomography was performed. The 54° tilted SEM views of a plated Cu sphere on a pyramid summit along FIB tomography (50 nm steps) are presented (only selected slices) in **Figure 5**. The nature of the different layers is represented by colored circles all along the tomography: ITO (blue), Cu (orange), $Al/AlO_x$ (green), and plated Cu (yellow). In the first picture (I), two round particles are observed on the ITO surface as well as a gap between the ITO and Cu/Al layers. However, the Al layer is present without discontinuity below the plated Cu. On the slice (II), an interruption in the Al layer may start as also suggested by the energy-dispersive X-Ray (EDX) mapping. The additional EDX line scan with two peaks for the Al enables to highlight the vertical shift of the Al layer at the particles (carbon related) position which could be responsible for the parasitic Cu deposition. In (III), a direct contact of the plated Cu to the ITO is observed without sputtered Cu/Al layer in between. The particle seems to be the reason for uncomplete covering of the ITO by the sputtered Cu/Al stack enabling the parasitic Cu deposition. Such a parasitic copper deposition should be avoided by realizing the complete PVD sequence (TCO and metal stack) in the same tool without breaking the vacuum. Further optimizations such as a homogeneous current density at the wafer edges and automation of handling are ongoing to reach zero parasitic Cu deposition.

### 2.4. *I–V* Performance of the Metallized SHJ Solar Cells

The potential of the NOBLE metallization was tested on M2 industrial SHJ precursors. SHJ solar cells from groups 2 and 3 (Ti/Ag/Al and $Ag/Al_{thin}$, respectively) were metallized. While plating, the higher current density at the wafer edge was reduced to prevent parasitic Cu deposition. As introduced above, different $NaOH_{aq}$ printing methods were used for patterning the Al layer: the optimized inkjet-printing (group 2)[25] or more recently tested FlexTrail-printing (group 3)[26] processes. **Table 1** presents the best *I–V* characteristics reached for both patterning technologies.

Both patterning techniques enabled to reach similar conversion efficiencies $\eta$ up to 22.8% for these SHJ solar cells. To be noticed as reference, comparable conversion efficiencies were reached with silver-paste screen-printing metallization on the same medium-quality industrial SHJ precursors. Independently

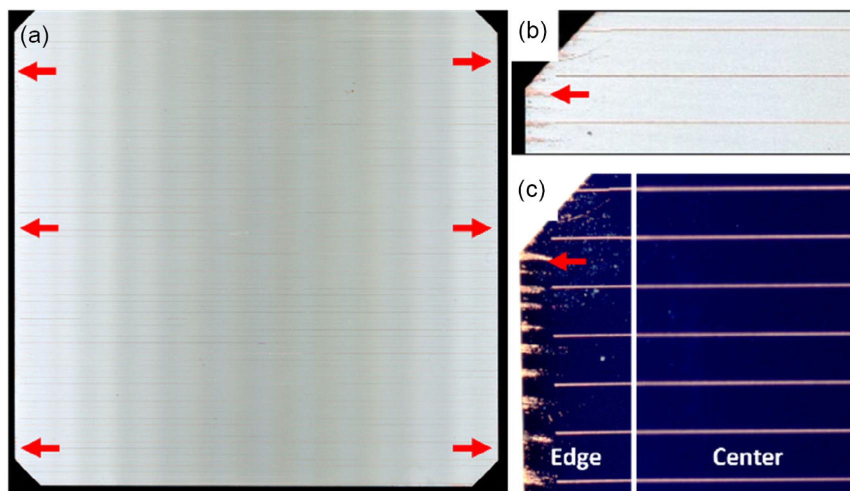


**Figure 4.** Pictures of a M2 SHJ solar cell along the NOBLE processing using a topmost sputtered 50 nm thin Al layer (stack Cu/Al) functionalized with OPDA as mask: a) after reverse pulsed Cu electroplating, b) enlarged at the edge, and c) enlarged at the edge and center after PVD metal layers etch back.


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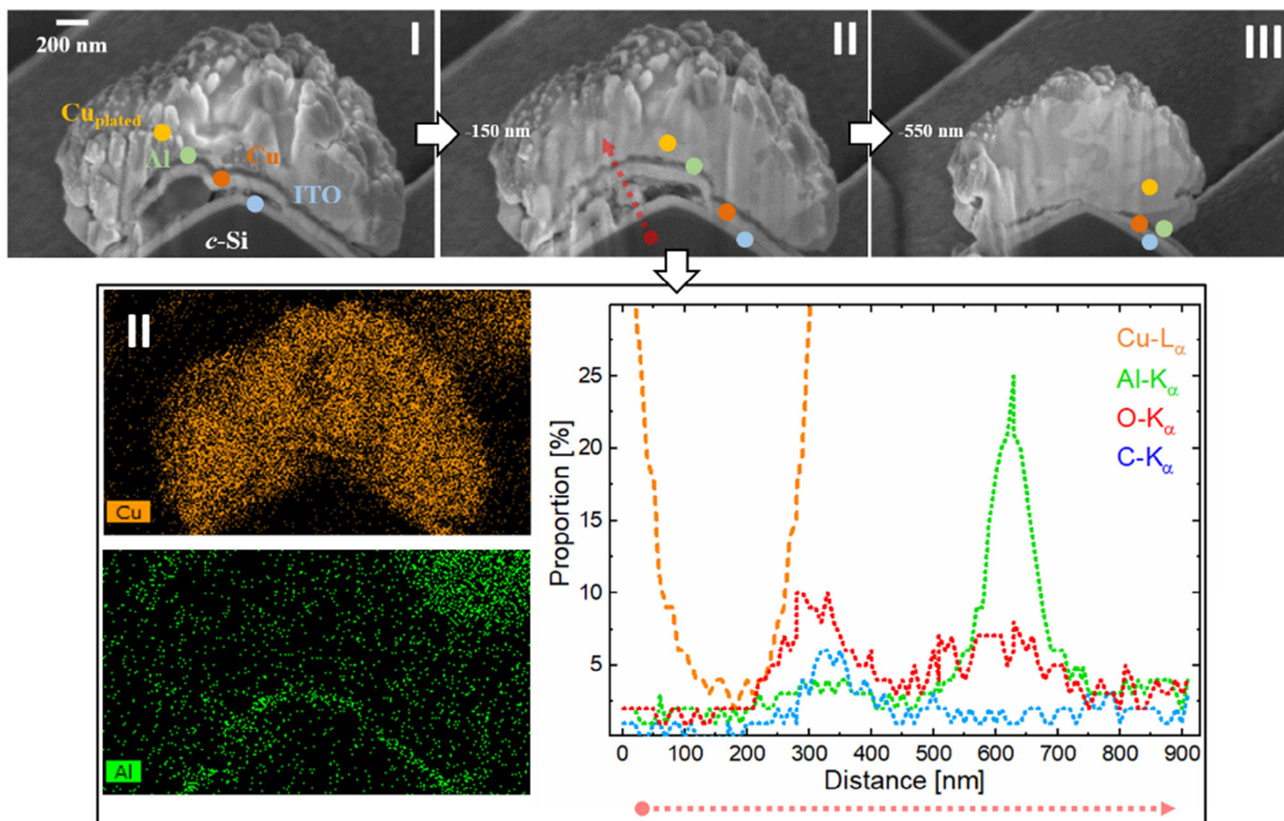


**Figure 5.** SEM and EDX pictures (tilted 54°, EDX line scan along the red arrow) along FIB tomography (50 nm steps, not all slices shown) of a parasitic Cu sphere electroplated on a pyramid summit of a SHJ precursor covered by ITO, a sputtered Cu/Al stack (100/50 nm, after wafer shipment), and native $AlO_x$.

**Table 1.** *I–V* characteristics (measured with aperture 222 $cm^2$) at 1 sun under standard 1.5AMG of the best SHJ solar cells metallized by the NOBLE approach with inkjet- or FlexTrail-printing of $NaOH_{aq}$ to pattern the Al masking layer (respectively group 2 and 3).

| Patterning of the Al masking by $NaOH_{aq}$: | $V_{oc}$ [mV] | $j_{sc}$ [mA $cm^{-2}$] | FF [%] | $\eta$ [%] |
|---|---|---|---|---|
| Inkjet-printing | 736.0 | 37.9 | 81.3 | 22.7 |
| FlexTrail-printing | 733.4 | 38.2 | 81.5 | 22.8 |

from the patterning technique, a slightly lower open-circuit voltage $V_{oc}$ (–2.6 mV) is observed for the second solar cell which may be explained by the relatively low shunt resistance of $7.9 \times 10^3\,\Omega\,cm^2$ compared to the other cell ($2.2 \times 10^4\,\Omega\,cm^2$). This may be related to a local remaining of metal on the wafer rim due to an uncomplete etch back or parasitic Cu deposition (investigations to prevent entirely a higher electroplating current density on the edge are still ongoing). However, on module level this seems to have ignorable influence.[33] For group 2, the probable uncomplete etching of the Ti layer on the ITO may be responsible for the lower short-circuit current $j_{sc}$ ($-0.3$ mA $cm^{-2}$) reached with inkjet patterning. The relatively high $j_{sc}$, $V_{oc}$, and FF reached prove that it is possible with our plating approach to avoid shunts or parasitic Cu deposition. The $NaOH_{aq}$ inkjet- and FlexTrail-printing to pattern the thin Al masking layer are shown to be both suited for this metallization process.

## 3. Conclusion

This study gives several insights into the insulation masking quality of a native $AlO_x$ film grown in ambient on a thin sputtered Al layer on planar and textured substrates. Such an Al mask is then applied for copper plating of a grid on SHJ solar cells (NOBLE metallization). AFM characterization in peak force mode highlights the presence of insulation defects in the native $AlO_x$ (lab sputtered Al). Uncleanliness, pinholes or tunneling currents seem responsible for this localized loss of insulation. During forward/reverse pulsed plating in a mild acidic $CuSO_{4aq}$-based electrolyte, the Al layer seems to be anodized resulting in a better insulation after processing. However, the native $AlO_x$ insulation is strongly improved when adsorbing a short self-assembled monolayer. It is noteworthy that such a SAM layer is required along the NOBLE sequence for homogeneous patterning of the Al by $NaOH_{aq}$ printing.

The insulation quality of the native $AlO_x$/SAM while Cu plating is demonstrated on industrial M2 SHJ precursors. No

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parasitic Cu deposition is observed on the Al mask besides on the wafer edges due to a local higher current density and uncleanliness (i.e., lab manual handling) as seen by SEM/EDX tomography. By reducing the first effect, promising conversion efficiency up to 22.8% is reached using the NOBLE metallization. In addition, inkjet- and FlexTrail-printing of $NaOH_{aq}$ are both shown to be adequate to pattern the Al mask layer.

## 4. Experimental Section

*Samples Preparation*: The flat substrate for AFM measurements were based on a 50 µm thin polyimide foil. A thin metal stack composed of TiW/Cu/Al (15/300/100 nm) was sputtered on the PI foil in a Balzers LLS 801 vertical lab tool (direct current magnetron, $3 \times 10^{-3}$ mbar). After exposition to ambient without monitoring of the native $AlO_x$ growth, straight parallel lines were patterned in the Al layer by inkjet-printing a self-made diluted aqueous $NaOH_{aq}$ ink at 5 wt% at room temperature (≈25 °C) using a PIXDRO LP50 printer from Meyer Burger Technology AG. Disposable 1 pL drop size Fujifilm Dimatix Cartridges (DMC) were used to pattern the lines (length 50 mm, parallel with pitch of 2 mm). Prior to inkjet-printing, some samples were functionalized by adsorption of octadecyl phosphonic acid $C_{18}H_{39}O_3P$ (ODPA). The Al surface was first rinsed with EtOH and functionalized for 5 min by an ethanolic (EtOH > 99%) 1 mM ODPA solution. The sample was then rinsed with EtOH to remove the free ODPA molecules not adsorbed and dried with a nitrogen stream. The patterned foils were then immersed from one edge in an optimized aqueous mild acidic $CuSO_4$-based electrolyte. Electroplating was carried out by applying a pulsed current ($I_{forward} = 6$ A dm$^{-2}$) as tuned in ref. [28].

Industrial M2 silicon heterojunction solar cells (after depositions of a-Si:H layers and $ITO_{93:7}$) were used for the experiments on textured surface and divided into three groups. For group 1, the deposition of a full area Cu/Al stack (100/50 nm) was carried out in a horizontal SCALA sputtering tool by Von Ardenne (settings not further disclosed). It is noteworthy to note that the thickness on the textured surface of the wafers is expected to be thinner (factor ≈ 1.4) compared to the flat samples. However, this layer stack may not be ideal because the adhesion of Cu to ITO is relatively low.[27,34] For group 2, the SHJ wafers were covered by a Ti/Ag/Al stack deposited in lab by thermal evaporation (Balzers PLS570, $4 \times 10^{-6}$ mbar) and then patterned by inkjet-printing as the flat substrate. On group 3, an Ag/Al stack (100/30 nm) was deposited on the wafers in a vertical Viola sputtering tool at Von Ardenne. These wafers were further patterned by FlexTrail-printing[35]of a self-made 5 wt% $NaOH_{aq}$ ink solution at 500 mm s$^{-1}$.[26] Before patterning, the native $AlO_x$ was functionalized by a 1 mM ethanolic decylphosphonic acid $C_{10}H_{23}O_3P$ (DPA) solution for 1 min. The $NaOH_{aq}$ was printed at an atmospheric pressure of 50–100 mbar applied through a flexible glass capillary presenting an inner opening diameter of 15 µm. Finally, all the SHJ wafers (group 1–3) were plated as described above for the flat substrate. Then, the Al and Cu or (Ti)/Ag layers were etched back in 3 wt% $NaOH_{aq}$, 5 wt% $(NH_4)_2S_2O_{8aq}$ or $NH_3/H_2O_{2aq}$ (5/5.25 wt%), respectively. The SHJ solar cells with (Ti)/Ag seed layers were then annealed for 10 min at 200 °C in air on hot plate to activate the a-Si:H passivation and recover possible damage from ITO sputtering.

*Characterization Methods*: The AFM measurements of topography and electronic conductivity in PeakForce TUNA tapping mode were carried out in glove box (Ar atmosphere) with a Bruker Icon using a conductive diamond tip (Brucker DDESP). For higher resolution without simultaneously measured current samples were scanned with Bruker PFQNE-AL tips. The AFM recorded and evaluated at each points the force–distances curves. The image size was set to 3 µm and is measured at 0.501 Hz with 512 pixels. The applied bias was either 0.7 or 3 V. *I–V* curves were recorded at the measurement areas on several points between −4 and +4 V. The parasitic Cu deposition was observed by scanning of the solar cells and confocal microscopy (LEXT-Olympus OLS4000). The cross section of the parasitic Cu sphere was prepared by FIB milling (2 nA) in a Schottky emission SEM Auriga 60 from Zeiss equipped with an EDX analysis detector. The 1 sun current–voltage (*I–V*) parameters of the solar cell were measured under standard testing conditions (STC: AM1.5 G, 100 mW cm$^{-2}$) with/without aperture of 222 cm$^2$. The Grid$^{TOUCH}$ system from PASAN exhibits 30 wires for current and five wires for voltage measurements on the front side, which are excluded with respect to shading during the calibration procedure.

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

Research data are not shared.

## Keywords

aluminum, atomic force microscopy (AFM), copper electroplating, masking layer, metallization, native $AlO_x$, photovoltaics

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