First Results of the European Project "Hiding Dies"

Rolf Aschenbrenner, Andreas Ostmann

Fraunhofer IZM Berlin

aschenbrenner@izm.fhg.de
ostmann@izm.fhg.de

IZM
Fraunhofer Institut
Zuverlässigkeit und
Mikrointegration

berlin

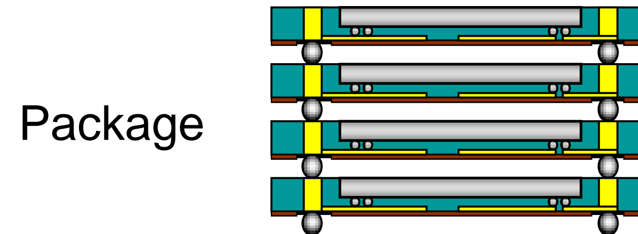
3D System Integration

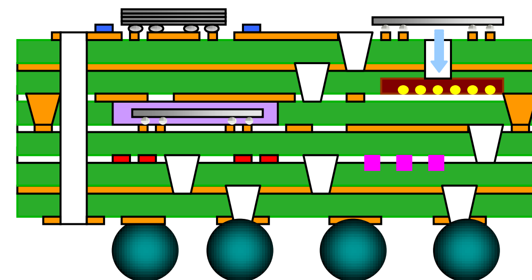
Potential:

- Increased performance
- Increased integration density
- More functionality
- Reduced power consumption
- Minimum volume and weight
- Mixed Technologies

Silicon

Package



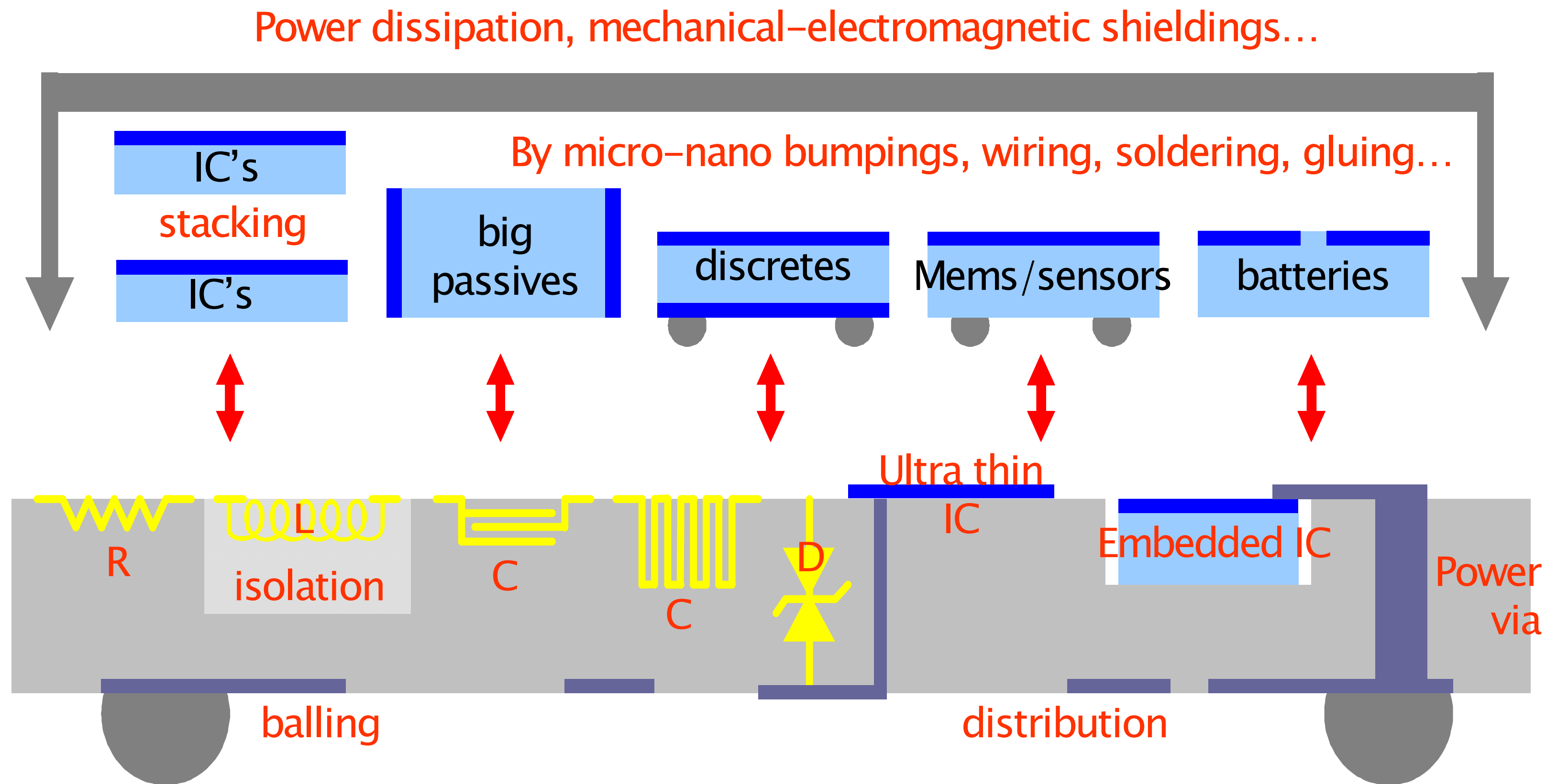


PWB

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

Substrate Level Integration Technology



Source: ST-Microelectronics

Fraunhofer Institut Zuverlässigkeit und Mikrointegration
IZM

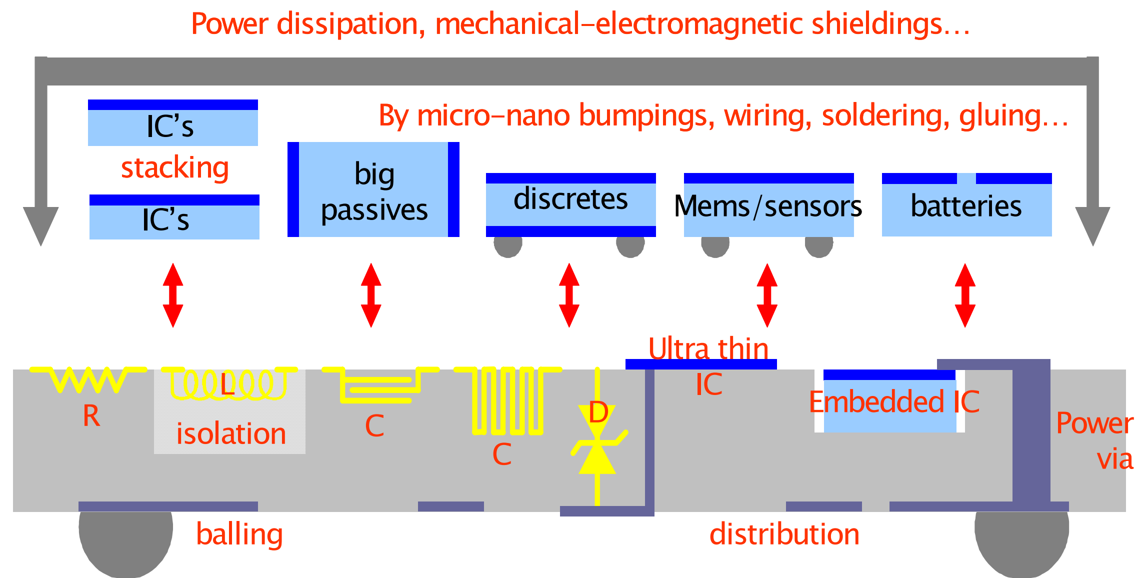
Substrate Level Integration Technology

European Nanoelectronics Initiative Advisory Council

2006+: Embedded devices
(MEMS, passives, antennas,IC´s)

2008+: New Materials
High k and low k dielectrics, High Tg polymers
CTE matching between dice and substrate

2008: Substrate and Interposer
Low cost finer line
& smaller via (25 µm)



2015:
Printable electronics

2012: New Substrate Technologies
Flexible substrates (reel to reel)
Integrated optical interconnects

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

TU berlin

Component Embedding

Components in PCBs

Passives

Resistors	Capacitors	Inductors
Thick Film ▪ polymer printing **Thin Film** ▪ sputtering ▪ electroless deposition ▪ laminate	▪ laminate ▪ polymer printing	▪ etched copper ▪ electroplating ▪ printing

embedding of integrated passive components (IPC)

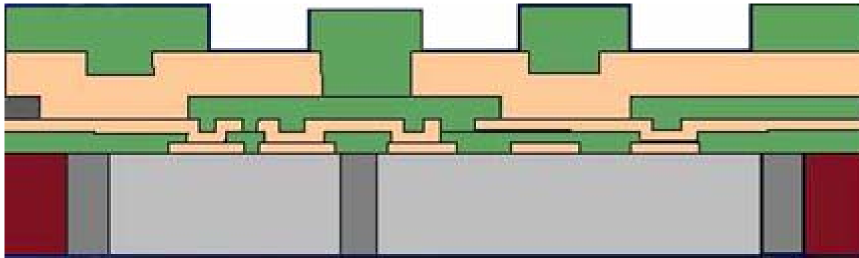
Actives

- Chip First
- Embedding in Core
- Embedded WLP
- Chip in Polymer
- ....

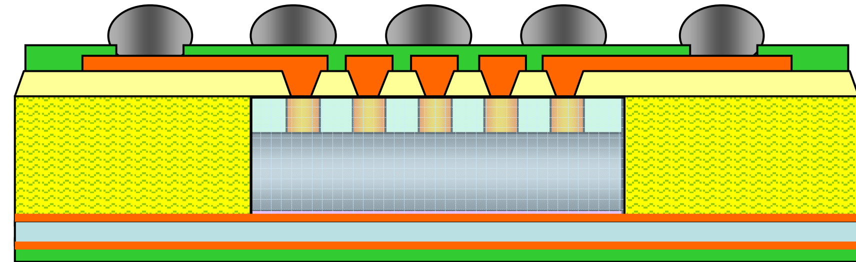
Fraunhofer Institut Zuverlässigkeit und Mikrointegration IZM

TU berlin

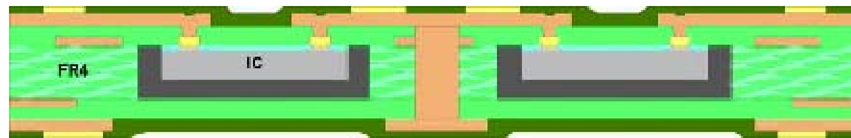
Embedded Chips in PCB – Technology Approaches



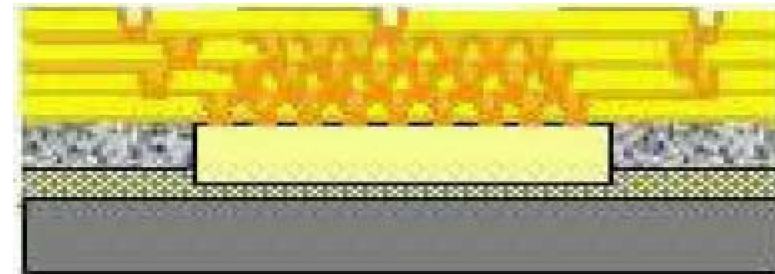
Intel - Bumpless Build-Up Layer



Casio - Embedded WLP



Imbera - Integrated Module Board



GE – Chips First Build-Up™

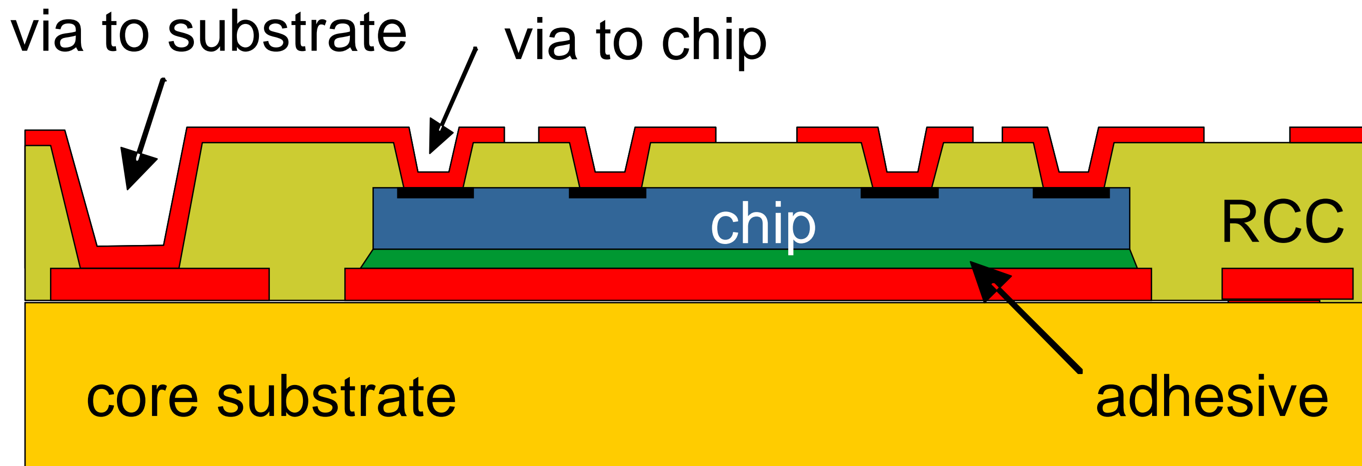
Fraunhofer IZM - Chip in Polymer

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

Chip In Polymer – Basic Concept

➔ **embedding of thin chips into build-up layers of printed circuit boards**



Advantages

- shortests interconnect between chips and substrate
- extremely thin packaging
- capability for 3D component stacking
- use of established processes ând materials
- use of existing machines

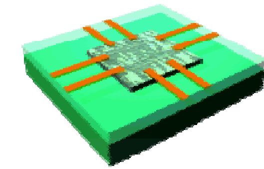
Chip In Polymer – History

- begin of joined development Fraunhofer IZM and
  Technical University of Berlin (TUB) 1998
- patent application 1999, granted 2001 (DE1995494, EP1230680)
- first announcement at PEP (Polymers in Electronic Packaging) 1999
- continuous technology development since 2000
- **Fraunhofer project "Chip in Polymer" 2000**
- **German research project „Chip in Polymer“ 2000 – 2003**
- installation of automatic laser drilling/structuring equipment 2003
- technology transfer to ITRI, Taiwan 2003/2004
- **European research project „Hiding Dies“ 2004 – 2006**
- **European reserch project „Shift“ 2004 – 2007**
- **Industry project „Sensor Embedding“ 2005**
- **German research project „KRAFAS“ 2005-2008 (77 GHz Radar)**

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

HIDING DIES - High Density Integration of Dies into Electronics Substrates

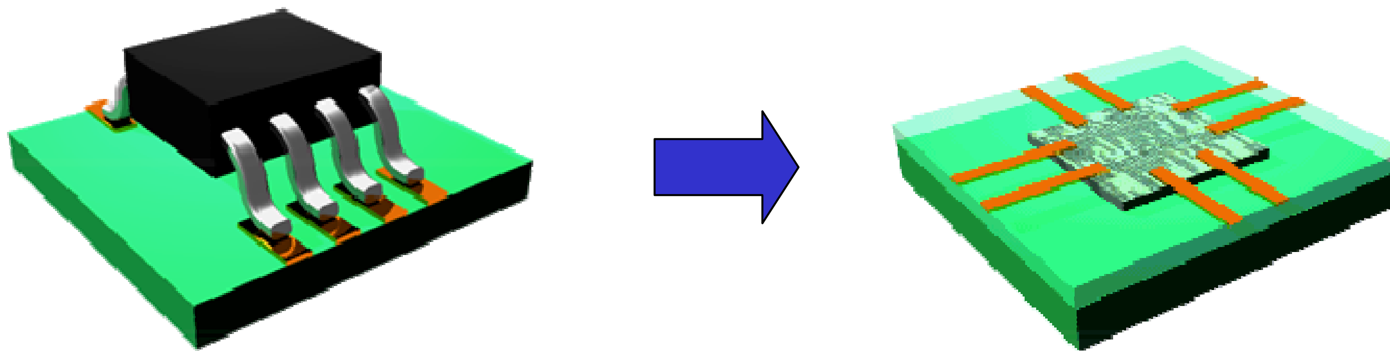


www.hidingdies.net

Project Goal:

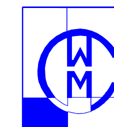
development of a PCB process for embedding of thin active chips

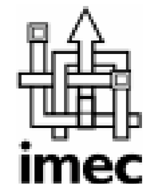
at a large area process on 18“x24“ panels



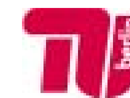
NOKIA

PHILIPS

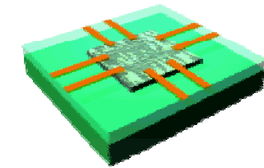




the project is supported by the European Commission, contract IST 507759

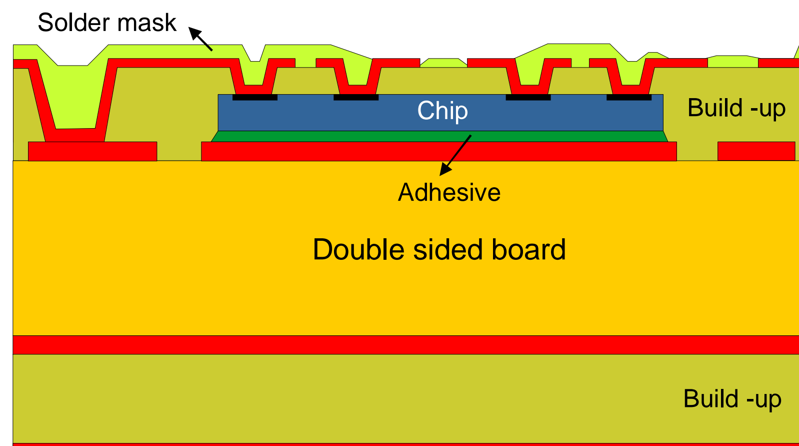


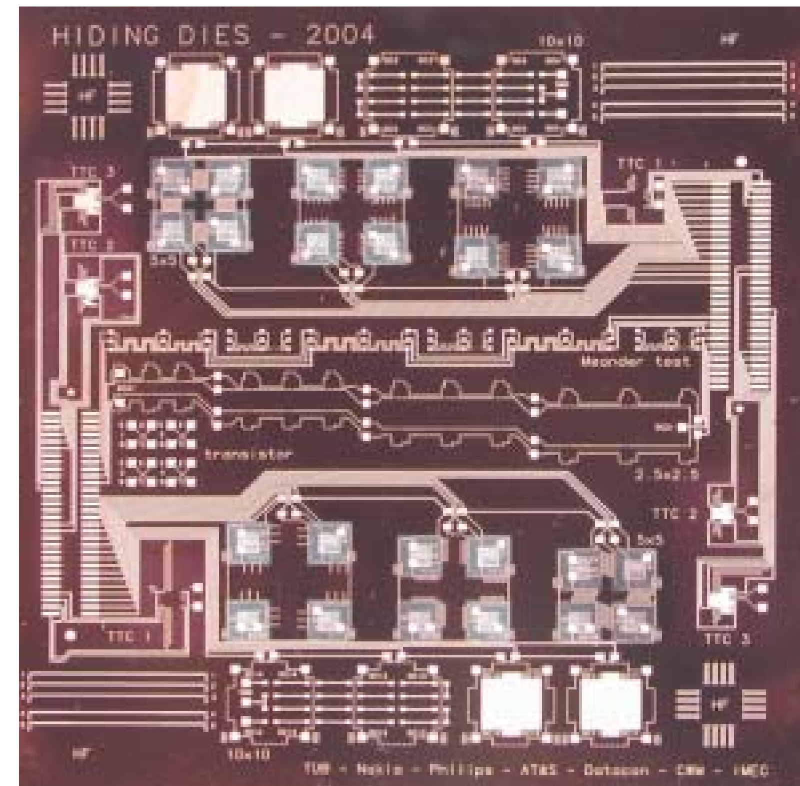
Test Vehicle



www.hidingdies.net

- manufacturing of test vehicles on 10x10 cm² panels for process development
- 18“x24“ panels containing 12 test vehicles were manufactured in PCB production line
- test vehicle features
  - 72 embedded test chips 2.5x2.5 – 10x10 mm², min. pitch 200 µm
  - thermal test chips, 2 W
  - daisy-chain and 4PK structures
  - rf test structures
  - SMDs over embedded chips



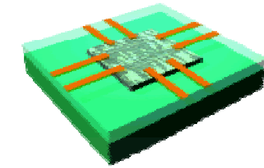


10x10 cm² test vehicle with embedded chips

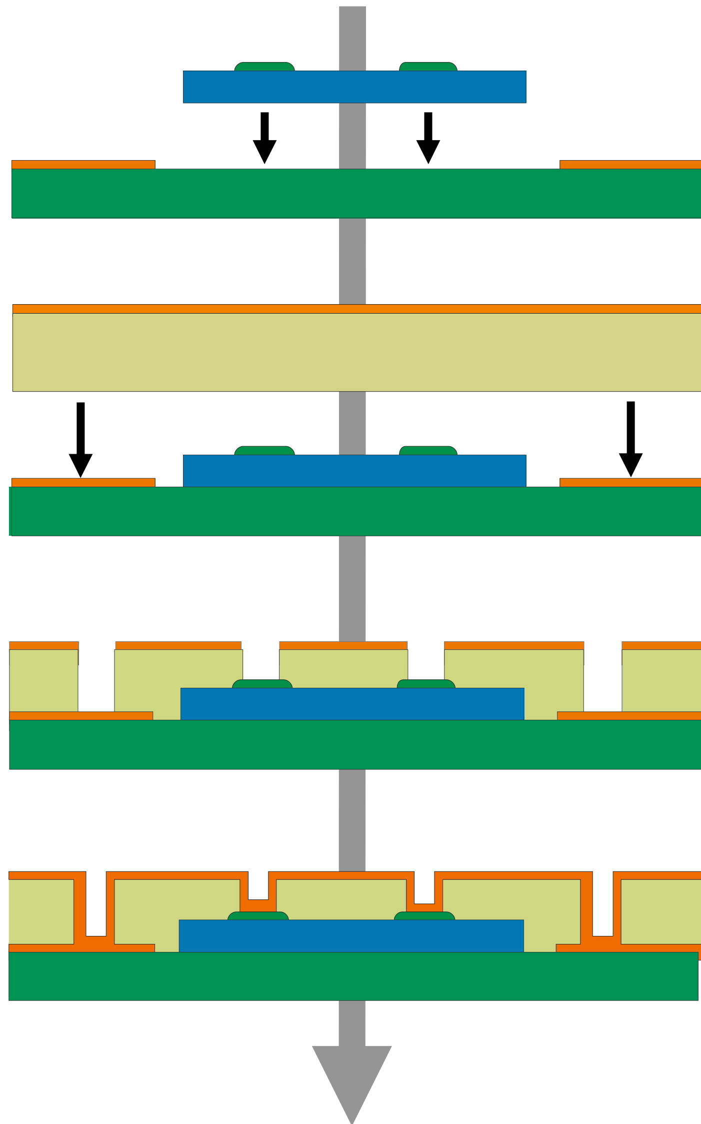
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

IZM

Chip in Polymer – Basic Process Flow



www.hidingdies.net

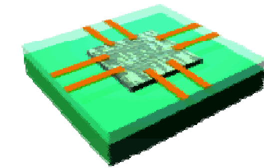


- conventional (multi-layer) substrate
- **die bonding** of thin chips (≤ 50 µm) with Cu bumps (5 µm)
- embedding of chips by vacuum **lamination** of RCC™ (Resin Coated Copper)
- **laser drilling** of vias to chip and substrate
- Cu **metallization** of vias
- **structuring** of Cu layer
- optional processing of further layers

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

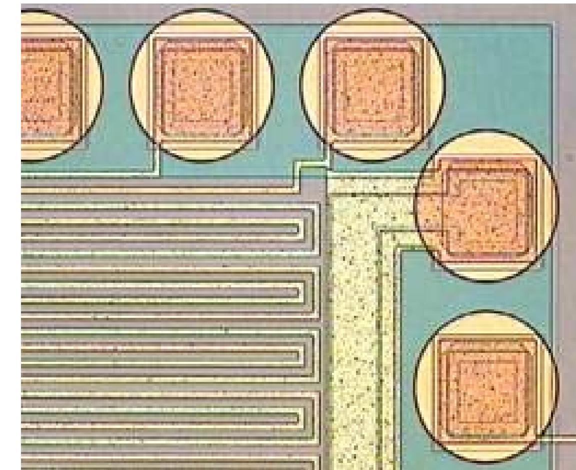
Wafer Bumping and Thinning



www.hidingdies.net

Cu Bumping

- metallization of bondpads is not compatible with laser drilling and PCB metallization process
- Cu bumps are applied by TiW/Cu sputtering, lithographic structuring and electroless Cu reinforcement to 5 µm thickness
- use of Cu redistribution layer (RDL) for chips with small pitches (<150 µm)



sputtered Cu layer over bondpads

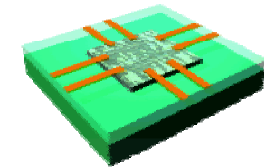
Wafer Thinning

- wafers are thinned to 50 µm
- thickness variation wafer to wafer is still an issue

Dicing

- mounting of wafers on UV dicing tape or Die Attach Film
- standard dicing and UV exposure of tape for reduced chip tackyness

Die Bonding - Methods



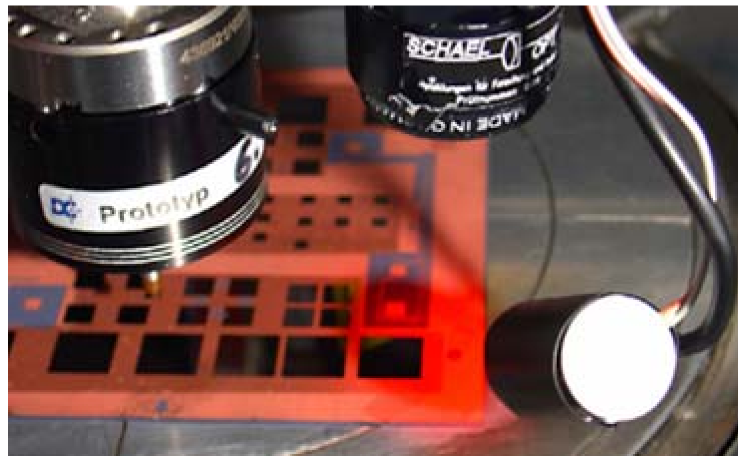
www.hidingdies.net

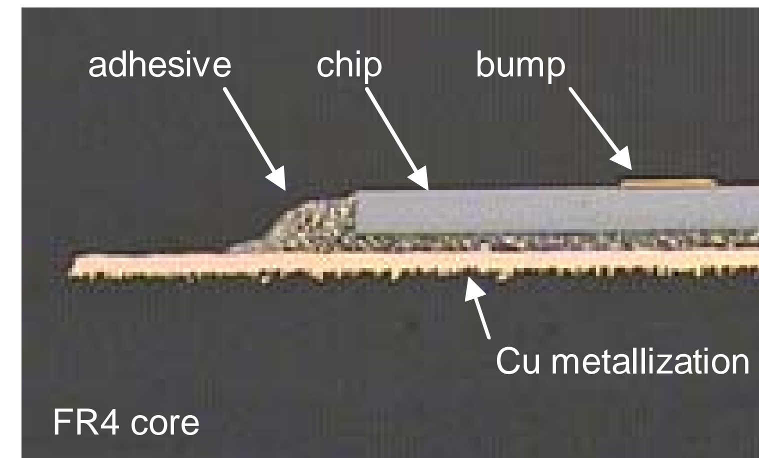
Adhesive

- different materials are evaluated
  - die attach film on wafer backside
  - screen printing of Ag-filled paste
  - screen printing of b-stage paste and drying

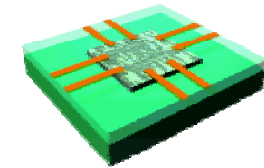
Bonding

- fully automatic die bonding of thin chips
- core substrate with oxidized Cu requires improved illumination





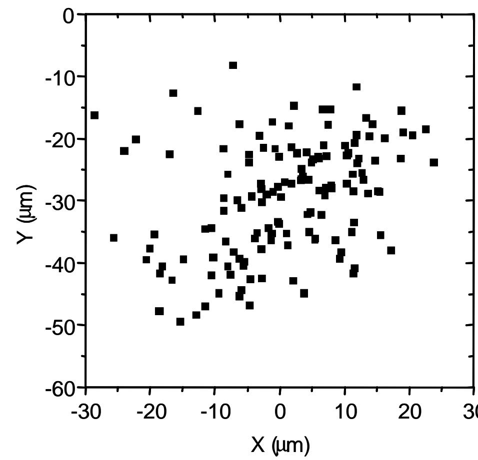
Die Bonding - Development

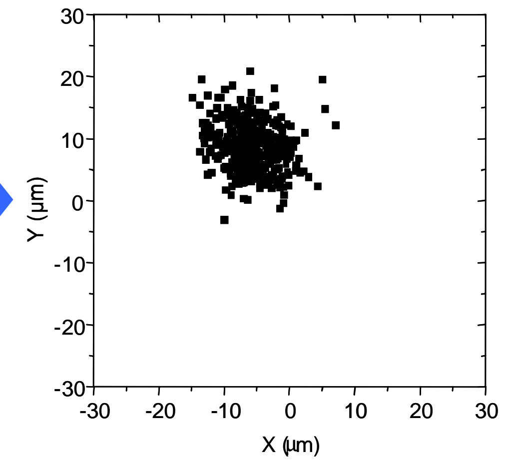


www.hidingdies.net

Process Optimization

- improvement of die bond accuracy for 50 µm chips with 10x10 mm² size
- ±11 µm @ 3σ achieved





improvement of die bond accuracy

needle-less eject heads

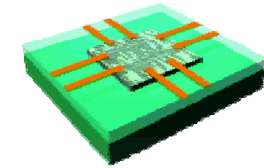
Equipment Development

- development of a needle-less eject system
- suitable for chips down to 20 µm thickness
- improved illumination system for recognition of dark PCB structures
- system already commercially available

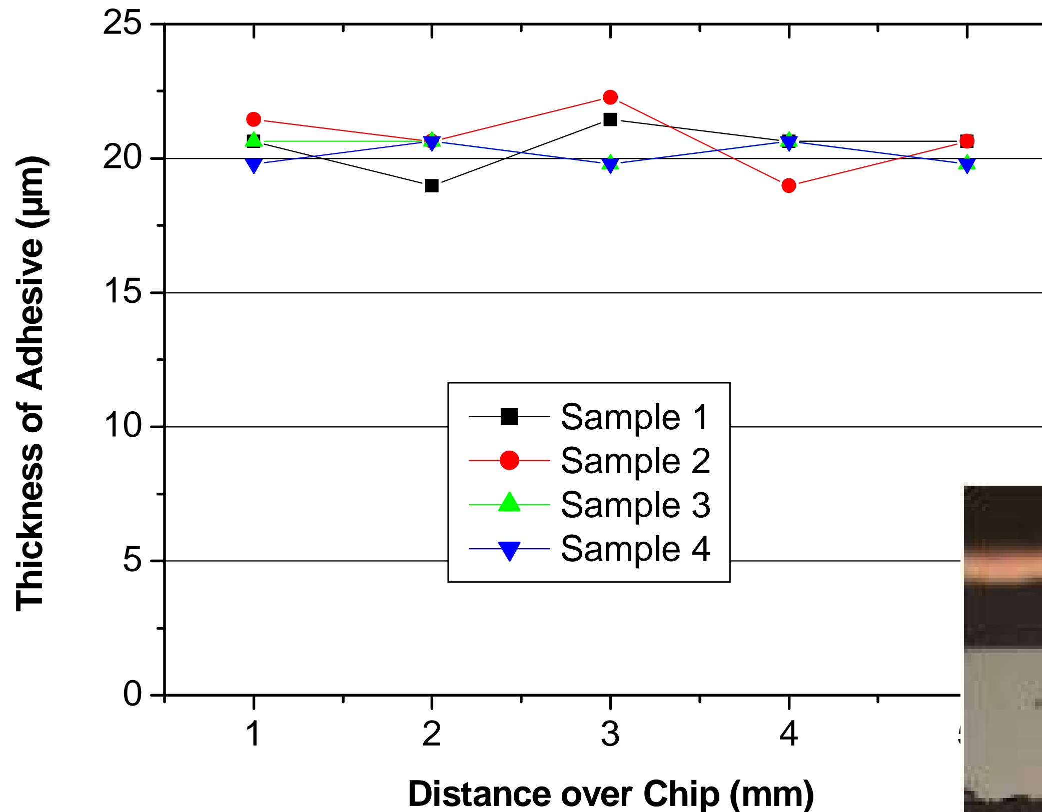
IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

Die Bonding – Bond Line Thickness

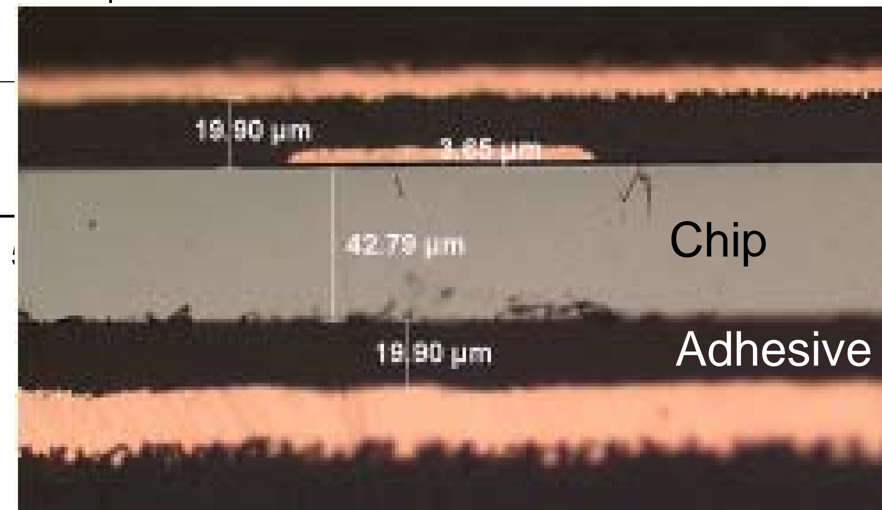


www.hidingdies.net



bond line thickness after lamination
(die attach film)

- die attach film provides very good bond line uniformity
- better thermal conductivity by printed paste
- but still issues with small voids

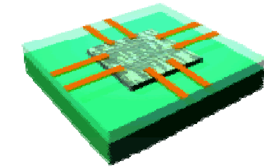


cross-section of embedded chip

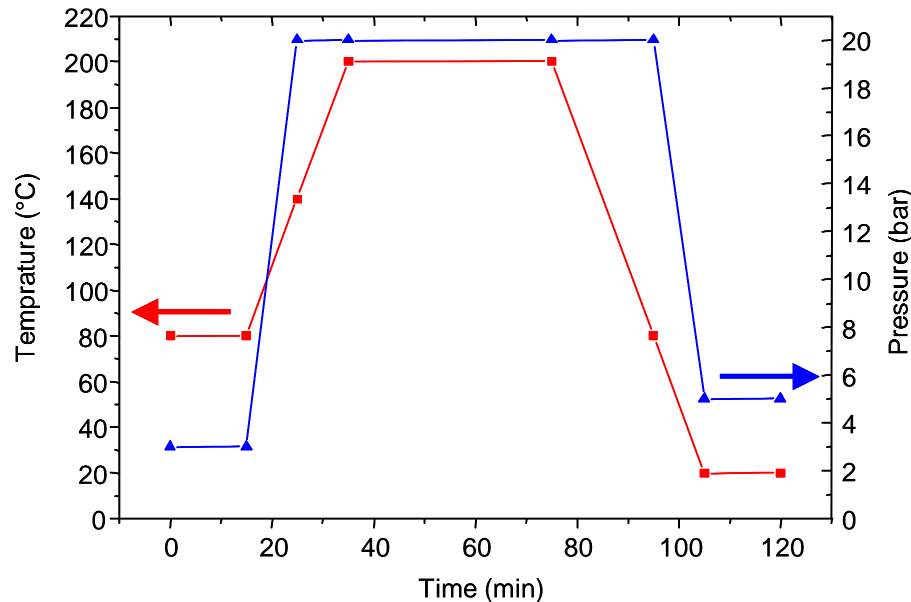
Fraunhofer Institut Zuverlässigkeit und Mikrointegration IZM

TU berlin

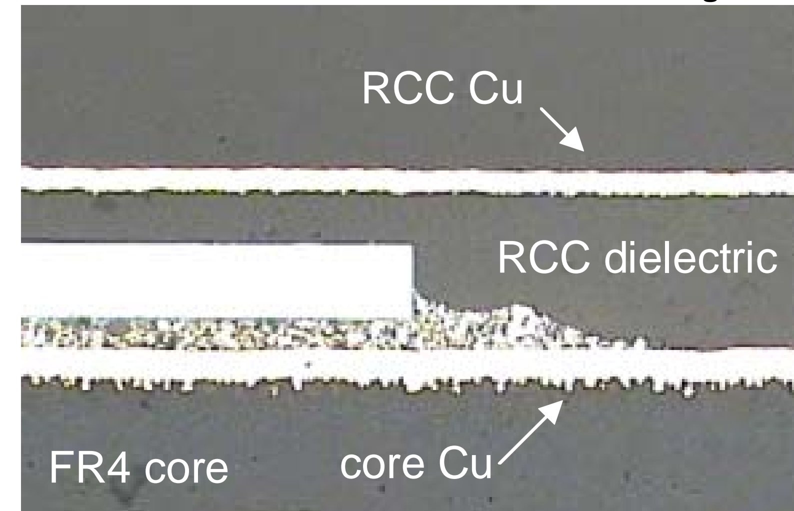
Lamination - Process



www.hidingdies.net



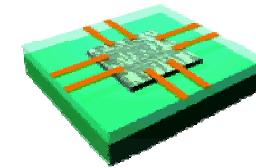
temperature / pressure profile for lamination

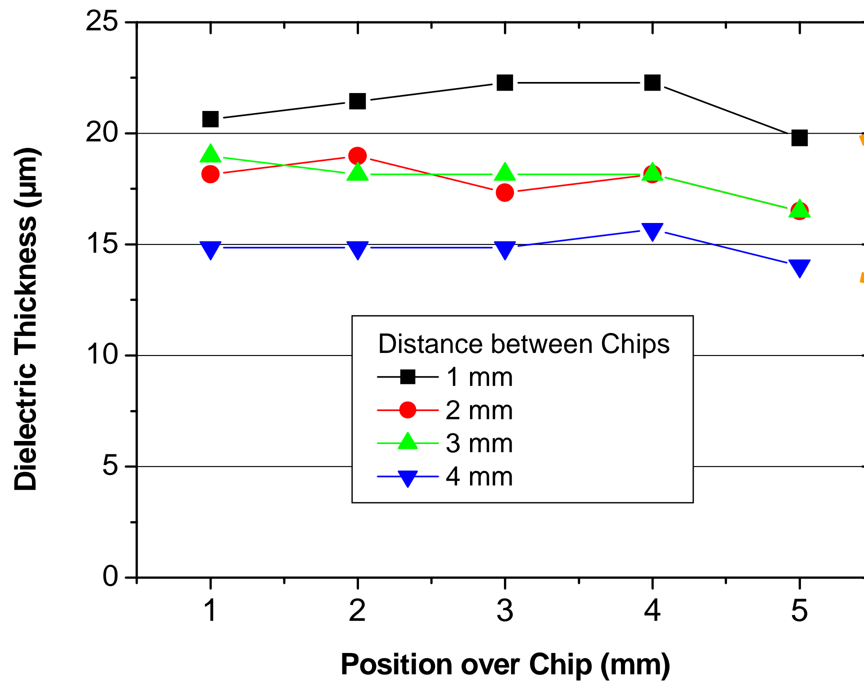


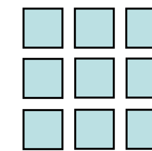
cross-section of embedded chip

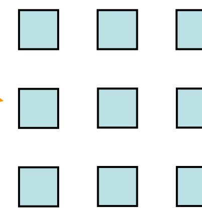
- use of filled epoxy-based RCC with 80 µm dielectric and 5 µm Cu
- embedding of chips by vacuum lamination of RCC
- at optimized parameters no chip breaking during or after lamination
- void-free embedding of 10x10 mm² chips
- no relevant movement of chips during lamination

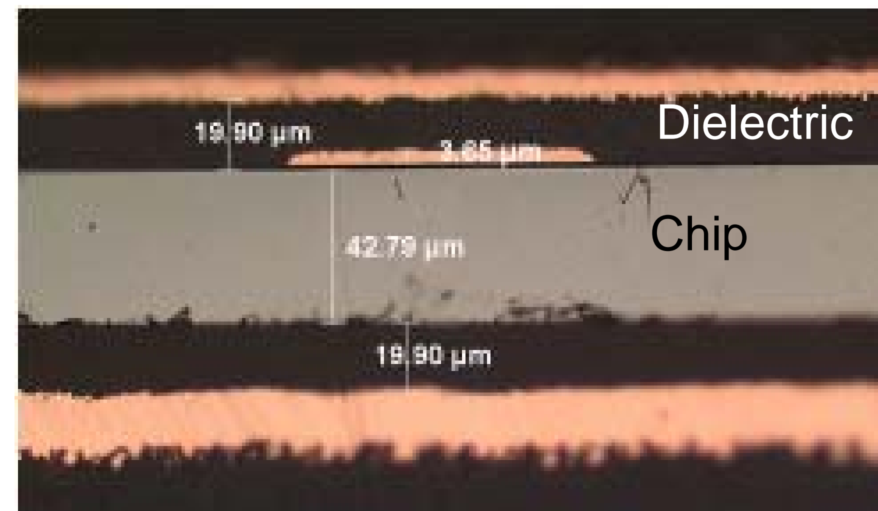
Lamination – Dielectric Thickness over Chip


www.hidingdies.net




1 mm space between 5 mm chips

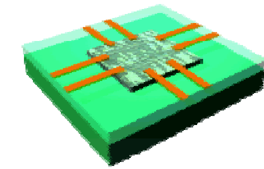

5 mm space between 5 mm chips



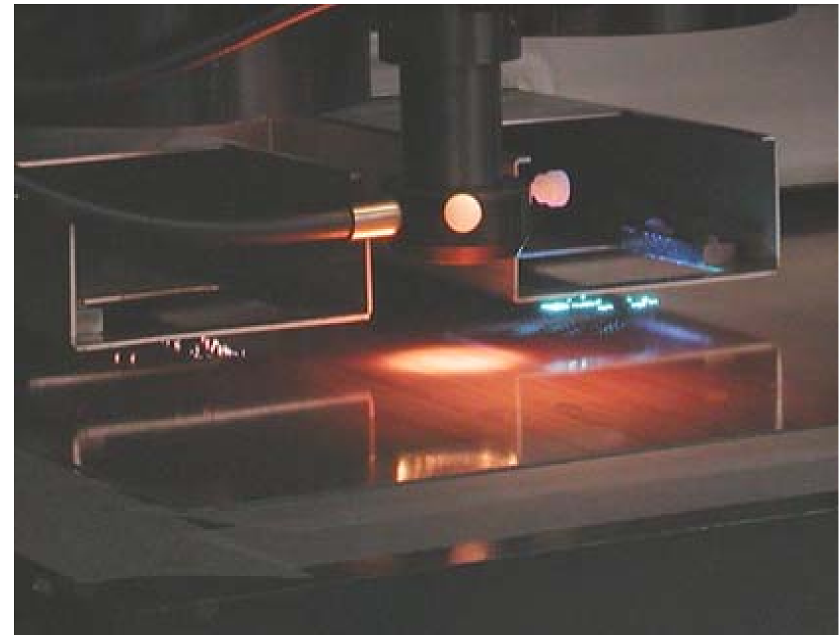
cross-section of embedded chip

- influence of chip density on dielectric thickness
- effect can be reduced by optimized lamination cycle
- optimum dielectric thickness above chip for via formation is 20 µm

Vias Formation - Laser Drilling and Metallization



www.hidingdies.net



via drilling with dual beam UV/CO_2 laser

Laser Drilling

- different processes were evaluated
- Cu opening by wet-etching, then CO_2 laser drilling down to Cu bump
  - additional litho step
- opening of Cu and dielectric removal by UV laser only
  - risk of drilling into chip

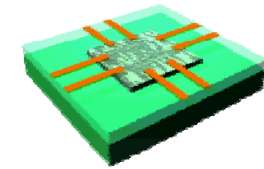
Production Process

- use of UV/CO_2 dual-beam laser
- opening Cu over chip with UV laser
- removing dielectric down to Cu bump by CO_2 laser, using top Cu as mask

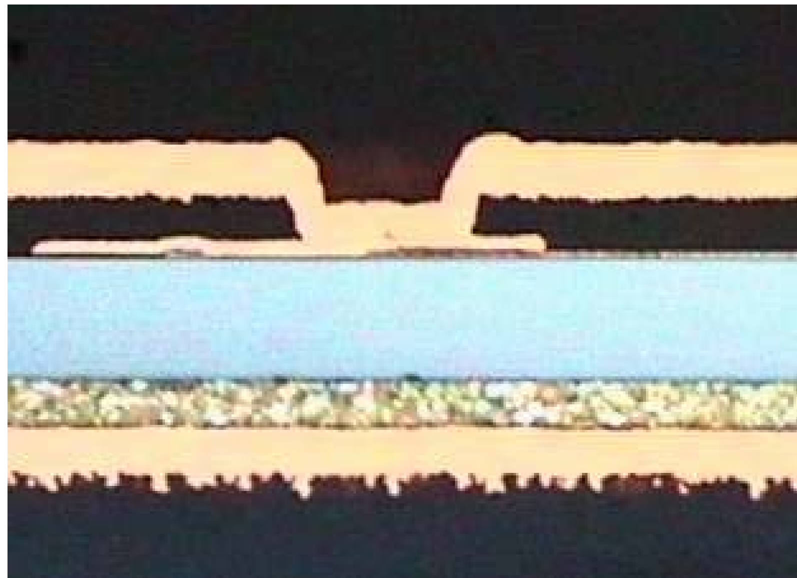
Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

TU berlin

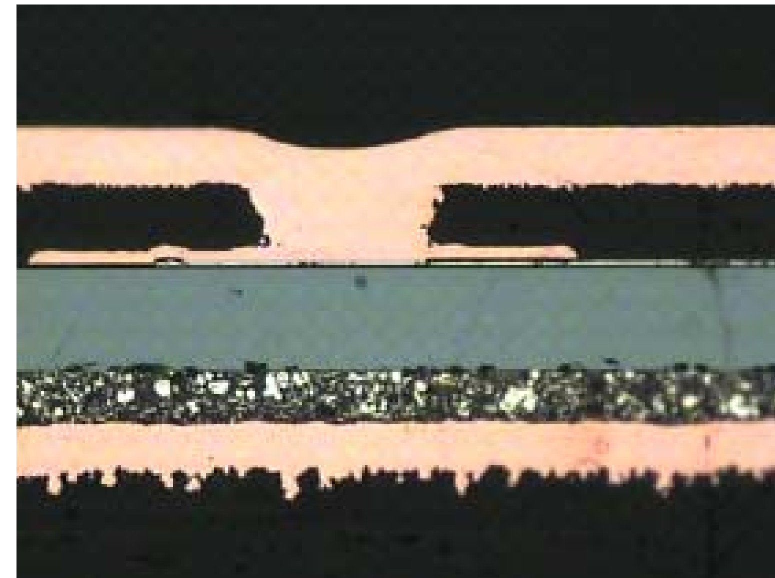
Vias Formation - Metallization



www.hidingdies.net



via to embedded chip



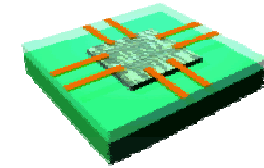
optimized via filling

- generation of electrical contact to embedded chips by via metallization
- chemical cleaning and dielectric activation by Pd solution
- first metallization by electroless Cu deposition
- deposition of thick Cu by electroplatng (DC or pulse plating)

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

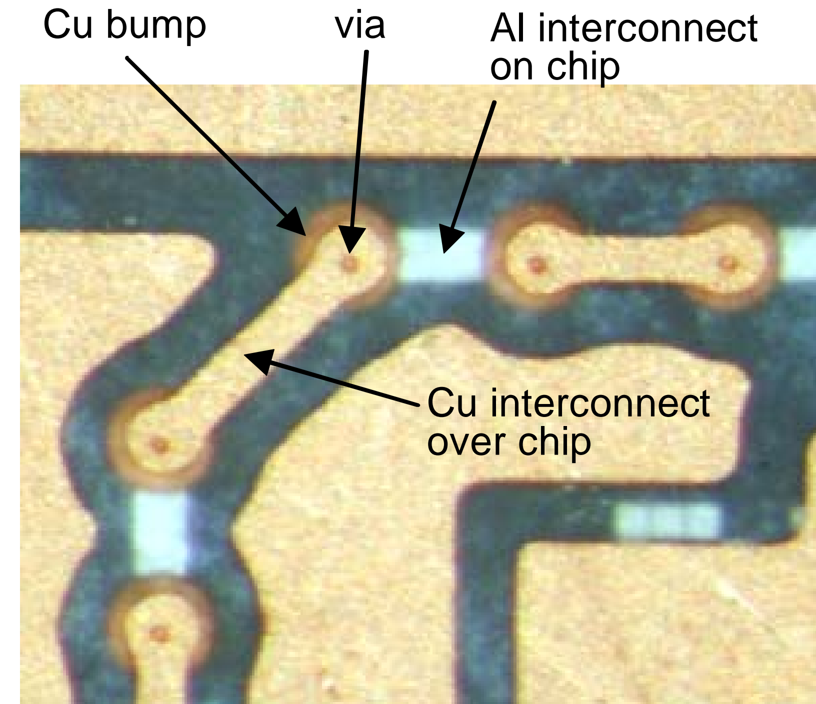
TU berlin

Cu Structuring



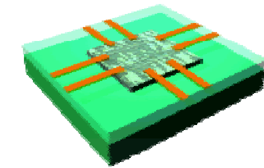
www.hidingdies.net

- on 10x10 cm² substrates
  mask alignment can be used
- large panels require recognition to local fiducials
  - exposure of „reticles“ and stepping
  - laser structuring
- subtractive etching of Cu



Cu layer over embedded chip

Test Vehicle – Reliability Tests



www.hidingdies.net

Jedec Level 3

humidity soak – 192h @ 30°C/60% RH

followed by 3 reflows peak temp. 260 °C (Pb-free)

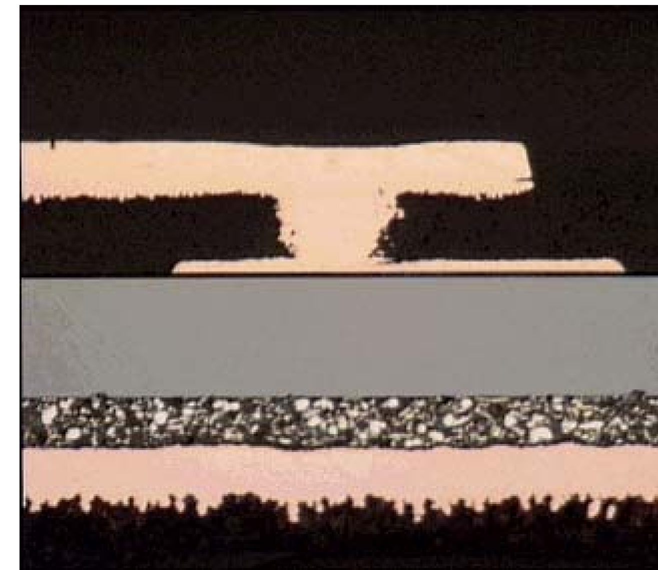
- no delamination after 3 reflows
- no cracks
- interconnections between chip and top layer are okay
- all measurable contacts survived

Thermal Cycling

condition -55 / +126 °C

1000 cycles passed

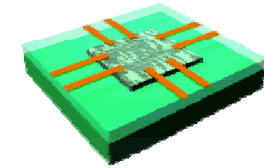
- no cracks
- interconnections between chip and top layer are okay
- all measurable contacts survived



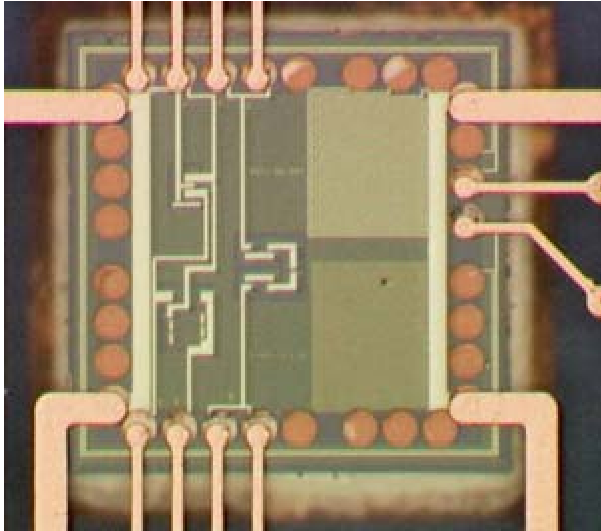
cross-section after Jedec level 3 test

- no delamination after 3rd reflow
- interconnection to chip survived

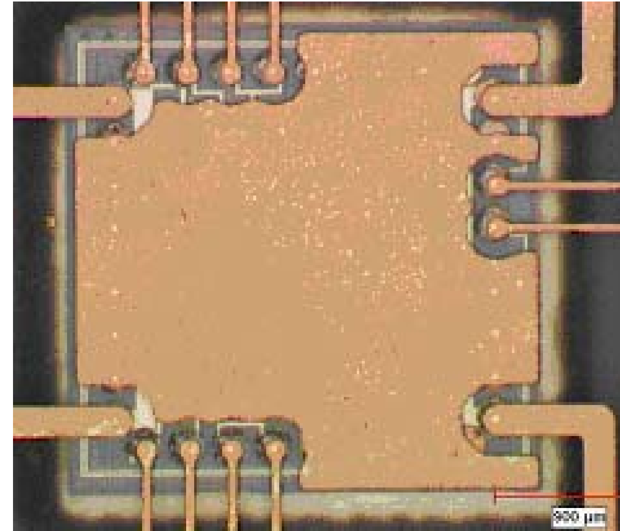
Test Vehicle – Thermal Tests



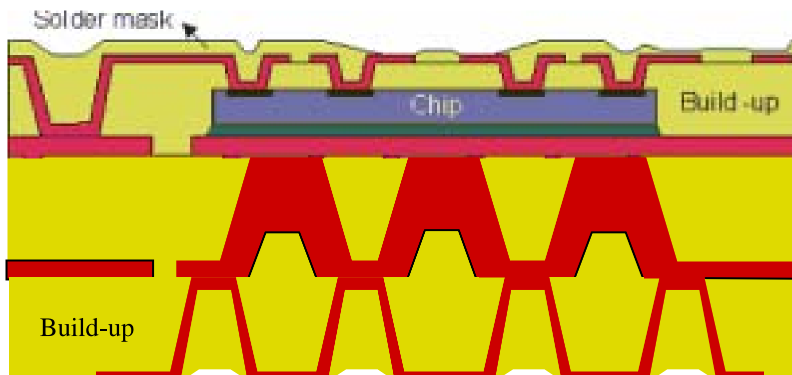
www.hidingdies.net



embedded thermal test chip



thermal test chip with large Cu area on top



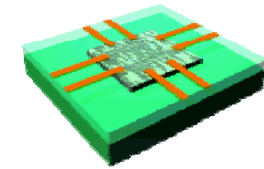
Thermal Evaluation

- heatable chips are bonded on Cu layer
- higher Cu density over chip for better heat spreading
- thermal vias under chip
- first results without thermal vias
  ΔT 35 K @ 1 W

IZM
Fraunhofer Institut
Zuverlässigkeit und
Mikrointegration

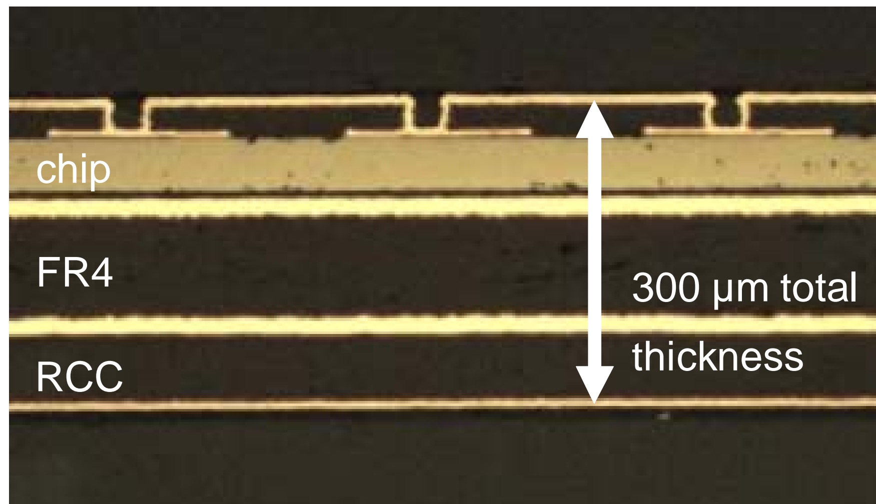
TU berlin

Mid-term Achievements

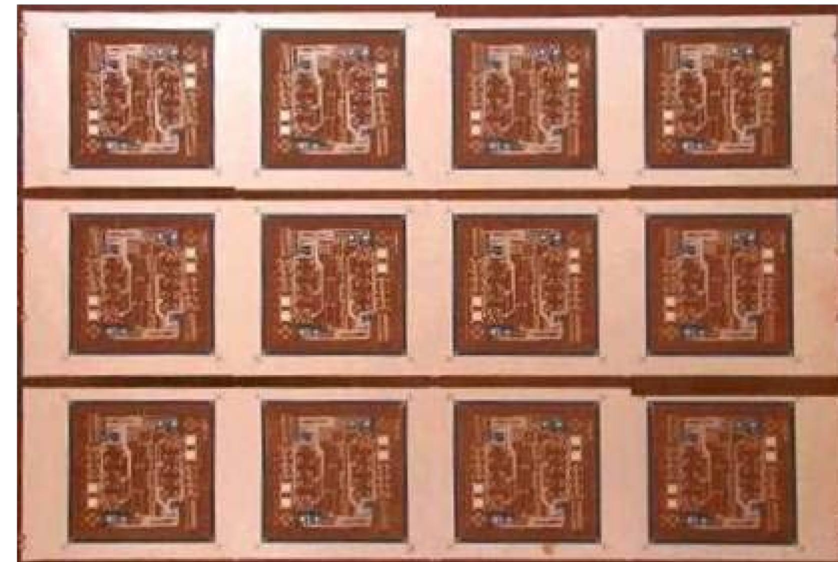


www.hidingdies.net

- after the first 24 months a generic technology for embedding ultra-thin chips into PCBs has been developed
- initial development done on 10x10 cm² substrates
- compatibility of process with 18“x24“ panels, demonstrated at a high-volume PCB production line



x-section of emdecced chip on thin core FR4

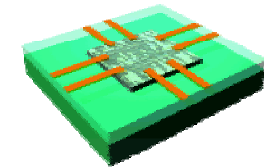


18” x 24” panel including 12 test vehicle substrates

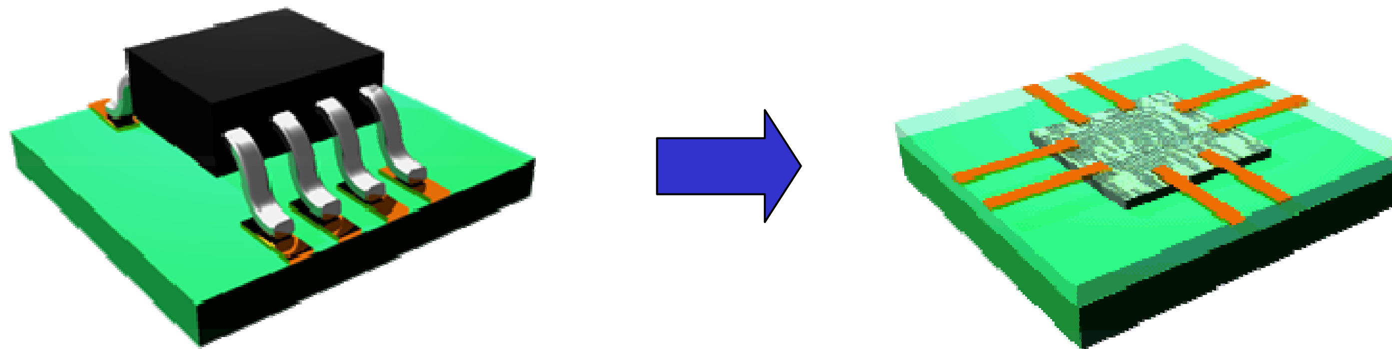
IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

HIDING DIES - High Density Integration of Dies into Electronics Substrates



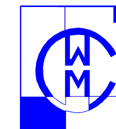
www.hidingdies.net

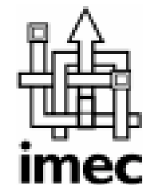


Next Goals

- focus on process cost and yield
- chips with contact pitches below 150 µm
- 3D stacking of multiple layers with integrated chips
- preparation of ddemonstrators

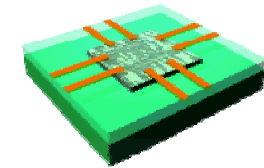
NOKIA PHILIPS





this project is supported by the European Commission, contract IST 507759

Demonstrators



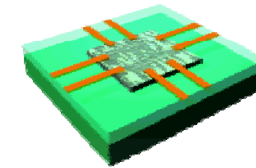
www.hidingdies.net

Chip Card Demonstrator (Philips)
- chip card module with ISO contacts
- one embedded controller IC
- total module thickness < 300 µm

Power RF Demonstrator (Philips)
- evaluation of embedded rf chip
- power dissipation ≈ 2 W
- thermal vias under and around the chip in different configurations

Sensor Demonstrator (Nokia)
- Multi Media Card form factor
- 3 embedded chips (controller ASIC)
- flip chip assembly of sensor chips
- additional SMDs

Outlook



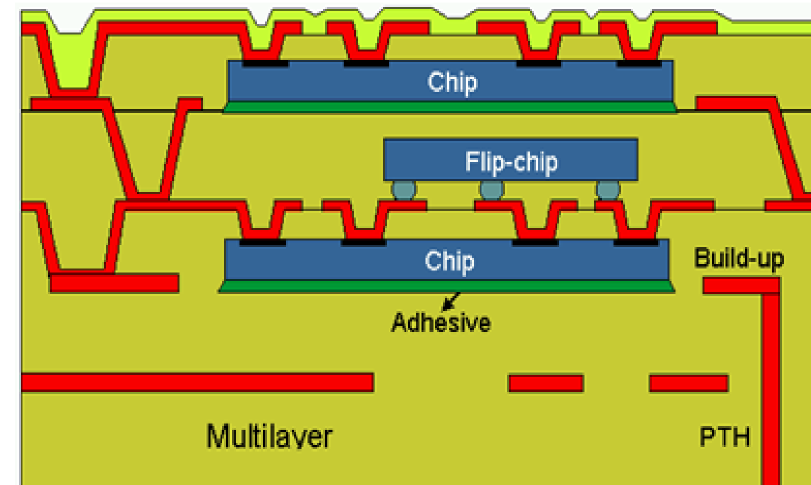
www.hidingdies.net

Coming Investigations

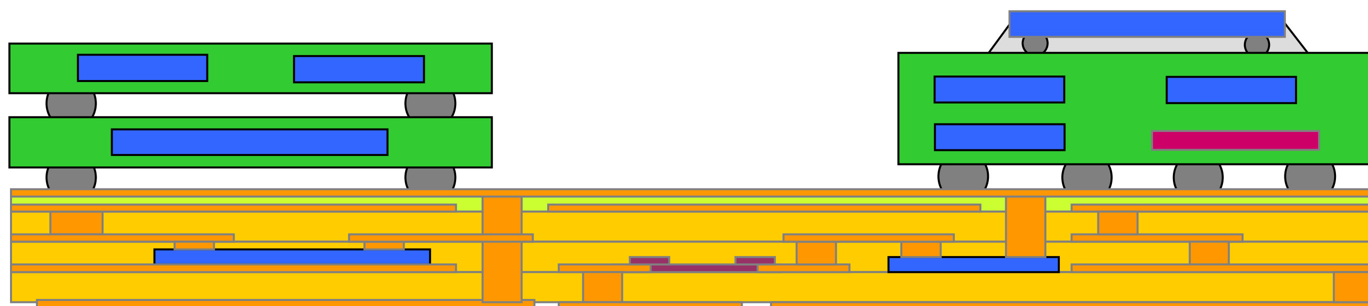
- thermal measurements will be correlated with simulation
- correlation of reliability tests to models
- embedding of extremely thin (20 µm) and large (> 10 mm) chips
- stacking of layers with embedded chips
- embedding of discrete passives

Potential Applications

- thin stackable chip packages
- SiPs for mobile applications
- RF modules

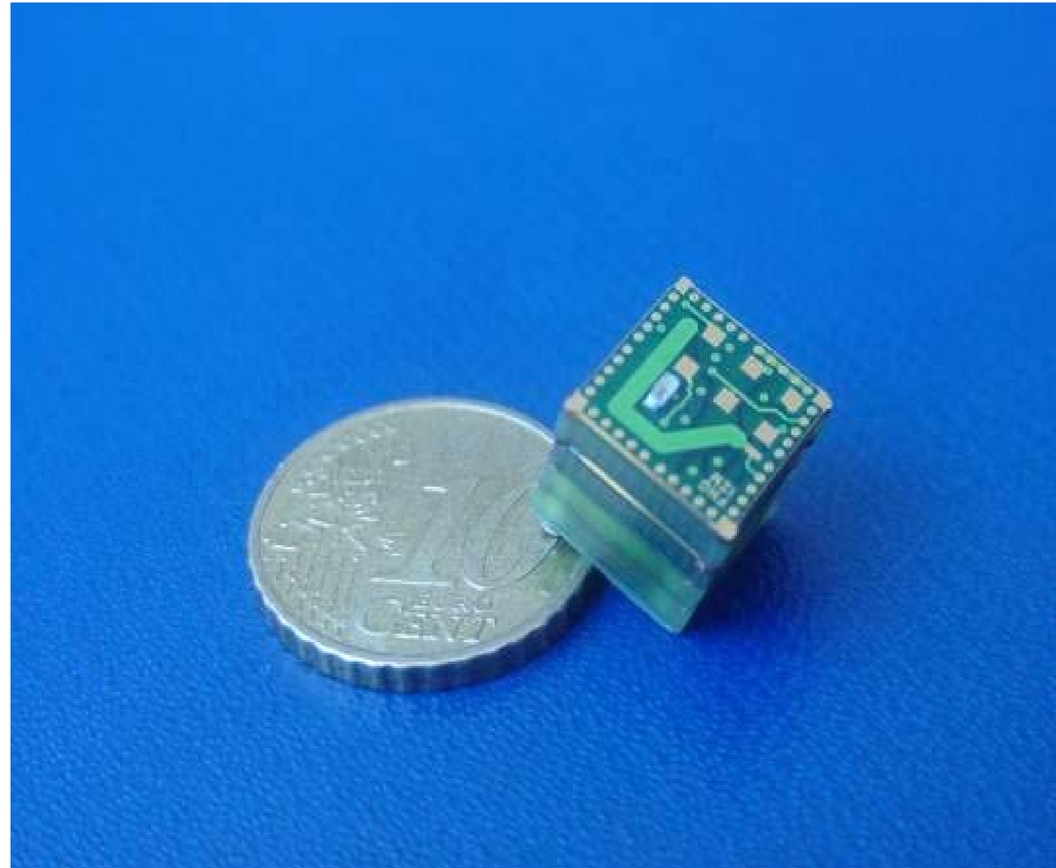


module with 3 layers of embedded chips



IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

eGrain: Wireless Sensor Module



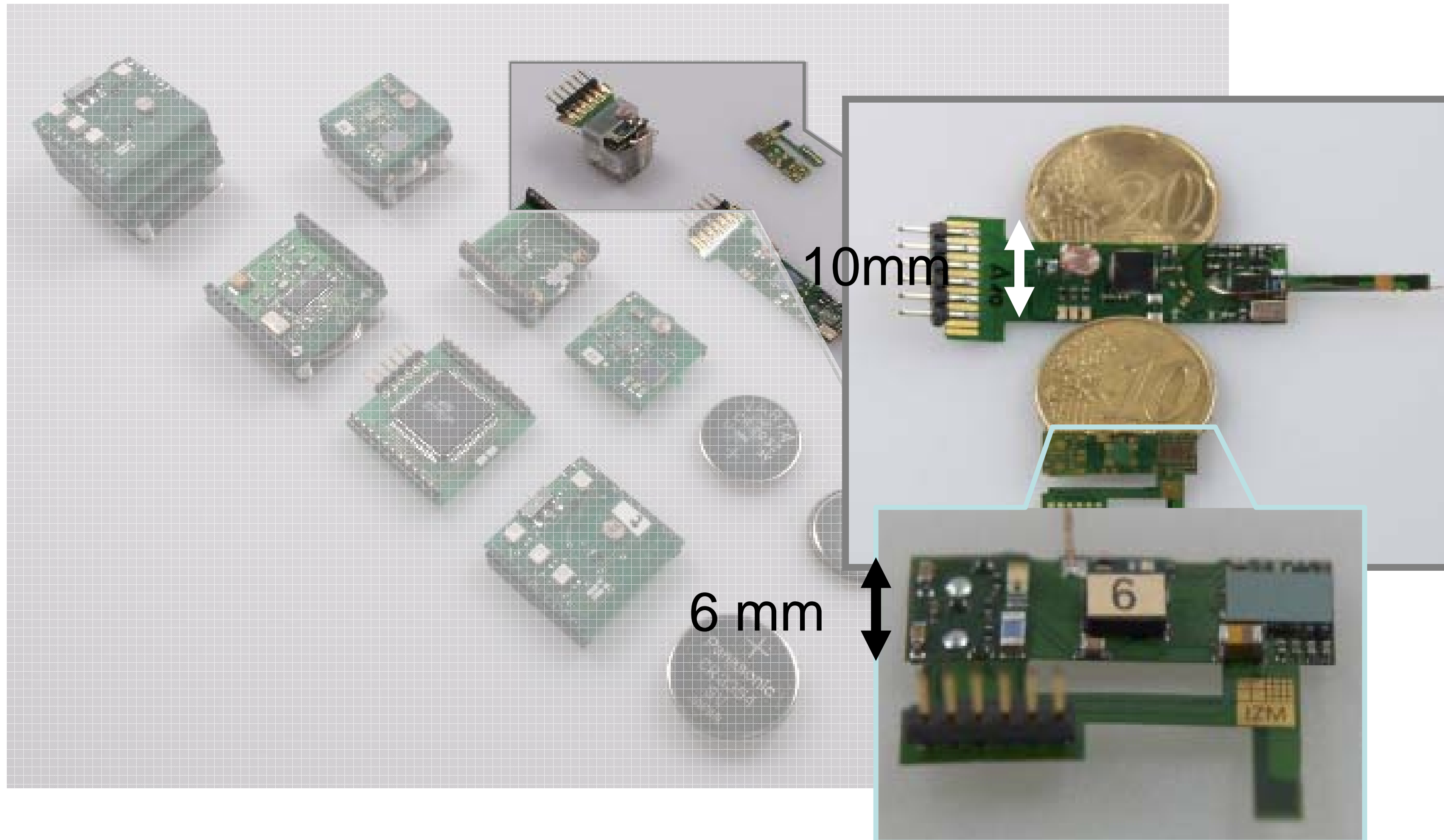
Prototype # 3

- **Communication distance: 1m**
- **Transmission Frequency: 2,4 GHz**
- **Voltage: 3 V (2 x 1,5 V)**
- **Duty cycle: 1 x per sec**
- **Duration time: 500 hour**
- **Size: 10 x 10 x 10 mm³**

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

eGrain Roadmap



IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

TU berlin

Thank You
Meander test
transistor
2.5x2.5
5x5
TTC 1
TTC 2
TTC 3
HF
CWM - IMEC