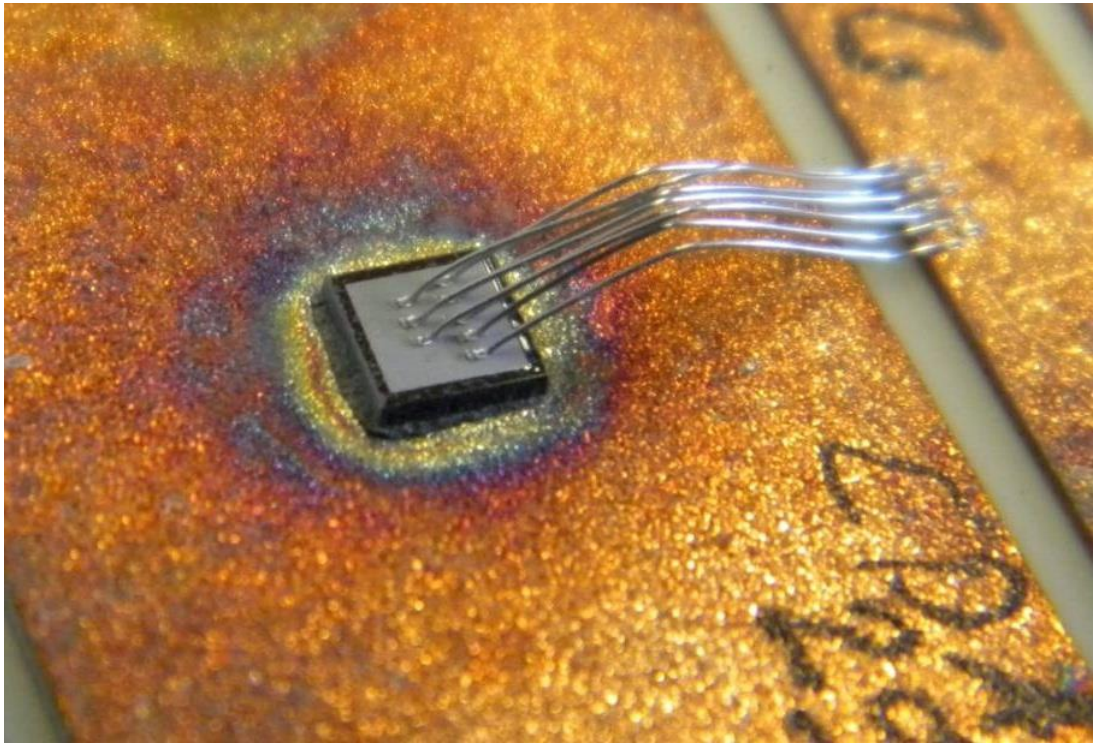
Testing Wide Band-Gap Devices II (Focus on Packaging)

ECPE Tutorial Wide-Bandgap User Training

Andreas Schletz



27.02.2019

ECPE

Fraunhofer IISB

Tests - Summary

- **Power Module** (Investigation of electrical and mechanical parameters)
  - Gate parameter
  - Nominal- und reverse currents
  - Forward voltage
  - XRay, Scanning acoustic microscopy (SAM)
- **Characterizing Tests**
  - Determination of the parasitic inductance (Lp)
  - Determination of the thermal resistance (Rth)
  - Determination of the of short circuit behaviour
  - Isolation test
  - Determination of the mechanical data

Tests - Summary

- **Environmental tests**
  - Thermal Shock (TST)
  - Contactability (CO)
  - Vibration (V)
  - Mechanical Shock (MS)
- **Lifetime tests**
  - Power Cycle (PCsec)
  - Power Cycle (PCmin)
  - High Temperature Storage (HTS)
  - Low Temperature Storage (LTS)
  - High Temperature Reverse Bias (HTRB)
  - High Temperature Gate Bias (HTGB)
  - High Humidity High Temperature Reverse Bias (H3TRB)

Standards

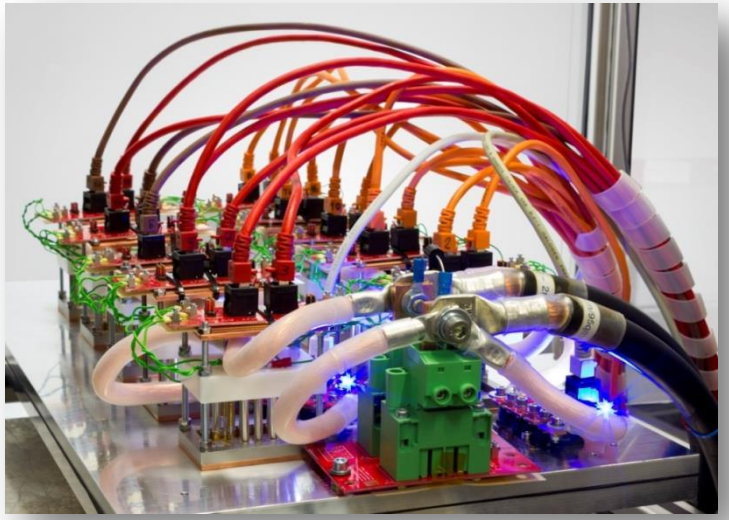
- DIN EN ISO/IEC 17025: Allgemeine Anforderungen an die Kompetenz von Prüf und Kalibrierlaboratorien
- IEC 60747-8:2010 Semiconductor devices - Discrete devices Part 8: Fieldeffect transistors
- IEC 60747-9:2007 Semiconductor devices - Discrete devices Part 9: Insulated-gate bipolar transistors (IGBTs)
- DIN EN 60747-15:2012 Einzel-Halbleiterbauelemente Teil 15: Isolierte Leistungshalbleiter
- IEC 60749-6:2002 Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature
- IEC 60749-34:2010 Semiconductor Devices – Mechanical and climatical test methods – Part 34: Power Cycling
- IEC 60749-25:2003 Semiconductor Devices – Mechanical and climatical test methods – Part 25: Temperature Cycling
- IEC 60068-2-48:1982 Environmental testing – Part 2: Tests Guidance on the application of the tests of IEC 60068 to simulate the effects of storage

Standards

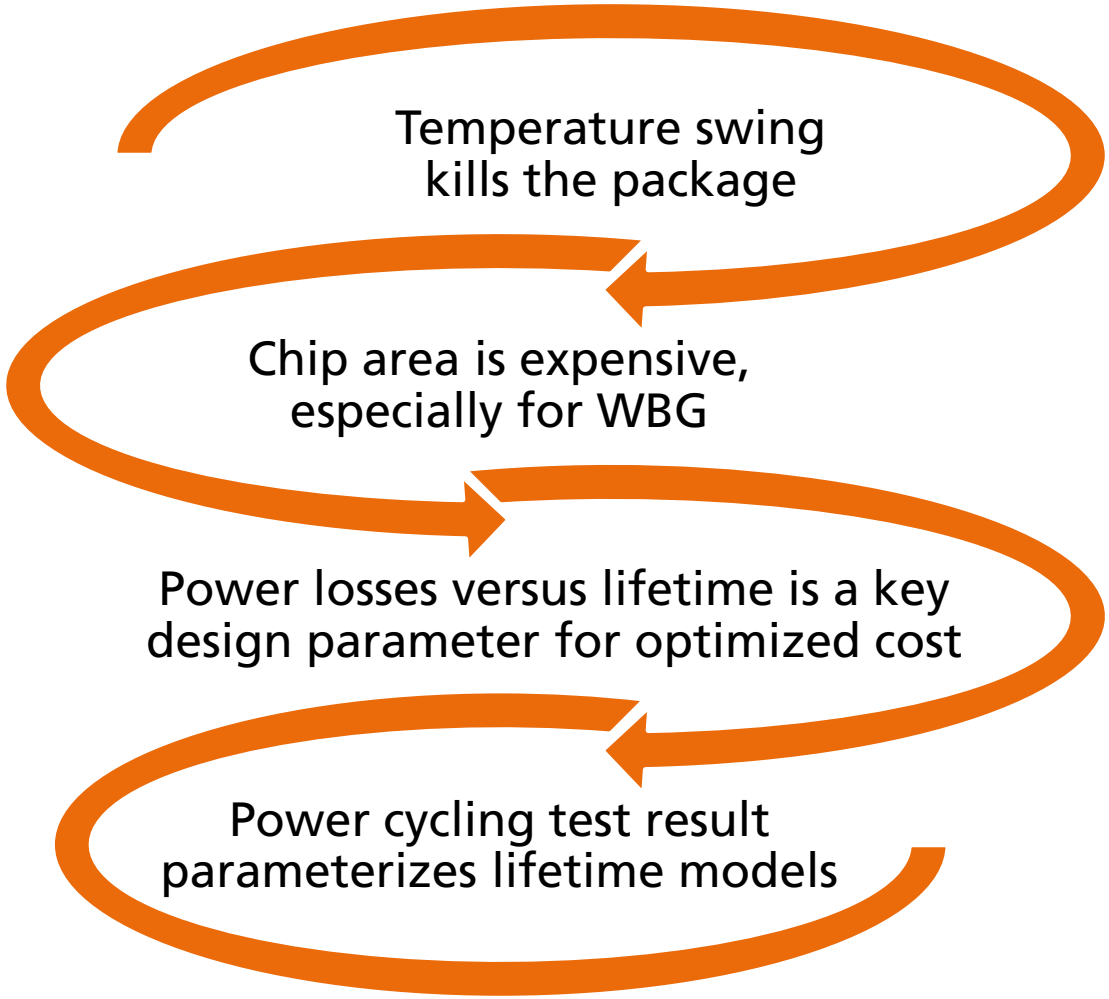
- ISO 6469-3 Electrically propelled road vehicles – Safety specifications Part 3: Protection of persons against electric shock
- DIN EN 60664-1 Isolationskoordination für elektrische Betriebsmittel in Niederspannungsanlagen Teil 1: Grundsätze, Anforderungen und Prüfungen
- DIN EN 60664-1 Beiblatt 1 Isolationskoordination für Niederspannungsbetriebsmittel - Teil 2-1: Anwendungsrichtlinie - Erläuterungen zur Anwendung der Normenreihe IEC 60664, Bemessungsbeispiele und Isolationsprüfungen (IEC/TR 60664-2-1:2011 + Cor. :2011)
- DIN EN 60664-4 Isolationskoordination für elektrische Betriebsmittel in Niederspannungsanlagen Teil 4: Berücksichtigung von hochfrequenten Spannungsbeanspruchungen
- DIN EN 60664-5 Isolationskoordination für elektrische Betriebsmittel in Niederspannungsanlagen Teil 5: Ein umfassendes Verfahren zur Bemessung der Luft- und Kriechstrecken für Abstände gleich oder unter 2 mm
- JESD22-A119:2009 Low Temperature Storage Life
- AQG324

Contents

- Motivation
- Failure Mechanisms
- Heating and Cooling Concepts
- Test Strategies
- Acquisition of the Temperatures
- WBG challenges
- Lifetime
- Interpretation of the Test Result
- Summary



Why Power Cycling Testing



Fraunhofer IISB

Reliability: »Physics-of-failure« Methode

Failure-Mode

Which effect has the failure?

Short circuit, open circuit, overheating and change of el. parameters, …

Failure-Cause

Which process, environmental or design condition triggers the failure?

Mission profile, concept, geometry, joining technology, material properties, cooling, stress …

Failure-Mechanism

Which thermodynamic, chemical or physical process is taking place?

Crack propagation, plastic deformation, creepage, migration, corrosion, diffusion …

Failure-Model

Which mathematical model represents the failure behavior?

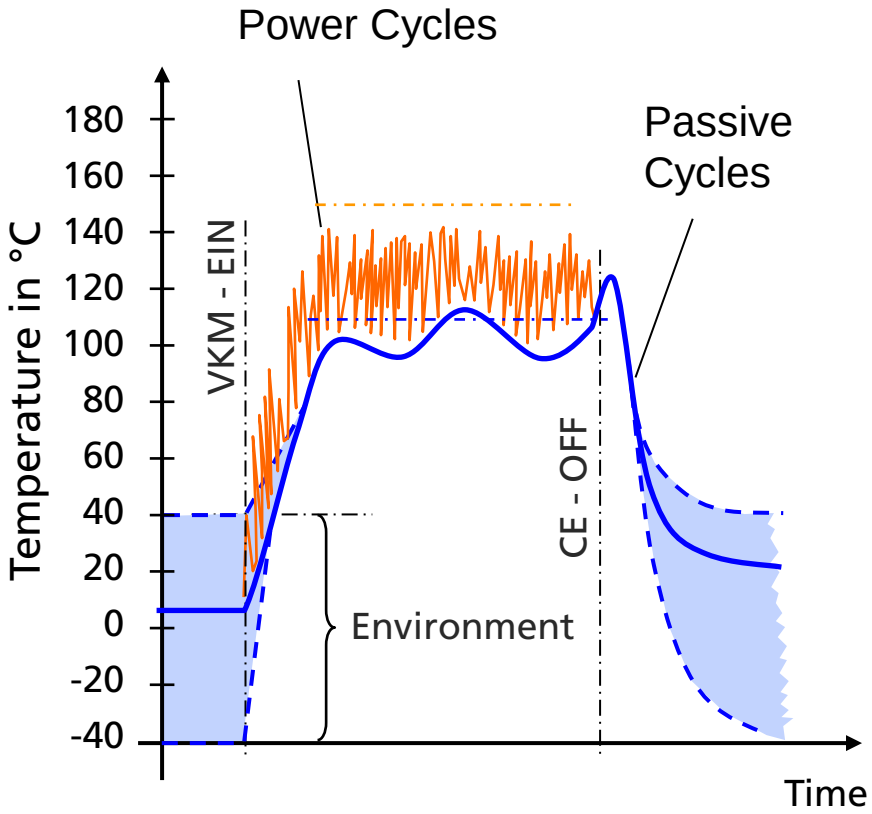
Arrhenius, Timoschenko/ Suhir, Coffin-Manson, Weibull, …

Fraunhofer IISB

Power Cycling, Failure Cause

- Example: Automotive:
  Typical mission profile

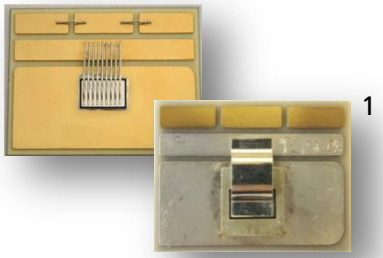
Descriptor	Requirements	Unit
Lifetime	15	a
Operating hours	8.000	h
Driving distance	300.000	km
Passive temperature cycles	10.000	#
Active temperature cycles	3...10 Mio.	#
Reliability	15	a

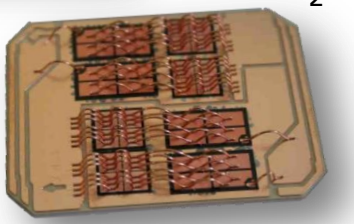


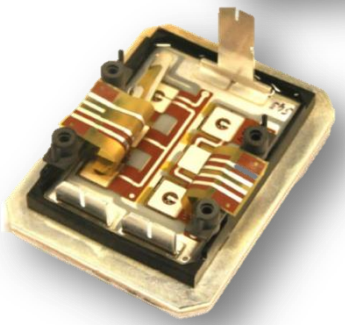
Definition: Temperature swing by self heating caused by the power losses

PCT: Impact on the lifetime: Concept/ Technology (Failure Cause)

- Concepts
  - Indirect/ direct baseplate cooling
  - Indirect/ direct insulating substrate cooling
- Joining Technology
  - State of the art: SnAgCu solder + Al – bond wire
  - Ag-Sintering + Al bond wire with Cu core
  - .XT Technology: Diffusion soldering (Cu, Zn) + Cu – bond wire
  - Skin-Technology: Ag-Sintering + Ag-Sintering of flex board
  - Molded power modules
  - IISB: Ag-Sintering + Ag Sintering of ribbons
- Semiconductor
  - Material properties
  - Geometry (size and thickness)


1


2


3

1) Kraft, S. et al. "Reliability of Silver Sintering on DBC and DBA Substrates for Power Electronic Applications", CIPS, 2012
2) Guth, K. et.al. "New assembly and interconnects beyond sintering methods", PCIM, 2010
3) Beckedahl, P. et. al. "Performance comparison of traditional packaging technologies to a novel bond wire less all sintered power module, PCIM", 2011

Fraunhofer IISB

PCT: Impact on the Lifetime (Failure Cause)

I: Current per bond wire
V: Die thickness
Chips size?
WBG?

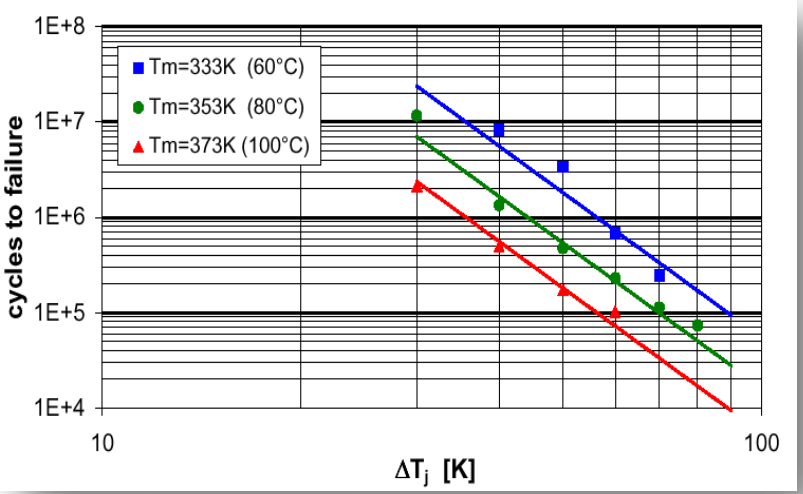
Test Parameter

- CIPS2008-Model (state of the art!)

$$N_f := K \cdot \Delta T_J^{\beta_1} \cdot e^{\frac{\beta_2}{T_j+273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \qquad (1)$$

  Tj: Max. junction temperature, I: Current per bond wire, Ton: Heating time, V: Blocking voltage of the die, D: Diameter of the bond wire)

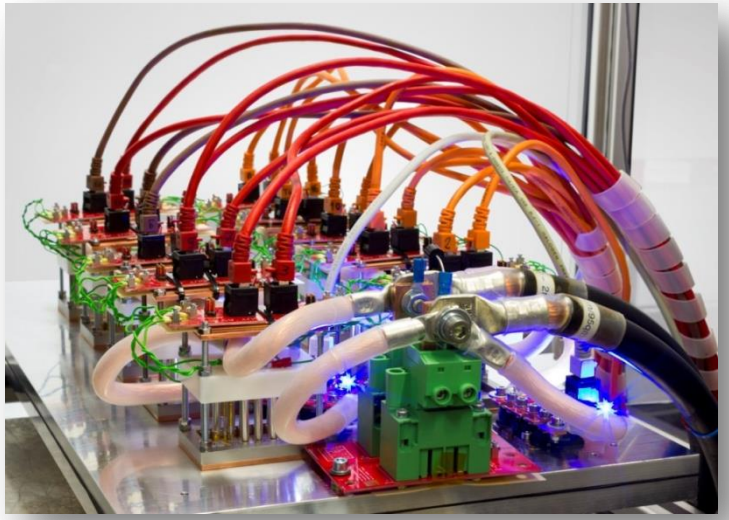
- LESIT:
  Impact on the mean temperature T_m (2)
- Others:
  Heating power over timer, (=temperature gradient), t_{off}, cooling concept, gate voltage, test strategy



1) Bayerer, R et. al. "Model for Power Cycling lifetime of IGBT Modules – various factors influencing lifetime", CIPS 2008
2) Held, M. et. al. "Fast Power Cycling Test for IGBT Modules in Traction Application, Proceedings Power Electronics and Drive Systems, IEEE 1997

Contents

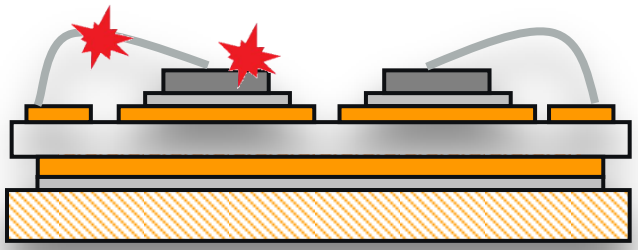
- Motivation
- Failure Mechanisms
- Heating and Cooling Concepts
- Test Strategies
- Acquisition of the Temperatures
- WBG challenges
- Lifetime
- Interpretation of the Test Result
- Summary

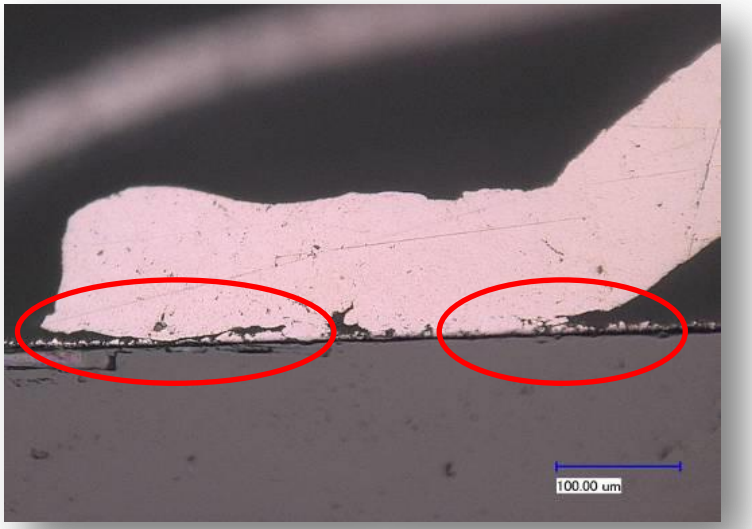


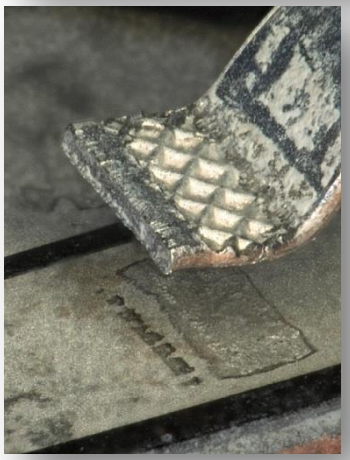
PCT: Failure Mechanisms

Degradation of Chip Metallization, Bond Wire Lift-off

- CTE mismatch of the used materials
- Material properties
- Displacement due to magnetic fields
- Vibration
- Quality of the surfaces
- Bonding parameters







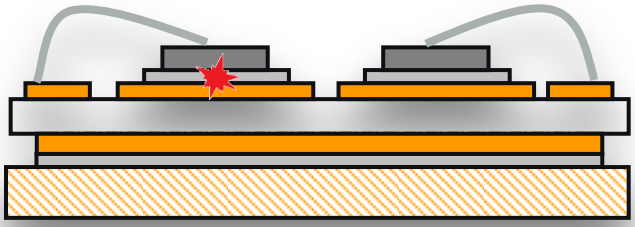
Picture source: Fraunhofer IISB

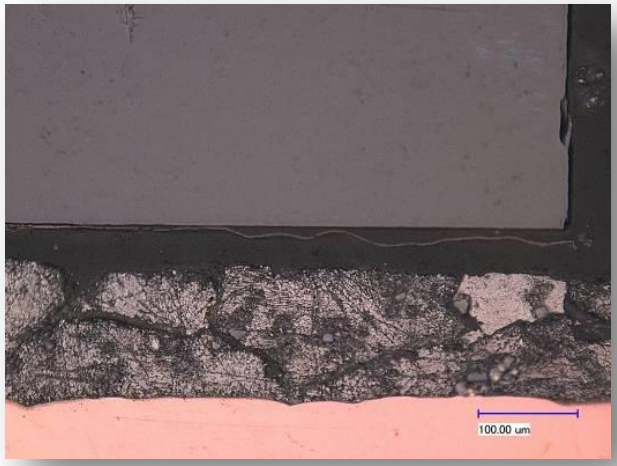
Fraunhofer IISB

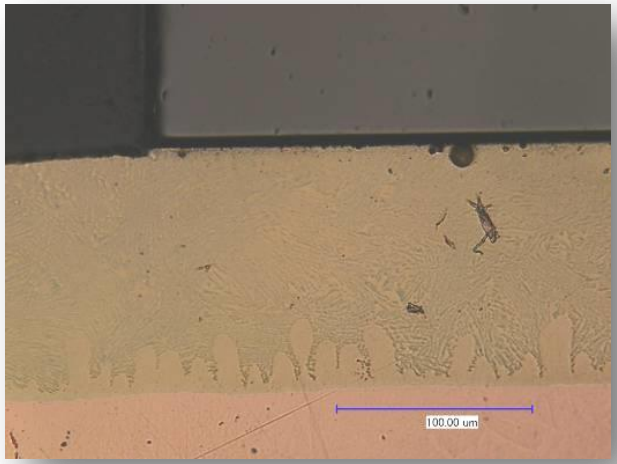
PCT: Failure Mechanisms

“Solder” Degradation

- CTE mismatch of the materials
- Material parameters like E-modulus
- Growth of intermetallic phases
- Cracks
- Delamination of the chip metallization







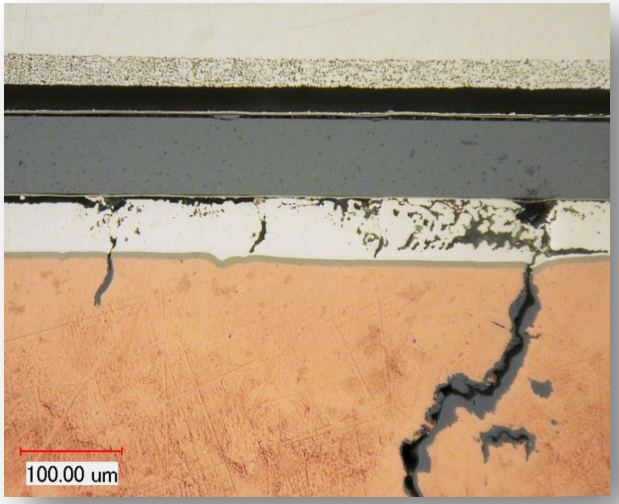
Picture source: Fraunhofer IISB

Fraunhofer IISB

PCT: Failure Mechanisms

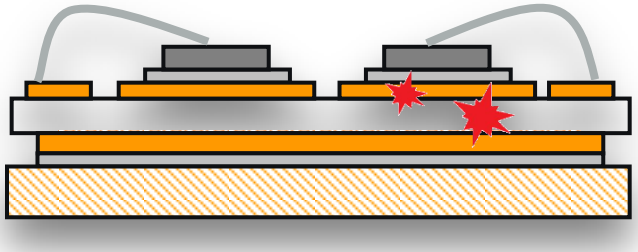
Damage at the insulating substrate DCB

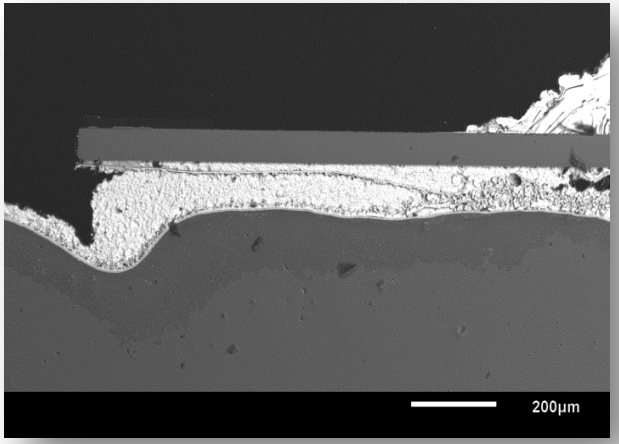
- Vertical cracks in the substrate metal
- Corrosion, oxidation, …



…insulating substrate DAB

- Recrystallization of the metal layer
  → Corrugated chip bond line



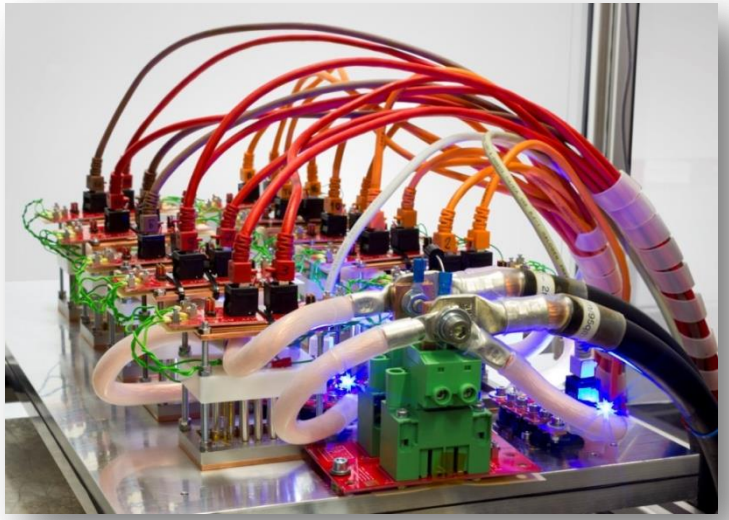


Picture source: Fraunhofer IISB

Fraunhofer IISB

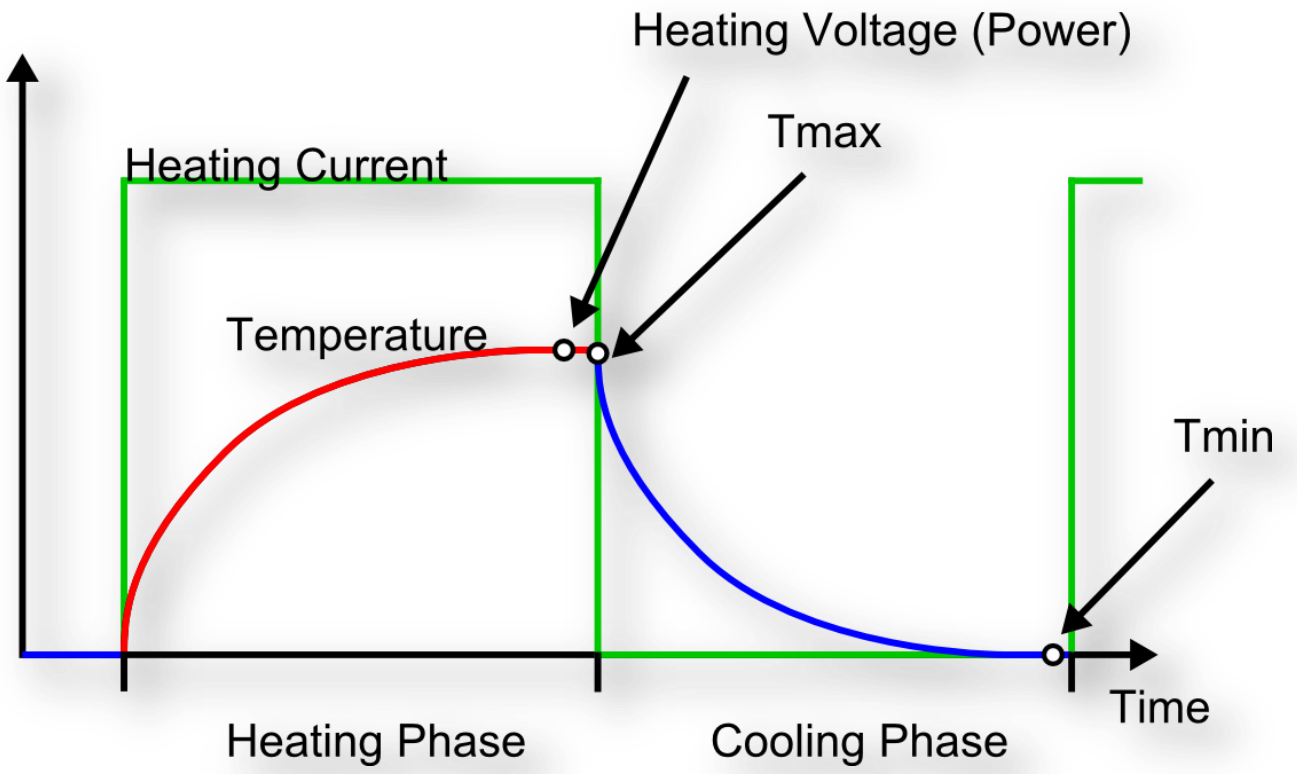
Contents

- Motivation
- Failure Mechanisms
- Heating and Cooling Concepts
- Test Strategies
- Acquisition of the Temperatures
- WBG challenges
- Lifetime
- Interpretation of the Test Result
- Summary



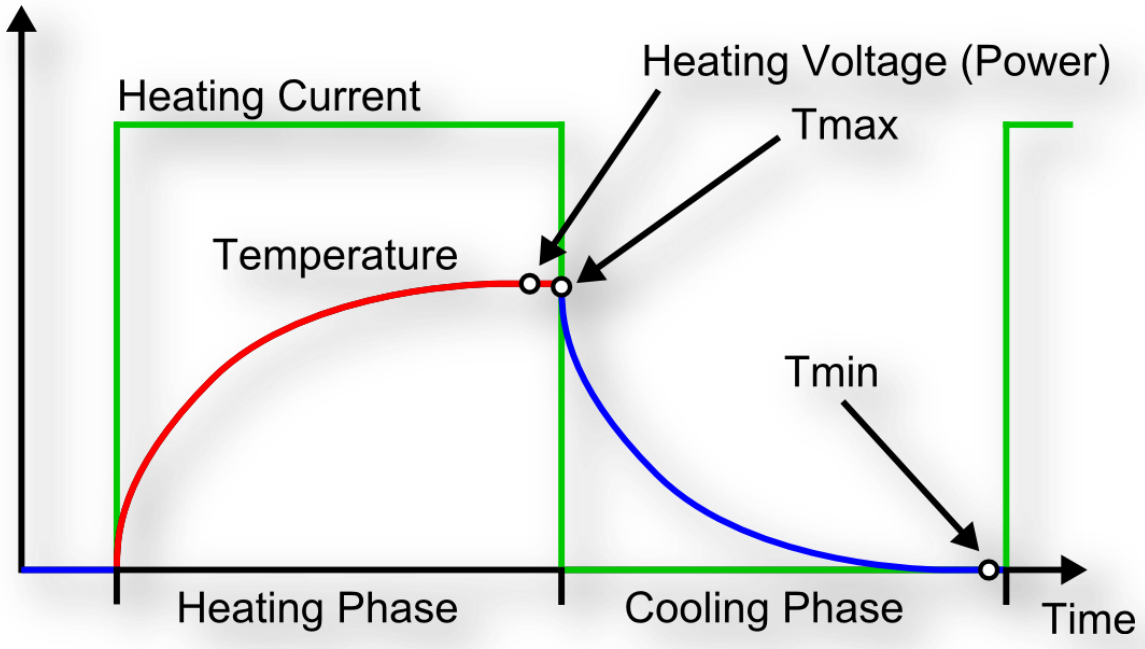
Power Cycling Test

Heating up and Cooling Down



Power Cycling: Heating and Cooling - Symmetric

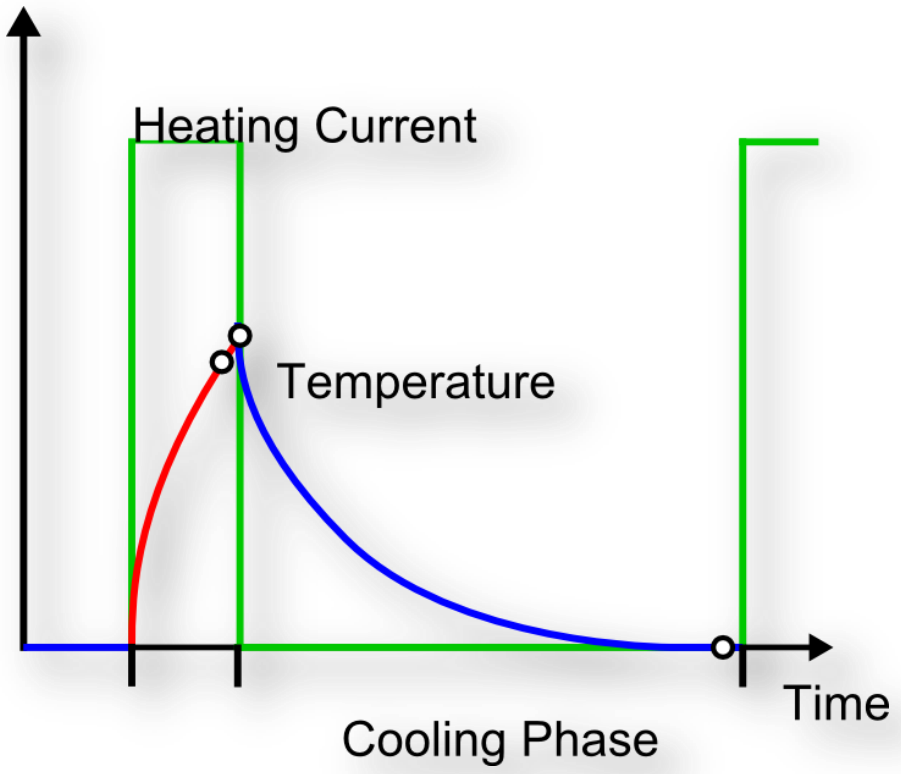
- Heating and cooling is symmetric ($t_{ON} = t_{OFF}$)
- Steady state condition at the end of the
  - heating phase and
  - cooling phase
- Easy measurement of heating power and temperatures
- T_{max} dependent on
  - $P_{Heating}$,
  - R_{th}
- T_{min} dependent on
  - $T_{Coolant}$ only



Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

Power Cycling: Heating and Cooling - Asymmetric



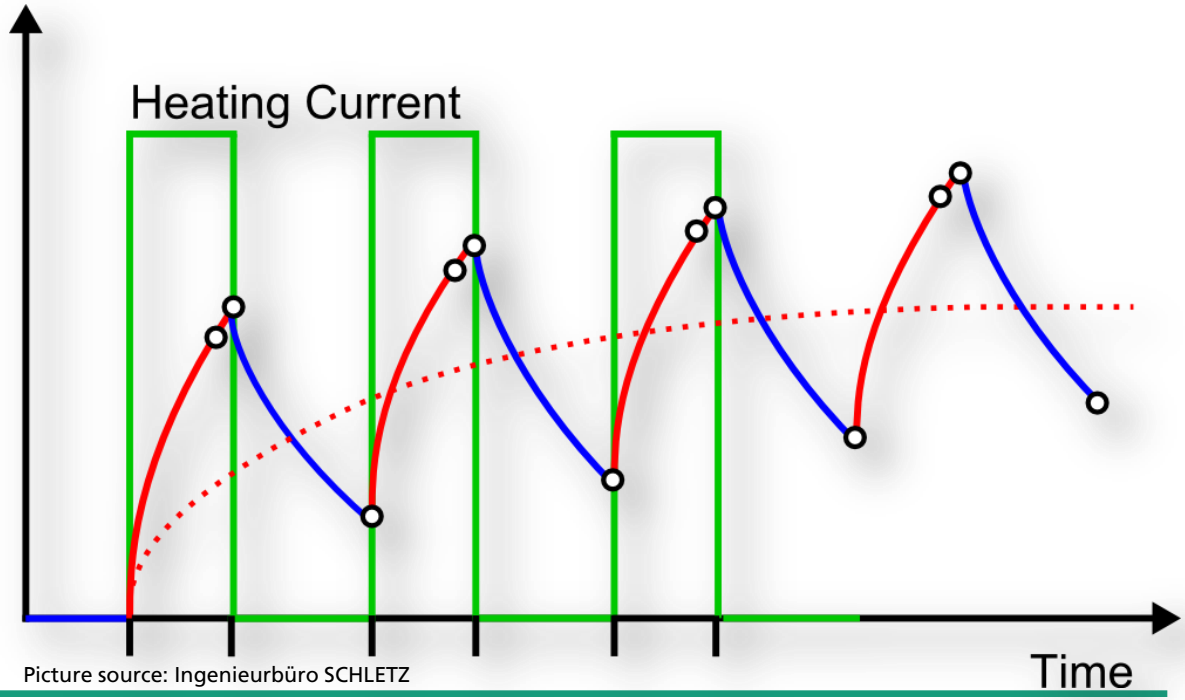
- Heating and cooling is asymmetric
- Short heating, long cooling
- No steady state condition at the end of the heating phase
- Heating power measurement is difficult
- Steady state condition at the end of the cooling phase
- T_{max} dependant on $P_{Heating}$, t_{ON}, R_{th}
- T_{min} dependant of $T_{Coolant}$ only

Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

Power Cycling: Heating and Cooling - Drifting

- No steady state conditions for the end of the heating nor cooling phase
- Heating and cooling is symmetric or asymmetric
- Heating power measurement is difficult
- Temperature measurement is difficult
- T_{max} dependant on $P_{Heating}$, t_{ON}, t_{OFF}, R_{th}
- T_{min} dependant of $T_{Coolant}$, t_{ON}, t_{OFF}, R_{th}
- Long term steady state conditions depending on R_{th}

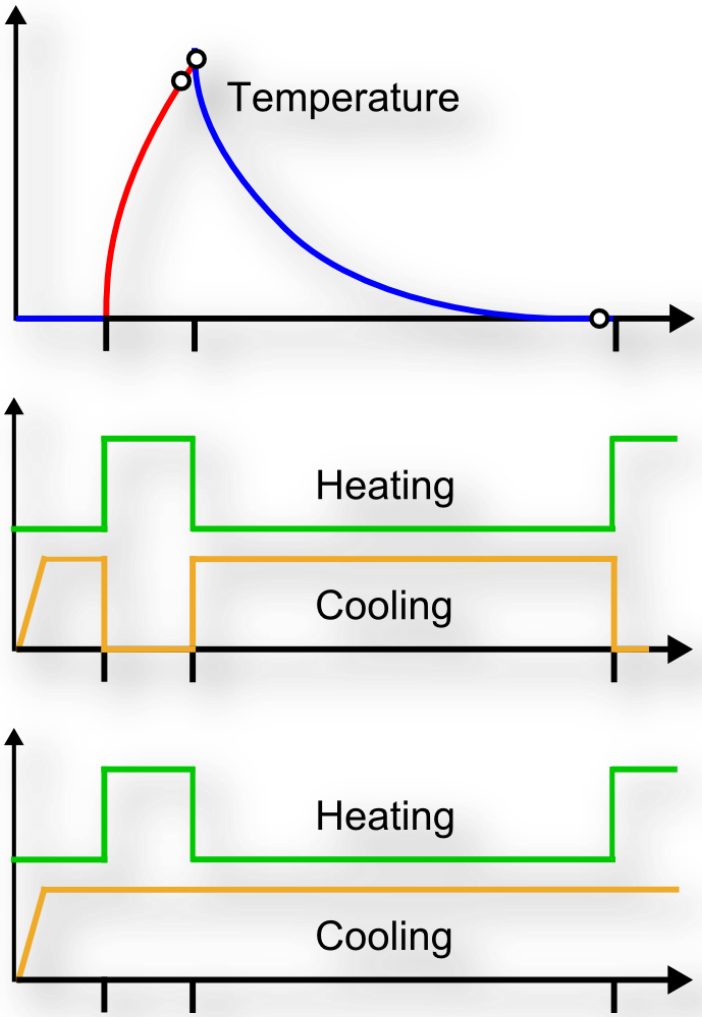


Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

Power Cycling: Cooling Concepts

- Interrupted cooling
  - Fast heating up
  - Less heating power
  - “No” temperature gradient from chip to coolant
- Constant Cooling
  - High heating power needed
  - Application near temperature gradient from chip to coolant



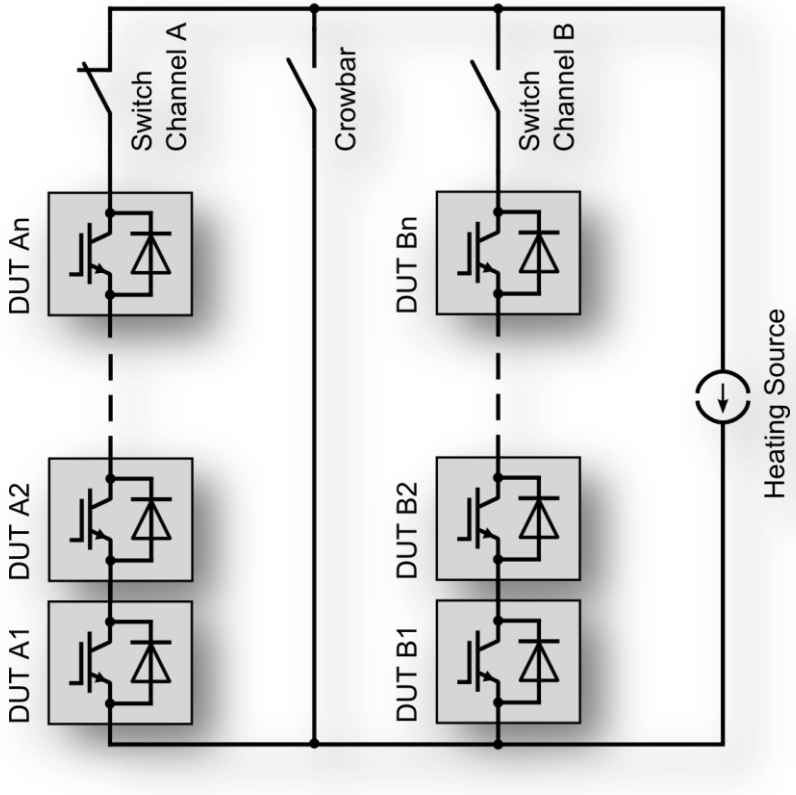
Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

PCT3 Power Cycling Test

Concept

- 2 Strings (Chanel A and B)
- Additional crowbar string
  - Unsymmetrical heating an cooling
  - Same condition for each string (Starting point of the heating phase)
- DUTs in series connection within one string
- DUTs are „passive“, switching on and off by „load switches“
- Alternating switching
  - Reduced cycling of the heating source
  - Reduced cycling of the tempering unit
- One acquisition input per DUT: synchronous data logging per cycle

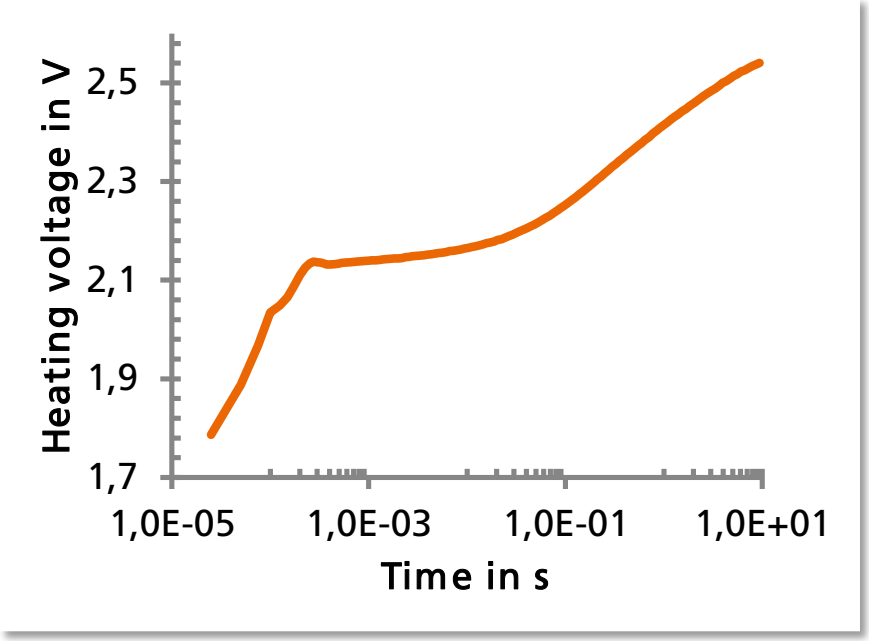


Fraunhofer IISB

Power Cycling: Test strategies

Used test strategies specifically for one specific temperature cycle

- Simple switching, no control of parameters
- Control of power at heating up
  - Speed up heating
  - Constant power
  - Prevent power surge



Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

Power Cycling: Test strategies for the Cycling

Most common used general test strategies:

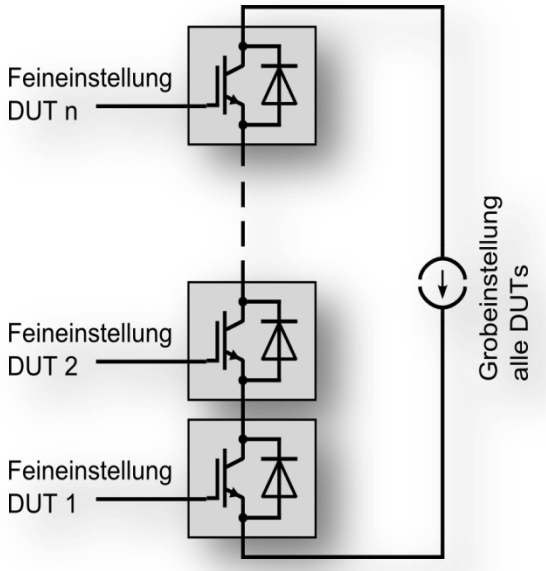
- Constant heating current
  Application near, e.g. motor torque ~ inverter current
- Constant ΔT
  Failure mechanisms related to ΔT will remain constant (Scientific test)
  No positive feedback on the number of cycles
  → High number of cycles to be achieved
- Constant heating time
- Constant heating power
- Constant baseplate temperature

➢ No test strategy reflects the reality 100% (it's a test only)

PCT: Test Run: Temperature Swing Adjustment

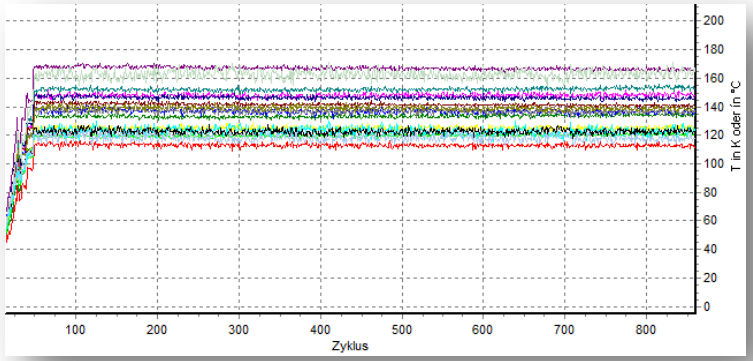
Goal:
Identical Temperature Swing for All DUTs

- Rough adjustment with heating current for all DUTs at the same time
- Fine tuning with gate voltage
- Fine tuning only possible with controllable devices (no diodes)



Different Test Methods

- Constant temperature swing (= constant failure mechanism)
- Constant heating current (= application near)

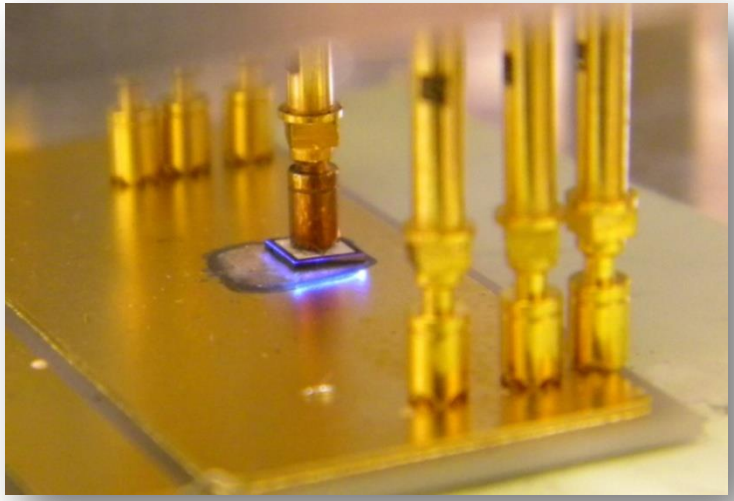


Fraunhofer IISB

PCT: Test Run: Power Cycling

Waiting for Test Stop Trigger

- Coolant temperature
- DUT temperature provided by external Pt100 sensor
- Voltage/ power during heating phase
- Calculated T_{min}, T_{max}, temperature swing
- (Gate leakage current)

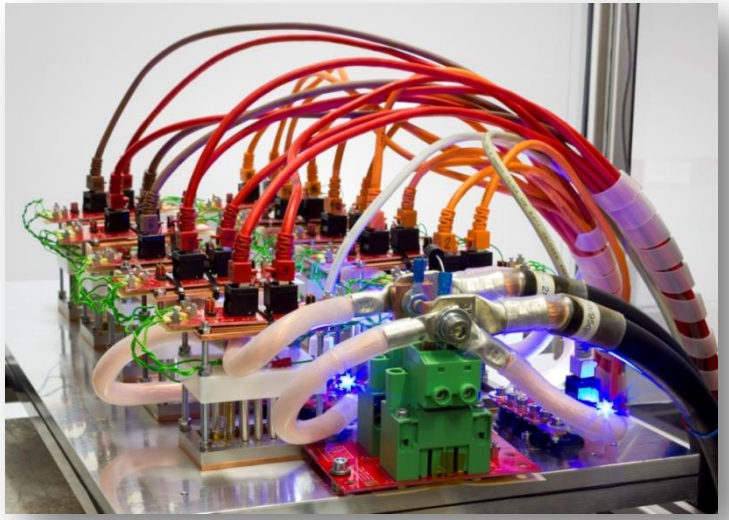


Picture source: Fraunhofer IISB

Fraunhofer IISB

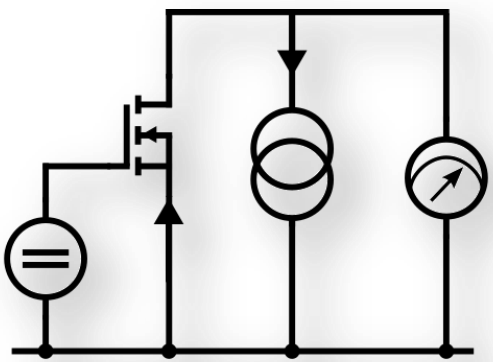
Contents

- Motivation
- Failure Mechanisms
- Heating and Cooling Concepts
- Test Strategies
- Acquisition of the Temperatures
- WBG challenges
- Lifetime
- Interpretation of the Test Result
- Summary

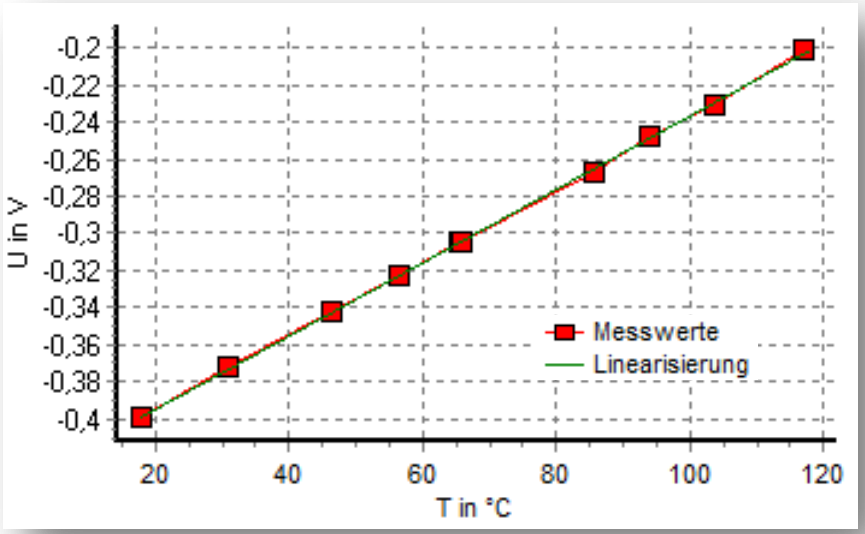


PCT: Test Run

Temperature-Voltage-Calibration



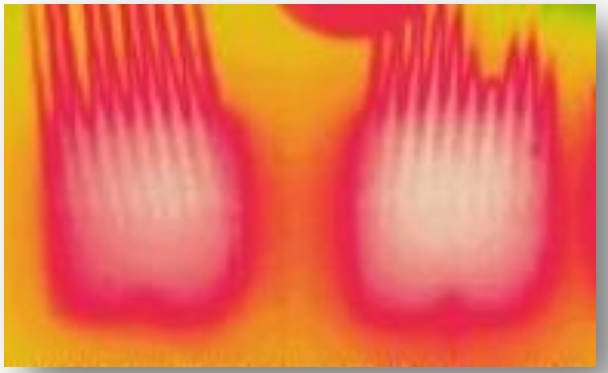
- Low measurement current applied (negligible self heating)
- Cold plate and DUTs are set to a defined temperature
- Waiting for static thermal condition
- Temperatures
  - Should be in the range of the power cycling test temperature cycles
  - WGB, especially SiC goes towards high temperatures (210°C is on the market@2017)
  - +20..+95°C very simple
  - <20°C → wetting, closed humidity free chamber needed
  - >95°C → absolute pressure in the coolant tubing or special tempering oil needed
  - >95°C → Oven: Special cabling and electrical contacts needed



Fraunhofer IISB

PCT: Acquisition of the Temperatures

- Challenge
  - Precise at high bandwidth
  - Temperature gradient over chip surface

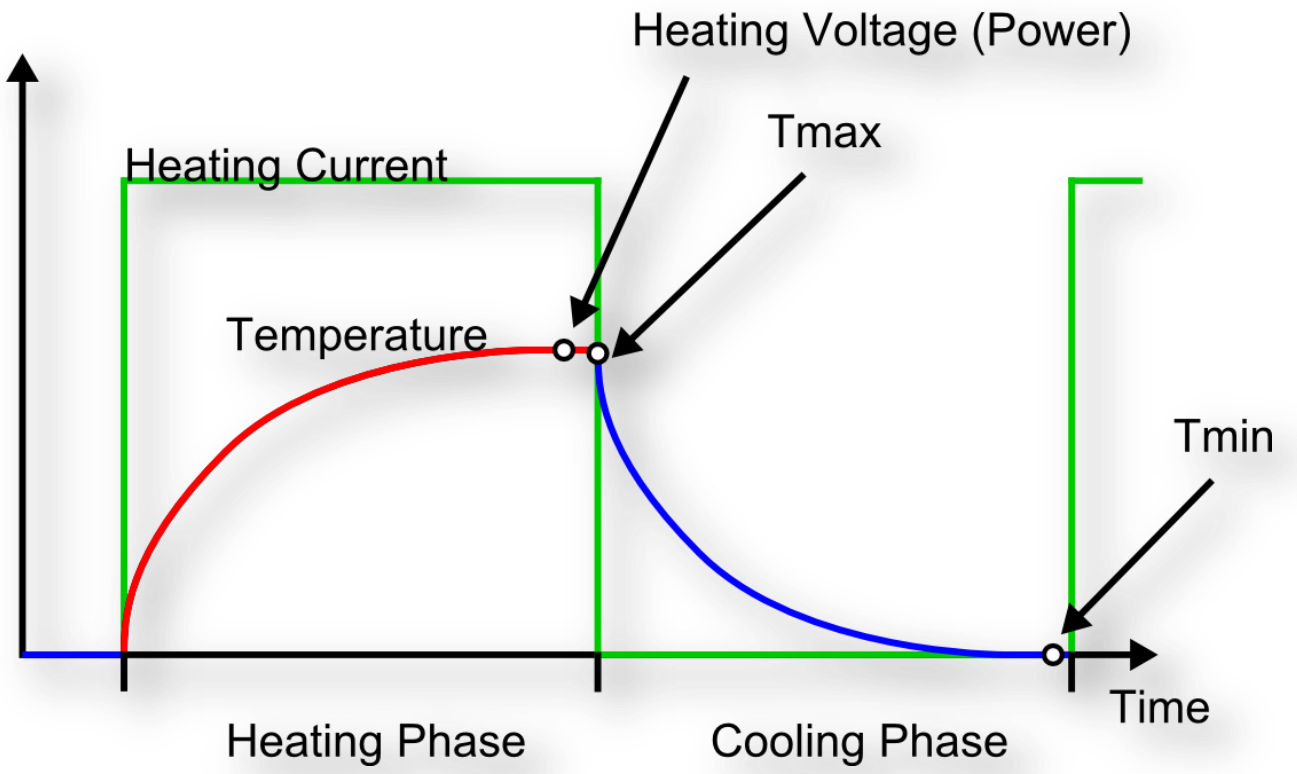


- WBG die size is small
- Exceptional thermal conductivity for SiC

→ Problem simplified

PCT: Temperature Measurement

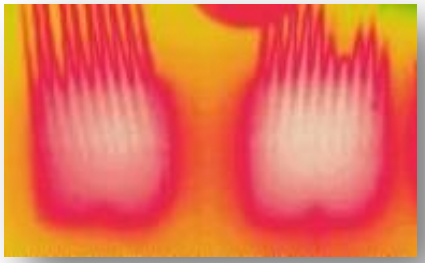
Determination of the temperatures/ heating voltage



PCT: Measurement of the Temperature

Without base plate
little heat spreading

With base plate
heat spreading



Picture source: Fraunhofer IISB

Thermography/ Pyrometer

- Advantage
  - Temperature distribution displayed
- Disadvantage
  - Direct view to the surfaces necessary
  - Metallic surfaces difficult to measure
  - Reflections and shading (e.g. bond wires) distort the result
  - Surfaces to be covered → defined emission coefficient
  - Emission coefficient probably dependent on the temperature
  - Acquisition of the absolute temperature is not trivial
  - High speed transient thermal measurements are linked to the resolution and availability (max. 1kHz@2014)
  - Requires great effort, practically possible for few DUTs only

Fraunhofer IISB

PCT: Measurement of the Temperature

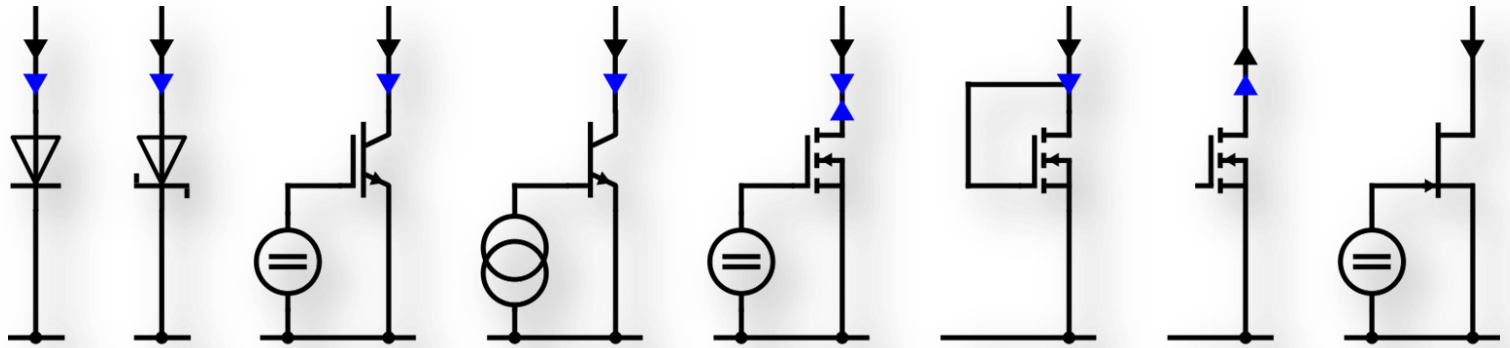
Indirect Temperature Acquisition Method

- Most mentioned in publications, widely used
- Use of temperature dependent semiconductor parameters
- Disadvantages
  - Measured temperature is an “Replacement”-Temperature (Link between current density and voltage)
  - → Extremely dependent on the device under test
  - Temperature gradient over chip surface reduced to one value
  - Overlaid electrical oscillations caused by parasitic external components
  - Overlaid distortions by the semiconductor device itself (Recombination, capacitances)
  - Linearity of the voltage-temperature-curve
- Advantages
  - Easy to use
  - Paralleling at relatively low cost
  - Transient electrical signal to measure at high bandwidth
- Temperature-Voltage-Calibration needed

PCT: Indirect Temperature Measurement

Possibilities and Setup

	Heating up	Measurement
Diode	Forward voltage	Forward voltage
MOSFET	Forward direction, lin. region	Forward voltage of the intrinsic diode
JFET norm. on, off	Forward direction, lin. region	Forward voltage of the intrinsic diode
BJT	Forward direction, lin. region	Forward voltage
IGBT	Forward direction	Forward voltage



…and now WBG shows its ugly face.

www.funnypica.com

WBG challenges…

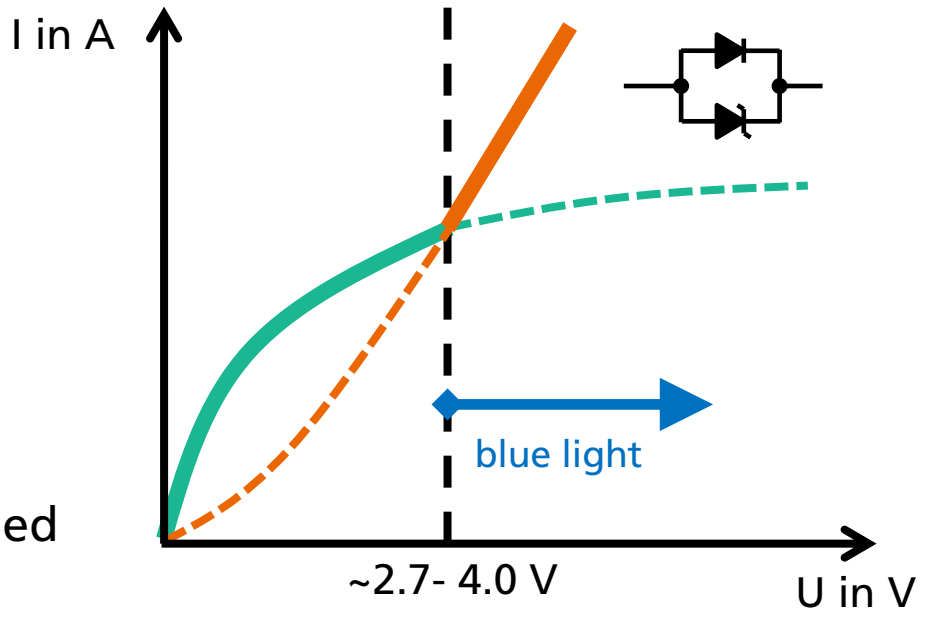
Test at Acceleration Limit

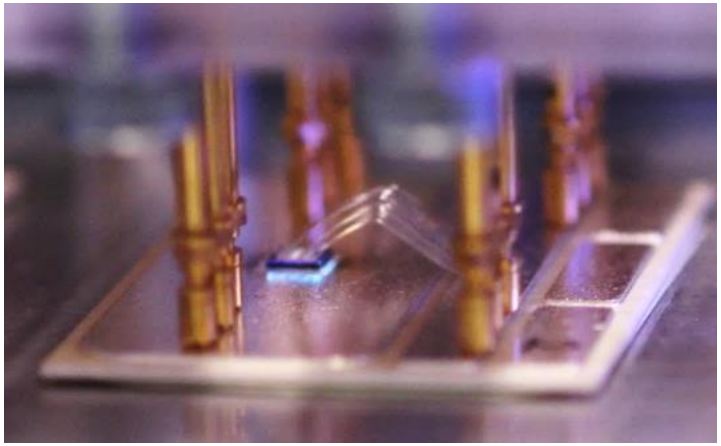
- Static Losses of FETs
  - Heating is done by DC current (state of the art)
  - $P = I^2 * R_{DS,ON}$
  - Extremely low $R_{DS,ON}$ limits the power losses
  - dT is hard to achieve by current only current; may be limited by package or semiconductor die
  - Gate voltage has to be reduced down to the limits (has to be well above threshold under all circumstances)
- Solution
  - Use body diode for heating
  - Use switching losses as additional heat source

www.leickel.de

Test at Acceleration Limit

- Electric performance of the semiconductor devices under test
- Example
  - Small device → excellent heat spreading → high power loss needed
  - High heating current needed
  - SiC schottky used
  - Device operating the merged pn structure (overcurrent protection)
  - Exceeding datasheet values …

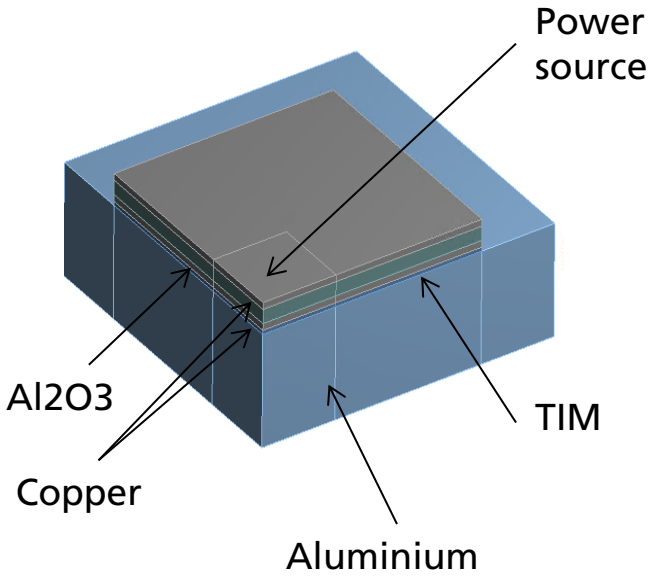


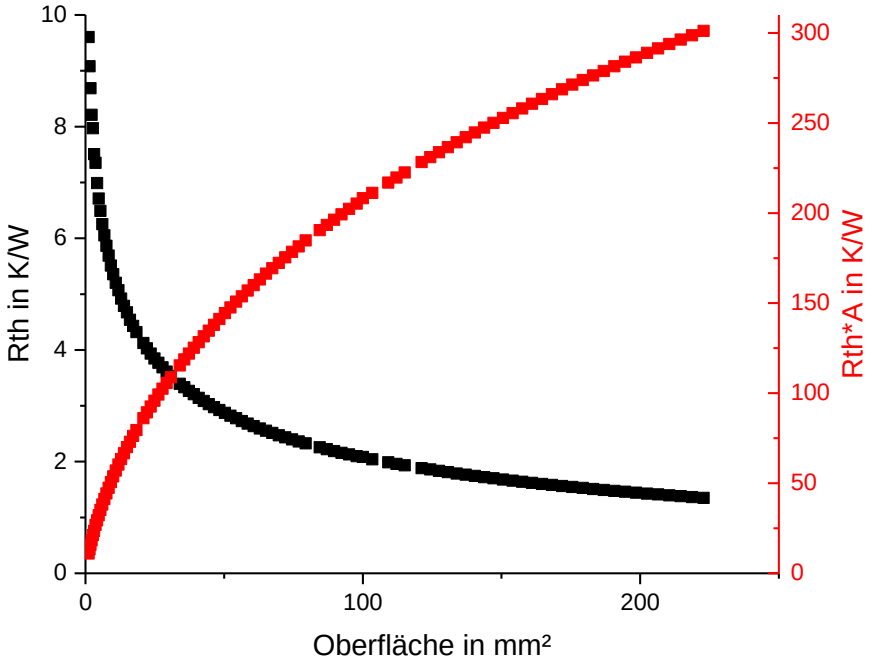


A.Hutzler et.al., Increasing the lifetime of electronic packaging by higher temperatures: solders vs. silver sintering, 64th Electronic Components and Technology Conference, ECTC 2014 : 27-30 May 2014, Orlando, Florida, USA

Test at Acceleration Limit

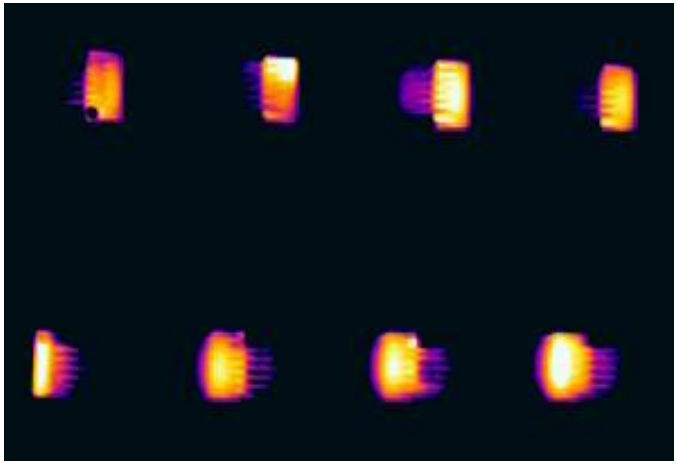
- Small device → excellent heat spreading

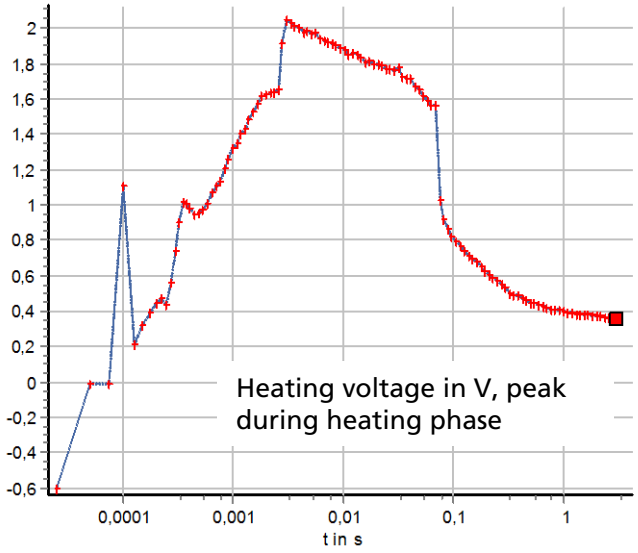




Test at Acceleration Limit

- For FETs: Use low gate voltage
  - Higher forward voltage, lower current, higher losses → higher temperature swing
- Drawback
  - Negative temperature coefficient of threshold voltage
  - Different heating of semiconductors according to they local electrical and thermal performance
  - No application relevant situation
  - Virtual temperature measurement becomes free to interpret
  - Inhomogeneous temperature distribution over chip surface
  - Overheating in the first 100ms (work around: soft start with higher gate voltage at the beginning)

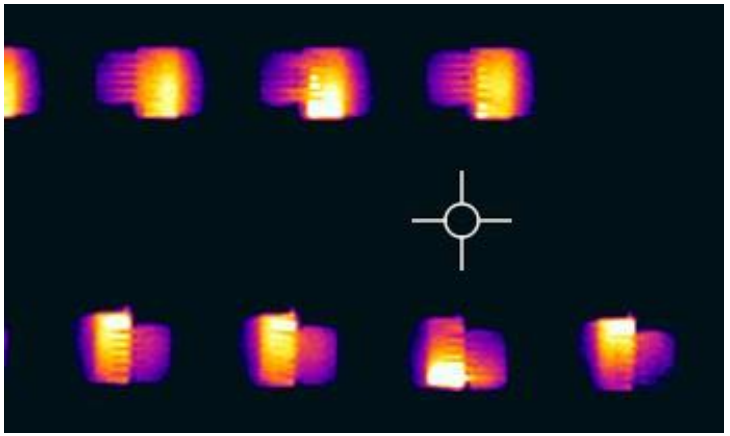


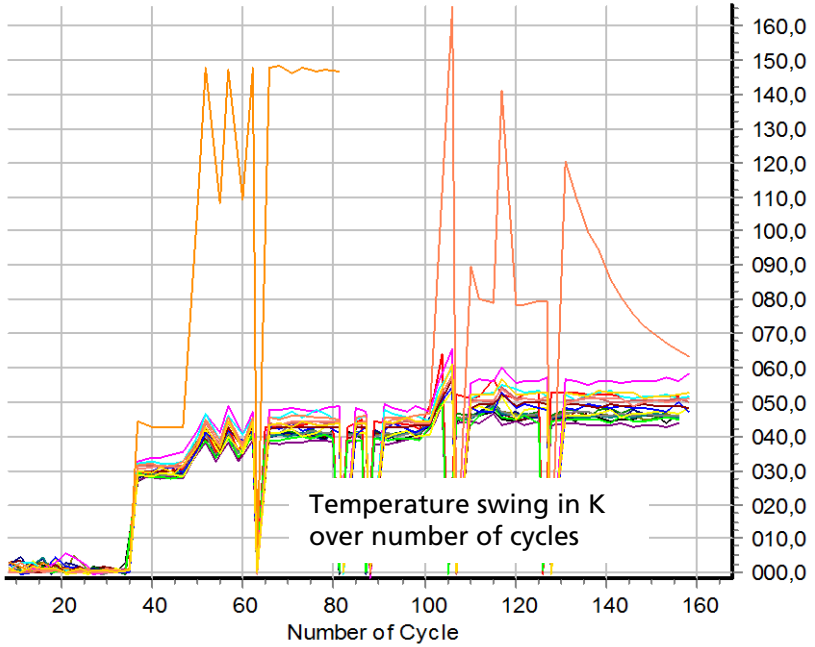


Fraunhofer IISB

Test at Acceleration Limit

- For FETs: Use body diode for heating
  - Higher forward voltage, lower current, higher losses → higher temperature swing
- Drawback
  - Negative temperature coefficient
  - Different heating of semiconductors according to they local electrical and thermal performance
  - No application relevant situation
  - Virtual temperature measurement becomes free to interpret
  - No control – no fine tuning
  - Inhomogeneous temperature distribution over chip surface



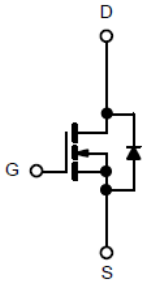


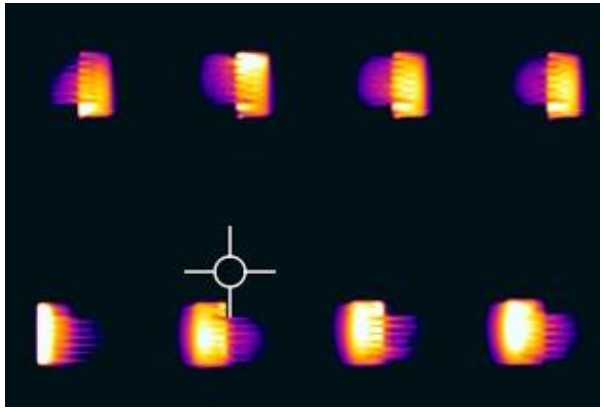
Funded by FuE-Program "*Elektronische Systeme*"
Freistaates Bayern/ Germany; Input taken from
Fabian Dresel/ Fraunhofer IISB

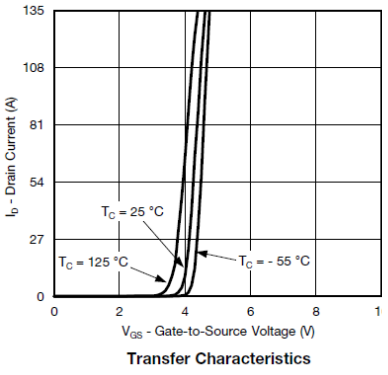
Fraunhofer IISB

Test at Acceleration Limit

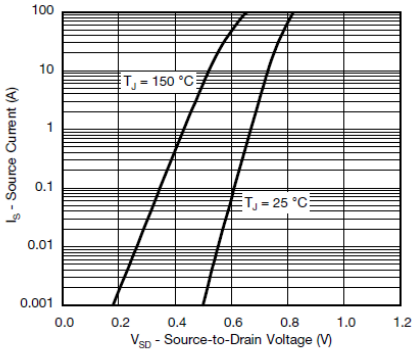
- Work around #1 (for FETs only):
- Use body diode for heating and slightly open FET channel at the same time
  - During the heating up: application of a positive gate voltage near the threshold
  - Temperature difference between chip is much better
  - More homogeneous temperature distribution on chip
- Operating principle
  - PN diode is in parallel to the FET
  - FET's threshold decreases with increasing temperature → channel opens at hot regions, cutting down temperature self-controlled
  - But: 2. theoretical possibility: dominant heating current flows through FET channel intensifying the hot spot
  - Behavior dependent on electro-/ thermal performance of the semiconductor







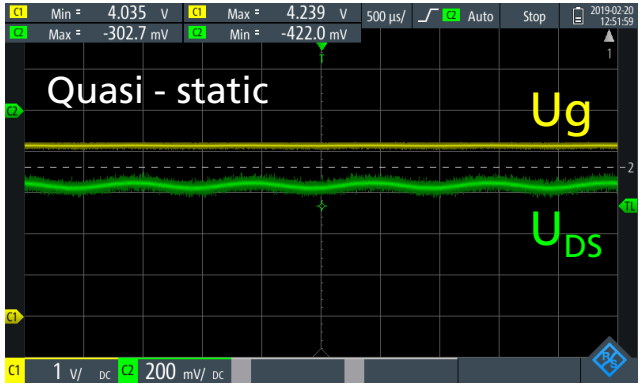
Transfer Characteristics

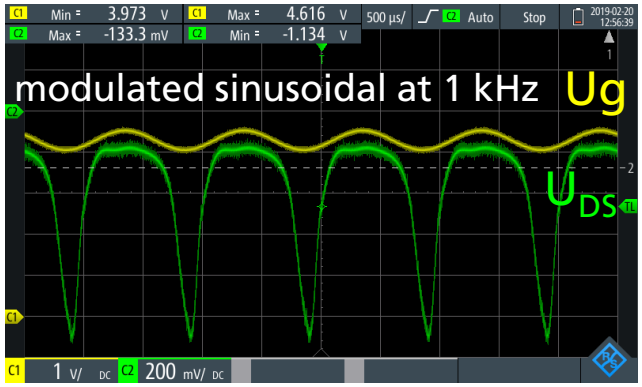


Source-Drain Diode Forward Voltage

Test at Acceleration Limit

- Work around #2 (for FETs only):
- Operating principle
  - Heating in forward direction
  - gate voltage with AC (any waveform) plus DC offset
  - Heating power is equivalent to the area below U_{DS} curve
  - Very stable operating point
  - No inhomogeneous chip temperature
- Drawback: Up to no commercial available test equipment





FET's Leakage Current Dependent on Gate Voltage

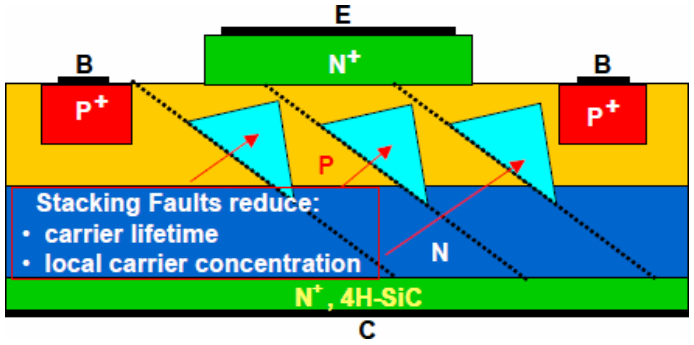
- Leakage current
  - Caused by not completely closed FET's channel
  - = body diode performance
  - = temperature sensor performance
  - Dependent on gate voltage level during cooling down
  - Gate voltage level may exceed datasheet values
- Solution
  - (High) negative gate voltage during indirect temperature measurement

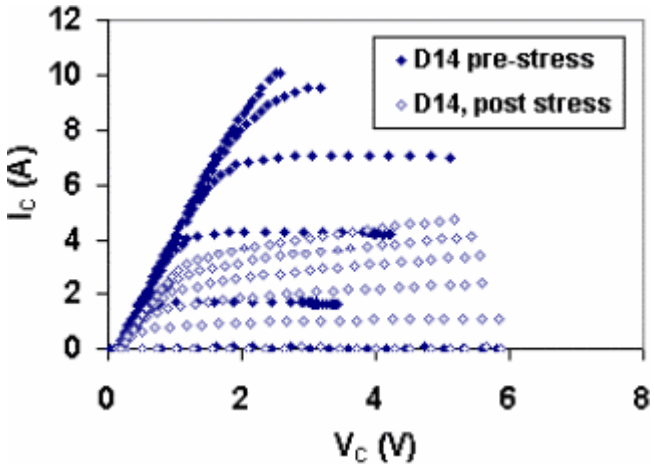
Drift of FET's Gate Threshold Voltage

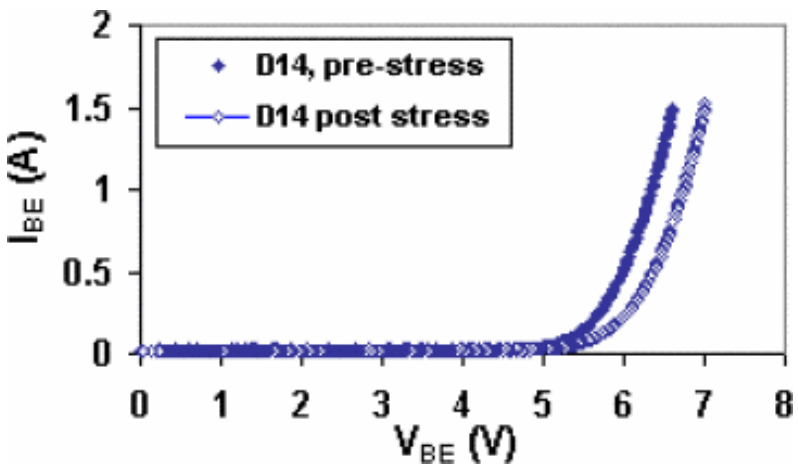
- Drift of gate threshold voltage
  - Heating power @ static gate voltage changes due to the effect
  - Dependent on test parameters
    - t_{on} t_{off} ratio
    - Temperature
    - Voltage levels for heating and cooling
    - Maybe pos./ neg. gate voltage impact different
    - Reversible, particular during test system shut down (undefined down time)
- Solution
  - Identify drift and re-adjust gate voltage during test
  - Develop new end of life failure criterion

SiC Bipolar Degradation

- SiC MOSFETs have **bipolar** body diodes
- SiC bipolar devices suffer from material defects
- Failure cause: Current and temperature





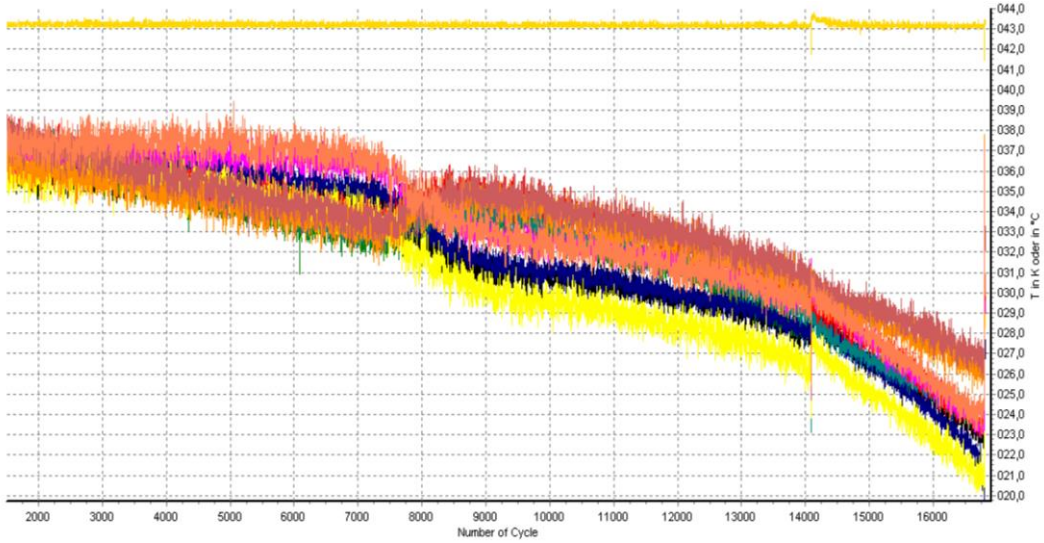


Qingchun (Jon) Zhang et.al.: Degradation Mechanisms in SiC Bipolar Junction Transistors

Fraunhofer IISB

SiC Bipolar Semiconductor Parameter Drift

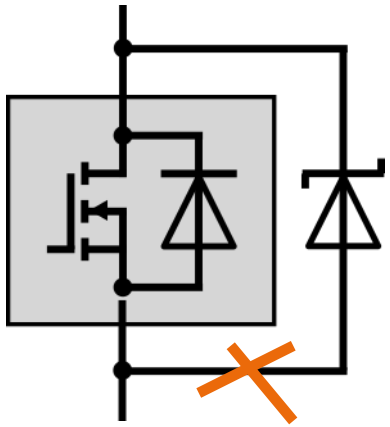
- SiC body diode my suffer from degradation (some manufacturers use a pre-scanning of wafers to sort out infected areas)
- Problem
  - Temperature sensor is drifting away
  - Poor results by indirect temperature measurement
- Solution
  - Recalculate temperature by voltage offset (error prone)
  - Recalibration of sensor voltage
  - Develop new end of life failure criterion
  - Just wait (seems to be a solved issue because of improved wafer quality)



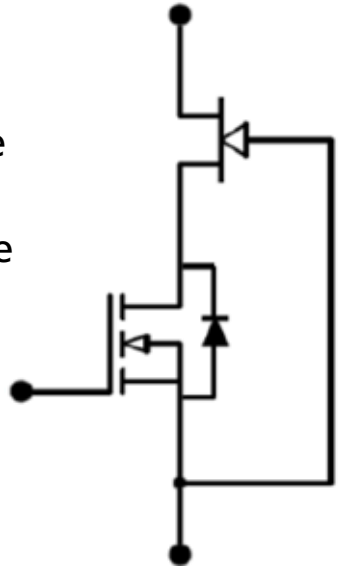
Fraunhofer IISB

SiC Power Module Configuration

- SiC body diode suffers from degradation/ high voltage drop
- Application needs unipolar (schottky) freewheeling diode for commutation (in addition to synchronous rectification)
- Problem:
  - Schottky diode has lower forward voltage drop compared to bipolar body diode
  - Heating in forward direction possible only no reverse heating
  - Indirect temperature measurement not possible for MOSFET
- Solution
  - Special module configuration without antiparallel diode

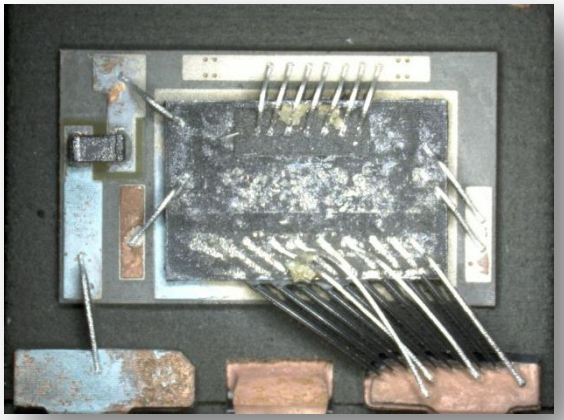


Cascode Configuration SiC and GaN

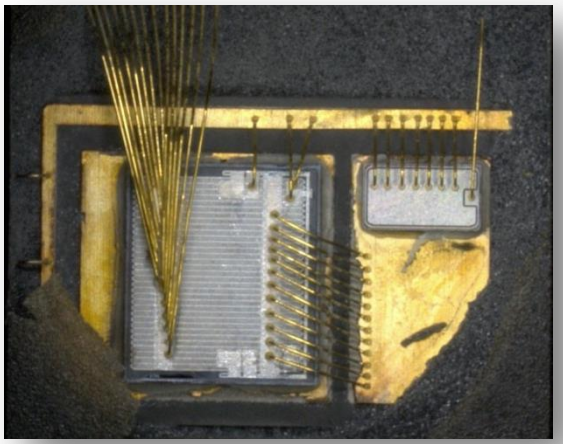


- No access to the internal node
- Problem: Testing of both devices separately not possible
- Cascode is reverse conductive
  - 1. path:
    SiC JFET gate pn junction
    approx. 3V forward drop
  - 2. path:
    Si MOSFET body pn diode approx. 0.7V
    forward voltage drop plus negligible
    JFET on resistance voltage drop
  - → Si MOSFET is the temperature sensor
  - Package 1: could work
  - Package 2: Information on the inexpensive Si chip only which might be over engineered
- Solution: Periodically investigation (SAM, sections) during the test runs

Package 1

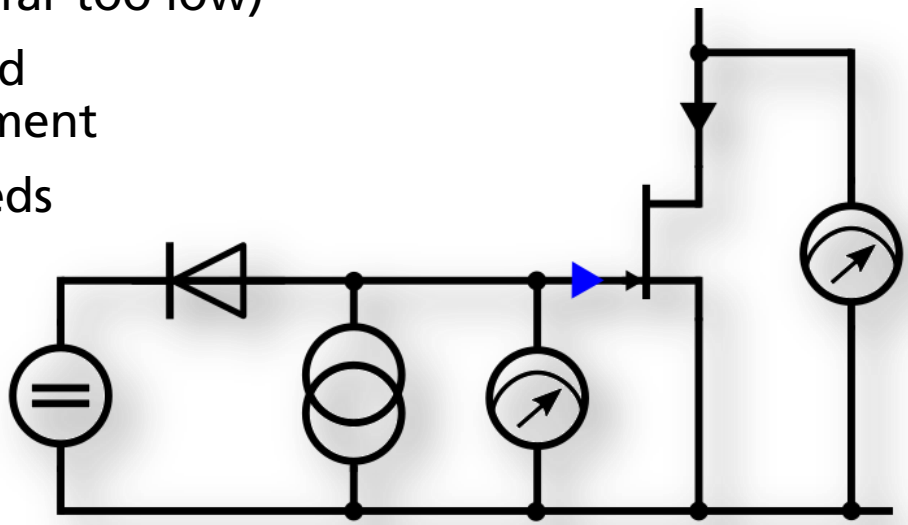


Package 2



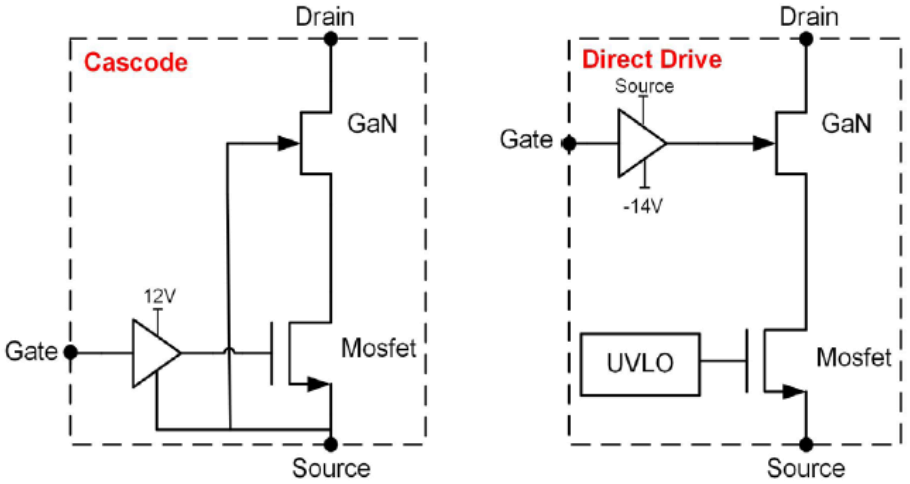
GaN HEMT

- No body diode, no sensor
  (forward voltage drop of HEMT is far too low)
- pn junction at the gate can be used
  for indirect temperature measurement
- Complex circuitry to fulfill PCT needs
  - Heating phase:
    Gate voltage provided by
    measurement current source;
    Fine tuning of temperature
    swing at the by voltage source
  - Heating phase:
    Heating voltage measurement
    by additional acquisition channel
- Problem: pn junction may drift (refer to SiC bipolar degradation)



Integrated Packages

- Problem
  - No access to internal nodes
  - No possibility for indirect temperature measurement
  - No possiblitiy for fine tuning by gate voltage
- Solution
  - Heating voltage measurement is still possible
  - $R_{DS,ON}$ indirect temperature measurement
  - External temperature sensor
  - Wait for better devices which have diode like reverse characteristic (like GaNSystems e-Mode)



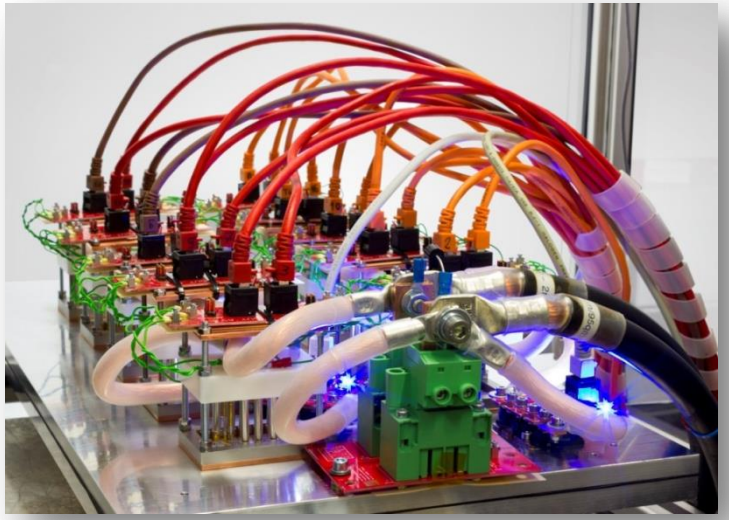
Paul L. Brohlin et.al.: The benefits of direct drive for GaN devices are achieving higher switching power efficiencies and better system level reliability due to the integration of device protections, Texas Instruments
Texas Instruments LMG3410 Datasheet

WBG Challenges Summary

- Big variety of challenges
- The test acceleration limit is a general problem for WBG
- Some module concepts need special setups for the testing
- The drift of the semiconductor parameters cause poor accuracy of the indirect temperature measurement
  - Solutions are available → Hints for the conduction of tests appreciated
  - The aging of semiconductors is an additional test result which is gained free of charge!
    → why not use it and define new EOL criteria

Contents

- Motivation
- Failure Mechanisms
- Heating and Cooling Concepts
- Test Strategies
- Acquisition of the Temperatures
- WBG challenges
- Lifetime
- Interpretation of the Test Result
- Summary



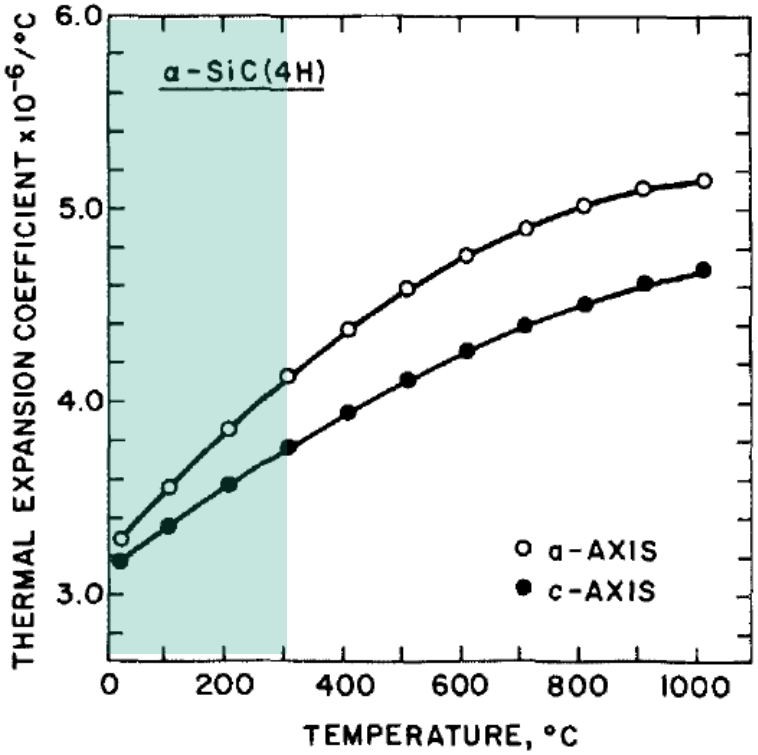
Power Cycling Lifetime - SiC

	Si @ 20°C	SiC-4H 20°C	Lifetime compared to Si
Thermal conductivity in W/(m*K)	150	380	☹ Chip have higher temperature due to better heat spreading[1]
Specific heat capacity in J/kg*K	700	690	😐 Not a big difference
CTE in ppm/K	3	4,3	☺ Better „matching“ to packaging materials
Youngs Modulus in GPa	162	507/547/ 159/108 (anisotropic)	☹ Increased stress
Die thickness in µm for 650V	40...120	180…325 +/-40µm	☹ Increased stress ☹ Wider distribution
Normalized die size in mΩcm² @ 25°C	142mm²*11mΩ = 15,6 [3]	26mm²*25mΩ = 6,5 [2]	☺ or ☹ 2,4x smaller die size
Normalized die size in mΩcm² @ 150°C	142mm²*14mΩ = 19,9 [3]	26mm²*25mΩ = 11,1 [2]	☺ or ☹ 1,8x smaller die size

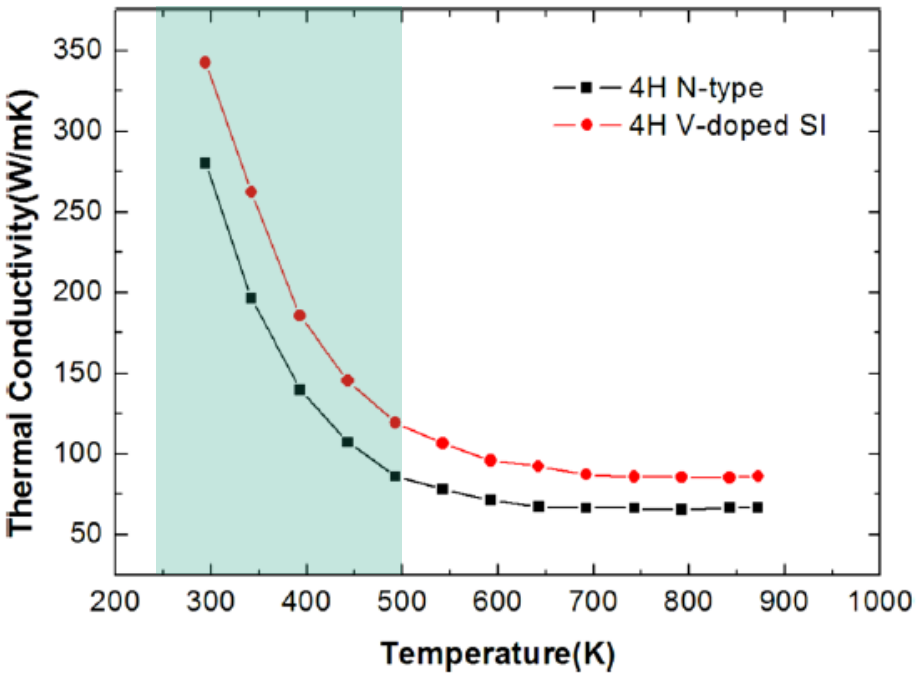
[1] Ch. Herold et.al.: Power cycling capability of Modules with SiC-Diodes, CIPS 2014, February, 25 – 27, 2014, Nuremberg/Germany
[2] Wolfspeed CPM2-1200-0025B
[3] Infineon IGC142T120T8RH

Alpha-4H SiC Material Parameters

All (!) material parameters are heavily dependent on temperature



Z. Li and R. C. Bradt: Thermal expansion of the hexagonal (4H) polytype of SiC, Journal of Applied Physics 60, 612 (1986); doi: 10.1063/1.337456



Rusheng Wie et.al.: Thermal conductivity of 4H-SiC single crystals, Journal of Applied Physics 113, 053503 (2013); doi: 10.1063/1.4790134

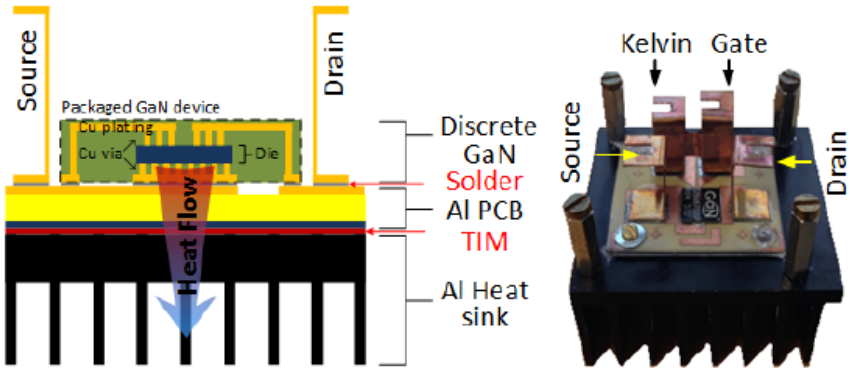
Power Cycling Lifetime - SiC

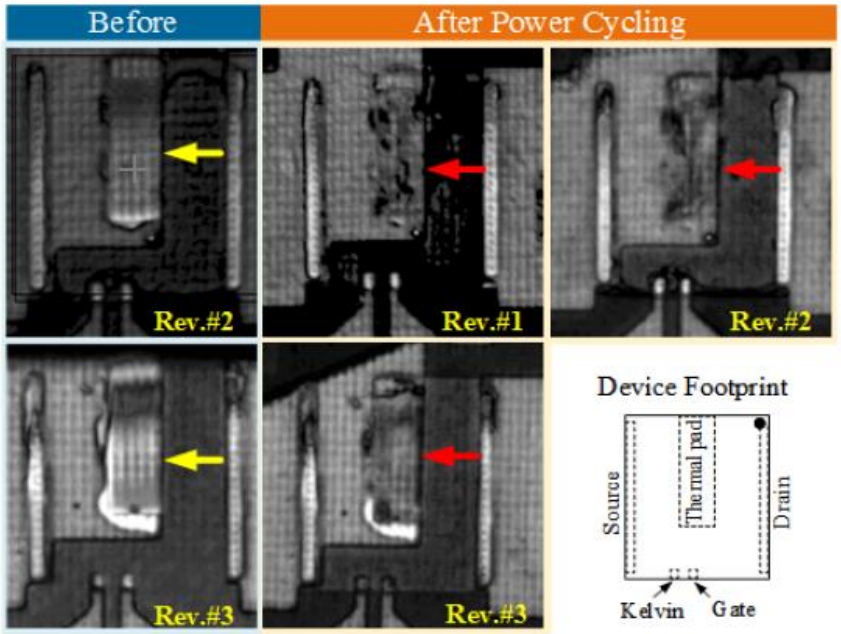
- Lifetime of SiC is about 30%..40%[1] than of Si (Sn solder, Al bond wires)
- Application
  - Temperature swing has to be lower in order to fulfill lifetime requirements
  - Bigger chip size is needed
- Outlook to the future
  - $R_{DS,ON}$ reduction will go on
  - Improvement is based on technology improvements and back grinding of SiC-Wafers
  - Dies will be less thick
  - At the same time the current density will increase → smaller die

[1] Ch. Herold et.al.: Power cycling capability of Modules with SiC-Diodes, CIPS 2014, February, 25 – 27, 2014, Nuremberg/Germany

Power Cycling Lifetime

- GaN
  - Very limited data available
  - Song et.al.
    - 3x GaNSystems device tested
    - 74k (dT)
    - 160k (I_{GS})
    - 214kcycles (I_{GS})
    - Parameter set
      t_{on}=1s, t_{off}=2s,
      I=6,5A, dT=100K, T_{min}=40°C



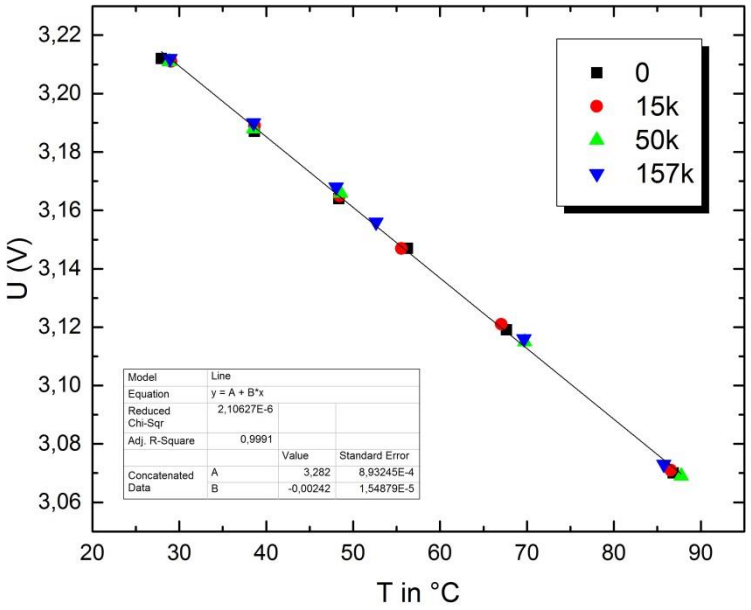


S. Song et.al.:"Failure mechanism analysis of a discrete 650V enhancement mode GaN-on-Si power device with reverse conduction accelerated power cycling test," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 756-760.

Fraunhofer IISB

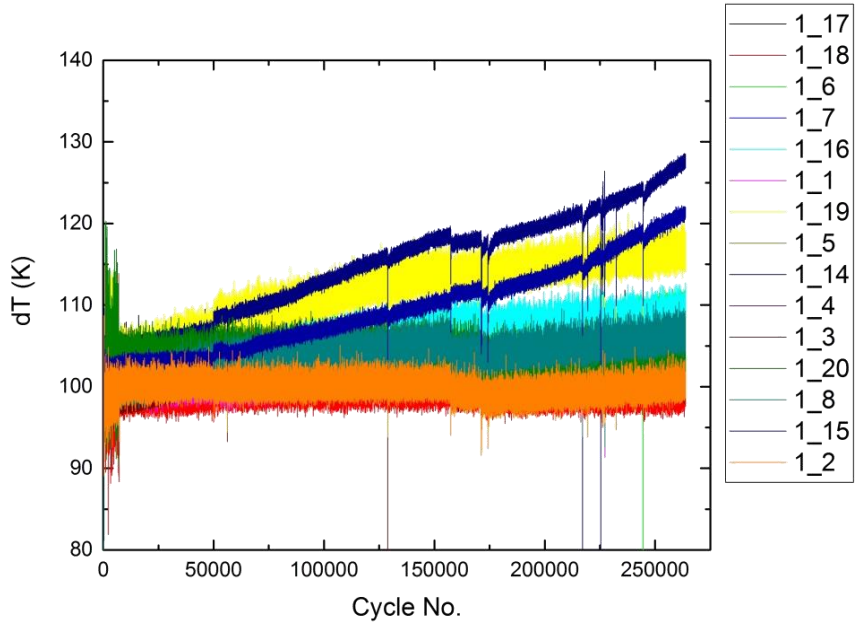
Power Cycling Lifetime, Own Measurements

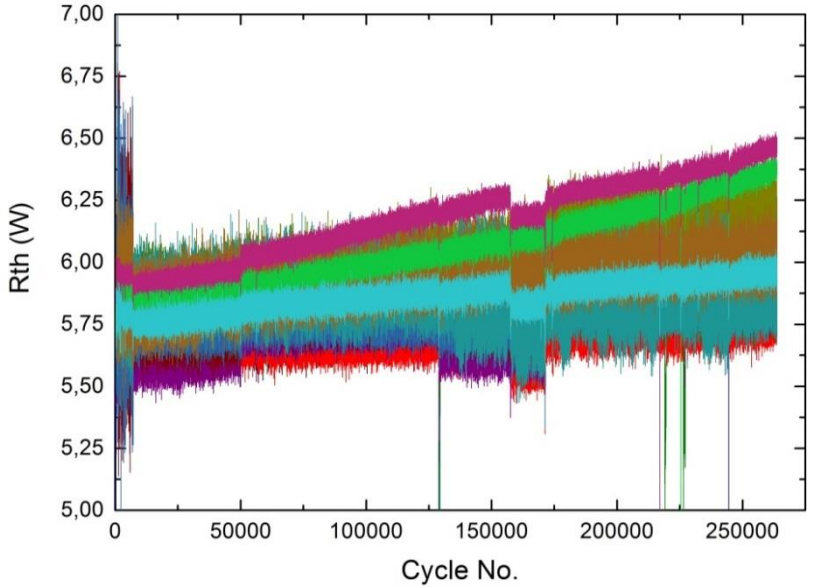
- HELENE project (public funded German BMBF)
  - Panasonic PGA26E07BA
  - Indirect temperature measurement: Gate-Source
  - No drift of calibration over 150k cycles!



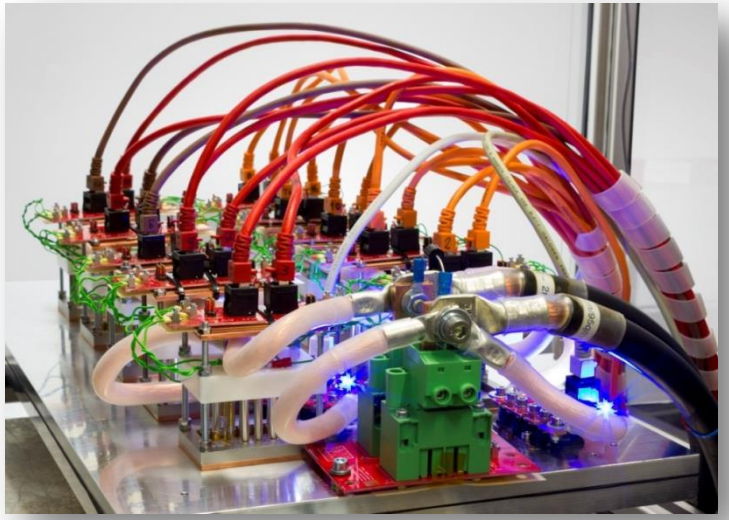
Active Power Cycling, Own Measurements

- 16 (!) samples
- dT = approx. 100K
- Test ongoing, current cycle number: 300.000
- 2 samples failed
- → first positive test results





Contents



Fraunhofer IISB

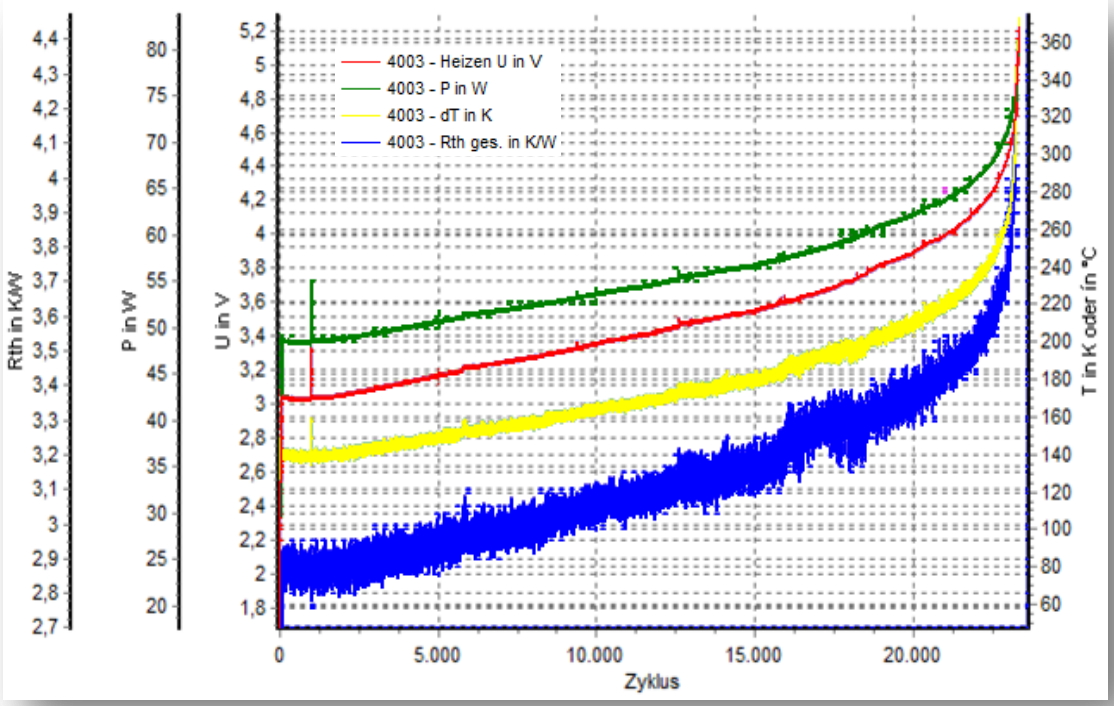
Result of the Power Cycling Test

- Needed:
  Performance of the power module vs. material cost
  (at a certain lifetime)
- Test-Result:
  Link between ΔT, T_{min} and the number of cycles
- ➢ Temperature is a technical figure only
  (Temperature dependence of electrical parameters neglected)
- Lifetime is modelled based on temperature parameters
- Lifetime is very sensitive to absolute temperature values
- Application is designed based on the thermal resistance or impedance
- ➢ Determination of R_{th} and lifetime with the identical equipment advisable
- ➢ Precise temperature measurement needed

PCT: Interpretation of the Test Results

Change of the **Thermal** Resistance

- As a result of the solder/ sintering/ glue bond line degradation, insulating substrate
- Increase of the temperature swing
- Leeds to a change of the voltage during the heating phase dependent on the temperature coefficient
- Increasing calculated thermal resistance (Junction to Coolant)



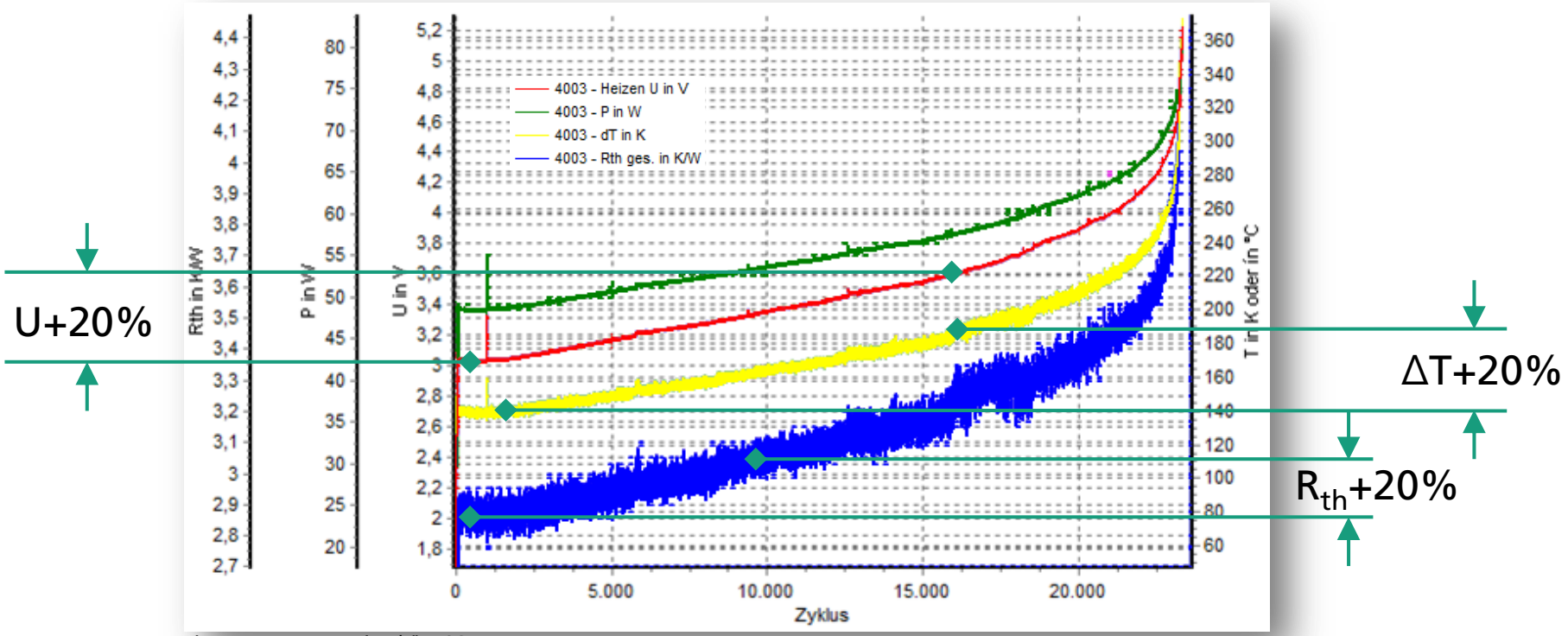
Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

PCT: Interpretation of the Test Results

End-of-Life - Criteria

- Increase of ΔT by 5, 10, 20%
- Increase of the voltage during heating phase by 5, 10, 20%



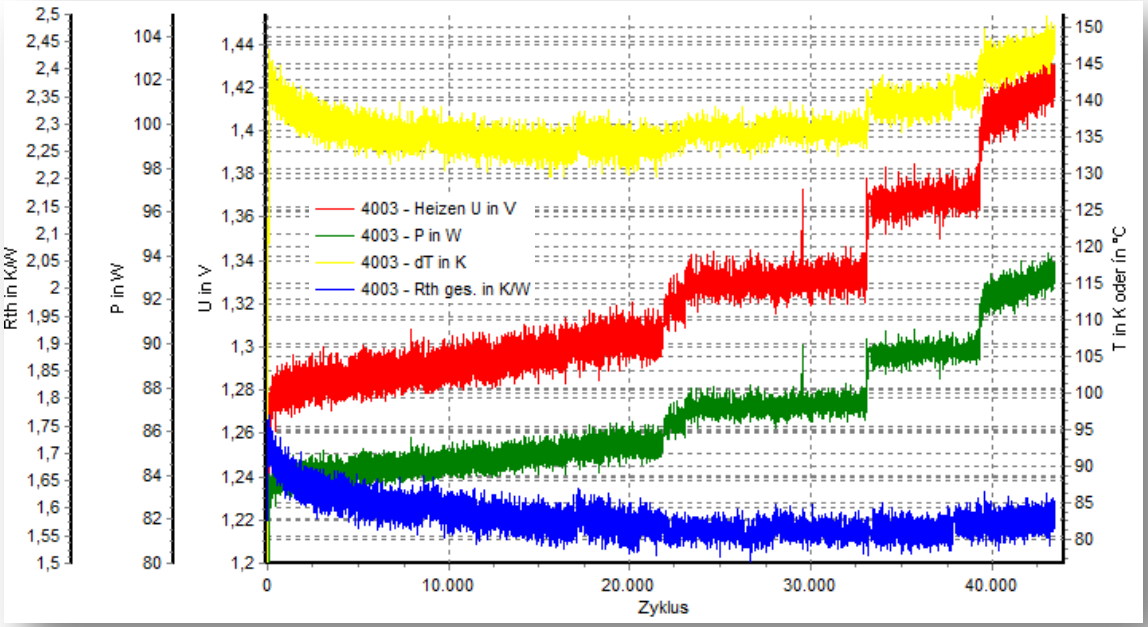
Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

PCT: Interpretation of the Test Results

Change of the **Electrical** Resistance

- As a result of
  e.g. bond wire, chip metallization,
  as well as substrate metal, drift of the semiconductor parameters
- Increase of the heating power and voltage during the heating phase
- Leads to increase of the temperature swing
- Thermal resistance remains unchanged (Junction to Coolant)



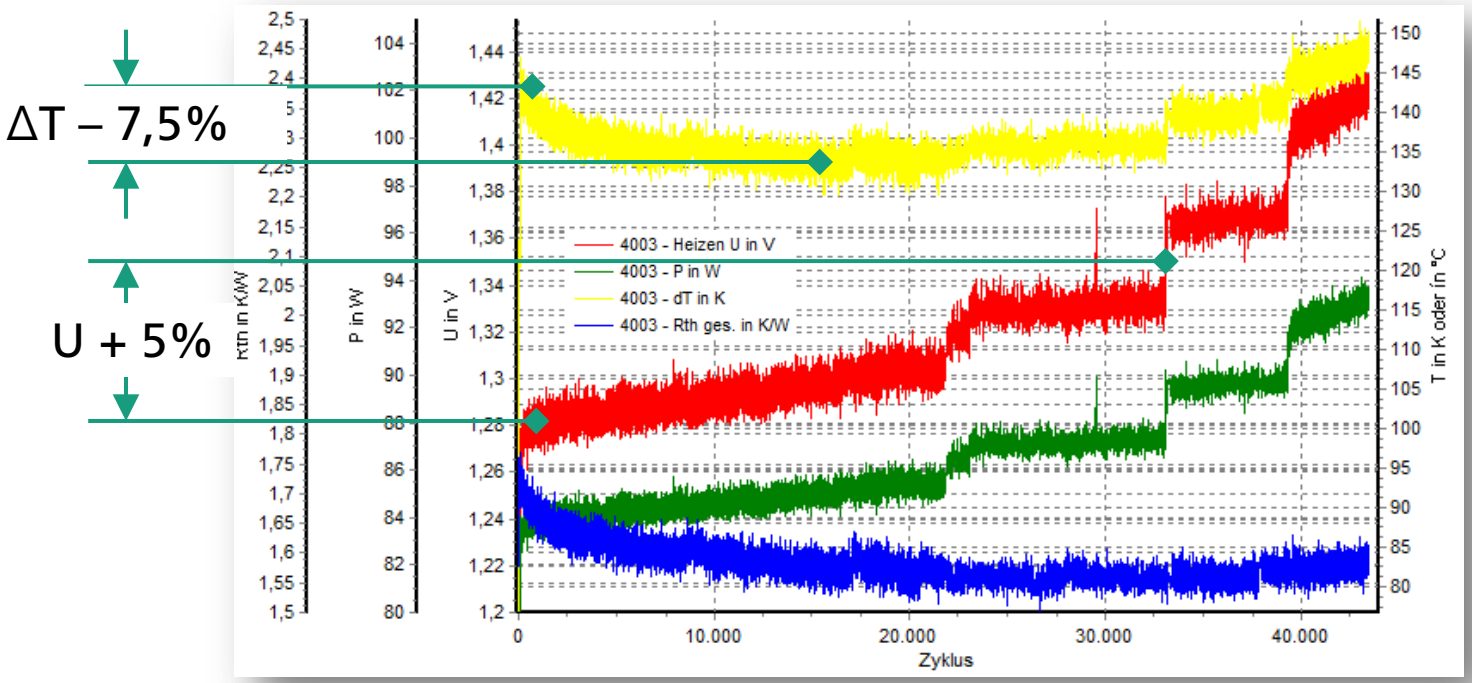
Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

PCT: Interpretation of the Test Results

End-of-Life - Criteria

- Increase of ΔT by 5, 10 or 20%
- Increase of the voltage during the heating phase by 5, 10 or 20%



Picture source: Ingenieurbüro SCHLETZ

Fraunhofer IISB

Standards

- MIL-STD 750-1 (USA Military)
  - Angaben in Auswertung: Tamb; Rth; Vf; If; Ncyc; Ton; EOL-Kriterium
  - Aktives Heizen über Chipverluste, Kühlung mit Gebläse nur während T_{off}
  - Zu Messen: Tj
  - Δ Tj > 100K; Tj,max < maximum rated; ΔTc > 85K
- IEC 607419-34 (international)
  - Angaben in Auswertung: dTc; Tvj, tcyc; dTvj; If; Ncyc; Montagebedingung; Stromform (=Applikation); Stichprobenumfang
  - Aktives Heizen über Chipverluste, Kühlung mit nat. Konvektion oder Gebläse oder Wasserkühler
  - Zu Messen: Tj ; Ts oder Tc unter einem DUT
  - dTj = 60…95K ; Tj,min =45°C; dTc = 30…60K
  - Tcyc = 1…15s (Bondalterung) / 1…15min (Lotalterung)
  - Strategie: const Zeit, const dTc; const dTs

Standards

- JEDEC JESD22-A122 (USA)
  - Angaben in Auswertung: Montagebedingung; Heizart; Temperaturextrema; Zyklen pro Stunde; Beispielzyklus (Temperaturen); Temperaturmessstellen; EOL-Kriterium
  - Aktives Heizen über Chipverluste oder Heizdraht / Heizelement
  - Kühlung mit nat. Konvektion oder Gebläse oder Wasserkühler oder Kühlelement (Peltier, Heat pipes..)
  - Spannungen, Temperaturprofile, Heizspannung, Ausgewählte Temperaturen
  - Δ Tj = 60…115K ; Tj,min =10…40°C
  - Strategie: const Power, var. Power, const cooling, var. Cooling
- Liefervereinbarung Automobil LV324
  - Angaben in Auswertung: Δ Tvj, IL, tON, tOFF, Tvj,min, Tvj,max, Tcool, UG, Tc/s, Rth
  - Aktives Heizen über Chipverluste, Feineinstellung durch UG
  - Strategie: Konst tON mit zwei Versionen: tON < 5s / tON > 15s
  - EOL: UCE + 5% oder dTvj + 20%
  - Temperaturbestimmung mittel UCE-Methode
  - Freie Parameter: tOFF, dTvj, IL, Tvj,min

Summary

- Brief introduction to power cycling testing
  - Failure Mechanisms
  - Heating and Cooling Concepts
  - Test Strategies
  - Acquisition of the Temperatures
  - WBG challenges
    - Integration will go on
      → hopefully test measures will be integrated as well
    - $R_{DS,ON}$ will be enhanced → more challenging
  - Lifetime will change into positive
    - By higher absolute temperatures
    - Back grinding
    - Data basis will be massively improved
  - Interpretation of the Test Result

Fraunhofer IISB

Andreas Schletz
Andreas.Schletz@iisb.fraunhofer.de
Tel. +49 9131 761 187
Schottkystr. 10
91058 Erlangen
www.iisb.fraunhofer.de

Fraunhofer IISB