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Continuous Sense-FET Current Measurement in a GaN-Based T-Type Bridge-Leg With Monolithic Bidirectional Switch

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***Abstract*—This letter introduces a GaN-based T-type bridge-leg using three GaN power ICs, including a monolithic bidirectional switch (MBDS), with a novel sense-FET-based method for continuous phase current measurement. Experimental results at 200 V demonstrate the current sensing up to ±4 A across all four operating quadrants. The approach could enable high-bandwidth, nearly lossless current measurement, and is applicable to various converter topologies.**

***Index Terms*—Gallium nitride (GaN), T-type bridge-leg, monolithic bidirectional switch (MBDS), current measurement, sense-FET, phase current sensing, power integrated circuits, monolithic integrated circuit.**

I. INTRODUCTION

THE modularity of power modules is increasingly important in power electronics, driven by resource limits and sustainability. Traditional power stage configurations (half-bridge, 3-phase half-bridge, full/H-bridge) are now enhanced by advanced semiconductors (SiC MOSFETs, GaN HEMTs), integrated solutions (IPMs, SiPs, power ICs), and multi-level topologies. Beyond the 2-level half-bridge or bridge-leg, there are various 3-level options (neutral-point-clamped NPC, T-type TT, flying capacitor FC, etc.) that are used for AC/DC rectifiers or DC/AC inverters, or bidirectionally in both directions. The TT bridge-leg is gaining attention thanks to GaN-based monolithic bidirectional switches (MBDS) [1, 2], requiring fewer devices. In 3-phase systems with an 800 V DC bus voltage, two 1200 V high/low-side HS/LS transistors and one 600 V mid bidirectional switch are typically used [3], which has recently also become possible with GaN (see Fig. 1).

For advanced power module functionality, phase current measurement is essential for control, diagnostics, and protection [4]. There are various current sensing approaches, such as shunt, Hall- or magneto-resistive (MR)-sensors or others, each with pros and cons [5, 6] (see Fig. 1). The sense-FET (current mirror technique) is mainly used for protection, as it provides current data only when the device is turned-on. The first products featuring GaN transistors and sense-FETs (also known as sense-HEMT) are now on the market [7, 8], along with ongoing research [9–14], further increasing interest in this approach. These devices are mainly used in topologies that employ one or more LS transistors, such as flyback or bridgeless power factor correction (PFC) topologies, whereby the current can be easily read out using the sense-transistor and used for control or protection purposes. But how can a continuous current be reconstructed as easily as possible from the sense-FETs, for example in the TT bridge-leg?

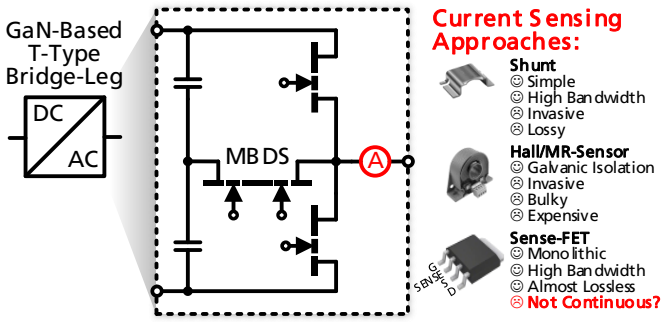

Fig. 1. GaN-based T-type (TT) bridge-leg as DC/AC or AC/DC converter stage with current sensing approaches.

This letter presents a novel, continuous sense-FET current measurement method and demonstrates its implementation in an 800 V GaN-based TT bridge-leg using three GaN power ICs with integrated sense-FET. Section II explains the method and the current state-of-the-art. Section III details implementation and measurement results. Section IV concludes this letter.

II. PROPOSED CONTINUOUS SENSE-TRANSISTOR CURRENT SENSING METHOD

The state-of-the-art in current measurement with sense-FETs typically employs source sensing, i.e., readout of the sense-transistor via a common drain connection to the power (main) transistor. This approach applies to both lateral devices (e.g., GaN HEMTs) and vertical devices (e.g., Si or SiC MOSFETs). The current mirror ratio between main- and sense-transistors is defined as $N = I_{\mathrm{D,MAIN}}/I_{\mathrm{D,SENSE}} = W_{\mathrm{G,MAIN}}/W_{\mathrm{G,SENSE}} = R_{\mathrm{ON,SENSE}}/R_{\mathrm{ON,MAIN}}$. The gate width W_{G} in lateral devices (also referred to as the unit cell or cell pitch in vertical devices) is proportional to the on-resistances R_{ON}. Two principal readout methods for sense-FETs are reported [15–17] (see Fig. 2):

1. Sense-resistor method:
   A resistor R_{SENSE} is in series with the sense-transistor produces a voltage drop

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$$V_{\mathrm{SENSE}} = I_{\mathrm{D}} \cdot R_{\mathrm{ON,MAIN}} \frac{R_{\mathrm{SENSE}}}{R_{\mathrm{SENSE}}+R_{\mathrm{ON,SENSE}}}. \quad (1)$$

2. Virtual ground sensing:
   A transimpedance amplifier (TIA) converts the sense current into a voltage while maintaining $I_{\mathrm{IN-}} = 0$ A and $V_{\mathrm{DIFF}} = 0$ V:

$$V_{\mathrm{SENSE}} = -R \cdot I_{\mathrm{D,SENSE}} \approx -R \cdot \frac{I_{\mathrm{D}}}{N}, \text{ for } N \gg 1 \text{ [9]}. \quad (2)$$

For typical parameters, V_{SENSE} in eq. (1) is small (<0.1 V), making accurate amplification challenging. This limitation is mitigated by virtual-ground sensing, where the readout is independent of R_{SENSE}. Hence, this work focuses on this configuration. Typically, $N \gg 1$ (e.g., 500, 1000, or 1500), yielding low $R_{\mathrm{ON,SENSE}}$ and nearly lossless measurement, though the readout consumes some power.

A drain sensing variant operates similarly [11] (shown in Fig. 2) but has drawbacks: (i) in LS transistors, the drain potential varies relative to the virtual-grounded source, and (ii) in vertical devices, the drain contact on the backside complicates assembly. Source sensing can be extended to a half-bridge [9], but the proportional voltage $V_{\mathrm{SENSE,HS/LS}}$ have different reference potentials. The novel, patent-pending method for continuous sense-transistor current sensing [18] addresses this by summing time-segmented current information. If the transistors share a common node (e.g., the switching node V_{SW}), a voltage proportional to the phase current can be reconstructed by combining source and drain sensing—applicable to various converter topologies.

Fig. 2 illustrates the generalized concept. The virtual ground sensing circuit can be extended to multiple power transistors Q_i ($i \in \{\mathbb{N}\}$), each incorporating a corresponding sense-FET for current measurement. Each transistor branch is represented by an ideal switch and its associated on-resistance. In practical implementations, this enables the simultaneous current monitoring of several switching devices – for example, the high-side and low-side transistors of a bridge-leg or multiple parallel-connected switches in high-current applications. Depending on the N_i, the total branch current $I_{j,i}$ divides between the main transistor ($I_{j,\mathrm{MAIN},i}$) and the sense transistor ($I_{j,\mathrm{SENSE},i}$). The sense terminals of all devices (SENSE_i) are connected together to form the virtual ground node N_{ZVP}, which is held at a constant potential by the TIA. Conversely, all power terminals $j \in \{\mathrm{D}, \mathrm{S}, \mathrm{S}_1, \mathrm{S}_2\}$ are tied to a common reference node N_{REF}, connected to the noninverting amplifier input.

This configuration allows the TIA to sum the sense currents of all devices, yielding an aggregate output voltage proportional to the combined phase or leg current:

$$V_{\mathrm{SENSE}} = -R \cdot \sum_{i=1}^{n} I_{j,\mathrm{SENSE},i}. \quad (3)$$

If all sense-transistor on-resistances are equal $R_{\mathrm{ON,SENSE},1} = R_{\mathrm{ON,SENSE},2} = \cdots = R_{\mathrm{ON,SENSE},n}$ and identical current mirror ratios $N_1 = N_2 = \cdots = N_n$ are used, each sense current contributes equally to V_{SENSE}. If the main- or sense-transistor resistances, or the ratios N_i, differ, additional compensation resistors R_i can be added (see Fig. 2). The effective mirror ratio then becomes $N_i = (R_{\mathrm{ON,SENSE},i} + R_i)/R_{\mathrm{ON,MAIN},i}$, which adjusts the sense current $I_{j,\mathrm{SENSE},i}$. Equal current-to-voltage conversion among all branches is achieved when $N_i = \text{const}$.

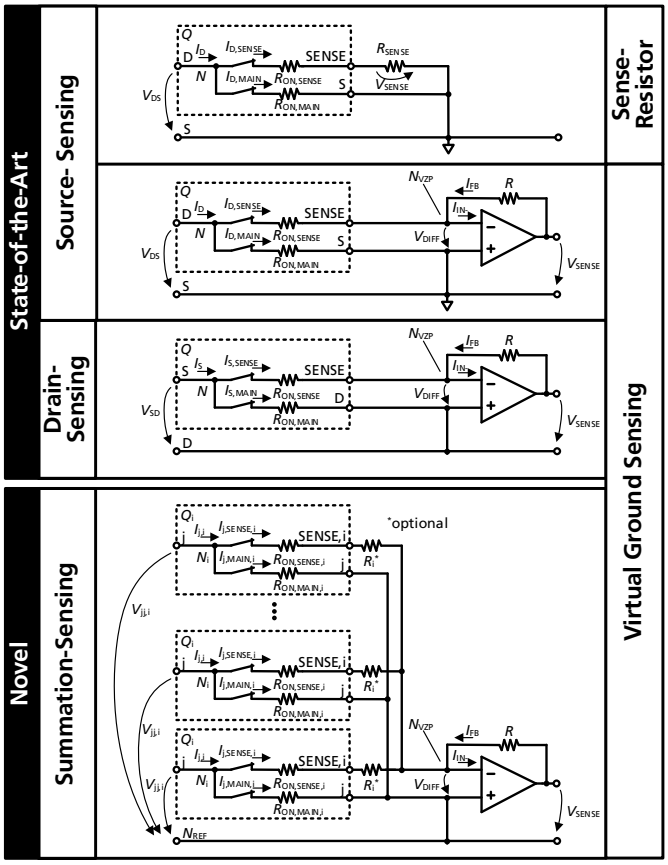

Fig. 2. General overview of conventional and proposed sense-FET current readout circuits.

This approach ensures proportional current summation in V_{SENSE} and is applicable to various power semiconductor devices, including transistors and diodes, as well as diverse converter topologies. In addition, the method does not impose a duty-cycle limitation, since the readout is directly coupled to the power devices and follows their behavior. The configuration allows continuous, low-loss phase-current measurement, even with multiple parallel GaN or SiC switches, providing high bandwidth and accurate dynamic current information without additional shunt elements.

III. Experimental Results

A. GaN-Based T-Type Bridge-Leg Setup

The 800 V GaN-based TT bridge-leg comprises two identical 1200 V GaN transistors and one 600 V MBDS. All three devices are realized as GaN power IC with integrated functions, including a sense-FET [9, 19]. The ICs (chip area: 3.0×2.5 mm^2) are soldered and wire-bonded onto a daughter PCB (63.50×60.69 mm^2), as shown in Fig. 3. Key design parameters of the uni- and bidirectional HEMTs are summarized in Table I. The bidirectional HEMT (GaN-based MBDS), reported in [19], is fabricated on a Si substrate, limiting its voltage rating to the 600 V-class. For current sensing, an OPA818 operational amplifier (±5 V supply, generated by LDOs on the daughter PCB) is configured as a TIA with a 660 Ω feedback resistor, providing a theoretical

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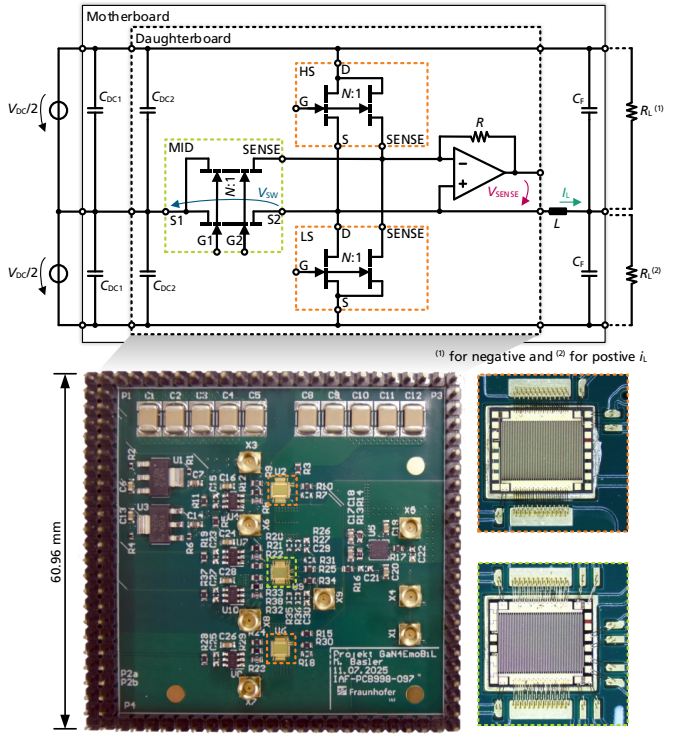

Fig. 3. Schematic and PCB assembly of the 800 V T-type bridge-leg with inset showing the GaN power ICs (including power transistor and sense-FET). The HS and LS devices employ different sense-FET connection schemes.

conversion ratio of approx. –0.53 V/A (N listed in Table I). A 2 pF capacitor in parallel to the feedback resistor R enhances stability. The daughter PCB also contains four gate drivers (MPN: UCC27511) and DC link capacitors (each C_{DC2}: 5×100 nF MLCC). All GaN transistors are d-mode devices. Therefore, the gate drivers are supplied with negative and positive voltage (see Table I, gate-source off/on voltage). Identical external gate resistors are used for all four gates: 22 Ω in the pull-up path and 10 Ω in the pull-down path. This PCB is plugged into a motherboard PCB with additional DC link capacitors (each C_{DC1}: 2×25 µF film capacitors and 100 nF MLCC), filter capacitors (each C_F: 10 nF MLCC) power inductor L of 100 µH (MPN 74437529203101), four isolated power supplies with signal isolation, two temperature read-out circuits, and all connectors.

B. Measurement Results

The main transistors were characterized, and the measured parameters are summarized in Table I. To characterize the sense transistors, exemplary on-wafer IV characteristics were measured and scaled by the current mirror ratio N (calculated by the gate widths W_G), and compared with the IV characteristics of the main transistors, see Fig. 4. The current mirror ratio $I_{D,MAIN}/I_{D,SENSE}$ exhibits an error within approx. ±10%, computed as $(N \cdot I_{j,SENSE} - I_{j,MAIN})/I_{j,MAIN}$. To evaluate the current-to-voltage ratio, a static current of 1 A (toward V_{SW}, see Fig. 3) was applied to each turned-on power transistor, and the corresponding V_{SENSE} was recorded, as listed in Table I. For turned-on MID transistor, V_{SENSE} = -527 mV, closely matches the calculated value of -0.53 V/A within an

TABLE I
PARAMETERS OF THE GAN POWER ICS

		HS/LS	MID
Design	HEMT Device	Single-gate	Dual-gate (MBDS)
	Voltage class	1200 V	600 V
	Depletion Length #	21.5 µm	17 µm
	Main (power) gate-width W_G	124 mm	125 mm
	Sense gate-width W_G	100 µm	100 µm
	Current mirror ratio N	1240	1250
Measurement	Main on-resistance $R_{ON,MAIN}$ @V_{DS} = 1 V	~114 mΩ @V_{GS} = 0 V	~359 mΩ @$V_{G1S1/G2S2}$ = 4 V
	Threshold voltage V_{TH} @I_D = 0.1 A, V_{DS} = 1 V	-5.3 V	-0.3 V
	Gate-source off/on voltage $V_{GS,OFF/ON}$	-7/1.5 V	-2/4 V
	Sense voltage V_{SENSE} @I = 1 A	-132/-135 mV	-527 mV

for single-gate: gate-drain length L_{GD}, for dual-gate: gate-gate length L_{GG}

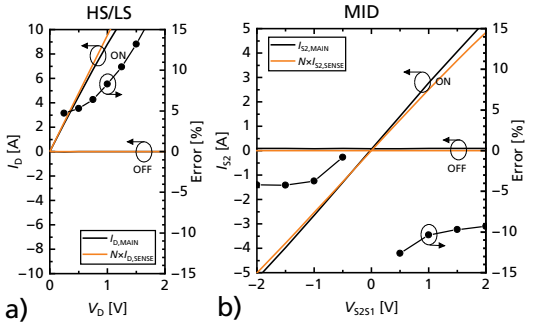

Fig. 4. Measured on-wafer IV characteristic and current error of main and sense transistor for a) a HS/LS transistor in single quadrant and b) the MID transistor in two quadrants. Sense currents are scaled by the current mirror ratio N, and the gate-source turn-on/off voltages are listed in Table I.

TABLE II
PWM SIGNAL CONFIGURATION

MBDS Operation	HS	S2	S1	LS	Meas.	R_L Connection #
$v_{SW} > 0$ V, $i_L > 0$ A	*DC*	ON	1-*DC*	OFF	Fig. 5 b) +e)	(2)
$v_{SW} > 0$ V, $i_L < 0$ A	1-*DC*	ON	*DC*	OFF	Fig. 5 a)	(1)
$v_{SW} < 0$ V, $i_L < 0$ A	OFF	1-*DC*	ON	*DC*	Fig. 5 c)	(1)
$v_{SW} < 0$ V, $i_L > 0$ A	OFF	*DC*	ON	1-*DC*	Fig. 5 d)	(2)

see Fig. 3

error of <1%. Under static conditions, however, it drifts with increasing self-heating. The current mirror error and the slight deviation of the current-to-voltage ratio are attributed to variations in the GaN fabrication process (sheet resistances, device dimensions, gate module, etc.), assembly influences(bond-wires, PCB traces), , and self-heating under current. Under other conditions, V_{SENSE} deviates significantly from -0.53 V/A, primarily due to leakage currents in the mA range within the bidirectional GaN HEMTs (main and sense transistor). These leakage currents affect the readout and current-to-voltage conversion of HS and LS sense transistor, as the sense currents in the turned-on state are also in the mA range (see Fig. 4). In particular, the elevated leakage current in the MBDS transistors introduces a differential voltage V_{DIFF} at the inputs of the OPA818, counteracting the TIA, which ideally operates with V_{DIFF} = 0 V. Consequently, V_{SENSE} (precisely the converted $I_{D,SENSE,i}$ and $I_{S,SENSE,i}$) also cannot be adjusted via the resistors R_i, $i \in \{HS, LS\}$. To reduce error, GaN transistors with integrated sense-FETs are available that undergo post-trim calibration during production, improving current measurement accuracy over the complete temperature range to ±4% [7]. The gate width ratio between main and sense transistors also

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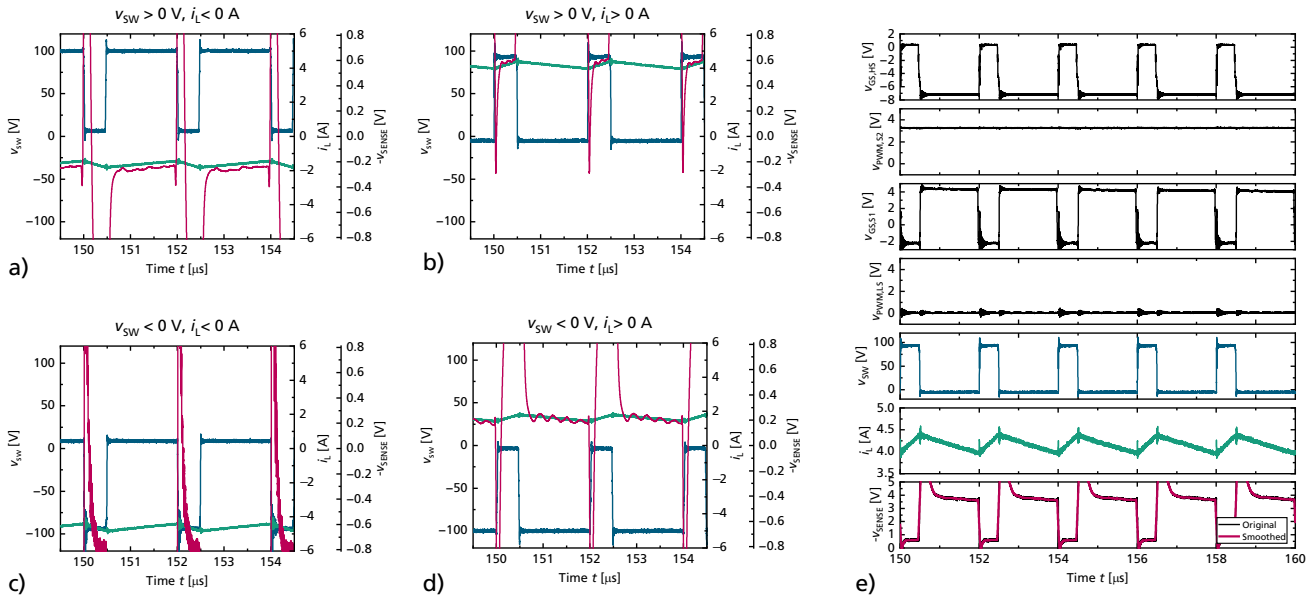

Fig. 5. Experimental validation of the proposed continuous sense-transistor current sensing method using the GaN-based T-type bridge-leg at V_{DC} = 200 V in all four operating quadrants of the GaN-based MBDS. (a)-(d) show measured waveforms of $v_{SW}(t)$, $i_L(t)$ and $v_{SENSE}(t)$. (e) presents the waveforms $v_{GS,HS}(t)$, $v_{PWM,S1}(t)$, $v_{GS,S2}(t)$, $v_{PWM,LS}(t)$, $v_{SW}(t)$, $i_L(t)$ and $v_{SENSE}(t)$ for the case shown in (b).

represents a design trade-off: a larger N reduces accuracy but lowers the feedback current of the TIA, thereby reducing power consumption.

To evaluate the performance of the GaN-based TT bridge-leg and the proposed current measurement method, all four operating quadrants of the GaN-based MBD were characterized at a DC-voltage V_{DC} of 200 V, as shown in Fig. 5 in a similar manner as in [3]. The gate-source off/on voltage is listed in Table I, and Table II summarizes the PWM signal configuration of the three switches in the TT bridge-leg (S2 and S1 denote the two gates of the MBDS). For all four operating modes, the switching frequency f_{SW} is set to 500 kHz, and the duty cycle DC is 25%, including a dead-time of 40 ns. Fig. 5 a)-d) show the measurement waveforms of $v_{SW}(t)$, $i_L(t)$ and $v_{SENSE}(t)$ in the four operating quadrants of the MBDS. The proposed current-sensing approach has been demonstrated, with currents measured over ±4 A. The signal $v_{SENSE}(t)$ was smoothed using a moving average over 200 samples (oscilloscope resolution: 0.32 ns per point). The v_{SENSE} axes in Fig. 5 a)-d) are scaled to the current-voltage-ratio of -0.13 V/A (static ratio of HS/LS, see Table I), so v_{SENSE} and i_L should ideally overlap for accurate current measurement, similar to half-bridge source sensing in [9]. This overlap can indeed be seen for HS and LS. When applying a different scaling of v_{SENSE} using -0.53 V/A (static ratio of MID), no overlap is obtained, although the qualitative shape v_{SENSE} still follows that i_L (see Fig. 5 e)). Due to the high leakage currents and the dynamic switching behavior of the MBDS, meaningful readout is only possible under static conditions. These effects significantly reduce accuracy during dynamic operation. The settling time is approx. 500 ns. No optimization, such as adjusting the feedback capacitor or adding low-pass filtering, has yet been performed, and the dead time additionally influences the settling behavior. When the OPA818 operates near its supply rails (±5 V), substantial overshoot is observed due to non-optimized dynamic behavior. Reducing the feedback resistor R and thus gain results in a noticeable decrease in v_{SENSE} overshoot.

Comparable sense-FET readout circuits exhibit similar settling times [9], but achieve shorter sensor signal rise times of approx. 50 ns, corresponding to a bandwidth of about 7 MHz [10]. In addition, [10] provides a comparison of GaN power ICs with current sensing functionality. The losses associated with the proposed current sensing approach arise from the current flowing through the sense transistors and from the power consumption of the TIA and subsequent amplifier stages. Nevertheless, these losses are significantly lower than those of shunt-based current-measurement methods. Despite the limitations identified, mainly the sensitivity to high leakage currents of the MBDS and the non-optimized TIA circuit, the results demonstrate the feasibility of the proposed sensing approach and indicate that further improvement is possible.

IV. Conclusion

The proposed sense-FET-based current measurement method was demonstrated in a GaN-based T-type bridge-leg. Experimental results confirm continuous phase current reconstruction in all operating quadrants. While conversion ratio discrepancies require further optimization, the method offers high bandwidth, low loss, and applicability to advanced converter topologies needing precise current sensing.

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