High Endurance Strategies for Hafnium Oxide Based Ferroelectric Field Effect Transistor

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***Abstract*— In this paper potential strategies to overcome the endurance limitations of hafnium oxide based ferroelectric field effect transistors are discussed. These pathways are based on the assumption that the high interfacial field stress and the accompanying charge injection in the metal-ferroelectric-insulator-semiconductor gate stack are the dominant degradation mechanisms during program and erase operation. Three different approaches capable of lowering or eliminating the interfacial field stress are being assessed - lowering the electrical field stress induced by polarization reversal; utilizing low voltage sub-loop operation; altering the capacitive divider within the gate stack.**

hafnium oxide; ferroelectric; FRAM; FeFET, NVM

I. INTRODUCTION

With the appearance of ferroelectric hafnium oxide (FE-HfO_2) the ferroelectric field effect transistor (FeFET) has experienced a renaissance in terms of scalability and CMOS-compatibility and has become a serious contender for an embedded memory solution in 2X nm HKMG technologies and beyond ([1] and Ref. therein). However, at this stage of development and device implementation the FeFET faces some trade-off between endurance and retention, as well as between scalability and memory window (MW). In particular, the key feature of the FE-HfO_2 based FeFET - a high coercive field (E_c) in combination with an ultra-thin SiO(N) interface - has proven ambivalent in nature. On the one hand the high E_c is the key enabler for device scaling and retention, on the other hand it challenges the cycling endurance of the novel FeFET device [2]. The degradation of the SiO(N) interface driven by cyclic charge trapping during program (PGM) and erase (ERS) operation was identified as the root cause for this endurance degradation [3]. According to these findings new strategies need to be derived to overcome this endurance limitation. Based on experimental data and theoretical considerations this paper will review and assess different strategies to overcome this dilemma towards a higher endurance FE-HfO_2 based FeFET. The following strategies to reduce or eliminate the high interfacial field stress during PGM and ERS operation in FE-HfO_2 based FeFET will be examined: In section II – the tailoring of the polarization of FE-HfO_2 will be examined. In section III – the possibilities of ferroelectric sub-loop operation will be analyzed. Finally in section IV – the engineering of the capacitive voltage divider of the gate stack utilizing higher-k interfaces or direct growth of FE-HfO_2 on silicon as well as the separate area scaling of the ferroelectric and the insulator capacitance in metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gate structures will be discussed.

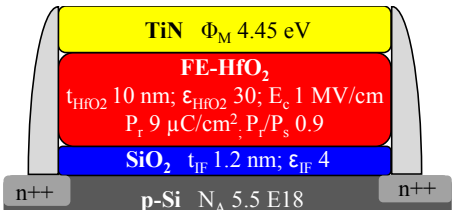

Figure 1. Schematic cross-section and gate stack parameters of the FE-HfO_2-based FeFET used for modelling and obtaining the experimental results discussed in this paper.

The numerical simulation results shown in this paper are based on the FeFET description given by Miller and McWorther [4]. The polarization hysteresis is simulated according to a Preisach [5] behavior, including sub-loop operation. The parameters of the FE-HfO_2 based FeFET device used as a reference are given in Fig. 1., with P_r and P_S representing the remanent and spontaneous polarization and ε_{HfO2} and ε_{IF} the dielectric constants and t_{HfO2} and t_{IF} the thickness of HfO_2 and the interfacial layer respectively. N_A

represents the doping concentration of the p-Si, whereas the work function of the TiN metal gate is represented by Φ_M.

II. Tailoring the Ferroelectric Polarization

In order to assess the potential use to be expected from a tunable polarization, its role during polarization switching in the FeFET has to be examined. In Fig. 2 the electrical field hysteresis in the HfO_2 (a) as well as in the interfacial layer (b) for both a ferroelectric and a dielectric gate stack are shown.

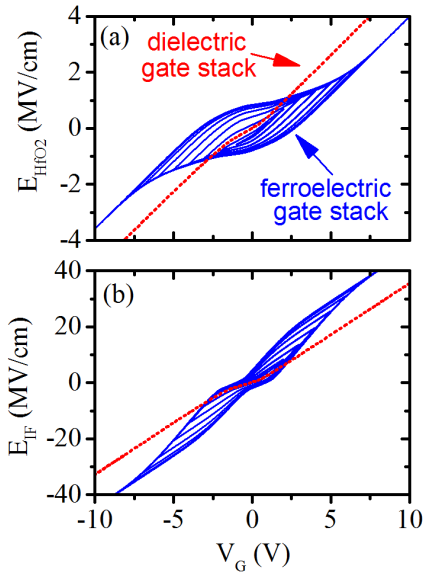

Figure 2. Simulated electrical field strength hysteresis for a ferroelectric (blue solid lines, parameters according to Fig. 1) and a dielectric (red dashed lines, same stack, but without polarization) gate stack for a V_G excitation voltage oscillating from ±10V to zero. In (a) the electrical field in the hafnium oxide is given, whereas in (b) the electrical field in the interfacial layer (here SiO_2) is given.

The bipolar gate voltage excitation (V_G) is decreasing from ±10V to zero. The simulation with HfO_2 possessing ferroelectric properties was performed according to the parameters given in Fig. 1, whereas the simulation for dielectric HfO_2 was performed with a similar stack but excluding polarization.

In Fig. 3a the electrical field in the HfO_2 (E_{HfO2}) and in the interface (E_{IL}) were extracted assuming a program operation at V_G = 5V. In Fig 2 and 3a it is readily observed that the trends in electric field distribution for the two stacks, ferroelectric and dielectric, are inverted. For the ferroelectric stack, the polarization reversal from the negative polarization state to the positive polarization state leads on the one hand to a reduced electrical field in the HfO_2 and on the other hand to an even further increased interfacial field strength.

Due to the fact that charge injection was not considered in this simulation, this behavior can simply be explained by conservation of the electric displacement field

$$D = \varepsilon_0 E + P = \varepsilon_0 \varepsilon_{HfO_2} E_{HfO_2} + P_S \overset{!}{=} \varepsilon_0 \varepsilon_{IF} E_{IF}, \qquad (1)$$

where D is the electric displacement field and ε_0 the vacuum permittivity. Accordingly, simply judging from the analytical description of the electric displacement field it becomes clear that P_S is both responsible for the increase in E_{IF} as well as for the decrease in E_{HfO2}. Unfortunately, this is disadvantageous for device operation since it increases the gate voltage required for saturated polarization switching and also affects device reliability due to the fact that E_{IF} is increased.

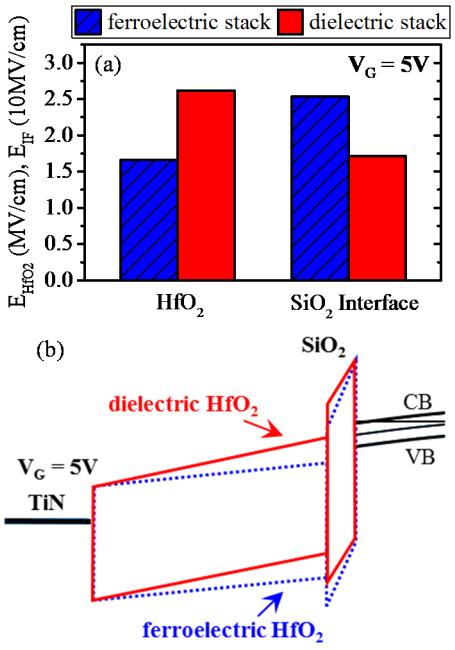

Figure 3. Simulated electrical field strength for a ferroelectric (parameters according to Fig. 1) and dielectric (same stack, but without polarization) gate stack at 5 V applied gate bias. In (a) the electrical field in the hafnium oxide and the interfacial layer were extracted. The striped blue bars illustrate results for the ferroelectric stack and the blank red bars for the stack containing dielectric HfO_2 only. Below, (b) compares the band diagram of both stacks at 5 V applied gate voltage (blue dashed: ferroelectric; red solid: dielectric).

This increase in E_{IF} is additionally illustrated in the band diagram in Fig. 3b. In the example given here the ferroelectric stack already enables Fowler-Nordheim tunneling, whereas the dielectric stack remains in a direct tunneling regime for V_G = 5V.

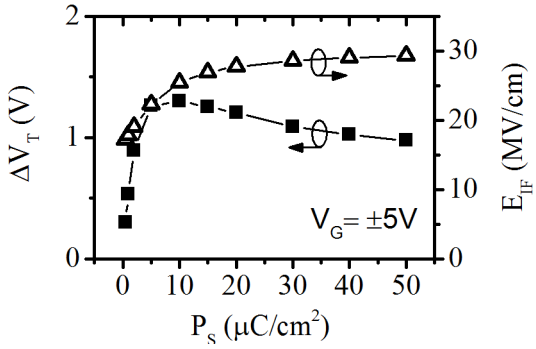

Figure 4. Simulated memory window ΔV_T (primary y-axis) and interfacial field stress E_{IF} (secondary y-axis) of a ferroelectric gate stack as a function of the spontaneous polarization P_S (remaining parameters according to Fig. 1). The data were extracted for a V_G excitation of ±5V.

In order to analyze the impact of P_S on FeFET device operation in more detail, additional simulations were performed in which P_S was varied and its impact on both memory window (MW) and interfacial field stress E_{IF} was analyzed (see Fig. 4).

For a fixed gate voltage of ±5 V, varying the spontaneous polarization from 0 to 50 µC/cm² yields a maximum memory window of around 1.3 V for a spontaneous polarization between 5 – 10 µC/cm². Below 5 µC/cm² the memory window drops dramatically and above 10 µC/cm² the memory window decreases gradually. Even though the memory window should be rather independent of P_S due to the fact that MW ~ $2 \cdot E_C \cdot t_{HfO2}$ [6], the behavior can reasonably be explained as follows: For P_S values smaller than 5 µC/cm² the channel surface charge density induced by the spontaneous polarization is not sufficient for the given parameterization of the simulation (this does however not imply that small P_S values cannot induce large memory windows [7]). Moreover, for P_S values larger than 10 µC/cm² and for 5 V fixed gate voltage the ferroelectric is more and more operated in a sub-loop state (P_S reduces E_{HfO2}, Fig. 2-3), which effectively decreases the memory window. Hence, the expected saturation of the memory window for larger spontaneous polarization even turns into a degradation of MW.

Besides these observations, Fig. 4 shows that the interfacial field stress monotonically increases with larger P_S values and gradually saturates. The increase of E_{IF} with increasing P_S can be explained by equation 1 whereas the saturating behavior is caused by the inability of 5 V gate bias to fully polarize ferroelectric films with a higher P_S. Saturating the MW at high P_S values requires large switching voltages and lead to a further increase of E_{IF}.

In total, these simulations show that besides being in general detrimental to data retention [8], a large spontaneous polarization and the accompanying large E_{IF} might be one of the possible origins for the interface degradation of nonvolatile FE-HfO_2 based FeFETs [3].

Accordingly, the possibilities for reducing the spontaneous polarization need to be discussed. Due to the fact that the value of the spontaneous polarization is intrinsically connected to the ions and crystal structure of the ferroelectric, it is highly challenging to influence the basic value of P_S. For ferroelectric hafnium oxide, the theoretical value for spontaneous polarization was recently predicted to be around 51 µC/cm² and showed only minor response to different dopants [9]. Referring back to the statements of the last paragraphs, such a high spontaneous polarization would exert significant electrical field stress on the interface between FE-HfO_2 and silicon bulk when switched into saturation. Assuming it is not possible to influence the intrinsic value of P_S, the only possibility to reduce the spontaneous polarization is by orientation control of the polarization axis with respect to the axis of the electrical field being applied (see **Error! Reference source not found.**).

However, even in case it would be possible to control the polarization axis (texture control or epitaxial growth would be required), there is an obvious drawback connected to rotated polarization axis: The reduction of the projected polarization onto the field axis is accompanied by a reduced projection of the electrical field onto the polarization axis. Accordingly, a higher gate voltage needs to be applied to switch polarization states which again increases the interfacial field stress due to the overall increased gate voltage.

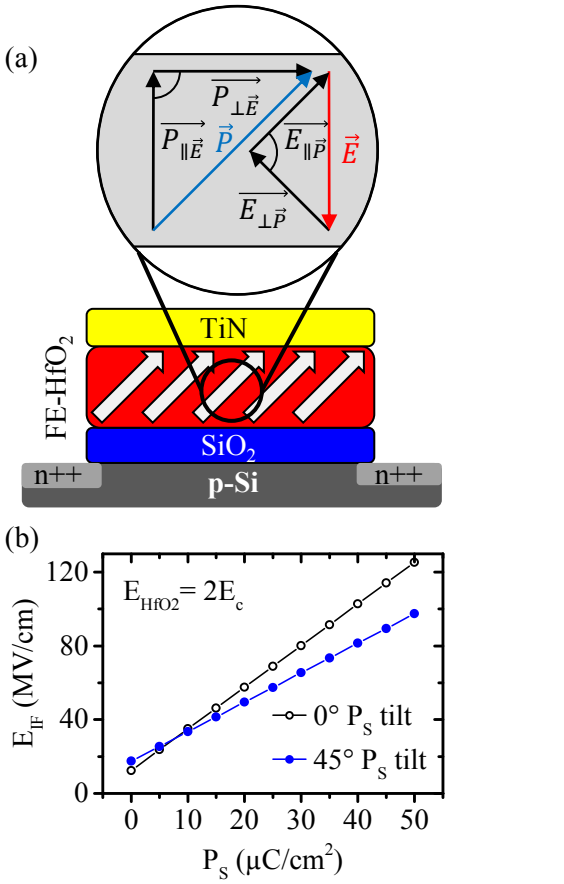

Figure 5. Orientation control of polarization axis to reduce effective value of spontaneous polarization. In (a) a FeFET transistor with homogenously tilted polarization axis is shown. The magnification shows the mutual projections of polarization and electrical field axis (whereas ∥ and ⊥ represent the parallel and perpendicular projections). In (b) the impact of the polarization axis orientation on the electric field in the interface E_{IF} during saturated polarization switching at $E_{HfO2} = 2E_c$ is illustrated as a function of spontaneous polarization P_S (parameters according to Fig. 1). The tilt is defined with respect to the surface normal of the channel.

This trade-off is illustrated in Fig. 5b assuming a tilted polarization axis with respect to the surface normal of the channel. Nevertheless, for P_S values above 10 µC/cm² a reduced E_{IF} can be observed for saturated polarization switching at $E_{FE} = 2E_c$. Hence, the control of polarization orientation is limited for reducing interfacial field stress but it represents one possible approach to improve FeFET endurance. The first experimental work on controlling polarization axis alignment for FE-HfO_2 are currently being performed by research groups in Japan [10][11][12] and represent important contributions to further enhance FeFET performance.

III. UTILIZING SUB-LOOP OPERATION

A viable solution to suppress charge trapping and to achieve endurance cycles of more than 10^{12} (limited by testing time) has been experimentally demonstrated for large area, µm-sized FE-HfO_2 based FeFET devices utilizing low voltage operation in combination with an about 3 nm thick SiO_2 interface [13], [14]. A possible explanation for this improved endurance performance was given in [2]. It is assumed that due to the non-saturated polarization and E_c of the ferroelectric sub-loops, which are accessed at low voltage, the MW remains small, but also the electric field stress on the rather thick interface can be minimized yielding significantly less charge trapping and therewith higher endurance.

This assumption is further supported by the simulation results given in Figure 6a. Here the programming slope of the memory window and the corresponding interfacial field stress E_{IF} for different interfacial layer thicknesses t_{IF} of a FE-HfO_2-based FeFET are shown. In the saturated memory window regime the system is bound by constant field scaling, meaning that in order to obtain a saturating switching field in the ferroelectric the PGM/ERS voltage has to be increased with increasing interfacial layer thickness t_{IF}, whereas the maximum electric field stress in the interface E_{IF} for saturated polarization switching remains largely independent of t_{IF}.

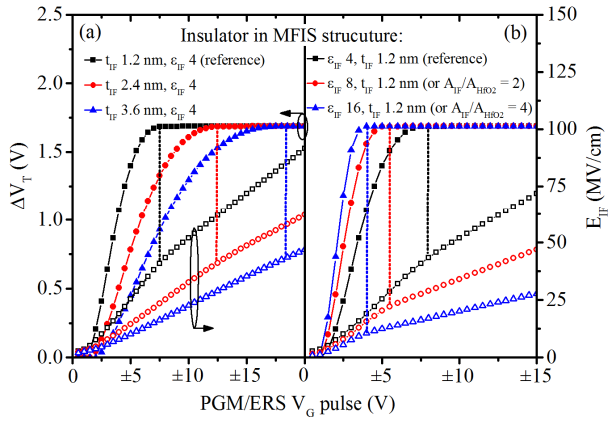

Figure 6. Simulated memory window ΔV_T (primary y-axis) and interfacial field stress E_{IF} (secondary y-axis) of a ferroelectric gate stack (parameters according to Fig. 1) are shown as a function of the PGM/ERS voltage. Part (a) of the figure shows a variation of the thickness of the interfacial layer t_{IF}, whereas part (b) shows a variation of the dielectric constant of the interfacial layer ε_{IF}. Alternatively, the variation of ε_{IF} can be interpreted as a variation of the area ratio between the interfacial layer A_{IF} and the ferroelectric HfO_2 layer A_{HfO2} within the gate stack.

However, when considering the ability of ferroelectrics to access minor hysteresis loops it is possible to define operating conditions below the saturated polarization switching and therewith below the maximum field stress in the interfacial layer. The existence of this sub-loop behavior in FE-HfO_2-based systems has been directly observed in the polarization hysteresis of metal-insulator-metal capacitors as well as in the programming slope of long channel FeFETs [15]. Since the simulation results shown here are based on a sub-loop containing Preisach description of the ferroelectric polarization hysteresis, this programing slope is also reflected in the memory window evolutions shown in Fig. 6a. Especially for larger t_{IF} this slope extends over a broad voltage range offering a stable operating range at reduced memory window.

In contrast to the constant field scaling in the saturated polarization regime described above, the increase of interfacial layer thickness in the non-saturated regime may now offer a true benefit. The possibility to significantly reduce E_{IF} by low voltage operation allows for PGM/ERS conditions that are no longer dominated by Fowler-Nordheim tunneling [2]. The remaining charge injection into the conduction band of the hafnium oxide may now rely on direct tunneling alone, which in turn is strongly suppressed with increasing t_{IF}.

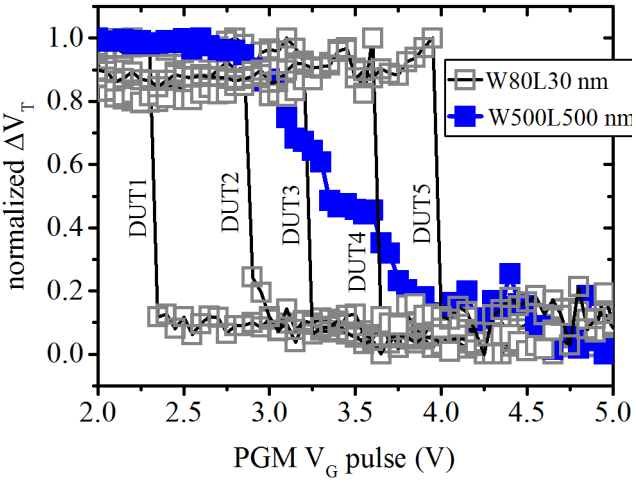

Figure 7. Simulated memory window ΔV_T (primary y-axis) and interfacial field stress E_{IF} (secondary y-axis) of a ferroelectric gate stack as a function of the spontaneous polarization P_S (remaining parameters according to Fig. 1). The data were extracted for a V_G excitation of ±5V.

Even though this high endurance strategy jeopardizes long time retention due to the low stability of unsaturated polarization loops, it suggests a possible pathway to a 1T DRAM application of the FE-HfO_2 based FeFET. However, since the minor hysteresis loop behavior of FE-HfO_2 forms the core of this high endurance strategy its physical origin and scalability needs to be considered.

The existence of sub-loops in the polarization hysteresis of a ferroelectric is a cumulative phenomenon relying on a multi-grain, multi-domain state and a statistical distribution of ferroelectric switching events. When shrinking the device size to the dimensions of the grains or even single domains a different situation arises, that was recently investigated by Mulaosmanovic et al. [16] using highly scaled FE-HfO_2 based FeFETs. In this context Fig. 7 shows experimentally obtained programming slopes for differently sized FE-HfO_2 based FeFETs (fabrication described elsewhere [16]) measured on the same wafer. For the W:500 nm L: 500 nm device the gradual programming slope due to sub-loop switching with a memory window saturation above 5V can be observed. This behavior is in accordance with the simulation results shown in Fig. 6 assuming a Preisach like polarization reversal. However, when further scaling device size to W: 80 nm L: 30

nm a programming slope is no longer present. Instead the devices are characterized by an abrupt switching process with no intermediate polarization states. The onset voltage of this abrupt switching is statistically distributed as illustrated by the five DUTs of similar dimension. From these experimental findings it can be deduced that large area devices may be viewed as a superposition of this statistical fluctuation of discrete switching voltages observed in devices scaled to the ferroelectric domain size.

As a consequence of this size-induced transition from an "analog" to a more or less "digital" device behavior, the utilization of sub-loop operation to overcome the endurance limitations of FE-HfO_2 based FeFETs has to be viewed with caution. Based on these results the sizing of the memory window and the related interfacial field stress is no longer possible. Nevertheless, when considering the possibility of future improvements in the microscopic homogeneity of the material, the domains, which are responsible for the low voltage onset of switching in large array devices, may be homogenously stabilized in highly scaled devices. However, the impact of the full polarization switching in these devices and the possibility that a reduced switching voltage is correlated with a higher impact of polarization on the interfacial field stress (discussion of polarization axis in section II) needs to be investigated in detail. Furthermore it should be noted that based on the assumption of a superposition of different switching voltages in large area devices, the local polarization impact of early switching grains on the interfacial field stress remains unclear and is not covered by the simulation results, which assume a continuous system and therewith an overall lowered polarization within the sub-loop regime.

Beyond the scope of this paper it is interesting to note that the "digital" switching behavior of highly scaled device does no longer support the application space of neuromorphic functionality, for which the FeFET is believed to be a suitable candidate [17].

IV. Tailoring the Capacitive Divider

In order to switch the ferroelectric polarization of a FeFET, a voltage drop across the ferroelectric layer exceeding the coercive voltage needs to be realized. The distribution of the applied gate voltage within the gate stack of a MFIS based FeFET is determined by the capacitive voltage divider between the capacitance of the ferroelectric layer, the capacitance of the interfacial layer and the semiconductor capacitance. Hence, the reduction of the gate voltage required for switching and the minimization of unnecessary voltage drops across the interface and the semiconductor can be influenced by the capacitive divider of the gate stack. However, simply altering the capacitive divider by scaling the layer thicknesses (see section III and Fig. 6a) will result in constant field scaling and therewith fails to reduce the interfacial field stress which is responsible for the endurance degradation in FE-HfO_2 based FeFETs. Additionally, it can be noted that during PGM and ERS operation the FeFET is either in strong inversion or in strong accumulation, thus reducing the impact of the semiconductor capacitance to a minimum. Hence, the only remaining means to influence the interfacial field stress E_{IF} during saturated polarization switching ($E_{HfO2} \approx 2E_c$) are the maximization of the dielectric constant ratio $\varepsilon_{IF}/\varepsilon_{HfO2}$ or alternatively the maximization of the area ratio A_{IF}/A_{HfO2}, where A_{HfO2} represents the area of the ferroelectric HfO_2 layer and A_{IF} the area of the interfacial layer, which is in direct contact with the semiconductor channel material.

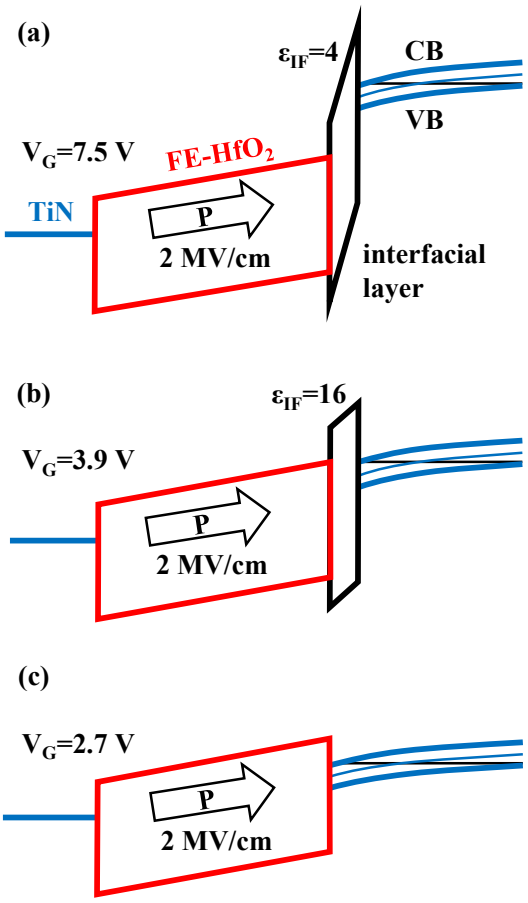

Figure 8. Band diagrams of HfO_2-based FeFETs during program operation. A saturated polarization switching with $E_{HfO2}=2E_c$. is achieved at (a) V_G=7.5V for the reference device according to Fig.1; (b) V_G=3.9V for the reference device with ε_{IF} enhanced to 16 or A_{IF}/A_{HfO2} enhanced to 4; (c) V_G=2.7V for the reference device configured as an MFS-FET.

Since the dielectric constant and the ferroelectric properties of a material are rather intrinsic, only ε_{IF} remains as a material parameter capable of changing the capacitive divider towards lower interfacial field stress E_{IF}. The simulation results depicted in Fig. 6b clearly illustrate the reduced switching voltage and interfacial field stress to be expected when increasing ε_{IF} beyond the dielectric constant of SiO_2. The improved band bending with increasing ε_{IF} for a FE-HfO_2 based FeFET during program operation is further illustrated in Fig. 8b. The increased ε_{IF} suppresses the Fowlwer-Nordheim tunneling, which most likely dominates the program operation of the reference device illustrated in Fig. 8a. A further increase of ε_{IF} would ultimately require modified FN tunneling through the HfO_2 to reach its conduction band. Charge trapping would be reduced to direct tunneling into energetically available trap sites close to the interface.

However, the replacement of SiO_2 by a higher-k interfacial layer poses a severe technological challenge that was extensively investigated during the introduction of high-k metal gate transistor technologies [18]. Proven concepts such as increasing the nitrogen content in SiON or the use of SiN instead of SiO_2 only offer a minor increase of ε_{IF} and may result in a reliability trade-off due to a higher interfacial trap density [19], [20]. Ultimately the replacement of SiO_2 by a high-k material with ε_{IF} above 8 will require the direct growth of a CMOS compatible metal oxide with a sufficiently large band offset and thermal stability in direct contact with silicon [18][21]. This significantly narrows down the choice of material to a few metal oxides, amongst which HfO_2 itself can be found. This means that if technological challenges such as the regrowth of a SiO_2 interfacial layer after thermal treatment or the availability of manufacturing ready direct growth techniques of metal oxides on silicon can be overcome, the more logical choice appears to be the direct transition to a metal-ferroelectric-semiconductor-FET (MFS-FET). The moderate band bending experienced by such a FE-HfO_2 based MFS-FET structure during PGM operation is displayed in Fig. 8c. Depending on the interface quality endurance values similar to the best results (>10^9) obtained for saturated polarization switching in metal-ferroelectric-metal capacitors might be expected [22].

Considering first indications of an orthorhombic phase in HfO_2 directly grown on silicon [23], [24] and the significant progress in the interface-less growth of FE-HfO_2 on Ge [25], first feasibility studies on actual MFS-FET devices might soon be available.

Finally the rather straight forward approach to alter the capacitive divider within the gate stack of a FeFET by influencing the area ratio A_{IF}/A_{HfO2} will be discussed. The separate scaling of the individual capacitor areas requires the utilization of a MFMIS gate structure, whose feasibility for FeFET devices has already been demonstrated [26]. In terms of a reduction of E_{IF} changing the area ratio A_{IF}/A_{HfO2} is equivalent to changing the ratio of the dielectric constants $\varepsilon_{IF}/\varepsilon_{HfO2}$. For this reason the improved electric field distribution within the gate stack for A_{IF}/A_{HfO2} = 2 and A_{IF}/A_{HfO2} = 4 can be observed in Fig 6b. The improved band bending for A_{IF}/A_{HfO2} = 4 is illustrated in Fig 8b. Considering the ability of the floating gate (FG) to store electrical charge, achieving a large area ratio to suppress charge trapping appears mandatory for the functionality of the MFMIS-FET gate stack.

Different pathways to realize such a structure in contemporary technologies are illustrated in Fig. 9. In a gate first technology the enlargement of the interfacial area with respect to the ferroelectric area might simply be achieved by separately patterning the dielectric and the ferroelectric part of the gate stack using the FG as an etch stop (Fig. 9a). Alternatively, shrinking of the control gate (CG) alone may suffice. As a major drawback the enhanced complexity of the gate stack and the reduced scalability with increasing area ratio has to be accepted.

When utilizing a high-k first metal last process technology as a starting point for the conformal deposition of FE-HfO_2, area scaling of the MFMIS-FET will occur naturally (Fig. 9b). However, the sizing of the CG plug responsible for this area scaling depends on the gate length and the thickness of the FE-HfO_2. This imposes a restriction on the available area ratios.

Achieving a large area ratio, while simultaneously maintaining the lateral footprint of the device may be achieved by using a recess gate approach as depicted in Fig. 9c. The depth of the recess defines the size of the dielectric capacitor, whereas the buried CG contact defines the area of the ferroelectric capacitor. Restrictions for the achievable area ratio are given by the technological limits of the recess and the decreasing on-current of the FeFET with increasing channel length.

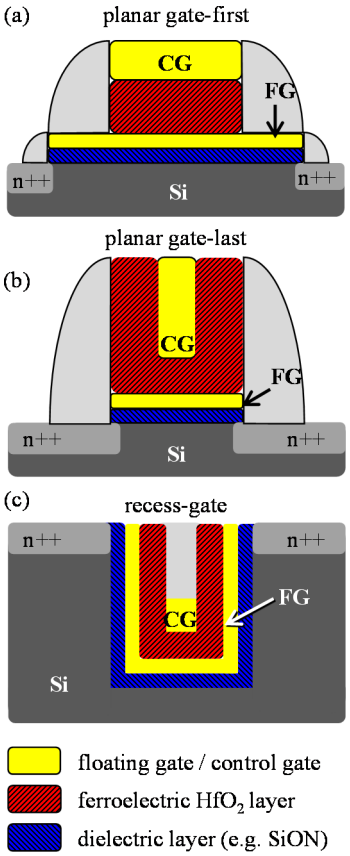

Figure 9. Schematic FeFET device cross sections illustrating different pathways towards a reduction of interfacial field stress in HfO_2-based FeFETs by separately scaling the area of the ferroelectric and the dielectric capacitor within a MFMIS-FET gate stack. (a) lithographically sizing the capacitor areas in a gate first technology; (b) utilizing the intrinsic size reduction of the gate plug in replacement gate; (c) sizing of the gate contact in a recess gate.

V. Conclusion

In conclusion, we assessed different strategies to cope with the high interfacial field strength present during program and erase operation in hafnium oxide based MFIS-FETs. It was found that besides the high external biasing required to reach the coercive field strength of the FE-HfO_2, additionally the polarization reversal itself significantly contributes to the interfacial field stress. When accepting the polarization as an

intrinsic material property, the technological challenge to homogenously tilt the polarization axis remains as the only viable option to reduce the polarization contribution. Although the accompanying increase of switching voltage with increasing tilt angle results in a trade-off, a lower interfacial field strength is still to be expected for polarization values above 10 $\mu C/cm^2$.

A simultaneous decrease of the switching voltage and polarization contribution to the interfacial field stress may be expected when operating the FeFET in a sub-loop regime, accessing intermediate memory window states below saturation. However, as was proven experimentally in this paper, this sub-loop behavior observed in large area devices most likely originates from the statistical superposition of individual switching voltages and grain orientations and therewith vanishes with decreasing device size or in single crystal FeFETs. It should be noted that based on these findings the Preisach description of polarization hysteresis becomes inadequate for highly scaled devices and should be substituted by a Landau based model in future simulation work.

Finally, the feasibility of altering the capacitive divider of the gate stack by increasing the dielectric constant or the area of the interfacial layer with respect to the ferroelectric layer has been discussed. It was concluded that if the technological challenges to replace SiO_2 with an interface-less high-k material can be overcome the direct transition to a MFS structure appears to be the more likely pathway. In the case of an improved field distribution within the gate stack by a simple capacitor area sizing in an MFMIS structure, the increased integration complexity and scaling penalties would need careful evaluation.

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REFERENCES

[1] J. Müller *et al,* "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEEE International Electron Devices Meeting (IEDM)*, 2013, p. 10.8.1.

[2] J. Müller, S. Müller, P. Polakowski, and T. Mikolajick, "Ferroelectric hafnium oxide: a game changer to FRAM?," in *14th Non-Volatile Memory Technology Symposium (NVMTS)*, 2014.

[3] E. Yurchuk *et al,* "Origin of the endurance degradation in the novel HfO_2-based 1T ferroelectric non-volatile memories," in *IEEE International Reliability Physics Symposium (IRPS)*, 2014, p. 2E.5.1.

[4] S. L. Miller and P. J. McWhorter, "Physics of the ferroelectric nonvolatile memory field effect transistor," *J. Appl. Phys,* vol. 72, no. 12, pp. 5999–6010, Dec. 1992.

[5] F. Preisach, "Über die magnetische Nachwirkung," *Zeitschrift für Physik*, vol. 94, no. 5, pp. 277–302, 1935.

[6] M. Ullmann, "Ferroelektrische Feldeffekttransistoren: Modellierung und Anwendung," Dissertation, Universität der Bundeswehr Hamburg, Hamburg, 2002.

[7] S. Müller *et al,* "Performance Investigation and Optimization of Si:HfO_2 FeFETs on a 28 nm Bulk Technology," in *Applications of Ferroelectric and Workshop on the Piezoresponse Force Microscopy (ISAF/PFM), 2013 IEEE International Symposium on the*, 2013, pp. 248–251.

[8] T. P. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?," *IEEE Electron Device Lett,* vol. 23, no. 7, pp. 386–388, 2002.

[9] S. Clima *et al,* "Identification of the ferroelectric switching process and dopant-dependent switching properties in orthorhombic HfO_2: A first principles insight," *Appl. Phys. Lett,* vol. 104, no. 9, p. 92906, 2014.

[10] T. Shimizu *et al,* "Growth of epitaxial orthorhombic $YO_{1.5}$-substituted HfO_2 thin film," *Applied Physics Letters*, vol. 107, no. 3, p. 32910, 2015.

[11] K. Katayama *et al,* "Orientation control and domain structure analysis of {100}-oriented epitaxial ferroelectric orthorhombic HfO_2-based thin films," *Journal of Applied Physics*, vol. 119, no. 13, p. 134101, 2016.

[12] T. Kiguchi, S. Nakamura, A. Akama, T. Shiraishi, and T. J. Konno, "Solid state epitaxy of (Hf,Zr)O_2 thin films with orthorhombic phase," *Journal of the Ceramic Society of Japan*, vol. 124, no. 6, pp. 689–693, 2016.

[13] C.-H. Cheng and A. Chin, "Low-Leakage-Current DRAM-Like Memory Using a One-Transistor Ferroelectric MOSFET With a Hf-Based Gate Dielectric," *IEEE Electron Device Lett,* vol. 35, no. 1, pp. 138–140, 2014.

[14] Y. C. Chiu *et al,* "Low power 1T DRAM/NVM versatile memory featuring steep sub-60-mV/decade operation, fast 20-ns speed, and robust 85°C-extrapolated 10^{16} endurance," in *Symposium on VLSI Technology (VLSIT)*, 2015, pp. T184-T185.

[15] J. Müller *et al,* "Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO_2," *IEEE Electron Dev. Lett,* vol. 33, no. 2, p. 185, 2012.

[16] H. Mulaosmanovic *et al,* "Evidence of single domain switching in hafnium oxide based FeFETs: Enabler for multi-level FeFET memory cells," in *IEEE International Electron Devices Meeting (IEDM)*, 2015, p. 26.8.1.

[17] S.-M. Yoon and H. Ishiwara, "Adaptive-Learning Synaptic Devices Using Ferroelectric-Gate Field-Effect Transistors for Neuromorphic Applications," in *Ferroelectric-Gate Field Effect Transistor Memories: Device Physics and Applications*, B.-E. Park, H. Ishiwara, M. Okuyama, S. Sakai, and S.-M. Yoon, Eds, Dordrecht: Springer Netherlands, 2016, pp. 311–333.

[18] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Reports on Progress in Physics*, vol. 69, no. 2, p. 327, 2006.

[19] K. Kushida-Abdelghafar, K. Watanabe, J. Ushio, and E. Murakami, "Effect of nitrogen at SiO_2/Si interface on reliability issues—negative-bias-temperature instability and Fowler–Nordheim-stress degradation," *Applied Physics Letters*, vol. 81, no. 23, pp. 4362–4364, 2002.

[20] J. Ocker *et al,* "Influence of nitrogen trap states on the electronic properties of high-k metal gate transistors," in *IEEE International Integrated Reliability Workshop (IIRW)*, 2014, pp. 86–89.

[21] K. J. Hubbard and D. G. Schlom, "Thermodynamic stability of binary oxides in contact with silicon," *J. Mater. Res,* vol. 11, no. 11, p. 2757, 1996.

[22] P. Polakowski *et al,* "Ferroelectric deep trench capacitors based on Al:HfO_2 for 3D nonvolatile memory applications," in *6th IEEE International Memory Workshop (IMW)*, 2014.

[23] S. Migita, Y. Morita, W. Mizubayashi, and H. Ota, "Preparation of epitaxial HfO_2 film (EOT=0.5 nm) on Si substrate using atomic-layer deposition of amorphous film and rapid thermal crystallization (RTC) in an abrupt temperature gradient," in *IEEE International Electron Devices Meeting (IEDM)*, 2010, p. 11.5.1.

[24] Y. Morita, S. Migita, W. Mizubayashi, M. Masahara, and H. Ota, "Two-step annealing effects on ultrathin EOT higher-k (k = 40) ALD-HfO_2 gate stacks," in *42nd European Solid-State Device Research Conference (ESSDERC)*, 2012, pp. 81–84.

[25] P. D. Lomenzo *et al,* "Ferroelectric Si-Doped HfO_2 Device Properties on Highly Doped Germanium," *Electron Device Letters, IEEE*, vol. 36, no. 8, pp. 766–768, 2015.

[26] E. Tokumitsu, K. Okamoto, and H. Ishiwara, "Low Voltage Operation of Nonvolatile Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS)-Field-Effect-Transistors (FETs) Using Pt/$SrBi_2Ta_2O_9$/Pt/$SrTa_2O_6$/SiON/Si Structures," *Jap. J. Apl. Phys,* vol. 40, no. 4S, p. 2917, 2001.